National Semiconductor

January 2006

# DS90LV004
# 4-Channel LVDS Buffer/Repeater with Pre-Emphasis

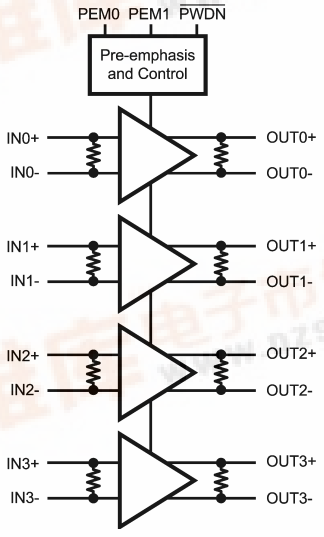
## General Description

The DS90LV004 is a four channel 1.5 Gbps LVDS buffer/repeater. High speed data paths and flow-through pinout minimize internal device jitter and simplify board layout, while configurable pre-emphasis overcomes ISI jitter effects from lossy backplanes and cables. The differential inputs interface to LVDS, and Bus LVDS signals such as those on National's 10-, 16-, and 18- bit Bus LVDS SerDes, as well as CML and LVPECL. The differential inputs and outputs are internally terminated with a 100Ω resistor to improve performance and minimize board space. The repeater function is especially useful for boosting signals for longer distance transmission over lossy cables and backplanes.

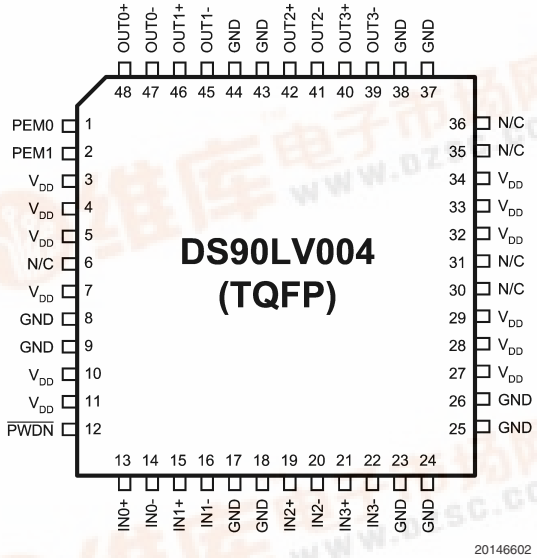
## Features

- 1.5 Gbps data rate per channel
- Configurable pre-emphasis drives lossy backplanes and cables
- Low output skew and jitter
- Hot plug protection
- LVDS/CML/LVPECL compatible input, LVDS output
- On-chip 100Ω input and output termination
- 15 kV ESD protection on LVDS inputs and outputs
- Single 3.3V supply
- Very low power consumption
- Industrial -40 to +85˚C temperature range
- Small TQFP Package Footprint
- Evaluation Kit Available
- See SCAN90004 for JTAG-enabled version

## Block and Connection Diagrams




**DS90LV004 Block Diagram**




**Pinout - Top View**

## Pin Descriptions

| Pin Name | TQFP Pin Number | I/O, Type | Description |
|---|---|---|---|
| **DIFFERENTIAL INPUTS** | | | |
| IN0+<br>IN0– | 13<br>14 | I, LVDS | Channel 0 inverting and non-inverting differential inputs. |
| IN1+<br>IN1– | 15<br>16 | I, LVDS | Channel 1 inverting and non-inverting differential inputs. |
| IN2+<br>IN2– | 19<br>20 | I, LVDS | Channel 2 inverting and non-inverting differential inputs. |
| IN3+<br>IN3– | 21<br>22 | I, LVDS | Channel 3 inverting and non-inverting differential inputs. |
| **DIFFERENTIAL OUTPUTS** | | | |
| OUT0+<br>OUT0– | 48<br>47 | O, LVDS | Channel 0 inverting and non-inverting differential outputs. (Note 1) |
| OUT1+<br>OUT1– | 46<br>45 | O, LVDS | Channel 1 inverting and non-inverting differential outputs. (Note 1) |
| OUT2+<br>OUT2– | 42<br>41 | O, LVDS | Channel 2 inverting and non-inverting differential outputs. (Note 1) |
| OUT3+<br>OUT3- | 40<br>39 | O, LVDS | Channel 3 inverting and non-inverting differential outputs. (Note 1) |
| **DIGITAL CONTROL INTERFACE** | | | |
| $\overline{\text{PWDN}}$ | 12 | I, LVTTL | A logic low at $\overline{\text{PWDN}}$ activates the hardware power down mode. |
| PEM0<br>PEM1 | 1<br>2 | I, LVTTL | Pre-emphasis Control Inputs (affects all Channels) |
| **POWER** | | | |
| $V_{DD}$ | 3, 4, 5, 7, 10, 11, 27, 28, 29, 32, 33, 34 | I, Power | $V_{DD}$ = 3.3V, ±5% |
| GND | 8, 9, 17, 18, 23, 24, 25, 26, 37, 38, 43, 44 | I, Power | Ground |
| N/C | 6, 30, 31, 35, 36 | | No Connect |

**Note 1:** The LVDS outputs do not support a multidrop (BLVDS) environment. The LVDS output characteristics of the DS90LV004 device have been optimized for point-to-point backplane and cable applications.

## Absolute Maximum Ratings (Note 2)

| | |
|---|---|
| Supply Voltage ($V_{DD}$) | −0.3V to +4.0V |
| CMOS Input Voltage | −0.3V to ($V_{DD}$+0.3V) |
| LVDS Receiver Input Voltage | −0.3V to ($V_{DD}$+0.3V) |
| LVDS Driver Output Voltage | −0.3V to ($V_{DD}$+0.3V) |
| LVDS Output Short Circuit Current | +40 mA |
| Junction Temperature | +150˚C |
| Storage Temperature | −65˚C to +150˚C |
| Lead Temperature (Solder, 4sec) | 260˚C |
| Max Pkg Power Capacity @ 25˚C | 1.64W |
| Thermal Resistance ($\theta_{JA}$) | 76˚C/W |
| Package Derating above +25˚C | 13.2mW/˚C |
| ESD Last Passing Voltage | |
| HBM, 1.5kΩ, 100pF | 15 kV |
| EIAJ, 0Ω, 200pF | 250V |

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | 3.15V to 3.45V |
| Input Voltage ($V_I$) (Note 3) | 0V to $V_{CC}$ |
| Output Voltage ($V_O$) | 0V to $V_{CC}$ |
| Operating Temperature ($T_A$) | |
| Industrial | −40˚C to +85˚C |

**Note 2:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of products outside of recommended operation conditions.

**Note 3:** $V_{ID}$ max < 2.4V

## Electrical Characteristics

Over recommended operating supply and temperature ranges unless other specified.

| Symbol | Parameter | Conditions | Min | Typ (Note 4) | Max | Units |
|---|---|---|---|---|---|---|
| **LVTTL DC SPECIFICATIONS** ($\overline{PWDN}$, PEM0, PEM1) | | | | | | |
| $V_{IH}$ | High Level Input Voltage | | 2.0 | | $V_{DD}$ | V |
| $V_{IL}$ | Low Level Input Voltage | | GND | | 0.8 | V |
| $I_{IH}$ | High Level Input Current | $V_{IN} = V_{DD} = V_{DDMAX}$ | −10 | | +10 | µA |
| $I_{IL}$ | Low Level Input Current | $V_{IN} = V_{SS}$, $V_{DD} = V_{DDMAX}$ | −10 | | +10 | µA |
| $C_{IN1}$ | Input Capacitance | Any Digital Input Pin to $V_{SS}$ | | 3.5 | | pF |
| $V_{CL}$ | Input Clamp Voltage | $I_{CL}$ = −18 mA | −1.5 | −0.8 | | V |
| **LVDS INPUT DC SPECIFICATIONS** (INn±) | | | | | | |
| $V_{TH}$ | Differential Input High Threshold (Note 5) | $V_{CM}$ = 0.8V to 3.4V, $V_{DD}$ = 3.45V | | 0 | 100 | mV |
| $V_{TL}$ | Differential Input Low Threshold (Note 5) | $V_{CM}$ = 0.8V to 3.4V, $V_{DD}$ = 3.45V | −100 | 0 | | mV |
| $V_{ID}$ | Differential Input Voltage | $V_{CM}$ = 0.8V to 3.4V, $V_{DD}$ = 3.45V | 100 | | 2400 | mV |
| $V_{CMR}$ | Common Mode Voltage Range | $V_{ID}$ = 150 mV, $V_{DD}$ = 3.45V | 0.05 | | 3.40 | V |
| $C_{IN2}$ | Input Capacitance | IN+ or IN− to $V_{SS}$ | | 3.5 | | pF |
| $I_{IN}$ | Input Current | $V_{IN}$ = 3.45V, $V_{DD} = V_{DDMAX}$ | −10 | | +10 | µA |
| | | $V_{IN}$ = 0V, $V_{DD} = V_{DDMAX}$ | −10 | | +10 | µA |

## Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless other specified.

| Symbol | Parameter | Conditions | Min | Typ (Note 4) | Max | Units |
|---|---|---|---|---|---|---|
| **LVDS OUTPUT DC SPECIFICATIONS** (OUTn±) | | | | | | |
| $V_{OD}$ | Differential Output Voltage, 0% Pre-emphasis (Note 5) | $R_L$ = 100Ω external resistor between OUT+ and OUT– | 250 | 500 | 600 | mV |
| $\Delta V_{OD}$ | Change in $V_{OD}$ between Complementary States | | –35 | | 35 | mV |
| $V_{OS}$ | Offset Voltage (Note 6) | | 1.05 | 1.18 | 1.475 | V |
| $\Delta V_{OS}$ | Change in $V_{OS}$ between Complementary States | | –35 | | 35 | mV |
| $I_{OS}$ | Output Short Circuit Current | OUT+ or OUT– Short to GND | | –60 | –90 | mA |
| $C_{OUT2}$ | Output Capacitance | OUT+ or OUT– to GND when TRI-STATE | | 5.5 | | pF |
| **SUPPLY CURRENT (Static)** | | | | | | |
| $I_{CC}$ | Supply Current | All inputs and outputs enabled and active, terminated with differential load of 100Ω between OUT+ and OUT-. | | 117 | 140 | mA |
| $I_{CCZ}$ | Supply Current - Power Down Mode | $\overline{PWDN}$ = L | | 2.7 | 6 | mA |
| **SWITCHING CHARACTERISTICS — LVDS OUTPUTS** | | | | | | |
| $t_{LHT}$ | Differential Low to High Transition Time | Use an alternating 1 and 0 pattern at 200 Mbps, measure between 20% and 80% of $V_{OD}$. | | 210 | 300 | ps |
| $t_{HLT}$ | Differential High to Low Transition Time | | | 210 | 300 | ps |
| $t_{PLHD}$ | Differential Low to High Propagation Delay | Use an alternating 1 and 0 pattern at 200 Mbps, measure at 50% $V_{OD}$ between input to output. | | 2.0 | 3.2 | ns |
| $t_{PHLD}$ | Differential High to Low Propagation Delay | | | 2.0 | 3.2 | ns |
| $t_{SKD1}$ | Pulse Skew | $\lvert t_{PLHD} - t_{PHLD} \rvert$ | | 25 | 80 | ps |
| $t_{SKCC}$ | Output Channel to Channel Skew | Difference in propagation delay ($t_{PLHD}$ or $t_{PHLD}$) among all output channels. | | 50 | 125 | ps |
| $t_{JIT}$ | Jitter (0% Pre-emphasis) (Note 7) | RJ - Alternating 1 and 0 at 750 MHz (Note 8) | | 1.1 | 1.5 | psrms |
| | | DJ - K28.5 Pattern, 1.5 Gbps (Note 9) | | 43 | 62 | psp-p |
| | | TJ - PRBS $2^{23}$-1 Pattern, 1.5 Gbps (Note 10) | | 35 | 85 | psp-p |
| $t_{ON}$ | LVDS Output Enable Time | Time from $\overline{PWDN}$ to OUT± change from TRI-STATE to active. | | | 300 | ns |
| $t_{OFF}$ | LVDS Output Disable Time | Time from $\overline{PWDN}$ to OUT± change from active to TRI-STATE. | | | 12 | ns |

**Note 4:** Typical parameters are measured at $V_{DD}$ = 3.3V, $T_A$ = 25˚C. They are for reference purposes, and are not production-tested.

**Note 5:** Differential output voltage $V_{OD}$ is defined as ABS(OUT+–OUT–). Differential input voltage $V_{ID}$ is defined as ABS(IN+–IN–).

**Note 6:** Output offset voltage $V_{OS}$ is defined as the average of the LVDS single-ended output voltages at logic high and logic low states.

**Note 7:** Jitter is not production tested, but guaranteed through characterization on a sample basis.

**Note 8:** Random Jitter, or RJ, is measured RMS with a histogram including 1500 histogram window hits. The input voltage = $V_{ID}$ = 500mV, 50% duty cycle at 750MHz, $t_r$ = $t_f$ = 50ps (20% to 80%).

**Note 9:** Deterministic Jitter, or DJ, is measured to a histogram mean with a sample size of 350 hits. The input voltage = $V_{ID}$ = 500mV, K28.5 pattern at 1.5 Gbps, $t_r$ = $t_f$ = 50ps (20% to 80%). The K28.5 pattern is repeating bit streams of (0011111010 1100000101).

**Note 10:** Total Jitter, or TJ, is measured peak to peak with a histogram including 3500 window hits. Stimulus and fixture Jitter has been subtracted. The input voltage = $V_{ID}$ = 500mV, $2^{23}$-1 PRBS pattern at 1.5 Gbps, $t_r$ = $t_f$ = 50ps (20% to 80%).

# Feature Descriptions

### INTERNAL TERMINATIONS

The DS90LV004 has integrated termination resistors on both the input and outputs. The inputs have a 100Ω resistor across the differential pair, placing the receiver termination as close as possible to the input stage of the device. The LVDS outputs also contain an integrated 100Ω ohm termination resistor, this resistor is used to reduce the effects of Near End Crosstalk (NEXT) and does not take the place of the 100 ohm termination at the inputs to the receiving device. The integrated terminations improve signal integrity and decrease the external component count resulting in space savings.

### OUTPUT CHARACTERISTICS

The output characteristics of the DS90LV004 have been optimized for point-to-point backplane and cable applications, and are not intended for multipoint or multidrop signaling.

### POWERDOWN MODE

The $\overline{\text{PWDN}}$ input activates a hardware powerdown mode. When the powerdown mode is active ($\overline{\text{PWDN}}$=L), all input and output buffers and internal bias circuitry are powered off and disabled. Outputs are tri-stated in powerdown mode. When exiting powerdown mode, there is a delay associated with turning on bandgap references and input/output buffer circuits as indicated in the LVDS Output Switching Characteristics

### PRE-EMPHASIS

Pre-emphasis dramatically reduces ISI jitter from long or lossy transmission media. Two pins are used to select the pre-emphasis level for all outputs: off, low, medium, or high.

**Pre-emphasis Control Selection Table**

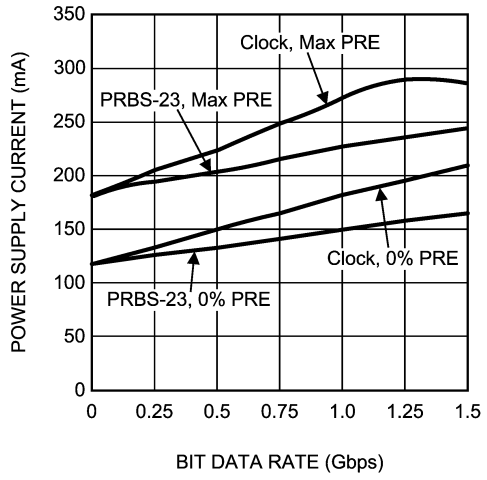
| PEM1 | PEM0 | Pre-Emphasis |
|---|---|---|
| 0 | 0 | Off |
| 0 | 1 | Low |
| 1 | 0 | Medium |
| 1 | 1 | High |

### INPUT FAILSAFE BIASING

External pull up and pull down resistors may be used to provide enough of an offset to enable an input failsafe under open-circuit conditions. This configuration ties the positive LVDS input pin to $V_{DD}$ thru a pull up resistor and the negative LVDS input pin is tied to GND by a pull down resistor. The pull up and pull down resistors should be in the 5kΩ to 15kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point ideally should be set to approximately 1.2V (less than 1.75V) to be compatible with the internal circuitry. Please refer to application note AN-1194 “Failsafe Biasing of LVDS Interfaces” for more information.

# Typical Performance Characteristics

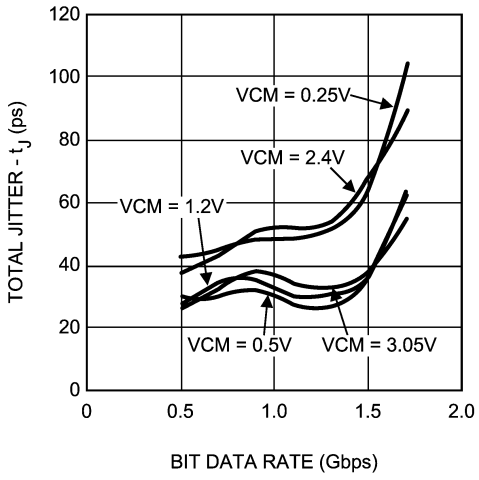
**Power Supply Current vs. Bit Data Rate**




20146641

Dynamic power supply current was measured while running a clock or PRBS $2^{23}$-1 pattern with all 4 channels active. $V_{CC}$ = 3.3V, $T_A$ = +25˚C, $V_{ID}$ = 0.5V, $V_{CM}$ = 1.2V

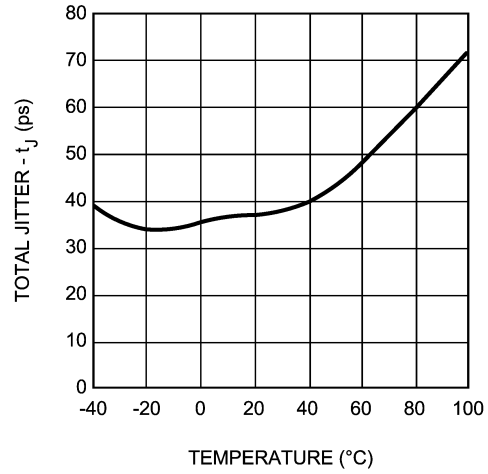
**Total Jitter ($T_J$) vs. Bit Data Rate**




20146642

Total Jitter measured at 0V differential while running a PRBS $2^{23}$-1 pattern with a single channel active. $V_{CC}$ = 3.3V, $T_A$ = +25˚C, $V_{ID}$ = 0.5V, 0% Pre-emphasis

**Total Jitter ($T_J$) vs. Temperature**




20146643

Total Jitter measured at 0V differential while running a PRBS $2^{23}$-1 pattern with a single channel active. $V_{CC}$ = 3.3V, $V_{ID}$ = 0.5V, $V_{CM}$ = 1.2V, 1.5 Gbps data rate, 0% Pre-emphasis

**Positive Edge Transition vs. Pre-emphasis Level**

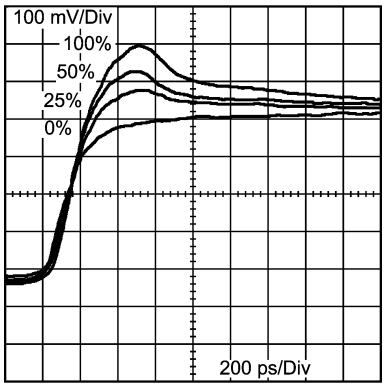



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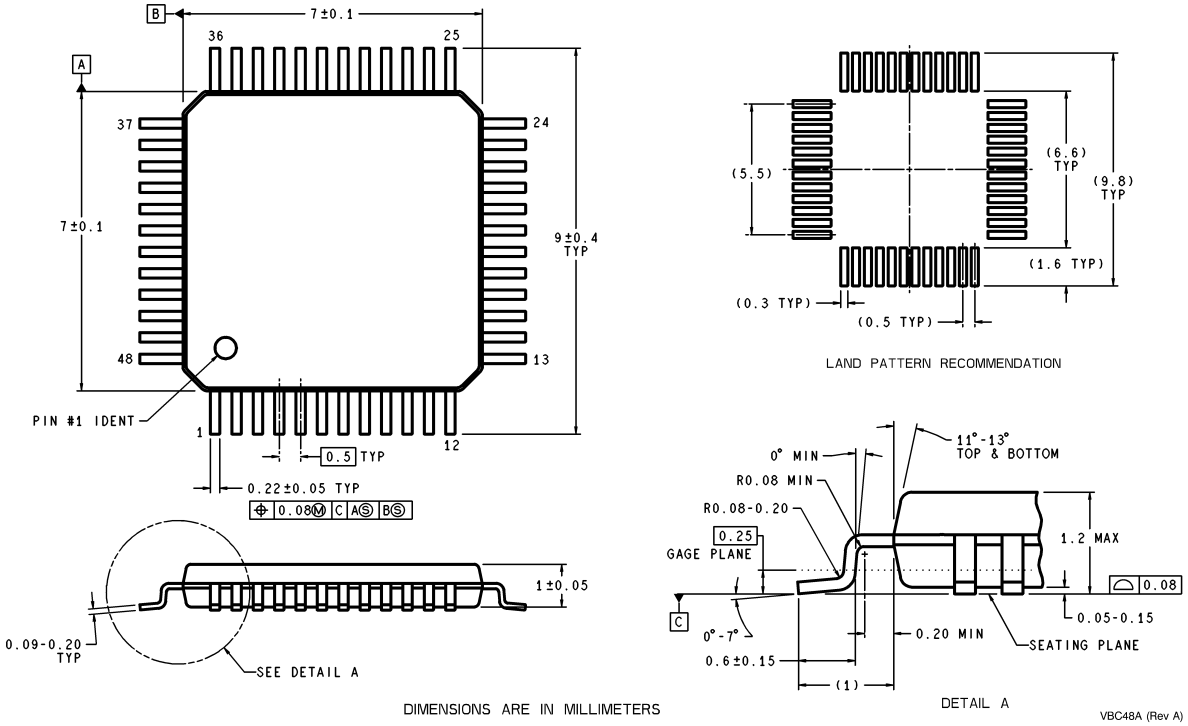
**FIGURE 1. Typical Performance Characteristics of the DS90LV004**

## Physical Dimensions inches (millimeters) unless otherwise noted




**48-TQFP**
**NS Package Number VBC48a**
**Order Number DS90LV004TVS (250 piece Tray)**



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