



PRELIMINARY
October 2005

DS90CF383B

+3.3V Programmable LVDS Transmitter 24-Bit Flat Panel Display (FPD) Link-65 MHz

General Description

The DS90CF383B transmitter converts 28 bits of CMOS/TTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. At a transmit clock frequency of 65 MHz, 24 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 455 Mbps per LVDS data channel. Using a 65 MHz clock, the data throughput is 227 Mbytes/sec. The DS90CF383B is fixed as a Falling edge strobe transmitter and will interoperate with a Falling edge strobe Receiver (DS90CF386) without any translation logic.

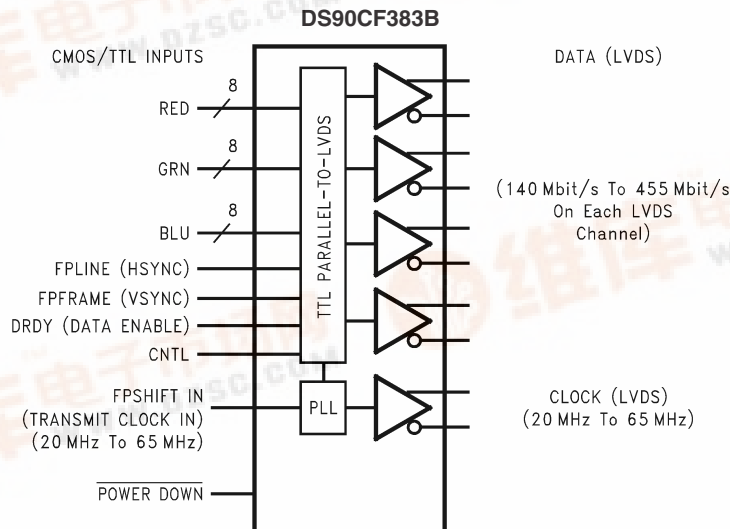
This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Features

- No special start-up sequence required between clock/data and /PD pins. Input signal (clock and data) can be applied either before or after the device is powered.
- Support Spread Spectrum Clocking up to 100KHz frequency modulation & deviations of $\pm 2.5\%$ center spread or -5% down spread.

- "Input Clock Detection" feature will pull all LVDS pairs to logic low when input clock is missing and when /PD pin is logic high.
- 18 to 68 MHz shift clock support
- Best-in-Class Set & Hold Times on TxINPUTs
- Tx power consumption < 130 mW (typ) @65MHz Grayscale
- 40% Less Power Dissipation than BiCMOS Alternatives
- Tx Power-down mode < 60 μ W (typ)
- Supports VGA, SVGA, XGA and Dual Pixel SXGA.
- Narrow bus reduces cable size and cost
- Up to 1.8 Gbps throughput
- Up to 227 Megabytes/sec bandwidth
- 345 mV (typ) swing LVDS devices for low EMI
- PLL requires no external components
- Compatible with TIA/EIA-644 LVDS standard
- Low profile 56-lead TSSOP package
- Improved replacement for: SN75LVDS83, DS90CF383A

Block Diagram



Order Number DS90CF383BMT
See NS Package Number MTD56

20098501

DS90CF383B +3.3V Programmable LVDS Transmitter 24-Bit Flat Panel Display (FPD) Link-65 MHz



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

| | |
|---|------------------------------|
| Supply Voltage (V_{CC}) | −0.3V to +4V |
| CMOS/TTL Input Voltage | −0.3V to ($V_{CC} + 0.3V$) |
| LVDS Driver Output Voltage | −0.3V to ($V_{CC} + 0.3V$) |
| LVDS Output Short Circuit Duration | Continuous |
| Junction Temperature | +150°C |
| Storage Temperature | −65°C to +150°C |
| Lead Temperature (Soldering, 4 sec) | +260°C |
| Maximum Package Power Dissipation Capacity @ 25°C | |
| MTD56 (TSSOP) Package: DS90CF383B | 1.63 W |

Package Derating:

DS90CF383B

12.5 mW/°C above +25°C

ESD Rating

(HBM, 1.5 kΩ, 100 pF)

7 kV

(EIAJ, 0Ω, 200 pF)

500V

Recommended Operating Conditions

| | Min | Nom | Max | Units |
|---|-----|-----|-----|------------------|
| Supply Voltage (V_{CC}) | 3.0 | 3.3 | 3.6 | V |
| Operating Free Air Temperature (T_A) | −10 | +25 | +70 | °C |
| Supply Noise Voltage (V_{CC}) | | | 200 | mV _{PP} |
| TxCLKIN frequency | 18 | | 68 | MHz |

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units | |
|----------------------------|---|--|------------|-------|-----------------|-------|----|
| CMOS/TTL DC SPECIFICATIONS | | | | | | | |
| V _{IH} | High Level Input Voltage | | 2.0 | | V _{CC} | V | |
| V _{IL} | Low Level Input Voltage | | GND | | 0.8 | V | |
| V _{CL} | Input Clamp Voltage | I _{CL} = −18 mA | | −0.79 | −1.5 | V | |
| I _{IN} | Input Current | V _{IN} = 0.4V, 2.5V or V _{CC} | | +1.8 | +10 | μA | |
| | | V _{IN} = GND | −10 | 0 | | μA | |
| LVDS DC SPECIFICATIONS | | | | | | | |
| V _{OD} | Differential Output Voltage | R _L = 100Ω | 250 | 345 | 450 | mV | |
| ΔV _{OD} | Change in V _{OD} between complimentary output states | | | | 35 | mV | |
| V _{OS} | Offset Voltage (Note 4) | | 1.13 | 1.25 | 1.38 | V | |
| ΔV _{OS} | Change in V _{OS} between complimentary output states | | | | 35 | mV | |
| I _{OS} | Output Short Circuit Current | V _{OUT} = 0V, R _L = 100Ω | | −3.5 | −5 | mA | |
| I _{OZ} | Output TRI-STATE® Current | Power Down = 0V, V _{OUT} = 0V or V _{CC} | | ±1 | ±10 | μA | |
| TRANSMITTER SUPPLY CURRENT | | | | | | | |
| ICCTW | Transmitter Supply Current Worst Case | R _L = 100Ω, C _L = 5 pF, Worst Case Pattern (Figures 1, 4) " Typ " values are given for V _{CC} = 3.6V and T _A = +25°C, " Max " values are given for V _{CC} = 3.6V and T _A = −10°C | f = 25 MHz | | 31 | 45 | mA |
| | | | f = 40 MHz | | 37 | 50 | mA |
| | | | f = 65 MHz | | 48 | 60 | mA |

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------------------------|--|--|---------------------|-----|-----|---------------|
| TRANSMITTER SUPPLY CURRENT | | | | | | |
| ICCTG | Transmitter Supply Current 16 Grayscale | $R_L = 100\Omega$, $C_L = 5\text{ pF}$, 16 Grayscale Pattern (Figures 2, 4) "Typ" values are given for $V_{CC} = 3.6\text{V}$ and $T_A = +25^\circ\text{C}$, "Max" values are given for $V_{CC} = 3.6\text{V}$ and $T_A = -10^\circ\text{C}$ | $f = 25\text{ MHz}$ | 29 | 40 | mA |
| | | | $f = 40\text{ MHz}$ | 33 | 45 | mA |
| | | | $f = 65\text{ MHz}$ | 39 | 50 | mA |
| ICCTZ | Transmitter Supply Current Power Down | Power Down = Low Driver Outputs in TRI-STATE under Power Down Mode | | 17 | 150 | μA |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for $V_{CC} = 3.3\text{V}$ and $T_A = +25^\circ\text{C}$ unless specified otherwise.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Note 4: V_{OS} previously referred as V_{CM} .

Recommended Transmitter Input Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

| Symbol | Parameter | Min | Typ | Max | Units |
|--------|---|-------|------|-------|---------------|
| TCIT | TxCLK IN Transition Time (Figure 5) | | | 5 | ns |
| TCIP | TxCLK IN Period (Figure 6) | 14.7 | T | 50 | ns |
| TCIH | TxCLK IN High Time (Figure 6) | 0.35T | 0.5T | 0.65T | ns |
| TCIL | TxCLK IN Low Time (Figure 6) | 0.35T | 0.5T | 0.65T | ns |
| TXIT | TxIN, and Power Down pin Transition Time | 1.5 | | 6 | ns |
| TXPD | Minimum pulse width for Power Down pin signal | 1 | | | μs |

Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

| Symbol | Parameter | | Min | Typ | Max | Units |
|--------|---|---------------|-------|-------|-------|-------|
| LLHT | LVDS Low-to-High Transition Time (Figure 4) | | | 0.75 | 1.4 | ns |
| LHLT | LVDS High-to-Low Transition Time (Figure 4) | | | 0.75 | 1.4 | ns |
| TPPos0 | Transmitter Output Pulse Position for Bit 0 (Figure 11) (Note 5) | f = 65 MHz | −0.20 | 0 | +0.20 | ns |
| TPPos1 | Transmitter Output Pulse Position for Bit 1 | | 2.00 | 2.20 | 2.40 | ns |
| TPPos2 | Transmitter Output Pulse Position for Bit 2 | | 4.20 | 4.40 | 4.60 | ns |
| TPPos3 | Transmitter Output Pulse Position for Bit 3 | | 6.39 | 6.59 | 6.79 | ns |
| TPPos4 | Transmitter Output Pulse Position for Bit 4 | | 8.59 | 8.79 | 8.99 | ns |
| TPPos5 | Transmitter Output Pulse Position for Bit 5 | | 10.70 | 10.99 | 11.19 | ns |
| TPPos6 | Transmitter Output Pulse Position for Bit 6 | | 12.99 | 13.19 | 13.39 | ns |
| TPPos0 | Transmitter Output Pulse Position for Bit 0 (Figure 11) (Note 5) | f = 40 MHz | −0.25 | 0 | +0.25 | ns |
| TPPos1 | Transmitter Output Pulse Position for Bit 1 | | 3.32 | 3.57 | 3.82 | ns |
| TPPos2 | Transmitter Output Pulse Position for Bit 2 | | 6.89 | 7.14 | 7.39 | ns |
| TPPos3 | Transmitter Output Pulse Position for Bit 3 | | 10.46 | 10.71 | 10.96 | ns |
| TPPos4 | Transmitter Output Pulse Position for Bit 4 | | 14.04 | 14.29 | 14.54 | ns |
| TPPos5 | Transmitter Output Pulse Position for Bit 5 | | 17.61 | 17.86 | 18.11 | ns |
| TPPos6 | Transmitter Output Pulse Position for Bit 6 | | 21.18 | 21.43 | 21.68 | ns |

Transmitter Switching Characteristics (Continued)

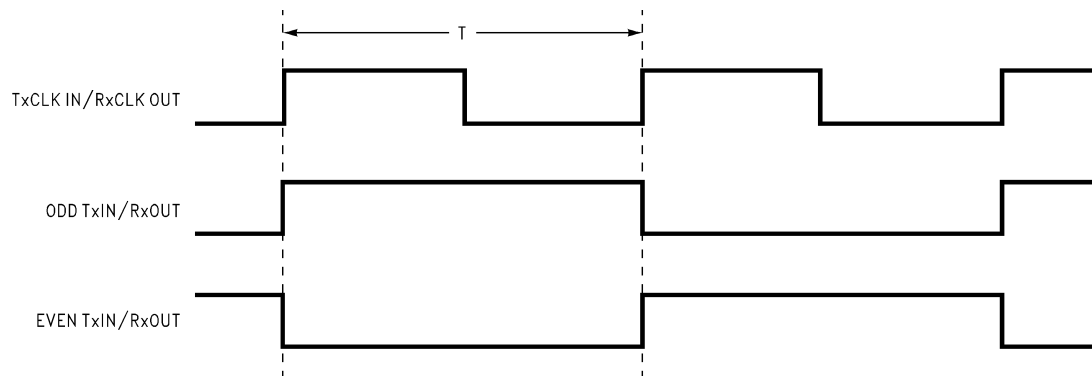
Over recommended operating supply and temperature ranges unless otherwise specified

| Symbol | Parameter | | Min | Typ | Max | Units |
|--------|--|---------------|-------|----------------------|-------|-------|
| TPPos0 | Transmitter Output Pulse Position for Bit 0 (Figure 11) (Note 5) | f = 25 MHz | −0.45 | 0 | +0.45 | ns |
| TPPos1 | Transmitter Output Pulse Position for Bit 1 | | 5.26 | 5.71 | 6.16 | ns |
| TPPos2 | Transmitter Output Pulse Position for Bit 2 | | 10.98 | 11.43 | 11.88 | ns |
| TPPos3 | Transmitter Output Pulse Position for Bit 3 | | 16.69 | 17.14 | 17.59 | ns |
| TPPos4 | Transmitter Output Pulse Position for Bit 4 | | 22.41 | 22.86 | 23.31 | ns |
| TPPos5 | Transmitter Output Pulse Position for Bit 5 | | 28.12 | 28.57 | 29.02 | ns |
| TPPos6 | Transmitter Output Pulse Position for Bit 6 | | 33.84 | 34.29 | 34.74 | ns |
| TSTC | TxIN Setup to TxCLK IN (Figure 6) | | 2.5 | | | ns |
| THTC | TxIN Hold to TxCLK IN (Figure 6) | | 0.5 | | | ns |
| TCCD | TxCLK IN to TxCLK OUT Delay (Figure 7) 50% duty cycle input clock is assumed, T _A = −10°C, and 65MHz for " Min ", T _A = 70°C, and 25MHz for " Max ", V _{CC} = 3.6V | | 3.011 | | 6.062 | ns |
| SSCG | Spread Spectrum Clock support; Modulation frequency with a linear profile (Note 6) | f = 25 MHz | | 100KHz ± 2.5%/−5% | | |
| | | f = 40 MHz | | 100KHz ± 2.5%/−5% | | |
| | | f = 65 MHz | | 100KHz ± 2.5%/−5% | | |
| TPLLS | Transmitter Phase Lock Loop Set (Figure 8) | | | | 10 | ms |
| TPDD | Transmitter Power Down Delay (Figure 10) | | | | 100 | ns |

Note 5: The Minimum and Maximum Limits are based on statistical analysis of the device performance over process, voltage, and temperature ranges. This parameter is functionality tested only on Automatic Test Equipment (ATE).

Note 6: Care must be taken to ensure TSTC and THTC are met so input data are sampling correctly. This SSCG parameter only shows the performance of tracking Spread Spectrum Clock applied to TxCLK IN pin, and reflects the result on TxCLKOUT+ and TxCLK- pins.

AC Timing Diagrams



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FIGURE 1. "Worst Case" Test Pattern

AC Timing Diagrams (Continued)

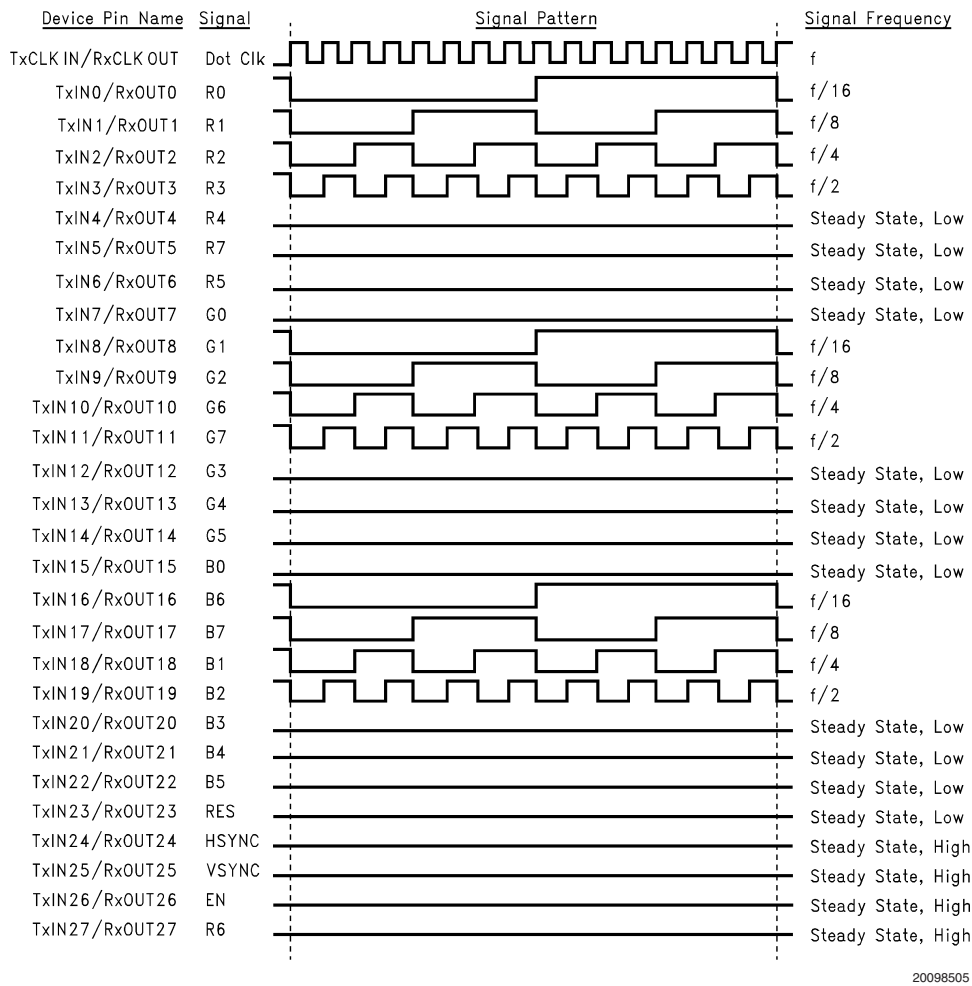


FIGURE 2. “16 Grayscale” Test Pattern (Notes 7, 8, 9, 10)

Note 7: The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

Note 8: The 16 grayscale test pattern tests device power consumption for a “typical” LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

Note 9: Figures 1, 2 show a falling edge data strobe (TxCLK IN/RxCLK OUT).

Note 10: Recommended pin to signal mapping. Customer may choose to define differently.

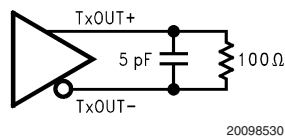


FIGURE 3. DS90CF383B (Transmitter) LVDS Output Load

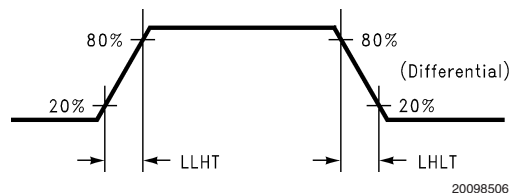


FIGURE 4. DS90CF383B (Transmitter) LVDS Transition Times

AC Timing Diagrams (Continued)

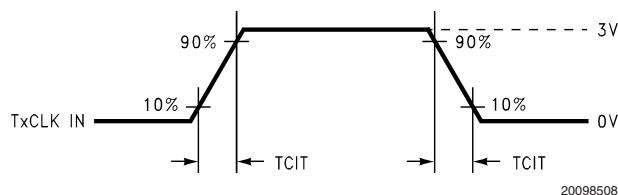


FIGURE 5. DS90CF383B (Transmitter) Input Clock Transition Time

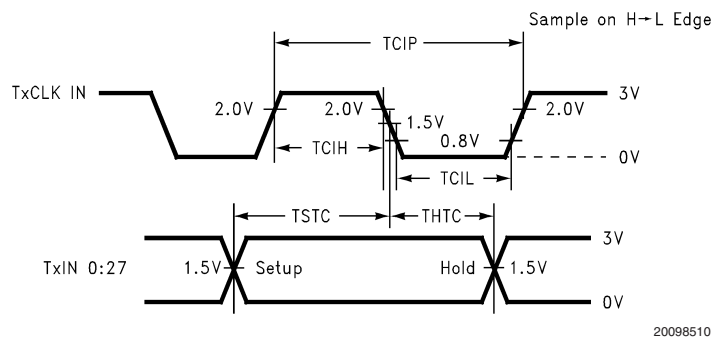


FIGURE 6. DS90CF383B (Transmitter) Setup/Hold and High/Low Times (Falling Edge Strobe)

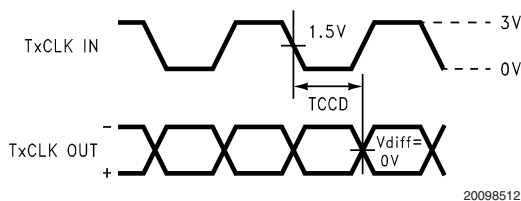


FIGURE 7. DS90CF383B (Transmitter) Clock In to Clock Out Delay (Falling Edge Strobe)

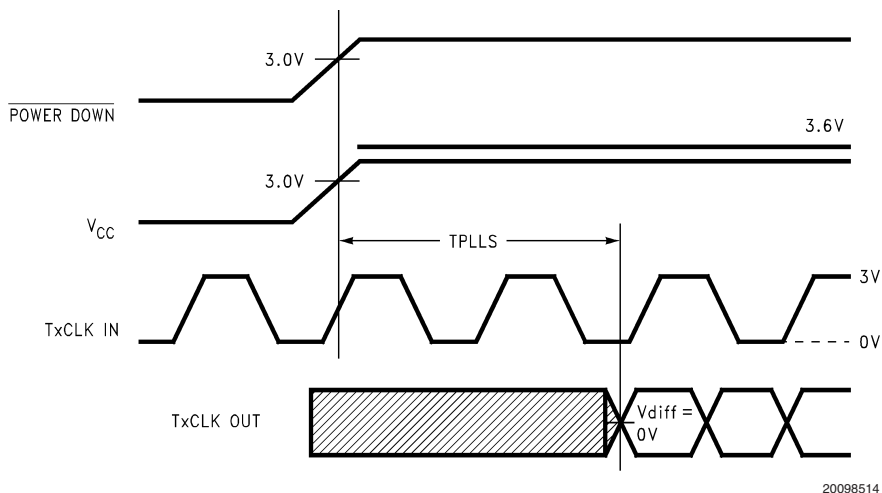


FIGURE 8. DS90CF383B (Transmitter) Phase Lock Loop Set Time

AC Timing Diagrams (Continued)

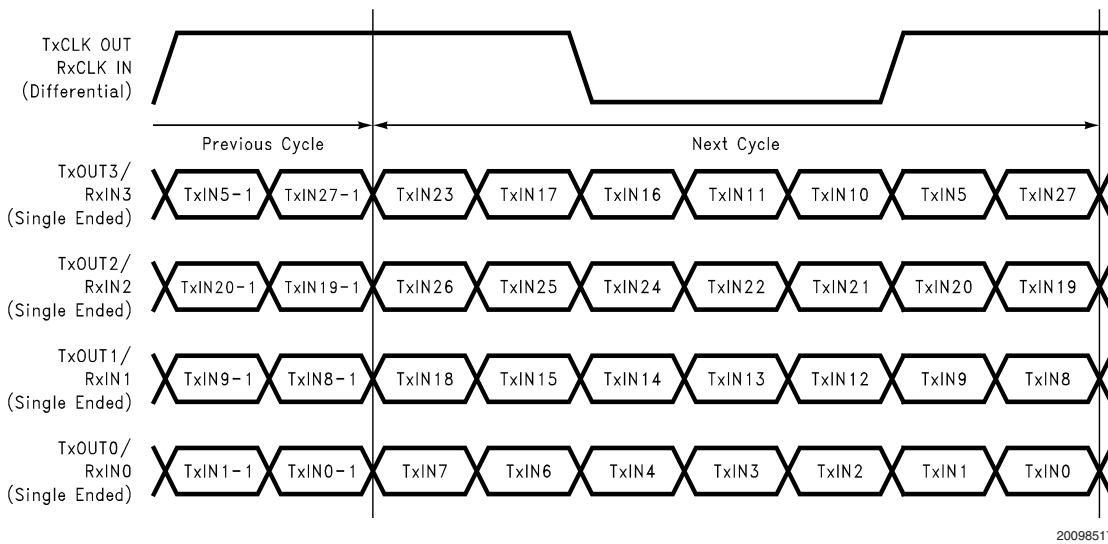


FIGURE 9.28 Parallel TTL Data Inputs Mapped to LVDS Outputs

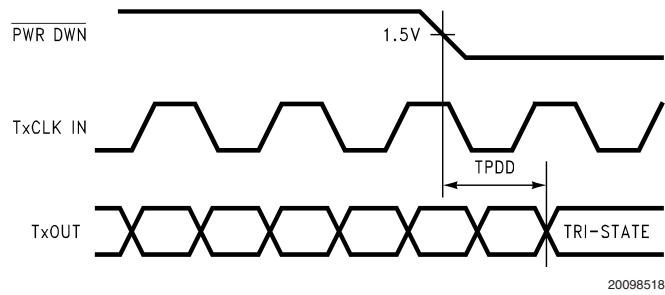
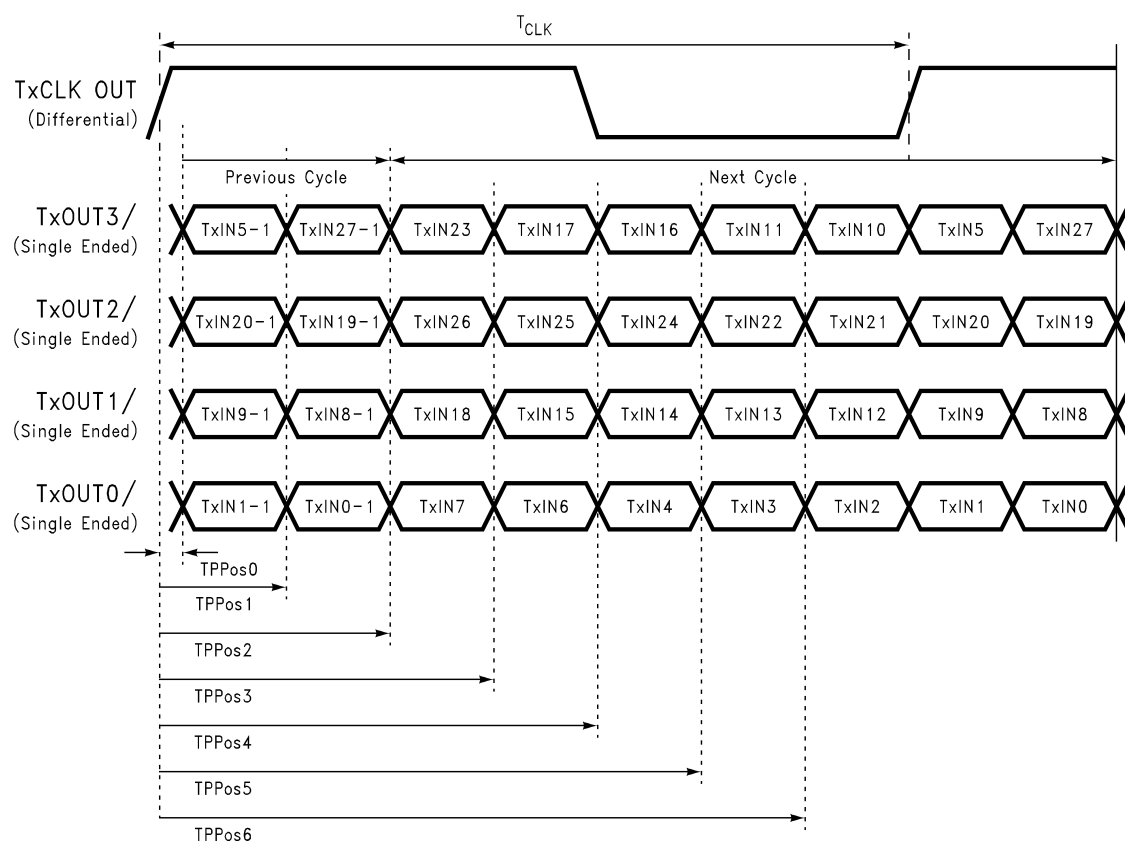


FIGURE 10. Transmitter Power Down Delay

AC Timing Diagrams (Continued)



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FIGURE 11. Transmitter LVDS Output Pulse Position Measurement

DS90CF383B Pin Descriptions — FPD Link Transmitter

| Pin Name | I/O | No. | Description |
|----------------------|-----|-----|--|
| TxIN | I | 28 | TTL level input. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines— FPLINE, FPFRAME and DRDY (also referred to as HSYNC, VSYNC, Data Enable). |
| TxOUT+ | O | 4 | Positive LVDS differential data output. |
| TxOUT– | O | 4 | Negative LVDS differential data output. |
| FPSHIFT IN | I | 1 | TTL level clock input. The falling edge acts as data strobe. Pin name TxCLK IN. |
| TxCLK OUT+ | O | 1 | Positive LVDS differential clock output. |
| TxCLK OUT– | O | 1 | Negative LVDS differential clock output. |
| PWR DOWN | I | 1 | TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down. See Applications Information section. |
| V _{CC} | I | 4 | Power supply pins for TTL inputs. |
| GND | I | 5 | Ground pins for TTL inputs. |
| PLL V _{CC} | I | 1 | Power supply pin for PLL. |
| PLL GND | I | 2 | Ground pins for PLL. |
| LVDS V _{CC} | I | 1 | Power supply pin for LVDS outputs. |
| LVDS GND | I | 3 | Ground pins for LVDS outputs. |

Applications Information

The DS90CF383B are backward compatible with the DS90C383/DS90CF383, DS90C383A/DS90CF383A and are a pin-for-pin replacement.

This device may also be used as a replacement for the DS90CF583 (5V, 65MHz) and DS90CF581 (5V, 40MHz) FPD-Link Transmitters with certain considerations/modifications:

1. Change 5V power supply to 3.3V. Provide this supply to the V_{CC}, LVDS V_{CC} and PLL V_{CC} of the transmitter.

TRANSMITTER INPUT PINS

The DS90CF383B transmitter input and control inputs accept 3.3V LVTTTL/LVCMOS levels. They are not 5V tolerant.

TRANSMITTER CLOCK/CLOCK/DATA SEQUENCING

The DS90CF383B does not require any special requirement for sequencing of the input clock/data and PD (PowerDown) signal. The DS90CF383B offers a more robust input sequencing feature where the input clock/data can be inserted after the release of the PD signal. In the case where the clock/data is stopped and reapplied, such as changing video mode within Graphics Controller, it is not necessary to cycle the PD signal. However, there are in certain cases where the PD may need to be asserted during these mode changes. In

cases where the source (Graphics Source) may be supplying an unstable clock or spurious noisy clock output to the LVDS transmitter, the LVDS Transmitter may attempt to lock onto this unstable clock signal but is unable to do so due the instability or quality of the clock source. The PD signal in these cases should then be asserted once a stable clock is applied to the LVDS transmitter. Asserting the PWR DOWN pin will effectively place the device in reset and disable the PLL, enabling the LVDS Transmitter into a power saving standby mode. However, it is still generally a good practice to assert the PWR DOWN pin or reset the LVDS transmitter whenever the clock/data is stopped and reapplied but it is not mandatory for the DS90CF383B.

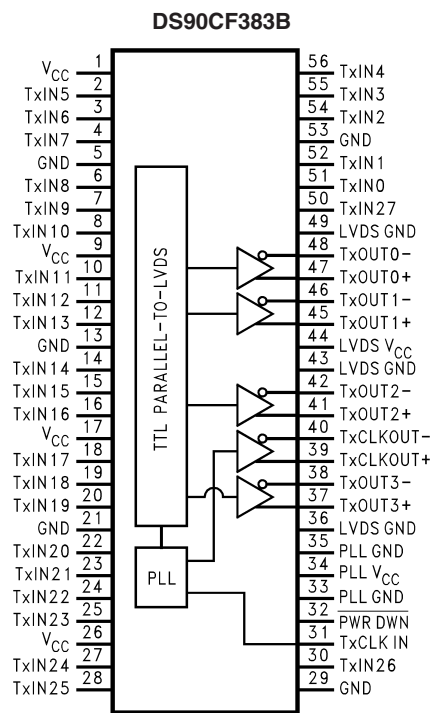
SPREAD SPECTRUM CLOCK SUPPORT

The DS90CF383B can support Spread Spectrum Clocking signal type inputs. The DS90CF383B outputs will accurately track Spread Spectrum Clock/Data inputs with modulation frequencies of up to 100KHz (max.) with either center spread of ±2.5% or down spread -5% deviations.

POWER SOURCES SEQUENCE

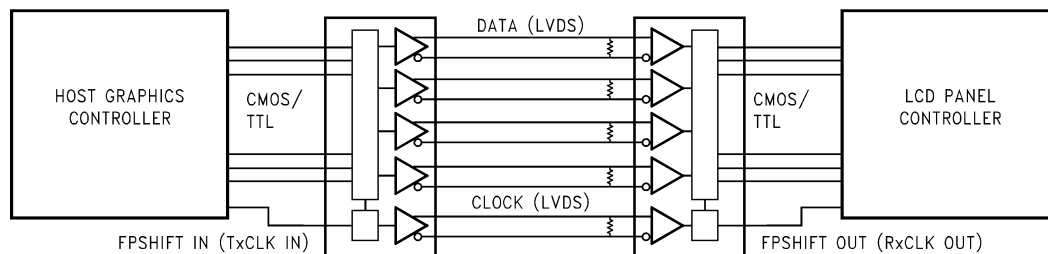
In typical applications, it is recommended to have V_{CC}, LVDS V_{CC} and PLL V_{CC} from the same power source with three separate de-coupling bypass capacitor groups. There is no requirement on which VCC entering the device first.

Pin Diagram



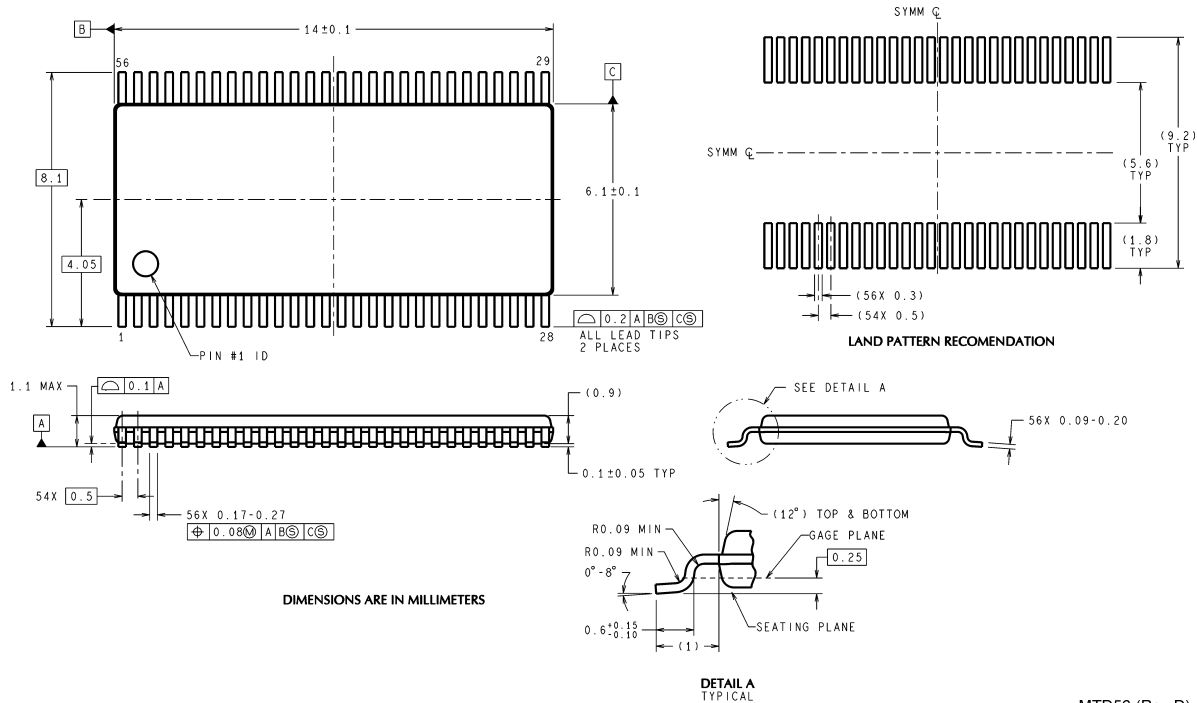
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Typical Application



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Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Molded Thin Shrink Small Outline Package, JEDEC
Order Number DS90CF383BMT
NS Package Number MTD56

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