National Semiconductor

March 2004

ADC11DL066
Dual 11-Bit, 66 MSPS, 450 MHz Input Bandwidth A/D Converter w/Internal Reference

General Description

The ADC11DL066 is a dual, low power monolithic CMOS analog-to-digital converter capable of converting analog input signals into 11-bit digital words at 66 Megasamples per second (MSPS), minimum. This converter uses a differential, pipeline architecture with digital error correction and an on-chip sample-and-hold circuit to minimize die size and power consumption while providing excellent dynamic performance and a 450 MHz Full Power Bandwidth. Operating on a single 3.3V power supply, the ADC11DL066 achieves 10.3 effective bits and consumes just 686 mW at 66 MSPS, including the reference current. The Power Down feature reduces power consumption to 75 mW.

The differential inputs provide a full scale differential input swing equal to 2 times V_{REF} with the possibility of a single-ended input. Full use of the differential input is recommended for optimum performance. The digital outputs from the two ADCs are available on separate 11-bit buses with an output data format choice of offset binary or two's complement.

To ease interfacing to lower voltage systems, the digital output driver power pins of the ADC11DL066 can be connected to a separate supply voltage in the range of 2.4V to the digital supply voltage.

This device is available in the 64-lead TQFP package and will operate over the industrial temperature range of −40˚C to +85˚C. An evaluation board is available to ease the evaluation process.

Features

- Single +3.3V supply operation
- Internal sample-and-hold
- Outputs 2.4V to 3.3V compatible
- Power down mode
- On-chip reference

Key Specifications

■ Resolution	11 Bits
■ DNL	±0.25 LSB (typ)
■ SNR (f_{IN} = 10 MHz)	64 dB (typ)
■ SFDR (f_{IN} = 10 MHz)	80 dB (typ)
■ Data Latency	6 Clock Cycles
■ Power Consumption	
— Operating	686 mW (typ)
— Power Down	75 mW (typ)

Applications

- Ultrasound and Imaging
- Instrumentation
- Communications Receivers
- Sonar/Radar
- xDSL
- Cable Modems
- DSP Front Ends

Connection Diagram

20077301

20040326

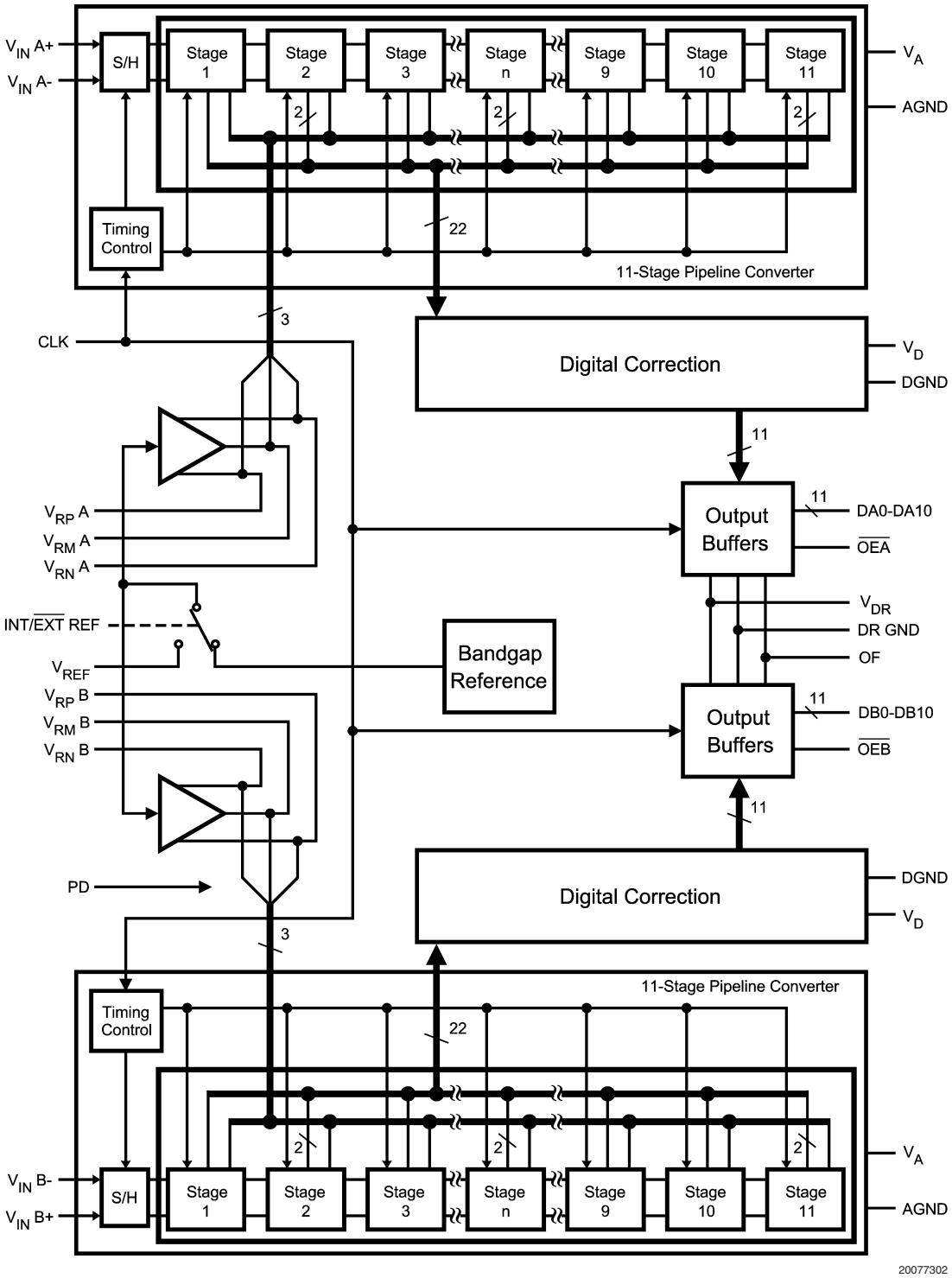
TRI-STATE® is a registered trademark of National Semiconductor Corporation.

ADC11DL066 Dual 11-Bit, 66 MSPS, 450 MHz Input Bandwidth A/D Converter w/Internal Reference

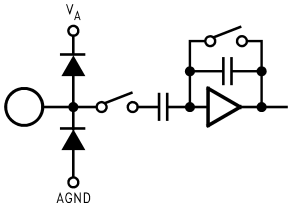
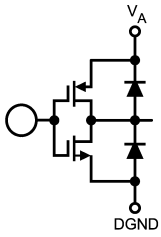
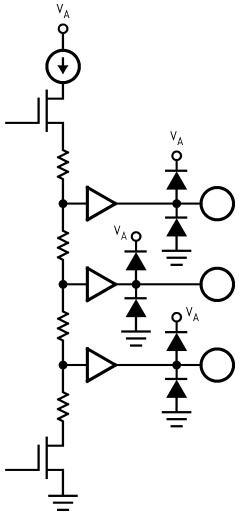
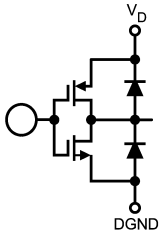
Ordering Information

Industrial (−40˚C T_A +85˚C)	Package
ADC11DL066CIVS	64 Pin TQFP

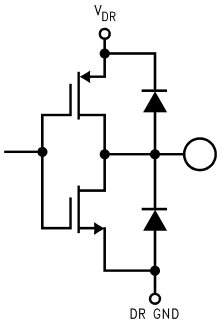
Block Diagram



Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
ANALOG I/O			
15 2	V_{IN}^{A+} V_{IN}^{B+}		Differential analog Inputs. With a 1.0V reference voltage the differential full-scale input signal level is 2.0 V_{P-P} with each input pin voltage centered on a common mode voltage, V_{CM}. The negative input pins may be connected to V_{CM} for single-ended operation, but a differential input signal is required for best performance.
16 1	V_{IN}^{A-} V_{IN}^{B-}		
7	V_{REF}		Reference input. This pin should be bypassed to AGND with a 0.1 µF capacitor when an external reference is used. V_{REF} is 1.0V nominal and should be between 0.8V to 1.5V.
11	$\overline{INT}$/EXT REF		Reference source select pin. With a logic low at this pin the internal 1.0V reference is selected and the V_{REF} pin need not be driven. With a logic high on this pin an external reference voltage should be applied to V_{REF} input pin 7.
13 5	V_{RP}^{A} V_{RP}^{B}		These pins are high impedance reference bypass pins. Bypass per Section 1.2. DO NOT LOAD these pins.
14 4	V_{RM}^{A} V_{RM}^{B}		
12 6	V_{RN}^{A} V_{RN}^{B}		
DIGITAL I/O			
60	CLK		Digital clock input. The range of frequencies for this input is as specified in the electrical tables with guaranteed performance at 66 MHz. The input is sampled on the rising edge of this input.
22 41	$\overline{OEA}$ $\overline{OEB}$		$\overline{OEA}$ and $\overline{OEB}$ are the output enable pins that, when low, holds their respective data output pins in the active state. When either of these pins is high, the corresponding outputs are in a high impedance state.
59	PD		PD is the Power Down input pin. When high, this input puts the converter into the power down mode. When this pin is low, the converter is in the active mode.
21	OF		Output Format pin. A logic low on this pin causes output data to be in offset binary format. A logic high on this pin causes the output data to be in 2's complement format.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
25–29 34–39	DA0–DA10		Digital data output pins that make up the 11-bit conversion results of their respective converters. DA0 and DB0 are the LSBs, while DA10 and DB10 are the MSBs of the output words. Output levels are TTL/CMOS compatible.
43–47 52–57	DB0–DB10		
ANALOG POWER			
9, 18, 19, 62, 63	V_A		Positive analog supply pins. These pins should be connected to a quiet +3.3V source and bypassed to AGND with 0.1 µF capacitors located within 1 cm of these power pins, and with a 10 µF capacitor.
3, 8, 10, 17, 20, 61, 64	AGND		The ground return for the analog supply.
DIGITAL POWER			
33, 48	V_D		Positive digital supply pin. This pin should be connected to the same quiet +3.3V source as is V_A and be bypassed to DGND with a 0.1 µF capacitor located within 1 cm of the power pin and with a 10 µF capacitor.
32, 49	DGND		The ground return for the digital supply.
24, 42	DGND		These two pins are grounded internally and may be grounded or left unconnected.
30, 51	V_{DR}		Positive digital supply pin for the ADC11DL066's output drivers. This pin should be connected to a voltage source of +2.4V to V_D and be bypassed to DR GND with a 0.1 µF capacitor. If the supply for this pin is different from the supply used for V_A and V_D, it should also be bypassed with a 10 µF tantalum capacitor. V_{DR} should never exceed the voltage on V_D. All bypass capacitors should be located within 1 cm of the supply pin.
23, 31, 40, 50, 58	DR GND		The ground return for the digital supply for the ADC11DL066's output drivers. These pins should be connected to the system digital ground, but not be connected in close proximity to the ADC11DL066's DGND or AGND pins. See Section 5 (Layout and Grounding) for more details.

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_A, V_D, V_{DR}	4.2V
$\|V_A - V_D\|$	100 mV
Voltage on Any Input or Output Pin	−0.3V to (V_A or V_D +0.3V)
Input Current at Any Pin (Note 3)	±25 mA
Package Input Current (Note 3)	±50 mA
Package Dissipation at T_A = 25˚C	See (Note 4)
ESD Susceptibility	
Human Body Model (Note 5)	2500V
Machine Model (Note 5)	250V
Soldering Temperature, Infrared, 10 sec. (Note 6)	235˚C
Storage Temperature	−65˚C to +150˚C

Operating Ratings (Notes 1, 2)

Operating Temperature	−40˚C T_A +85˚C
Supply Voltage (V_A, V_D)	+3.0V to +3.6V
Output Driver Supply (V_{DR})	+2.4V to V_D
V_{REF} Input	0.8V to 1.5V
CLK, PD, $\overline{OE}$	−0.05V to (V_D + 0.05V)
Analog Input Pins	0V to (V_A − 0.5V)
V_{CM}	0.5V to 1.8V
|AGND−DGND|	100mV

Converter Electrical Characteristics

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D = +3.3V, V_{DR} = +2.5V, PD = 0V, $\overline{INT}$/EXT REF pin = +3.3V, V_{REF} = +1.0V, f_{CLK} = 66 MHz, f_{IN} = 10 MHz, t_r = t_f = 2 ns, C_L = 15 pF/pin. **Boldface limits apply for T_J = T_{MIN} to T_{MAX}:** all other limits T_J = 25˚C (Notes 7, 8, 9)

Symbol	Parameter	Conditions		Typical (Note 10)	Limits (Note 10)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS						
	Resolution with No Missing Codes				**11**	Bits (min)
INL	Integral Non Linearity (Note 11)			±0.5	**±1.6**	LSB (max)
DNL	Differential Non Linearity			±0.25	**±0.68**	LSB (max)
PGE	Positive Gain Error			0.4	**±4**	%FS (max)
NGE	Negative Gain Error			−0.1	**±3.6**	%FS (max)
TC GE	Gain Error Tempco	−40˚C T_A +85˚C		0.5		ppm/˚C
V_{OFF}	Offset Error (V_{IN}+ = V_{IN}−)			−0.18	**+1.3** **-1.6**	%FS (max) %FS (min)
TC V_{OFF}	Offset Error Tempco	−40˚C T_A +85˚C		0.1		ppm/˚C
	Under Range Output Code			0	**0**	
	Over Range Output Code			2047	**2047**	
REFERENCE AND ANALOG INPUT CHARACTERISTICS						
V_{CM}	Common Mode Input Voltage			1.0	**0.5**	V (min)
					1.8	V (max)
C_{IN}	V_{IN} Input Capacitance (each pin to GND)	V_{IN} = 2.5 Vdc + 0.7 V_{rms}	(CLK LOW)	8		pF
			(CLK HIGH)	7		pF
V_{REF}	Reference Voltage (Note 13)			1.00	**0.8**	V (min)
					1.5	V (max)
	Reference Input Resistance			100		M

Converter Electrical Characteristics (Continued)

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, $V_A = V_D = +3.3V$, $V_{DR} = +2.5V$, PD = 0V, $\overline{INT}$/EXT REF pin = +3.3V, $V_{REF} = +1.0V$, $f_{CLK} = 66$ MHz, $f_{IN} = 10$ MHz, $t_r = t_f = 2$ ns, $C_L = 15$ pF/pin. **Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}:** all other limits $T_J = 25^{\circ}C$ (Notes 7, 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 10)	Units (Limits)
DYNAMIC CONVERTER CHARACTERISTICS					
FPBW	Full Power Bandwidth	0 dBFS Input, Output at –3 dB	450		MHz
SNR	Signal-to-Noise Ratio	f_{IN} = 1 MHz, V_{IN} = –0.5 dBFS	64		dB
		f_{IN} = 10 MHz, V_{IN} = –0.5 dBFS	64	**62**	dB (min)
		f_{IN} = 33 MHz, V_{IN} = –0.5 dBFS	62		dB
SINAD	Signal-to-Noise and Distortion	f_{IN} = 1 MHz, V_{IN} = –0.5 dBFS	63		dB
		f_{IN} = 10 MHz, V_{IN} = –0.5 dBFS	63	**62**	dB (min)
		f_{IN} = 33 MHz, V_{IN} = –0.5 dBFS	62		dB
ENOB	Effective Number of Bits	f_{IN} = 1 MHz, V_{IN} = –0.5 dBFS	10.3		Bits
		f_{IN} = 10 MHz, V_{IN} = –0,5 dBFS	10.3	**10.0**	Bits (min)
		f_{IN} = 33 MHz, V_{IN} = –0,5 dBFS	10.1		Bits
THD	Total Harmonic Distortion	f_{IN} = 1 MHz, V_{IN} = –0.5 dBFS	–78		dB
		f_{IN} = 10 MHz, V_{IN} = –0.5 dBFS	–78	**-69.7**	dB (max)
		f_{IN} = 33 MHz, V_{IN} = –0.5 dBFS	–78		dB
H2	Second Harmonic	f_{IN} = 1 MHz, V_{IN} = –0.5 dBFS	–84		dB
		f_{IN} = 10 MHz, V_{IN} = –0.5 dBFS	–84	**–73.5**	dB (max)
		f_{IN} = 33 MHz, V_{IN} = –0.5 dBFS	–84		dB
H3	Third Harmonic	f_{IN} = 1 MHz, V_{IN} = –0.5 dBFS	–84		dB
		f_{IN} = 10 MHz, V_{IN} = –0.5 dBFS	–84	**–73.3**	dB (max)
		f_{IN} = 33 MHz, V_{IN} = –0.5 dBFS	–83		dB
SFDR	Spurious Free Dynamic Range	f_{IN} = 1 MHz, V_{IN} = –0.5 dBFS	80		dB
		f_{IN} = 10 MHz, V_{IN} = –0.5 dBFS	80	**73.5**	dB (min)
		f_{IN} = 33 MHz, V_{IN} = –0.5 dBFS	74		dB
INTER-CHANNEL CHARACTERISTICS					
	Channel—Channel Offset Match		±0.03		%FS
	Channel—Channel Channel gain Match		±0.1		%FS
	Crosstalk	10 MHz Tested, Channel; 20 MHz Other Channel	80		dB
		10 MHz Tested, Channel; 195 MHz Other Channel	63		dB

DC and Logic Electrical Characteristics

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D = +3.3V, V_{DR} = +2.5V, PD = 0V, $\overline{INT}$/EXT REF pin = 3.3V, V_{REF} = +1.0V, f_{CLK} = 66 MHz, f_{IN} = 10 MHz, t_r = t_f = 2 ns, C_L = 15 pF/pin. **Boldface limits apply for T_J = T_{MIN} to T_{MAX}:** all other limits T_J = 25˚C (Notes 7, 8, 9)

Symbol	Parameter	Conditions		Typical (Note 10)	Limits (Note 10)	Units (Limits)
CLK, PD, $\overline{OE}$ DIGITAL INPUT CHARACTERISTICS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_D = 3.6V			**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	V_D = 3.0V			**1.0**	V (max)
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 3.3V		10		µA
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0V		−10		µA
C_{IN}	Digital Input Capacitance			5		pF
D0–D11 DIGITAL OUTPUT CHARACTERISTICS						
$V_{OUT(1)}$	Logical "1" Output Voltage	I_{OUT} = −0.5 mA	V_{DR} = 2.5V		**2.3**	V (min)
			V_{DR} = 3V		**2.7**	V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	I_{OUT} = 1.6 mA, V_{DR} = 3V			**0.4**	V (max)
I_{OZ}	TRI-STATE® Output Current	V_{OUT} = 2.5V or 3.3V		100		nA
		V_{OUT} = 0V		−100		nA
$+I_{SC}$	Output Short Circuit Source Current	V_{OUT} = 0V		−20		mA
$-I_{SC}$	Output Short Circuit Sink Current	V_{OUT} = V_{DR}		20		mA
C_{OUT}	Digital Output Capacitance			5		pF
POWER SUPPLY CHARACTERISTICS						
I_A	Analog Supply Current	PD Pin = DGND, V_{REF} = 1.0V		197	**237**	mA (max)
		PD Pin = V_{DR}		14		mA
I_D	Digital Supply Current	PD Pin = DGND		11	**35**	mA (max)
		PD Pin = V_{DR}, f_{CLK} = 0		8.7		mA
I_{DR}	Digital Output Supply Current	PD Pin = DGND, C_L = 0 pF (Note 14)		<2		mA
		PD Pin = V_{DR}, f_{CLK} = 0		0		mA
	Total Power Consumption	PD Pin = DGND, C_L = 0 pF (Note 15)		686	**898**	mW (max)
		PD Pin = V_{DR}, f_{CLK} = 0		75		mW
PSRR1	Power Supply Rejection Ratio	Rejection of Full-Scale Error with V_A = 3.0V vs. 3.6V		56		dB
PSRR2	Power Supply Rejection Ratio	Rejection of Power Supply Noise with 10 MHz, 500 mV riding on V_A		44		dB

AC Electrical Characteristics

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D = +3.3V, V_{DR} = +2.5V, PD = 0V, $\overline{INT}$/EXT REF pin = 3.3V, V_{REF} = +1.0V, f_{CLK} = 66 MHz, f_{IN} = 10 MHz, t_r = t_f = 3 ns, C_L = 15 pF/pin. **Boldface limits apply for T_J = T_{MIN} to T_{MAX}:** all other limits T_J = 25˚C (Notes 7, 8, 9, 12)

Symbol	Parameter	Conditions		Typical (Note 10)	Limits (Note 10)	Units (Limits)
f_{CLK}[1]	Maximum Clock Frequency			75	**66**	MHz (min)
f_{CLK}[2]	Minimum Clock Frequency			15		MHz
t_{CH}	Clock High Time				**6.6**	ns (min)
t_{CL}	Clock Low Time				**6.6**	ns (min)
t_{CONV}	Conversion Latency				**6**	Clock Cycles
t_{OD}	Data Output Delay after Rising CLK Edge	V_{DR} = 2.5V	rising	6.6	**9.0**	ns (max)
			falling	5.0	**8.5**	ns (max)
		V_{DR} = 3.3V	rising	5.4	**9.0**	ns (max)
			falling	5.6	**9.0**	ns (max)
t_{AD}	Aperture Delay			2		ns

AC Electrical Characteristics (Continued)

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, $V_A = V_D = +3.3V$, $V_{DR} = +2.5V$, PD = 0V, $\overline{INT}$/EXT REF pin = 3.3V, $V_{REF} = +1.0V$, $f_{CLK} = 66$ MHz, $f_{IN} = 10$ MHz, $t_r = t_f = 3$ ns, $C_L = 15$ pF/pin. **Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}:** all other limits $T_J = 25^\circ C$ (Notes 7, 8, 9, 12)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 10)	Units (Limits)
t_{AJ}	Aperture Jitter		1.2		ps rms
t_{HOLD}	Clock Edge to Data Transition		8		ns
t_{DIS}	Data outputs into TRI-STATE Mode		10		ns
t_{EN}	Data Outputs Active after TRI-STATE		10		ns
t_{PD}	Power Down Mode Exit Cycle	0.1 µF on pins 4, 14; series 1.5 & 1 µF between pins 5, 6 and between pins 12, 13	500		µs

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND = AGND = DGND = 0V, unless otherwise specified.

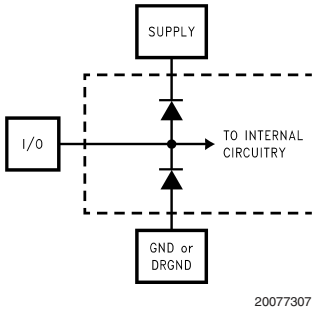
Note 3: When the input voltage at any pin exceeds the power supplies (that is, $V_{IN} <$ AGND, or $V_{IN} > V_A$), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.

Note 4: The absolute maximum junction temperature ($T_J$max) for this device is 150˚C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance ($_{JA}$), and the ambient temperature, (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A) / {}_{JA}$. In the 64-pin TQFP, $_{JA}$ is 50˚C/W, so P_DMAX = 2 Watts at 25˚C and 800 mW at the maximum operating ambient temperature of 85˚C. Note that the power consumption of this device under normal operation will typically be about 726 mW (686 typical power consumption + 40 mW TTL output loading). The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.

Note 5: Human body model is 100 pF capacitor discharged through a 1.5 k resistor. Machine model is 220 pF discharged through 0 .

Note 6: The 235˚C reflow temperature refers to infrared reflow. For Vapor Phase Reflow (VPR), the following Conditions apply: Maintain the temperature at the top of the package body above 183˚C for a minimum 60 seconds. The temperature measured on the package body must not exceed 220˚C. Only one excursion above 183˚C is allowed per reflow cycle.

Note 7: The inputs are protected as shown below. Input voltage magnitudes above V_A or below GND will not damage this device, provided current is limited per (Note 3). However, errors in the A/D conversion can occur if the input goes above V_A or below GND by more than 100 mV. As an example, if V_A is +3.3V, the full-scale input voltage must be +3.4V to ensure accurate conversions.



20077307

Note 8: To guarantee accuracy, it is required that $|V_A - V_D|$ 100 mV and separate bypass capacitors are used at each power supply pin.

Note 9: With the test condition for $V_{REF} = +1.0V$ ($2V_{P-P}$ differential input), the 11-bit LSB is 976 µV.

Note 10: Typical figures are at $T_J = 25^\circ C$, and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 11: Integral Non Linearity is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive and negative full-scale.

Note 12: Timing specifications are tested at TTL logic levels, $V_{IL} = 0.4V$ for a falling edge and $V_{IH} = 2.4V$ for a rising edge.

Note 13: Optimum performance will be obtained by keeping the reference input in the 0.8V to 1.5V range. The LM4051CIM3-ADJ (SOT-23 package) is recommended for external reference applications.

Note 14: I_{DR} is the current consumed by the switching of the output drivers and is primarily determined by load capacitance on the output pins, the supply voltage, V_{DR}, and the rate at which the outputs are switching (which is signal dependent). $I_{DR} = V_{DR}(C_0 \times f_0 + C_1 \times f_1 + ...C_{10} \times f_{10})$ where V_{DR} is the output driver power supply voltage, C_n is total capacitance on the output pin, and f_n is the average frequency at which that pin is toggling.

Note 15: Excludes I_{DR}. See note 14.

Specification Definitions

APERTURE DELAY is the time after the rising edge of the clock to when the input signal is acquired or held for conversion.

APERTURE JITTER (APERTURE UNCERTAINTY) is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

CLOCK DUTY CYCLE is the ratio of the time during one cycle that a repetitive digital waveform is high to the total time of one period. The specification here refers to the ADC clock input signal.

COMMON MODE VOLTAGE (V_{CM}) is the common d.c. voltage applied to both input terminals of the ADC.

CONVERSION LATENCY is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. Data for any given sample is available at the output pins the Pipeline Delay plus the Output Delay after the sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

CROSSTALK is coupling of energy from one channel into the other channel.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated as:

Gain Error = Positive Full Scale Error – Offset Error

A gain of unity occurs when the negative and positive full scale errors are equal to each other, including having the same sign.

GAIN ERROR MATCHING is the difference in gain errors between the two converters divided by the average gain of the converters.

INTEGRAL NON LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the intermodulation products to the total power in the original frequencies. IMD is usually expressed in dBFS.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is $V_{REF}/2^n$, where "n" is the ADC resolution in bits, which is 11 in the case of the ADC11DL066.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC11DL066 is guaranteed not to have any missing codes.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL SCALE ERROR is the difference between the actual first code transition and its ideal value of ½ LSB above negative full scale.

OFFSET ERROR is the difference between the two input voltages (V_{IN^+}–V_{IN}–) required to cause a transition from code 1023 to 1024.

OUTPUT DELAY is the time delay after the rising edge of the clock before the data update is presented at the output pins.

OVER RANGE RECOVERY TIME is the time required after V_{IN} goes from a specified voltage out of the normal input range to a specified voltage within the normal input range and the converter makes a conversion with its rated accuracy.

PIPELINE DELAY (LATENCY) See CONVERSION LATENCY.

POSITIVE FULL SCALE ERROR is the difference between the actual last code transition and its ideal value of 1½ LSB below positive full scale.

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well the ADC rejects a change in the power supply voltage. For the ADC11DL066, PSRR1 is the ratio of the change in Full-Scale Error that results from a change in the dc power supply voltage, expressed in dB. PSRR2 is a measure of how well an a.c. signal riding upon the power supply is rejected at the output.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or dc.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding dc.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

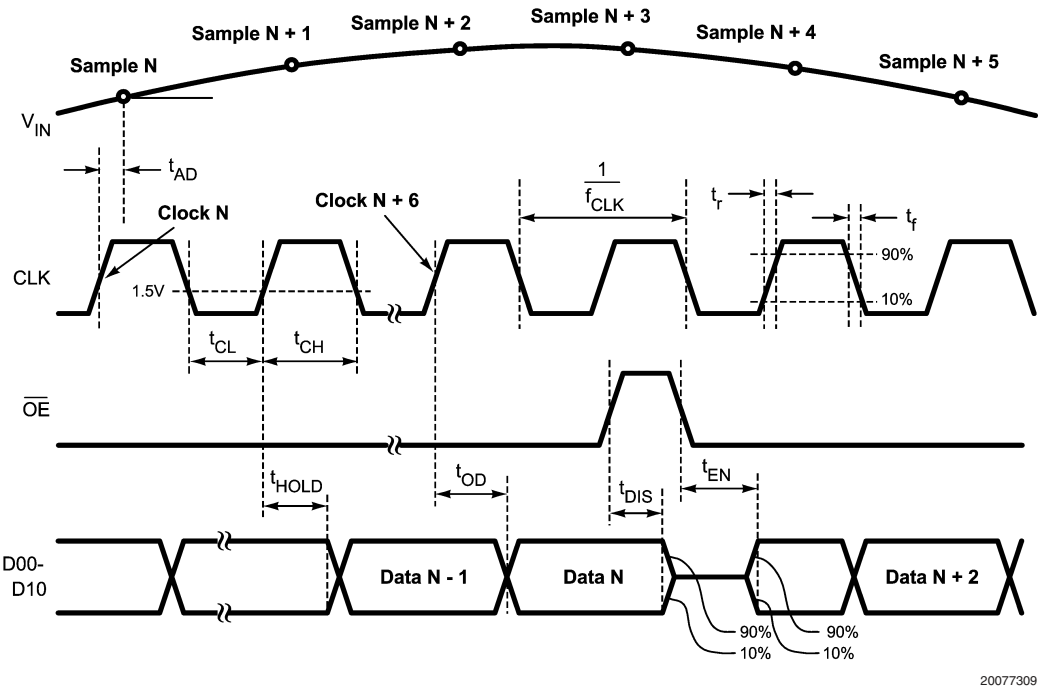
$$THD = 20 \times \log \sqrt{\frac{f_2^2 + \ldots + f_{10}^2}{f_1^2}}$$

where F_1 is the RMS power of the fundamental (output) frequency and f_2 through f_{10} are the RMS power of the first 9 harmonic frequencies in the output spectrum.

– Second Harmonic Distortion (2nd Harm) is the difference expressed in dB, between the RMS power in the input frequency at the output and the power in its 2nd harmonic level at the output.

– Third Harmonic Distortion (3rd Harm) is the difference, expressed in dB, between the RMS power in the input frequency at the output and the power in its 3rd harmonic level at the output.

Timing Diagram



Output Timing

Transfer Characteristic

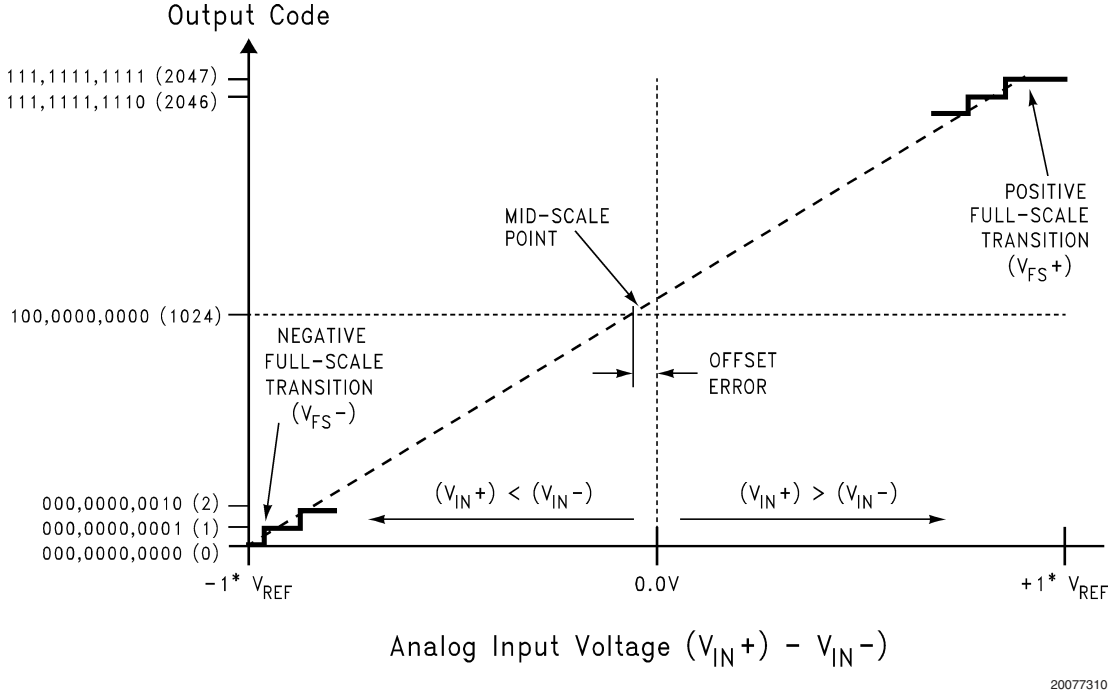


FIGURE 1. Transfer Characteristic

2.0 Applications Information

(Continued)

output capacitance, the more current flows through the die substrate and the greater the noise coupled into the analog channel.

The first solution to keeping digital noise out of the analog supply is to decouple the analog and digital supplies from each other or use separate supplies for them. To keep noise out of the digital supply, keep the output load capacitance as small as practical. If the load capacitance is greater than 50 pF, use a 100 Ω series resistor at the ADC output, located as close to the ADC output pin as practical. This will limit the charge and discharge current of the output capacitance and improve noise performance. Since the series resistor and the load capacitance form a low frequency pole, verify signal integrity once the series resistor has been added.

2.3 LAYOUT AND GROUNDING

Capacitive coupling between the noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry and the clock line as short as possible.

Digital circuits create substantial supply and ground current transients. The logic noise generated could have significant impact upon system noise performance. To avoid performance degradation of the ADC088S052 due to supply noise, do not use the same supply for the ADC088S052 that is used for digital logic.

Generally, analog and digital lines should cross each other at 90 to avoid crosstalk. However, to maximize accuracy in high resolution systems, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. In addition, the clock line should also be treated as a transmission line and be properly terminated.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter s input pins and ground or to the reference input pin and ground should be connected to a very clean point in the ground plane.

We recommend the use of a single, uniform ground plane and the use of split power planes. The power planes should be located within the same board layer. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed over the analog power plane. All digital circuitry and I/O lines should be placed over the digital power plane. Furthermore, all components in the reference circuitry and the input signal chain that are connected to ground should be connected together with short traces and enter the analog ground plane at a single, quiet point.