LDO with Low I_{SUPPLY}, High PSRR

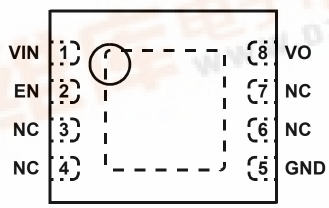
ISL9005 is a high performance Low Dropout linear regulator capable of sourcing 300mA current. It has a low standby current and high-PSRR and is stable with output capacitance of 1µF to 10µF with ESR of up to 200mΩ.

The ISL9005 has a high PSRR of 75dB and output noise less than 45µV_{RMS}. When coupled with a no load quiescent current of 50µA (typical), and 0.1µA shutdown current, the ISL9005 is an ideal choice for portable wireless equipment.

Several different fixed voltage outputs are standard. Other output voltage options for the LDO are available on request and range from 1.3V to 3.6V.

Pinout

ISL9005
(8 LD DFN 2x3)
TOP VIEW



Features

- 300mA high performance LDO
- Excellent transient response to large current steps
- Excellent load regulation: <0.1% voltage change across full range of load current
- High PSRR: 75dB @ 1kHz
- Wide input voltage capability: 2.3V - 6.5V
- Very low quiescent current: 50µA
- Low dropout voltage: typically 200mV @ 300mA
- Low output noise: typically 45µV_{RMS} @ 100µA (1.5V)
- Stable with 1-10µF ceramic capacitors
- Soft-start to limit input current surge during enable
- Current limit and overheat protection
- ±1.8% accuracy over all operating conditions
- Tiny 2x3mm 8 Ld DFN package
- -40°C to +85°C operating temperature range
- Pb-free plus anneal available (RoHS compliant)

Applications

- PDAs, cell phones and smart phones
- Portable instruments, MP3 players
- Handheld devices including medical handhelds

Ordering Information

PART NUMBER (Note 1)	PART MARKING	VO VOLTAGE (V) (Note 2)	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL9005IRNZ-T	ETA	3.3V	-40 to 85	8 Ld DFN 2x3 Tape and Reel	L8.2x3
ISL9005IRMZ-T	ESA	3.0V	-40 to 85	8 Ld DFN 2x3 Tape and Reel	L8.2x3
ISL9005IRLZ-T	ERA	2.9V	-40 to 85	8 Ld DFN 2x3 Tape and Reel	L8.2x3
ISL9005IRKZ-T	EPA	2.85V	-40 to 85	8 Ld DFN 2x3 Tape and Reel	L8.2x3
ISL9005IRJZ-T	ENA	2.8V	-40 to 85	8 Ld DFN 2x3 Tape and Reel	L8.2x3
ISL9005IRRZ-T	EVA	2.6V	-40 to 85	8 Ld DFN 2x3 Tape and Reel	L8.2x3
ISL9005IRFZ-T	EMA	2.5V	-40 to 85	8 Ld DFN 2x3 Tape and Reel	L8.2x3
ISL9005IRCZ-T	ELA	1.8V	-40 to 85	8 Ld DFN 2x3 Tape and Reel	L8.2x3
ISL9005IRBZ-T	EKA	1.5V	-40 to 85	8 Ld DFN 2x3 Tape and Reel	L8.2x3

NOTES:

1. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For other output voltages, contact Intersil Marketing.

Absolute Maximum Ratings

Supply Voltage (VIN) . . . . +7.1V
All Other Pins . . . . -0.3 to (VIN+0.3)V
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . .2500V
Machine Model (Per EIAJ ED-4701 Method C-111) 200V

Recommended Operating Conditions

Ambient Temperature Range (T_A) . . . . -40°C to 85°C
Supply Voltage (VIN) . . . . 2.3 to 6.5V

Thermal Information

Thermal Resistance (Notes 3, 4)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld DFN 2x3 Package	69	10

Junction Temperature Range . . . . -40°C to +125°C
Operating Temperature Range . . . . -40°C to +85°C
Storage Temperature Range . . . . -65°C to +150°C
Maximum Lead Temperature (Soldering 10s) . . . . +300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
4. θ_{JC}, "case temperature" location is at the center of the exposed metal pad on the package underside. See Tech Brief TB379.

Electrical Specifications

Unless otherwise noted, all parameters are guaranteed over the operational supply voltage and temperature range of the device as follows: T_A = -40°C to +85°C; V_{IN} = (V_O+0.5V) to 5.5V with a minimum V_{IN} of 2.3V; C_{IN} = 1µF; C_O = 1µF

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Supply Voltage	V_{IN}		2.3		6.5	V
Ground Current		Quiescent condition: I_O = 0µA				
	I_{DD}	LDO active		50	75	µA
Shutdown Current	I_{DDS}	LDO disabled @ 25°C		0.1	1.0	µA
UVLO Threshold	V_{UV+}		1.9	2.1	2.3	V
	V_{UV-}		1.6	1.8	2.0	V
Regulation Voltage Accuracy		Initial accuracy at V_{IN} = V_O+0.5V, I_O = 10mA, T_J = 25°C	-0.7		+0.7	%
		V_{IN} = V_O+0.5V to 5.5V, I_O = 10µA to 300mA, T_J = 25°C	-0.8		+0.8	%
		V_{IN} = V_O+0.5V to 5.5V, I_O = 10µA to 300mA, T_J = -40°C to 125°C	-1.8		+1.8	%
Maximum Output Current	I_{MAX}	Continuous	300			mA
Internal Current Limit	I_{LIM}		350	475	600	mA
Dropout Voltage (Note 6)	V_{DO1}	I_O = 300mA; V_O < 2.5V		300	500	mV
	V_{DO2}	I_O = 300mA; 2.5V ≤ V_O ≤ 2.8V		250	400	mV
	V_{DO3}	I_O = 300mA; V_O > 2.8V		200	325	mV
Thermal Shutdown Temperature	T_{SD+}			145		°C
	T_{SD-}			110		°C
AC CHARACTERISTICS						
Ripple Rejection (Note 5)		I_O = 10mA, V_{IN} = 2.8V (min), V_O = 1.8V				
		@ 1kHz		75		dB
		@ 10kHz		60		dB
		@ 100kHz		40		dB
Output Noise Voltage (Note 5)		I_O = 100µA, V_O = 1.5V, T_A = 25°C BW = 10Hz to 100kHz		45		μV_{RMS}

Electrical Specifications

Unless otherwise noted, all parameters are guaranteed over the operational supply voltage and temperature range of the device as follows: T_A = -40°C to +85°C; V_{IN} = (V_O+0.5V) to 5.5V with a minimum V_{IN} of 2.3V; C_{IN} = 1µF; C_O = 1µF **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DEVICE START-UP CHARACTERISTICS						
Device Enable TIme	T_{EN}	Time from assertion of the ENx pin to when the output voltage reaches 95% of the VO (nom)		250	500	µs
LDO Soft-start Ramp Rate	T_{SSR}	Slope of linear portion of LDO output voltage ramp during start-up		30	60	µs/V
EN PIN CHARACTERISTICS						
Input Low Voltage	V_{IL}		-0.3		0.5	V
Input High Voltage	V_{IH}		1.4		V_{IN}+0.3	V
Input Leakage Current	I_{IL}, I_{IH}				0.1	µA
Pin Capacitance	C_{PIN}	Informative		5		pF

NOTES:

5. Guaranteed by design and characterization.
6. VOx = 0.98 * VOx(NOM); Valid for VOx greater than 1.85V.

Typical Performance Curves

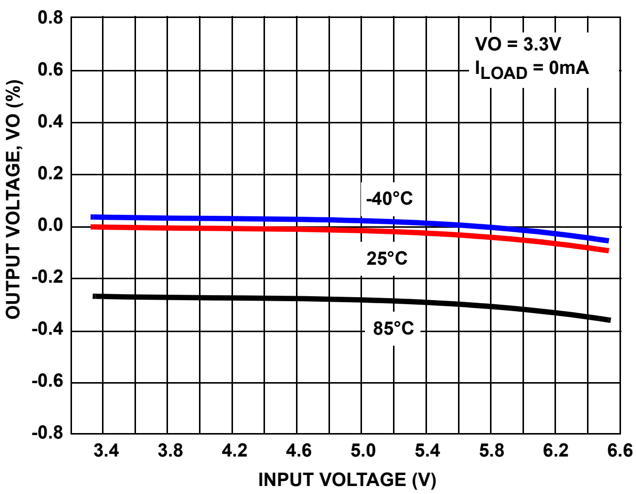


FIGURE 1. OUTPUT VOLTAGE vs INPUT VOLTAGE (3.3V OUTPUT)

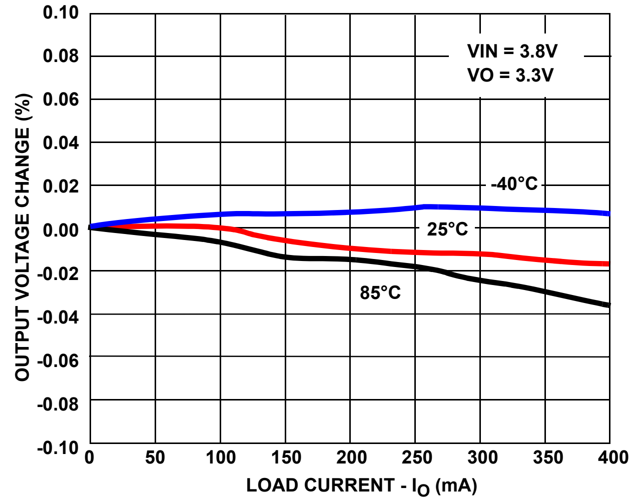


FIGURE 2. OUTPUT VOLTAGE CHANGE vs LOAD CURRENT

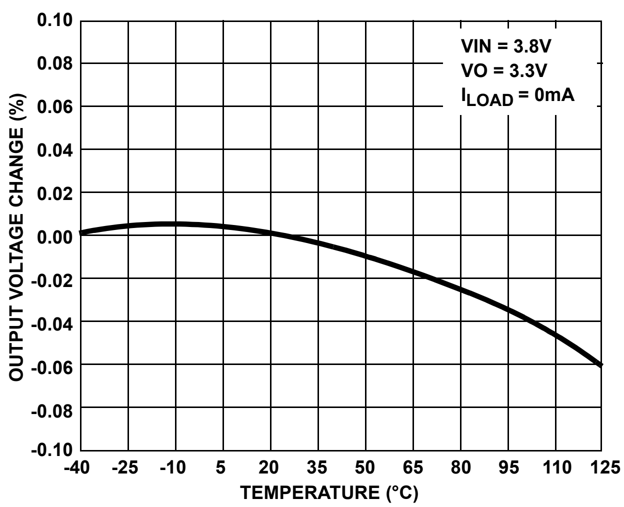


FIGURE 3. OUTPUT VOLTAGE CHANGE vs TEMPERATURE

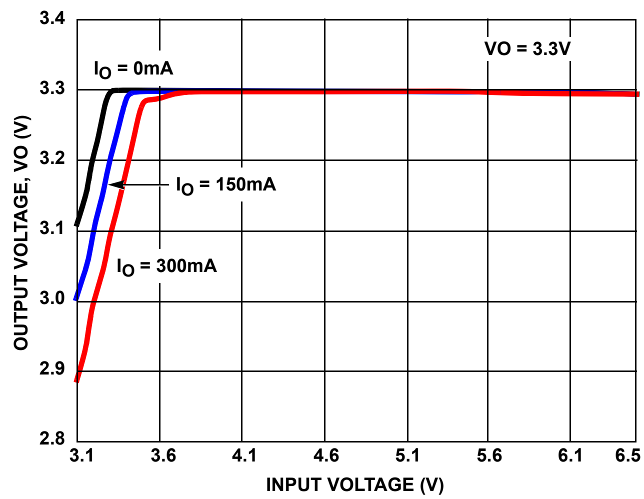


FIGURE 4. OUTPUT VOLTAGE vs INPUT VOLTAGE (3.3V OUTPUT)

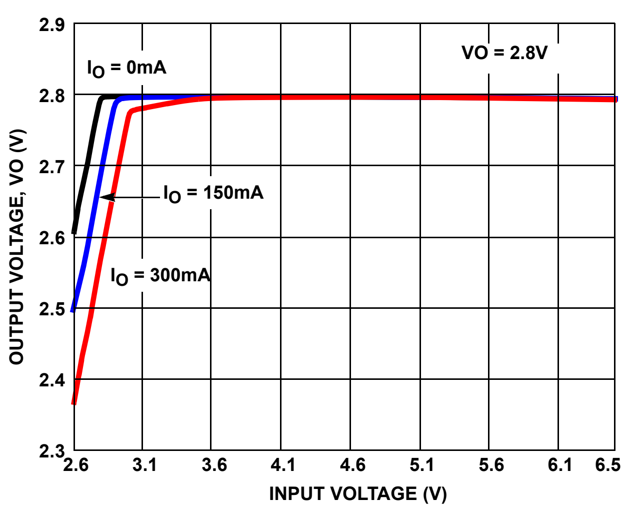


FIGURE 5. OUTPUT VOLTAGE vs INPUT VOLTAGE (2.8V OUTPUT)

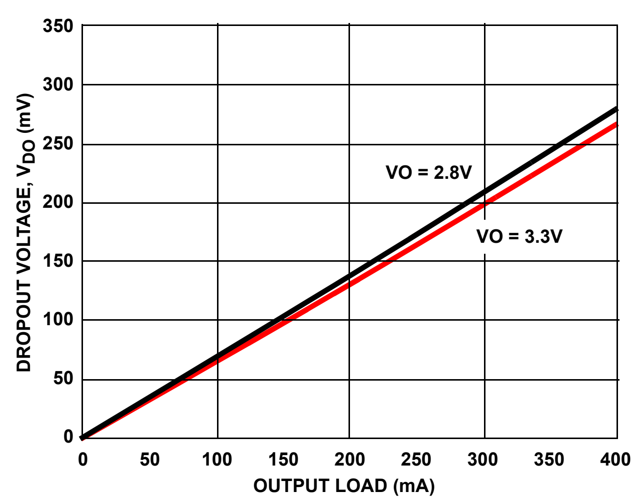


FIGURE 6. DROPOUT VOLTAGE vs LOAD CURRENT

Typical Performance Curves (Continued)

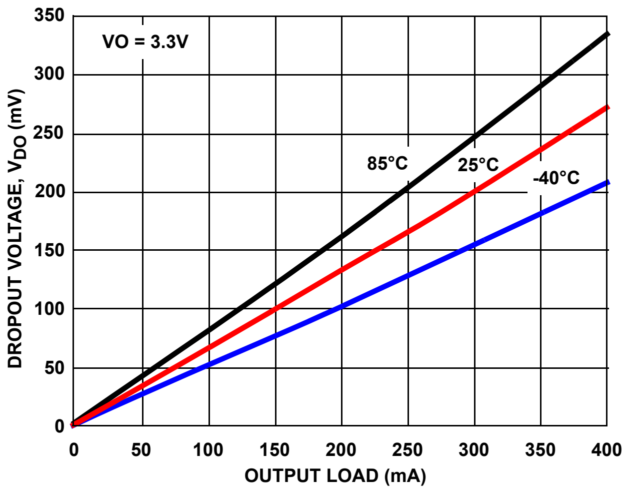


FIGURE 7. DROPOUT VOLTAGE vs LOAD CURRENT

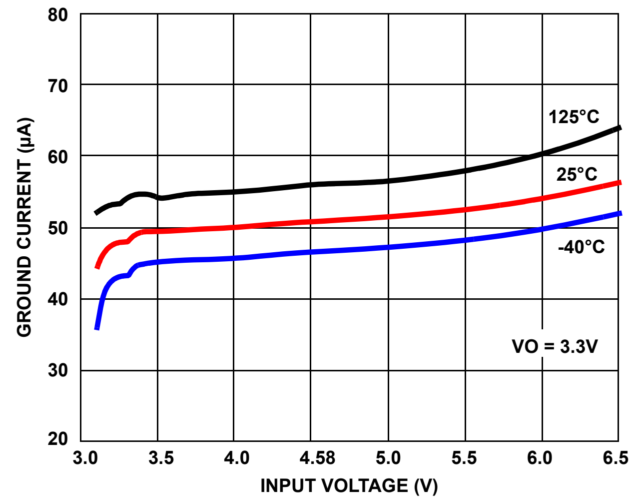


FIGURE 8. GROUND CURRENT vs INPUT VOLTAGE

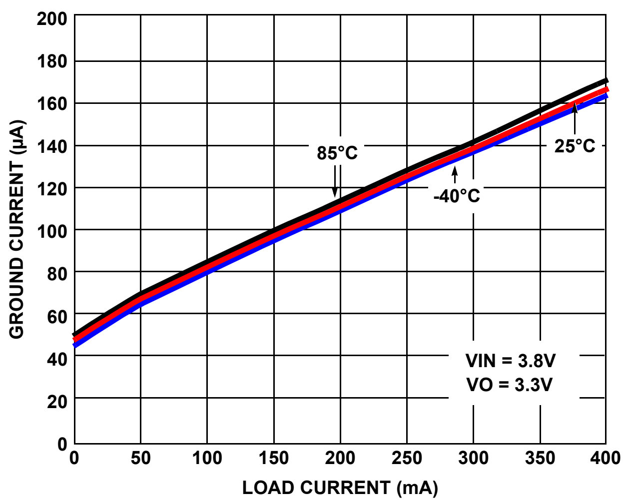


FIGURE 9. GROUND CURRENT vs LOAD

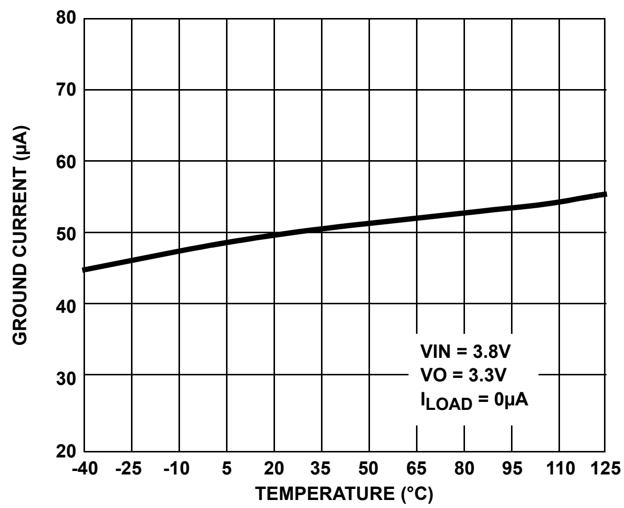


FIGURE 10. GROUND CURRENT vs TEMPERATURE

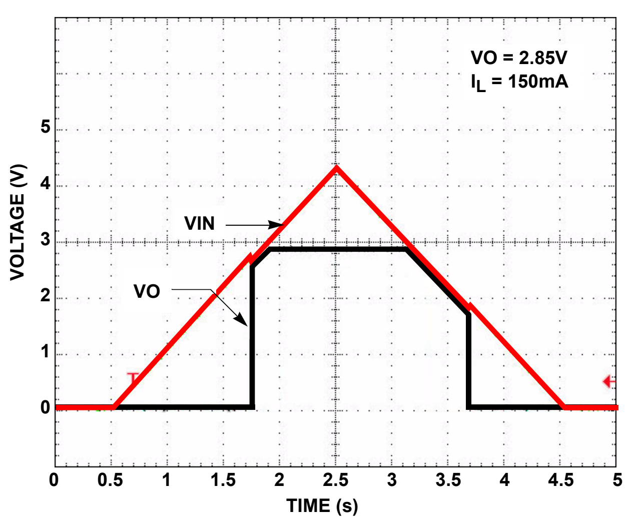


FIGURE 11. POWER-UP/POWER-DOWN

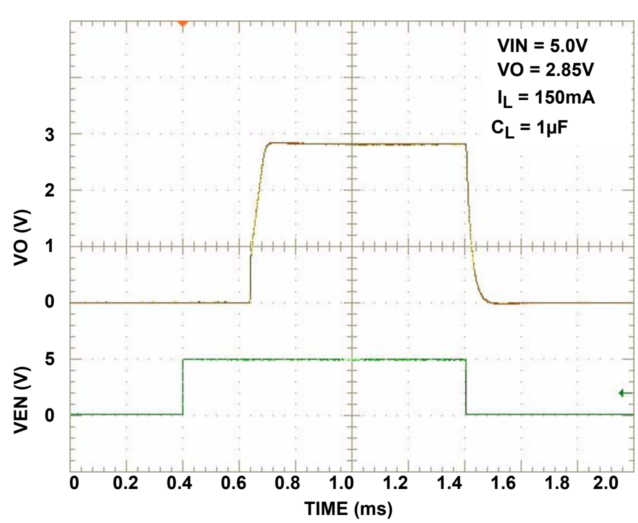


FIGURE 12. TURN ON/TURN OFF RESPONSE

Typical Performance Curves (Continued)

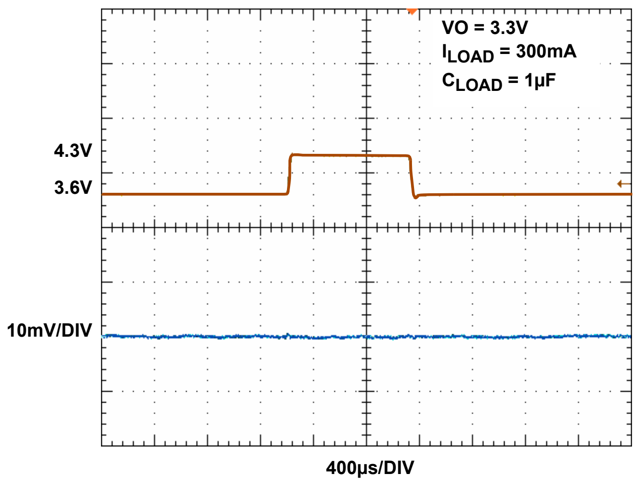


FIGURE 13. LINE TRANSIENT RESPONSE, 3.3V OUTPUT

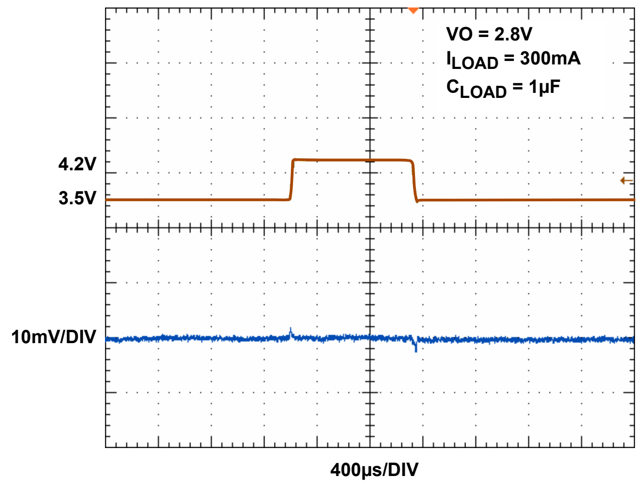


FIGURE 14. LINE TRANSIENT RESPONSE, 2.8V OUTPUT

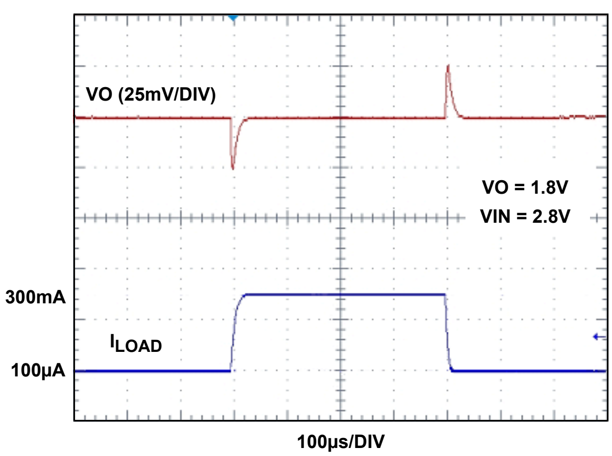


FIGURE 15. LOAD TRANSIENT RESPONSE

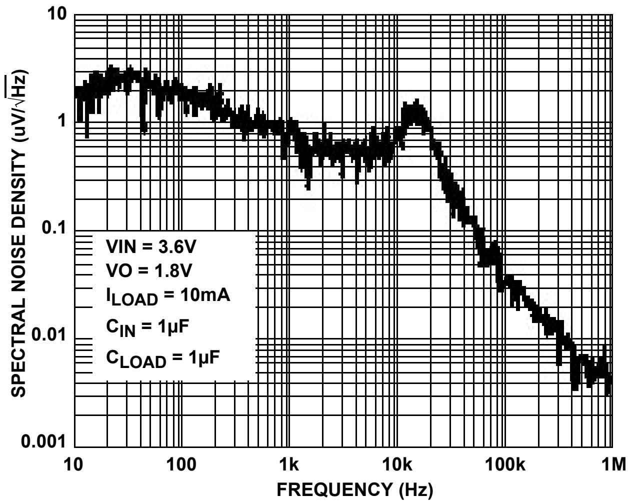


FIGURE 16. SPECTRAL NOISE DENSITY vs FREQUENCY

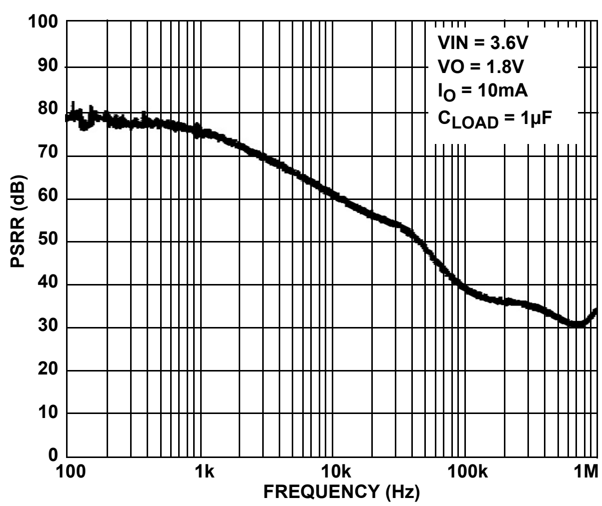
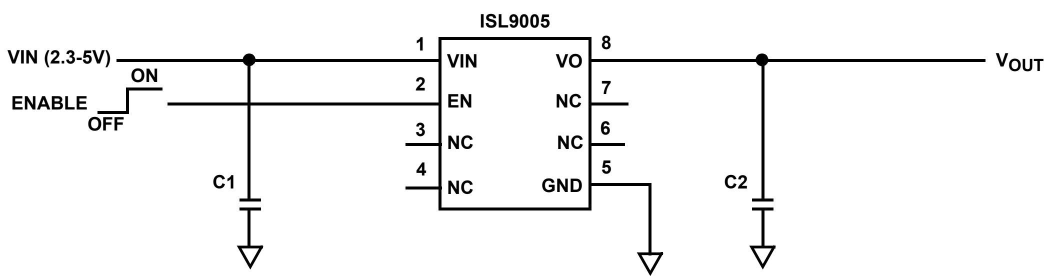


FIGURE 17. PSRR vs FREQUENCY

Pin Description

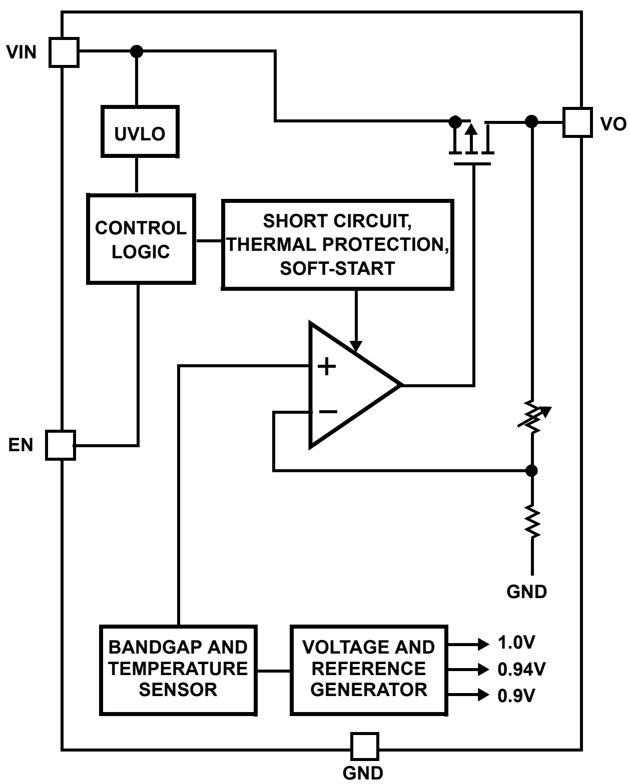
PIN #	PIN NAME	DESCRIPTION
1	VIN	Supply Voltage/LDO Input: Connect a 1µF capacitor to GND.
2	EN	LDO Enable.
3	NC	Do not connect.
4	NC	Do not connect.
5	GND	GND is the connection to system ground. Connect to PCB Ground plane.
6	NC	Do not connect.
7	NC	Do not connect.
8	VO	LDO Output: Connect capacitor of value 1µF to 10µF to GND (1µF recommended).

Typical Application



C1, C2: 1µF X5R ceramic capacitor

Block Diagram



Functional Description

The ISL9005 contains all circuitry required to implement a high performance LDO. High performance is achieved through a circuit that delivers fast transient response to varying load conditions. In a quiescent condition, the ISL9005 adjusts its biasing to achieve the lowest standby current consumption.

The device also integrates current limit protection, smart thermal shutdown protection, and soft-start. Smart Thermal shutdown protects the device against overheating.

Power Control

The ISL9005 has an enable pin, EN, to control power to the LDO output. When EN is low, the device is in shutdown mode. During this condition, all on-chip circuits are off, and the device draws minimum current, typically less than 0.1μA. When the enable pin is asserted, the device first polls the output of the UVLO detector to ensure that VIN voltage is at least about 2.1V. Once verified, the device initiates a start-up sequence. During the start-up sequence, trim settings are first read and latched. Then, sequentially, the bandgap, reference voltage and current generation circuitry power up. Once the references are stable, a fast-start circuit powers up the LDO.

During operation, whenever the VIN voltage drops below about 1.84V, the ISL9005 immediately disables the LDO output. When VIN rises back above 2.1V, the device re-initiates its start-up sequence and LDO operation will resume automatically.

Reference Generation

The reference generation circuitry includes a trimmed bandgap, a trimmed voltage reference divider, a trimmed current reference generator, and an RC noise filter.

The bandgap generates a zero temperature coefficient (TC) voltage for the reference divider. The reference divider provides the regulation reference and other voltage references required for current generation and over-temperature detection.

The current generator outputs references required for adaptive biasing as well as references for LDO output current limit and thermal shutdown determination.

LDO Regulation and Programmable Output Divider

The LDO Regulator is implemented with a high-gain operational amplifier driving a PMOS pass transistor. The design of the ISL9005 provides a regulator that has low quiescent current, fast transient response, and overall stability across all operating and load current conditions. LDO stability is guaranteed for a 1μF to 10μF output capacitor that has a tolerance better than 20% and ESR less than 200mΩ. The design is performance-optimized for a 1μF capacitor. Unless limited by the application, use of an output capacitor value above 4.7μF is not recommended as LDO performance improvement is minimal.

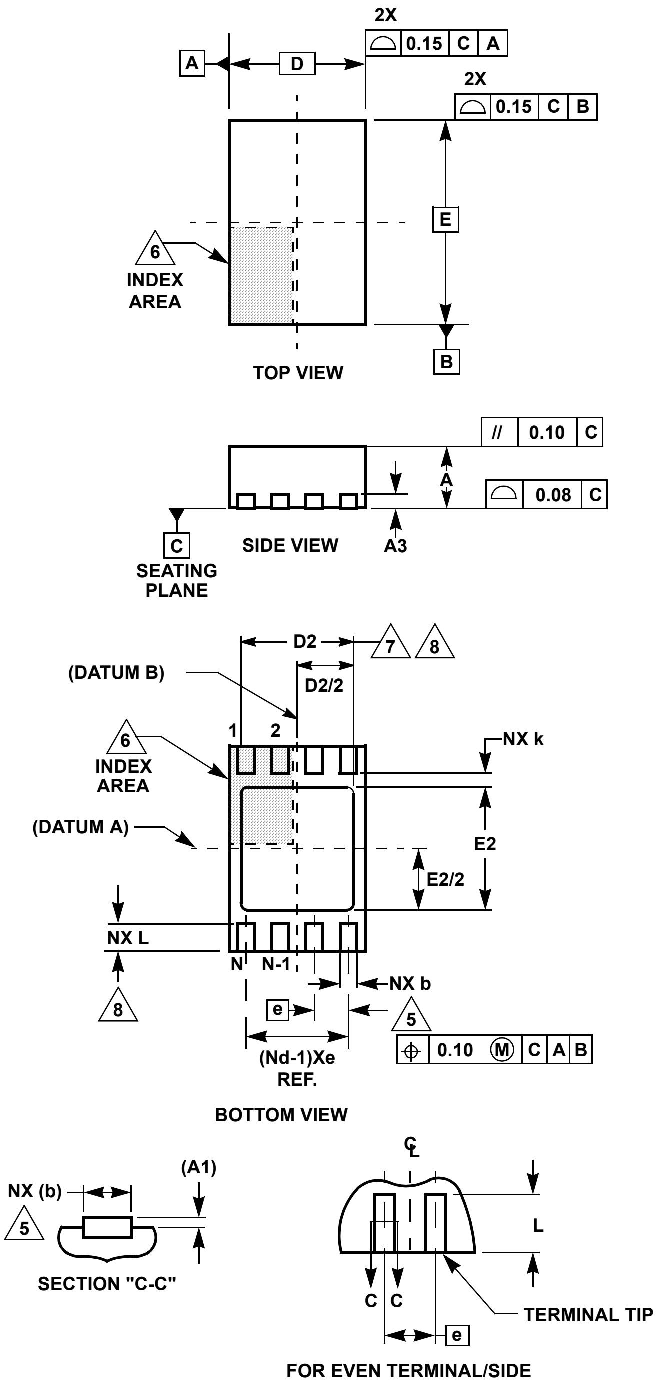
Soft-start circuitry integrated into each LDO limits the initial ramp-up rate to about 30μs/V to minimize current surge. The ISL9005 provides short-circuit protection by limiting the output current to about 425mA.

The LDO uses an independently trimmed 1V reference as its input. An internal resistor divider drops the LDO output voltage down to 1V. This is compared to the 1V reference for regulation. The resistor division ratio is programmed in the factory.

Overheat Detection

The bandgap outputs a proportional-to-temperature current that is indicative of the temperature of the silicon. This current is compared with references to determine if the device is in danger of damage due to overheating. When the die temperature reaches about 140°C, if the LDO is sourcing more than 50mA it shuts down until the die cools sufficiently. Once the die temperature falls back below about 110°C, the disabled LDO is re-enabled and soft-start automatically takes place.

Dual Flat No-Lead Plastic Package (DFN)



L8.2x3

8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A3	0.20 REF			-
b	0.20	0.25	0.32	5,8
D	2.00 BSC			-
D2	1.50	1.65	1.75	7,8
E	3.00 BSC			-
E2	1.65	1.80	1.90	7,8
e	0.50 BSC			-
k	0.20	-	-	-
L	0.30	0.40	0.50	8
N	8			2
Nd	4			3

Rev. 0 6/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.25mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.