Low-Voltage, Single and Dual Supply, 8 to 1 Multiplexer, Dual 4 to 1 Multiplexer and a Triple SPDT Analog Switches

The Intersil ISL84051, ISL84052, ISL84053 devices are precision, bidirectional, analog switches configured as a 8 channel multiplexer/demultiplexer (ISL84051), a dual differential 4 channel multiplexer/demultiplexer (ISL84052) and a triple single pole/double throw (SPDT) switch (ISL84053) designed to operate from a single +2V to +12V supply or from a ±2V to ±6V supply. All devices have an inhibit pin to simultaneously open all signal paths.

ON resistance is 60Ω with a ±5V supply and 125Ω with a single +5V supply. Each switch can handle rail to rail analog signals. The off-leakage current is only 0.1nA at +25°C or 5nA at +85°C with a ±5V supply.

All digital inputs have 0.8V to 2.4V logic thresholds, ensuring TTL/CMOS logic compatibility when using a single +3.3V and +5V supply or dual ±5V supplies.

The ISL84051 is a 8 to 1 multiplexer device. The ISL84052 is a dual 4 to 1 multiplexer device. The ISL84053 is a committed triple SPDT, which is perfect for use in 2-to-1 multiplexer applications.

Table 1 summarizes the performance of this family.

TABLE 1. FEATURES AT A GLANCE

CONFIGURATION	ISL84051 8:1 Mux	ISL84052 DUAL 4:1 Mux	ISL84053 TRIPLE SPDT
±5V R_{ON}	60Ω	60Ω	60Ω
±5V t_{ON}/t_{OFF}	50ns/40ns	50ns/40ns	50ns/40ns
5V R_{ON}	125Ω	125Ω	125Ω
5V t_{ON}/t_{OFF}	90ns/60ns	90ns/60ns	90ns/60ns
3V R_{ON}	250Ω	250Ω	250Ω
3V t_{ON}/t_{OFF}	180ns/100ns	180ns/100ns	180ns/100ns
Packages	16 Ld SOIC, 16 Ld SSOP		

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Application Note AN557 “Recommended Test Procedures for Analog Switches”

Features

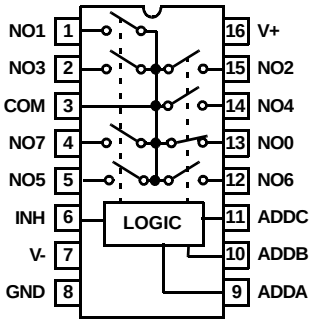
- Drop-in Replacements for MAX4051/A, MAX4052/A and MAX4053/A
- Pin Compatible with MAX4581, MAX4582, MAX4583 and with Industry Standard 74HC4051, 74HC4052 and 74HC4053
- ON Resistance (R_{ON}) Max, V_S = ±5V 100Ω
- ON Resistance (R_{ON}) Max, V_S = +3V 525Ω
- R_{ON} Matching Between Channels . . . . . <6Ω
- Low Charge Injection . . . . . 10pC (Max)
- Single Supply Operation . . . . . +2V to +12V
- Dual Supply Operation . . . . . ±2V to ±6
- Fast Switching Action (V_S = +5V)
  - t_{ON} 90ns
  - t_{OFF} 60ns
- Guaranteed Max Off-leakage @ V_S = ±5V 5nA
- Guaranteed Break-Before-Make
- TTL, CMOS Compatible
- Pb-free available

Applications

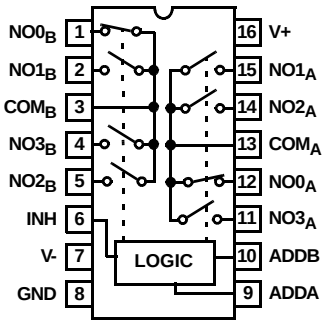
- Portable Equipment
- Communications Systems
  - Radios
  - Telecom Infrastructure
  - ADSL, VDSL Modems
- Test Equipment
  - Medical Ultrasound
  - Magnetic Resonance Image
  - CT and PET Scanners (MRI)
  - ATE
  - Electrocardiograph
- Audio and Video Signal Routing
- Various Circuits
  - +3V/+5V DACs and ADCs
  - Sample and Hold Circuits
  - Operational Amplifier Gain Switching Networks
  - High Frequency Analog Switching
  - High Speed Multiplexing
  - Integrator Reset Circuits

Pinouts

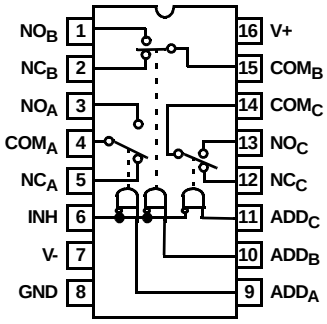
ISL84051 (SOIC, SSOP)
TOP VIEW



ISL84052 (SOIC, SSOP)
TOP VIEW



ISL84053 (SOIC, SSOP)
TOP VIEW



NOTE:

1. Switches Shown for Logic “0” Inputs.

Ordering Information

PART NO.	TEMP. RANGE (^{O}C)	PACKAGE	PKG. DWG. #
ISL84051IB	-40 to 85	16 Ld SOIC	M16.15
ISL84051IBZ (Note)	-40 to 85	16 Ld SOIC (Pb-free)	M16.15
ISL84051IA	-40 to 85	16 Ld SSOP	M16.15A
ISL84051IAZ (Note)	-40 to 85	16 Ld SSOP (Pb-free)	M16.15A
ISL84052IB	-40 to 85	16 Ld SOIC	M16.15
ISL84052IBZ (Note)	-40 to 85	16 Ld SOIC (Pb-free)	M16.15
ISL84052IA	-40 to 85	16 Ld SSOP	M16.15A
ISL84052IAZ (Note)	-40 to 85	16 Ld SSOP (Pb-free)	M16.15A
ISL84053IB	-40 to 85	16 Ld SOIC	M16.15
ISL84053IBZ (Note)	-40 to 85	16 Ld SOIC (Pb-free)	M16.15
ISL84053IA	-40 to 85	16 Ld SSOP	M16.15A
ISL84053IAZ (Note)	-40 to 85	16 Ld SSOP (Pb-free)	M16.15A

*Add “-T” suffix to part number for tape and reel packaging.

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B..

Pin Description

PIN	FUNCTION
V+	Positive Power Supply Input
V-	Negative Power Supply Input. Connect to GND for Single Supply Configurations.
GND	Ground Connection
INH	Digital Control Input. Connect to GND for Normal Operation. Connect to V+ to turn all switches off.
COM	Analog Switch Common Pin
NO	Analog Switch Normally Open Pin
NC	Analog Switch Normally Closed Pin
ADD	Address Input Pin

Truth Tables

ISL84051

INH	ADDC	ADDB	ADDA	SWITCH ON
1	X	X	X	None
0	0	0	0	NO0
0	0	0	1	NO1
0	0	1	0	NO2
0	0	1	1	NO3
0	1	0	0	NO4
0	1	0	1	NO5
0	1	1	0	NO6
0	1	1	1	NO7

ISL84052

INH	ADDB	ADDA	SWITCH ON
1	X	X	None
0	0	0	NO0
0	0	1	NO1
0	1	0	NO2
0	1	1	NO3

ISL84053

INH	ADD_C	ADD_B	ADD_A	SWITCH ON
1	X	X	X	None
0	X	X	0	NC_A
0	X	X	1	NO_A
0	X	0	X	NC_B
0	X	1	X	NO_B
0	0	X	X	NC_C
0	1	X	X	NO_C

NOTE: Logic “0” ≤0.8V. Logic “1” ≥2.4V, with V+ between 2.7V and 10V. X = Don’t Care.

Absolute Maximum Ratings

V+ to V- . . . . . -0.3 to15V
V+ to GND . . . . . -0.3 to15V
V- to GND. . . . . -15 to 0.3V
Input Voltages
INH, NO, NC, ADD (Note 2) . . . . . ((V-)-0.3) to ((V+) + 0.3V)
Output Voltages
COM (Note 2). . . . . ((V-)-0.3) to ((V+) + 0.3V)
Continuous Current (Any Terminal) . . . . . ±30mA
Peak Current NO, NC, or COM
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±100mA
ESD Rating
HBM (Per MIL-STD-883, Method 3015.7) . . . . . >2kV

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (^{o}C/W)
16 Ld SOIC Package	115
16 Ld SSOP Package	160

Maximum Junction Temperature (Plastic Package) . . . . . 150^{o}C
Maximum Storage Temperature Range . . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C
(Lead Tips Only)

Operating Conditions

Temperature Range
ISL8405XIX . . . . . -40^{o}C to 85^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

2. Signals on NC, NO, COM, ADD, or INH exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current ratings.
3. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications: ±5V Supply

Test Conditions: V_{SUPPLY} = ±4.5V to ±5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 4), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (^{o}C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	V-	-	V+	V
ON Resistance, R_{ON}	V_S = ±5V, I_{COM} = 1mA, V_{NO} or V_{NC} = ±3V, (See Figure 5)	25	-	60	100	Ω
		Full	-	-	125	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V_S = ±5V, I_{COM} = 1mA, V_{NO} or V_{NC} = ±3V, (Note 6)	25	-	-	6	Ω
		Full	-	-	12	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V_S = ±5V, I_{COM} = 1mA, V_{NO} or V_{NC} = ±3V, 0V, (Note 7)	25	-	-	10	Ω
		Full	-	-	15	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V_S = ±5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = $\overline{+}$4.5V, (Note 8)	25	-0.1	0.002	0.1	nA
		Full	-5	-	5	nA
COM OFF Leakage Current, $I_{COM(OFF)}$, (ISL84051)	V_S = ±5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = $\overline{+}$4.5V, (Note 8)	25	-0.1	0.002	0.1	nA
		Full	-5	-	5	nA
COM OFF Leakage Current, $I_{COM(OFF)}$, (ISL84052, ISL84053)	V_S = ±5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = $\overline{+}$4.5V, (Note 8)	25	-0.1	0.002	0.1	nA
		Full	-2.5	-	2.5	nA
COM ON Leakage Current, $I_{COM(ON)}$, (ISL84051)	V_S = ±5.5V, V_{COM} = V_{NO} or V_{NC} = ±4.5V, (Note 8)	25	-0.1	0.002	0.1	nA
		Full	-5	-	5	nA
COM ON Leakage Current, $I_{COM(ON)}$, (ISL84052, ISL84053)	V_S = ±5.5V, V_{COM} = V_{NO} or V_{NC} = ±4.5V, (Note 8)	25	-0.1	0.002	0.1	nA
		Full	-2.5	-	2.5	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}, V_{ADDH}		Full	2.4	-	-	V
Input Voltage Low, V_{INL}, V_{ADDL}		Full	-	-	0.8	V
Input Current, I_{INH}, I_{INL}, I_{ADDH}, I_{ADDL}	V_S = ±5.5V, V_{INH}, V_{ADD} = 0V or V+	Full	-1	0.03	1	µA

Electrical Specifications: ±5V Supply Test Conditions: V_{SUPPLY} = ±4.5V to ±5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 4), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS		TEMP (^oC)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
DYNAMIC CHARACTERISTICS							
Inhibit Turn-ON Time, t_{ON}	V_S = ±4.5V, V_{NO} or V_{NC} = ±3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3, (See Figure 1)		25	-	50	175	ns
			Full	-	-	225	ns
Inhibit Turn-OFF Time, t_{OFF}	V_S = ±4.5V, V_{NO} or V_{NC} = ±3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3, (See Figure 1)		25	-	40	150	ns
			Full	-	-	200	ns
Address Transition Time, t_{TRANS}	V_S = ±4.5V, V_{NO} or V_{NC} = ±3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3, (See Figure 1)		25	-	75	250	ns
Break-Before-Make Time, t_{BBM}	V_S = ±5.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, (See Figure 3)		25	2	10	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω, (See Figure 2)		25	-	2	10	pC
NO/NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, (See Figure 7)		25	-	3	-	pF
COM OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, (See Figure 7)	ISL84051	25	-	21	-	pF
		ISL84052	25	-	12	-	pF
		ISL84053	25	-	9	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V, (See Figure 7)	ISL84051	25	-	26	-	pF
		ISL84052	25	-	18	-	pF
		ISL84053	25	-	14	-	pF
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 100kHz, V_{NO} or V_{NC} = $1V_{RMS}$, (See Figures 4 and 6)		25	-	<90	-	dB
Crosstalk, (Note 9) (ISL84052, ISL84053 only)			25	-	<-90	-	dB
POWER SUPPLY CHARACTERISTICS							
Power Supply Range			Full	±2	-	±6	V
Positive Supply Current, I+	V_S = ±5.5V, V_{INH}, V_{ADD} = 0V or V+, Switch On or Off		25	-1	0.1	1	µA
			Full	-10	-	10	µA
Negative Supply Current, I-			25	-1	0.1	1	µA
			Full	-10	-	10	µA

NOTES:

4. V_{IN} = Input voltage to perform proper function.
5. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. $\Delta R_{ON} = R_{ON}$ (MAX) - R_{ON} (MIN).
7. Flatness is defined as the difference between maximum and minimum value of on-resistance over the specified analog signal range.
8. Leakage parameter is 100% tested at high temp, and guaranteed by correlation at 25^{o}C.
9. Between any two switches.

Electrical Specifications: 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, V- = GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 4), Unless Otherwise Specified

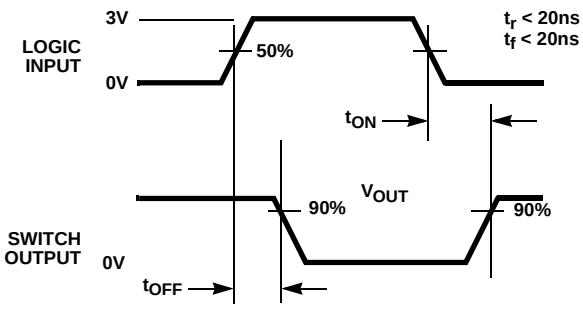
PARAMETER	TEST CONDITIONS	TEMP (^oC)	MIN (NOTE 5)	TYP	MAX (NOTE 5)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3.5V, (See Figure 5)	25	-	125	225	Ω
		Full	-	-	280	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5.5V, V_{COM} = 0V, 4.5V, V_{NO} or V_{NC} = 4.5V, 0V, (Note 8)	25	-1	0.002	1	nA
		Full	-10	-	10	nA
COM OFF Leakage Current, $I_{COM(OFF)}$, (ISL84051)	V+ = 5.5V, V_{COM} = 0V, 4.5V, V_{NO} or V_{NC} = 4.5V, 0V, (Note 8)	25	-1	0.002	1	nA
		Full	-10	-	10	nA
COM OFF Leakage Current, $I_{COM(OFF)}$, (ISL84052, ISL84053)	V+ = 5.5V, V_{COM} = 0V, 4.5V, V_{NO} or V_{NC} = 4.5V, 0V, (Note 8)	25	-1	0.002	1	nA
		Full	-5	-	5	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 5.5V, V_{COM} = V_{NO} or V_{NC} = 4.5V, (Note 8)	25	-1	0.002	1	nA
		Full	-10	-	10	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}, V_{ADDH}		Full	2.4	-	-	V
Input Voltage Low, V_{INL}, V_{ADDL}		Full	-	-	0.8	V
Input Current, I_{INH}, I_{INL}, I_{ADDH}, I_{ADDL}	V+ = 5.5V, V_{INH}, V_{ADD} = 0V or V+	Full	-1	0.03	1	µA
DYNAMIC CHARACTERISTICS						
Inhibit Turn-ON Time, t_{ON}	V+ = 4.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, (See Figure 1)	25	-	90	200	ns
		Full	-	-	275	ns
Inhibit Turn-OFF Time, t_{OFF}	V+ = 4.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, (See Figure 1)	25	-	60	125	ns
		Full	-	-	175	ns
Break-Before-Make Time, t_{BBM}	V+ = 5.5V, V_{NO} or V_{NC} = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, (See Figure 3)	25	-	30	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω, (See Figure 2)	25	-	2	10	pC
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 100kHz, V_{NO} or V_{NC} = $1V_{RMS}$, (See Figures 4 and 6)	25	-	<90	-	dB
Crosstalk, (Note 9) (ISL84052, ISL840533 only)		25	-	<-90	-	dB
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	2	-	12	V
Positive Supply Current, I+	V+ = 5.5V, V- = 0V, V_{INH}, V_{ADD} = 0V or V+, Switch On or Off	25	-1	-	1	µA
		Full	-10	-	10	µA

Electrical Specifications: 3.3V Supply

Test Conditions: V+ = +3.0V to +3.6V, V- = GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 4), Unless Otherwise Specified

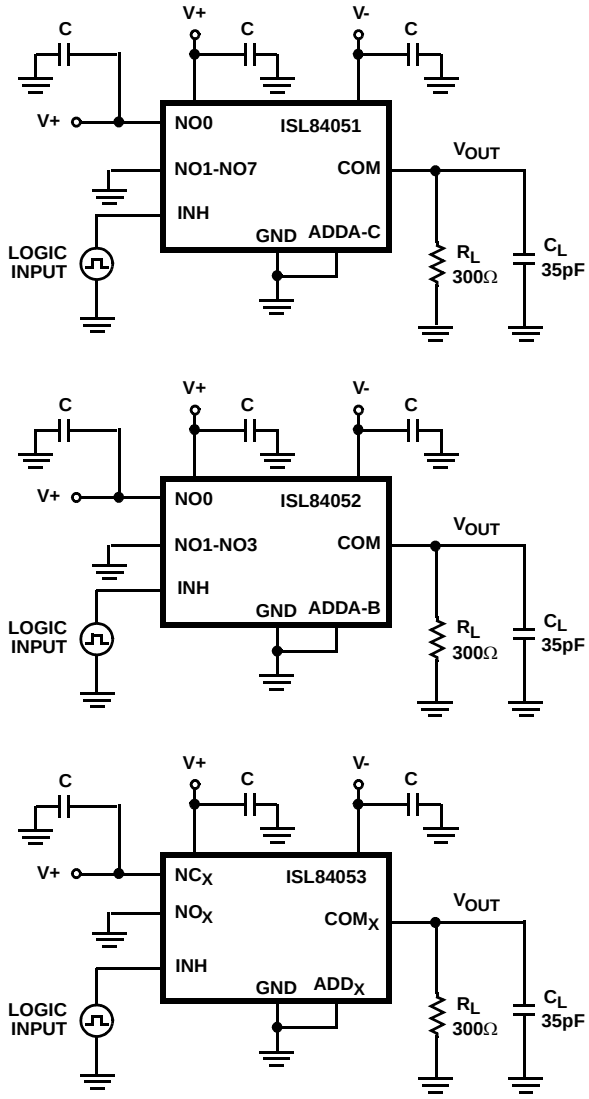
PARAMETER	TEST CONDITIONS	TEMP (^oC)	MIN (NOTE 5)	TYP	MAX (NOTE 5)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 3V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1.5V	25	-	250	525	Ω
		Full	-	-	700	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 3.6V, V_{COM} = 0V, 3V, V_{NO} or V_{NC} = 3V, 0V, (Note 8)	25	-1	0.002	1	nA
		Full	-10	-	10	nA
COM OFF Leakage Current, $I_{COM(OFF)}$, (ISL84051)	V+ = 3.6V, V_{COM} = 0V, 3V, V_{NO} or V_{NC} = 3V, 0V, (Note 8)	25	-1	0.002	1	nA
		Full	-10	-	10	nA
COM OFF Leakage Current, $I_{COM(OFF)}$, (ISL84052, ISL84053)	V+ = 3.6V, V_{COM} = 0V, 3V, V_{NO} or V_{NC} = 3V, 0V, (Note 8)	25	-1	0.002	1	nA
		Full	-5	-	5	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 3.6V, V_{COM} = V_{NO} or V_{NC} = 3V, (Note 8)	25	-1	0.002	1	nA
		Full	-10	-	10	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}, V_{ADDH}		Full	2.4	-	-	V
Input Voltage Low, V_{INL}, V_{ADDL}		Full	-	-	0.8	V
Input Current, I_{INH}, I_{INL}, I_{ADDH}, I_{ADDL}	V+ = 3.6V, V_{INH}, V_{ADD} = 0V or V+	Full	-1	0.03	1	µA
DYNAMIC CHARACTERISTICS						
Inhibit Turn-ON Time, t_{ON}	V+ = 3V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, (See Figure 1)	25	-	180	600	ns
		Full	-	-	700	ns
Inhibit Turn-OFF Time, t_{OFF}	V+ = 3V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, (See Figure 1)	25	-	100	300	ns
		Full	-	-	400	ns
Break-Before-Make Time, t_{BBM}	V+ = 3.6V, V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0 to 3V, (See Figure 3)	25	-	90	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω, (See Figure 2)	25	-	1	10	pC
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 100kHz, V_{NO} or V_{NC} = $1V_{RMS}$, (See Figures 4 and 6)	25	-	<-90	-	dB
Crosstalk, (Note 9) (ISL84052, ISL84053 only)		25	-	<-90	-	dB
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	2	-	12	V
Positive Supply Current, I+	V+ = 3.6V, V- = 0V, V_{INH}, V_{ADD} = 0V or V+, Switch On or Off	25	-1	-	1	µA
		Full	-10	-	10	µA

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. INHIBIT t_{ON}/t_{OFF} MEASUREMENT POINTS

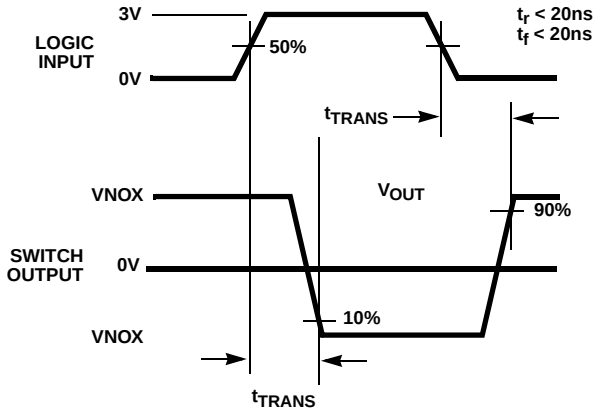


Repeat test for other switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + R_{(ON)}}$$

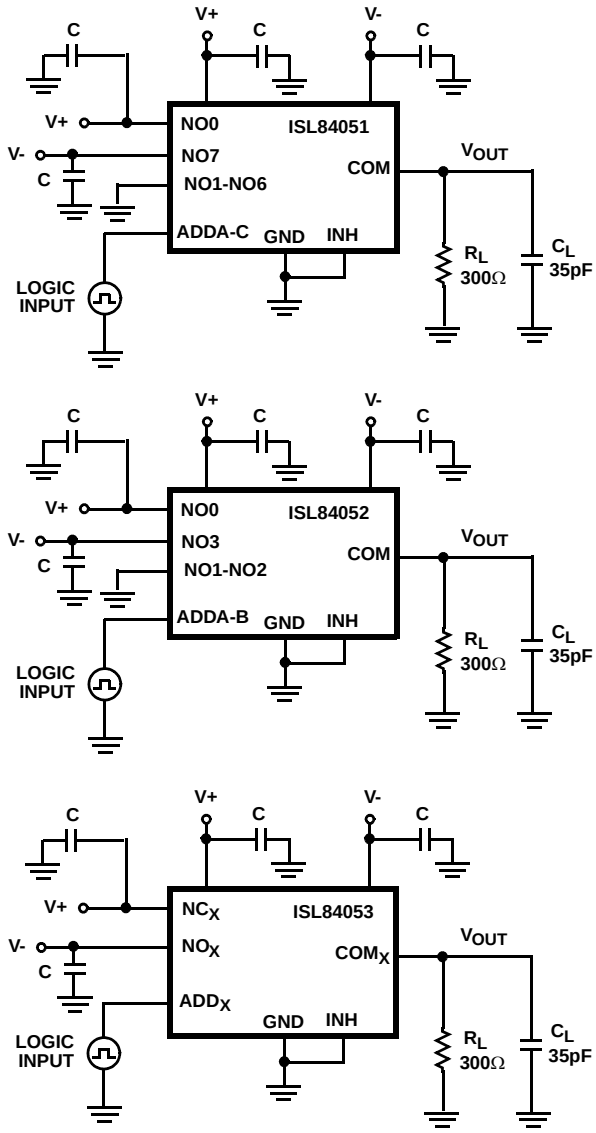
FIGURE 1B. INHIBIT t_{ON}/t_{OFF} TEST CIRCUIT

Test Circuits and Waveforms (Continued)



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1C. ADDRESS t_{TRANS} MEASUREMENT POINTS



Repeat test for other switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO \text{ or } NC)} \frac{R_L}{R_L + R_{(ON)}}$$

FIGURE 1D. ADDRESS t_{TRANS} TEST CIRCUIT

FIGURE 1. SWITCHING TIMES (Continued)

Test Circuits and Waveforms (Continued)

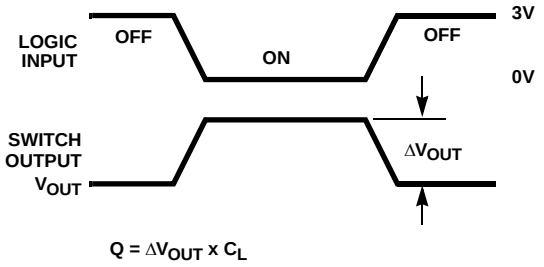
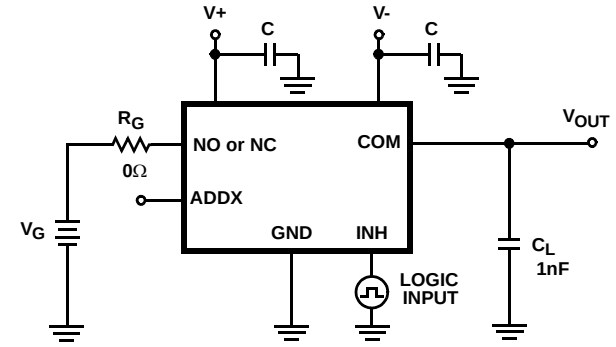


FIGURE 2A. Q MEASUREMENT POINTS



Repeat test for other switches.

FIGURE 2B. Q TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

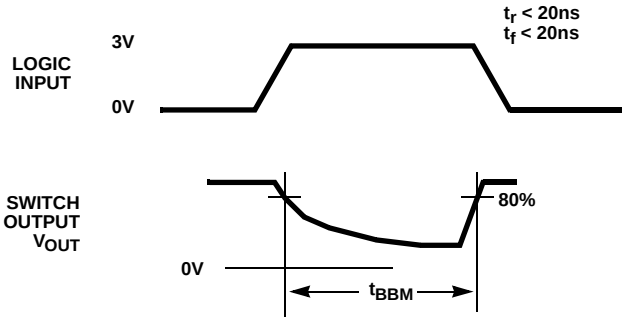
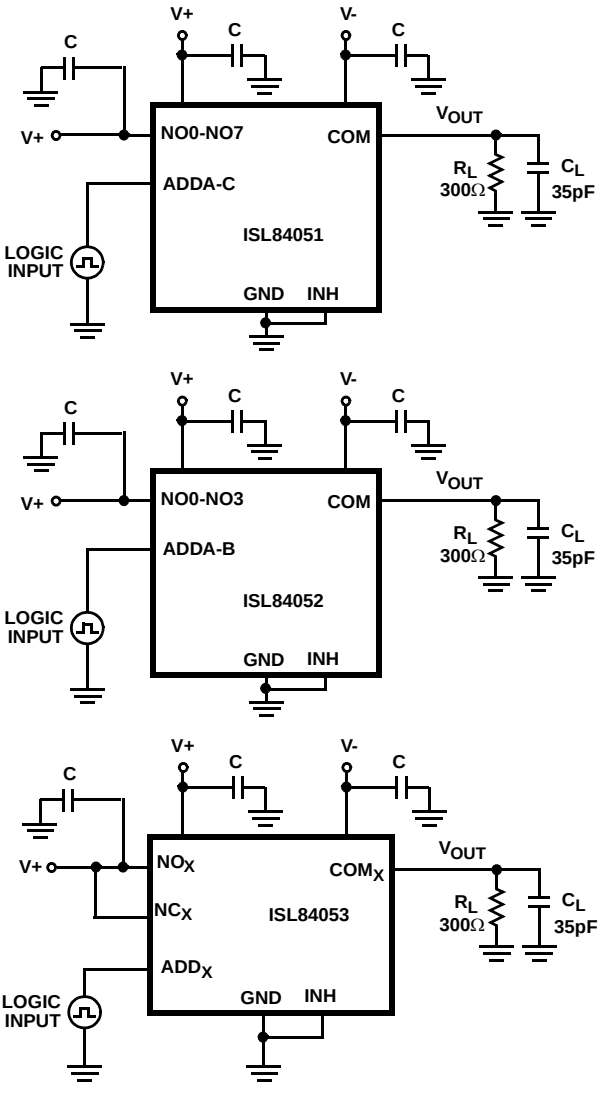


FIGURE 3A. t_{BBM} MEASUREMENT POINTS



Repeat test for other switches. C_L includes fixture and stray capacitance.

FIGURE 3B. t_{BBM} TEST CIRCUIT

FIGURE 3. BREAK-BEFORE-MAKE TIME

Test Circuits and Waveforms (Continued)

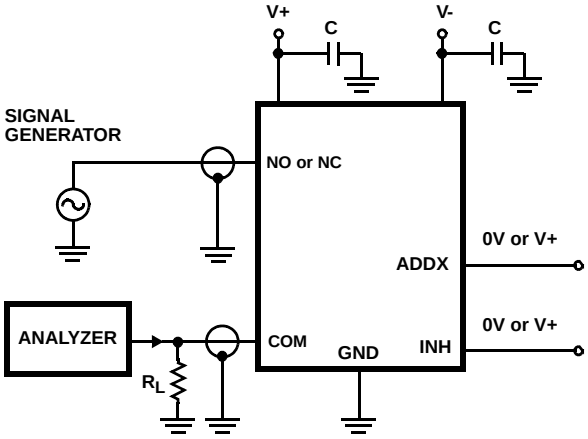


FIGURE 4. OFF ISOLATION TEST CIRCUIT

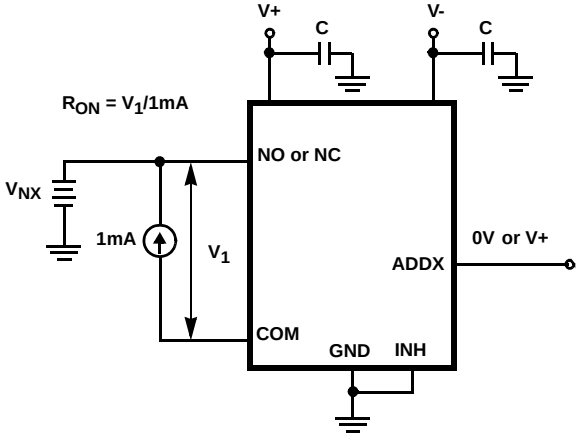


FIGURE 5. R_{ON} TEST CIRCUIT

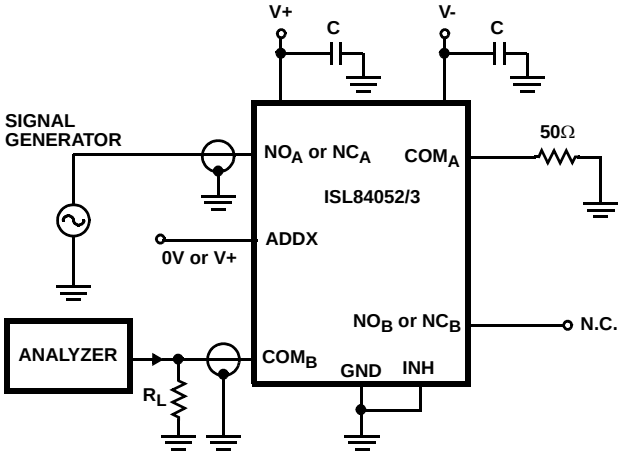


FIGURE 6. CROSSTALK TEST CIRCUIT

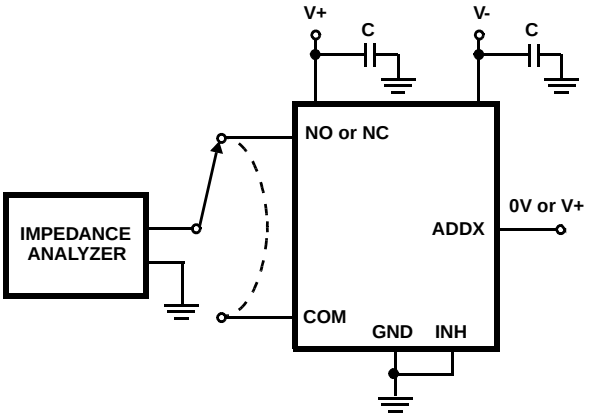


FIGURE 7. CAPACITANCE TEST CIRCUIT

Detailed Description

The ISL84051, ISL84052, ISL84053 analog switches offer precise switching capability from a bipolar ±2V to ±6V or a single 2V to 12V supply with low on-resistance (60Ω) and high speed operation (t_{ON} = 50ns, t_{OFF} = 40ns). The devices are especially well suited to portable battery powered equipment thanks to the low operating supply voltage (2V), low power consumption (3µW), low leakage currents (5nA max). High frequency applications also benefit from the wide bandwidth, and the very high off isolation and crosstalk rejection.

Supply Sequencing And Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to V- (see Figure 8). To prevent forward biasing these diodes, V+ and V- must be applied before any input signals, and input signal voltages must remain between V+ and V-. If these conditions cannot be guaranteed, then one of the following two protection methods should be employed.

Logic inputs can easily be protected by adding a 1kΩ resistor in series with the input (see Figure 8). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

This method is not applicable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low R_{ON} switch, so two small signal diodes can be added in series with the supply pins to provide overvoltage protection for all pins (see Figure 8). These additional diodes limit the analog signal from 1V below V+ to 1V above V-. The low leakage current performance is unaffected by this approach, but the switch resistance may increase, especially at low supply voltages.

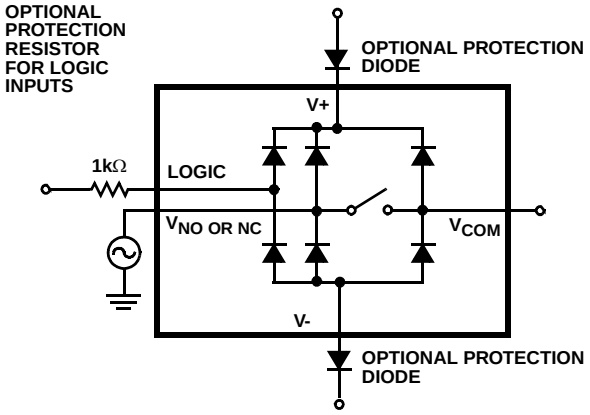


FIGURE 8. INPUT OVERVOLTAGE PROTECTION

Power-Supply Considerations

The ISL8405X construction is typical of most CMOS analog switches, in that they have three supply pins: V+, V-, and GND. V+ and V- drive the internal CMOS switches and set their analog voltage limits, so there are no connections between the analog signal path and GND. Unlike switches with a 13V maximum supply voltage, the ISL8405X 15V maximum supply voltage provides plenty of room for the 10% tolerance of 12V supplies (±6V or 12V single supply), as well as room for overshoot and noise spikes.

This family of switches performs equally well when operated with bipolar or single voltage supplies. The minimum recommended supply voltage is 2V or ±2V. It is important to note that the input signal range, switching times, and on-resistance degrade at lower supply voltages. Refer to the electrical specification tables and *Typical Performance* curves for details.

V+ and GND power the internal logic (thus setting the digital switching point) and level shifters. The level shifters convert the logic levels to switched V+ and V- signals to drive the analog switch gate terminals.

Logic-Level Thresholds

V+ and GND power the internal logic stages, so V- has no affect on logic thresholds. This switch family is TTL compatible (0.8V and 2.4V) over a V+ supply range of 2.7V to 10V. At 12V the V_{IH} level is about 3.5V. This is still below the CMOS guaranteed high output minimum level of 4V, but noise margin is reduced. For best results with a 12V supply, use a logic family that provides a V_{OH} greater than 4V.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat even past 100MHz (see Figure 17). Figure 17 also illustrates that the frequency response is very consistent over varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feed through from a switch's input to its output. Off Isolation is the resistance to this feed through, while Crosstalk indicates the amount of feed through from one switch to another. Figure 18 details the high Off Isolation and Crosstalk rejection provided by this family. At 10MHz, Off Isolation is about 55dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease Off Isolation and Crosstalk rejection due to the voltage divider action of the switch OFF impedance and the load impedance.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and V-. One of these diodes conducts if any analog signal exceeds V+ or V-.

Virtually all the analog leakage current comes from the ESD diodes to V+ or V-. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and V- pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and GND.

Typical Performance Curves $T_A = 25^oC$, Unless Otherwise Specified

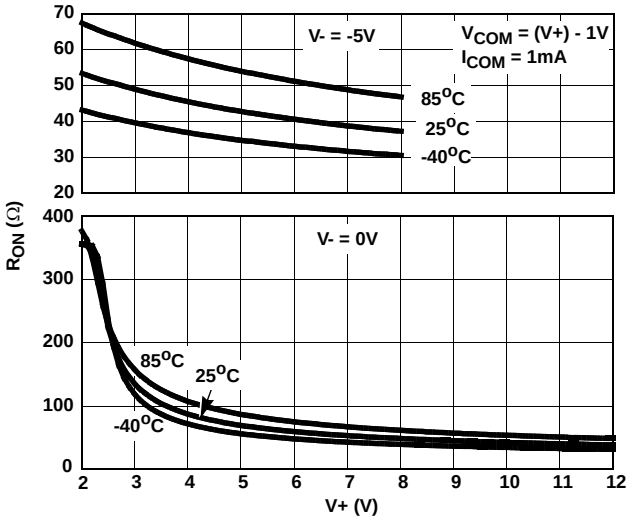


FIGURE 9. ON RESISTANCE vs SUPPLY VOLTAGE

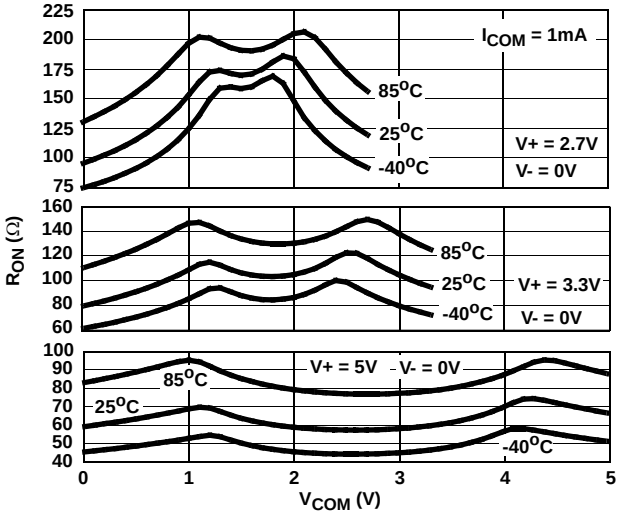


FIGURE 10. ON RESISTANCE vs SWITCH VOLTAGE

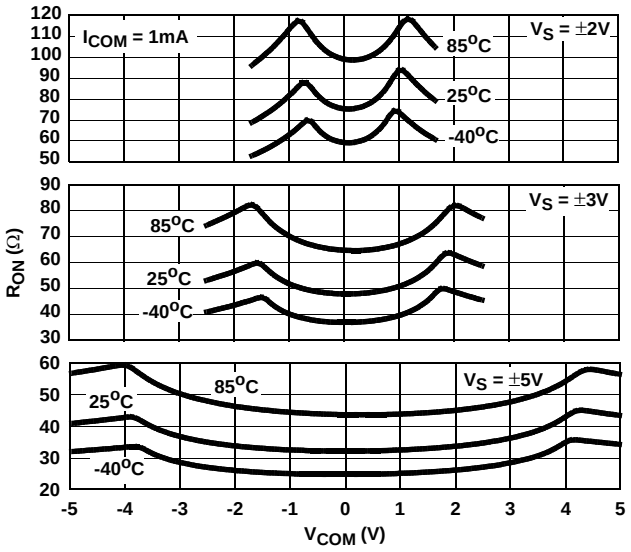


FIGURE 11. ON RESISTANCE vs SWITCH VOLTAGE

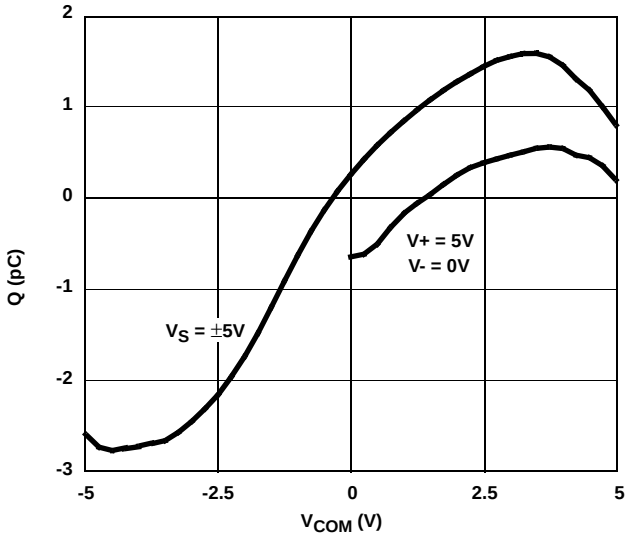


FIGURE 12. CHARGE INJECTION vs SWITCH VOLTAGE

Typical Performance Curves $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

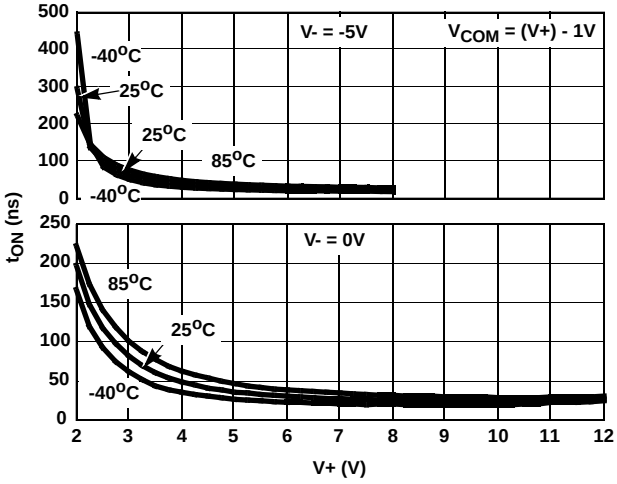


FIGURE 13. INHIBIT TURN - ON TIME vs SUPPLY VOLTAGE

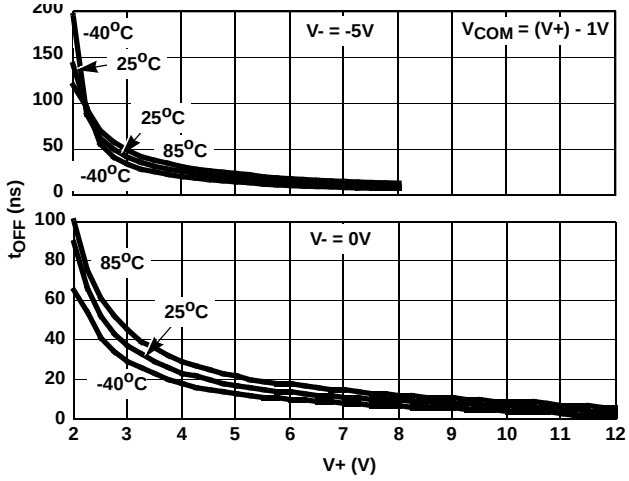


FIGURE 14. INHIBIT TURN - OFF TIME vs SUPPLY VOLTAGE

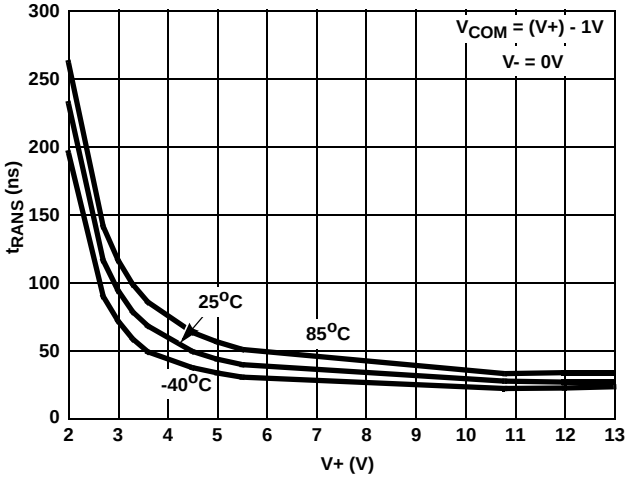


FIGURE 15. ADDRESS TRANS TIME vs SINGLE SUPPLY VOLTAGE

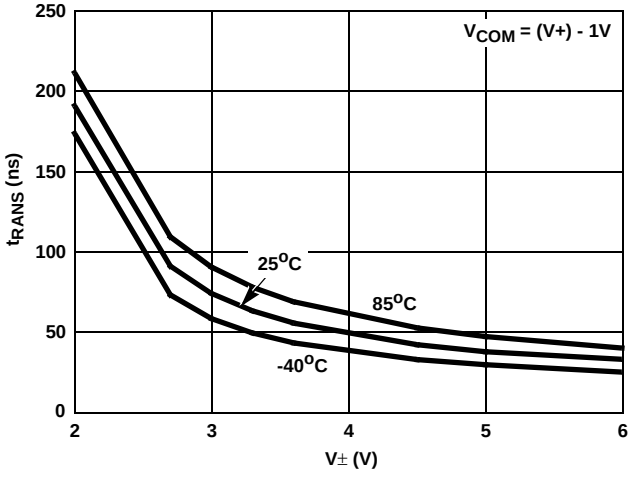


FIGURE 16. ADDRESS TRANS TIME vs DUAL SUPPLY VOLTAGE

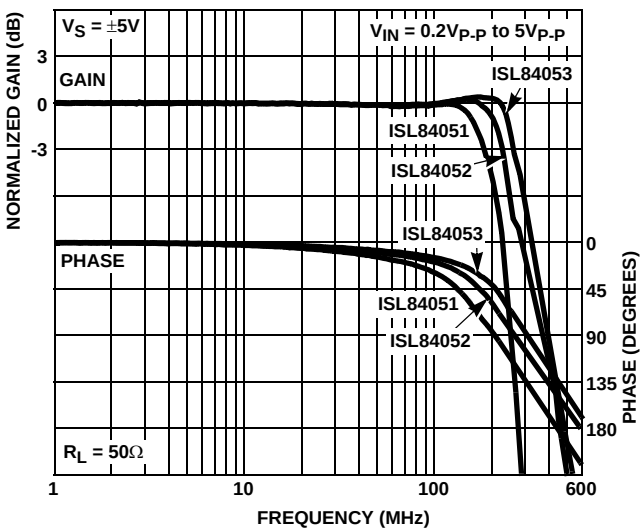


FIGURE 17. FREQUENCY RESPONSE

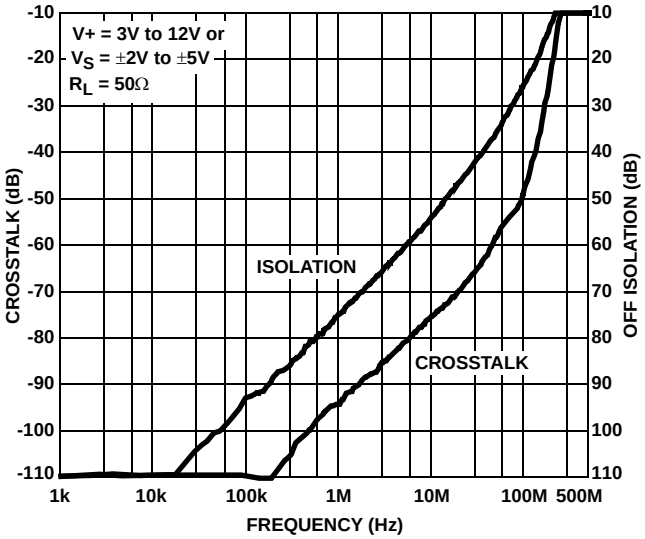


FIGURE 18. CROSSTALK AND OFF ISOLATION

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

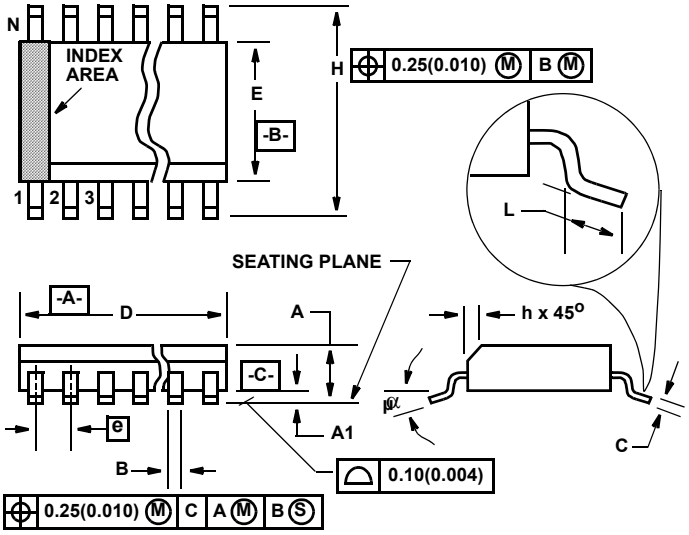
TRANSISTOR COUNT:

ISL84051: 193
ISL84052: 193
ISL84053: 193

PROCESS:

Si Gate CMOS

Small Outline Plastic Packages (SOIC)



M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

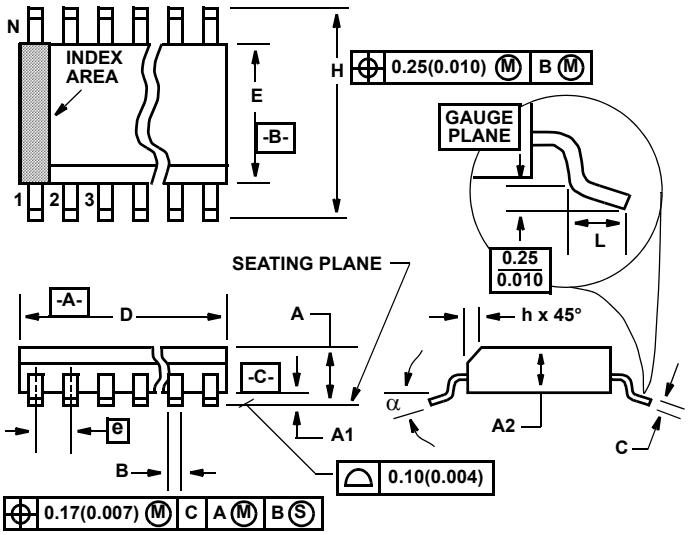
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
B	0.014	0.019	0.35	0.49	9
C	0.007	0.010	0.19	0.25	-
D	0.386	0.394	9.80	10.00	3
E	0.150	0.157	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.228	0.244	5.80	6.20	-
h	0.010	0.020	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0^o	8^o	0^o	8^o	-

Rev. 1 02/02

NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Shrink Small Outline Plastic Packages (SSOP)
Quarter Size Outline Plastic Packages (QSOP)



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2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
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4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

M16.15A

16 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE (0.150” WIDE BODY)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.061	0.068	1.55	1.73	-
A1	0.004	0.0098	0.102	0.249	-
A2	0.055	0.061	1.40	1.55	-
B	0.008	0.012	0.20	0.31	9
C	0.0075	0.0098	0.191	0.249	-
D	0.189	0.196	4.80	4.98	3
E	0.150	0.157	3.81	3.99	4
e	0.025 BSC		0.635 BSC		-
H	0.230	0.244	5.84	6.20	-
h	0.010	0.016	0.25	0.41	5
L	0.016	0.035	0.41	0.89	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 2 6/04