Two-Phase Buck PWM Controller with Integrated MOSFET Drivers for VRM9, VRM10, and AMD Hammer Applications

The ISL6568 two-phase PWM control IC provides a precision voltage regulation system for advanced microprocessors. The integration of power MOSFET drivers into the controller IC marks a departure from the separate PWM controller and driver configuration of previous multi-phase product families. By reducing the number of external parts, this integration is optimized for a cost and space saving power management solution.

Outstanding features of this controller IC include programmable VID codes compatible with Intel VRM9,VRM10, as well as AMD Hammer microprocessors. A unity gain, differential amplifier is provided for remote voltage sensing, compensating for any potential difference between remote and local grounds. The output voltage can also be positively or negatively offset through the use of a single external resistor.

A unique feature of the ISL6568 is the combined use of both DCR and $r_{DS(ON)}$ current sensing. Load line voltage positioning (droop) and overcurrent protection are accomplished through continuous inductor DCR current sensing, while $r_{DS(ON)}$ current sensing is used for accurate channel-current balance. Using both methods of current sampling utilizes the best advantages of each technique.

Protection features of this controller IC include a set of sophisticated overvoltage, undervoltage, and overcurrent protection. Overvoltage results in the converter turning the lower MOSFETs ON to clamp the rising output voltage and protect the microprocessor. The overcurrent protection level is set through a single external resistor. Furthermore, the ISL6568 includes protection against an open circuit on the remote sensing inputs. Combined, these features provide advanced protection for the microprocessor and power system.

Ordering Information

PART NUMBER*	TEMP. (°C)	PACKAGE	PKG. DWG. #
ISL6568CR	0 to 70	32 Ld 5x5 QFN	L32.5x5
ISL6568CRZ (Note)	0 to 70	32 Ld 5x5 QFN (Pb-free)	L32.5x5
ISL6568CRZA (Note)	0 to 70	32 Ld 5x5 QFN (Pb-free with Anneal)	L32.5x5
ISL6568IR	-40 to 85	32 Ld 5x5 QFN	L32.5x5
ISL6568IRZ (Note)	-40 to 85	32 Ld 5x5 QFN (Pb-free)	L32.5x5
ISL6568IRZA (Note)	-40 to 85	32 Ld 5x5 QFN (Pb-free with Anneal)	L32.5x5

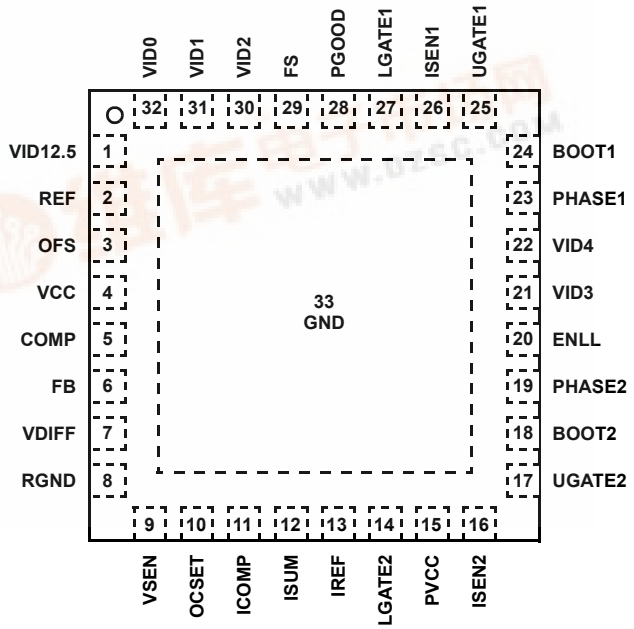
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

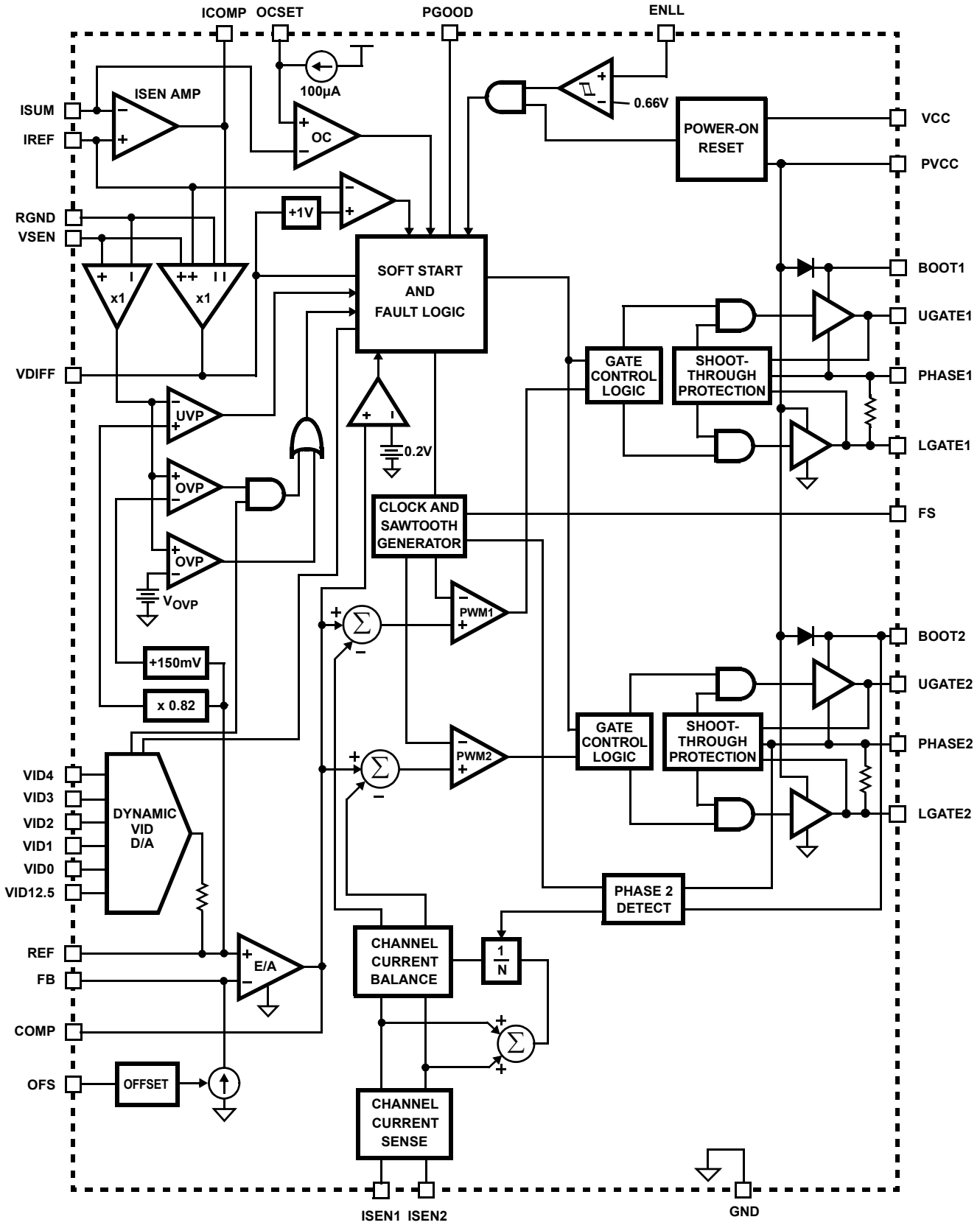
- Integrated Multi-Phase Power Conversion
  - 1 or 2-Phase Operation
- Precision Core Voltage Regulation
  - Differential Remote Voltage Sensing
  - ±0.5% System Accuracy Over Temperature
  - Adjustable Reference-Voltage Offset
- Precision Channel Current Sharing
  - Uses Loss-Less $r_{DS(ON)}$ Current Sampling
- Accurate Load Line Programming
  - Uses Loss-Less Inductor DCR Current Sampling
- Variable Gate Drive Bias: 5V to 12V
- Microprocessor Voltage Identification Inputs
  - Up to a 6-Bit DAC
  - Selectable between Intel's VRM9, VRM10, or AMD Hammer DAC codes
  - Dynamic VID-on-the-fly Technology
- Overcurrent Protection
- Multi-tiered Overvoltage Protection
- Digital Soft-Start
- Selectable Operation Frequency up to 1.5MHz Per Phase
- Pb-Free Plus Anneal Available (RoHS Compliant)

Pinout

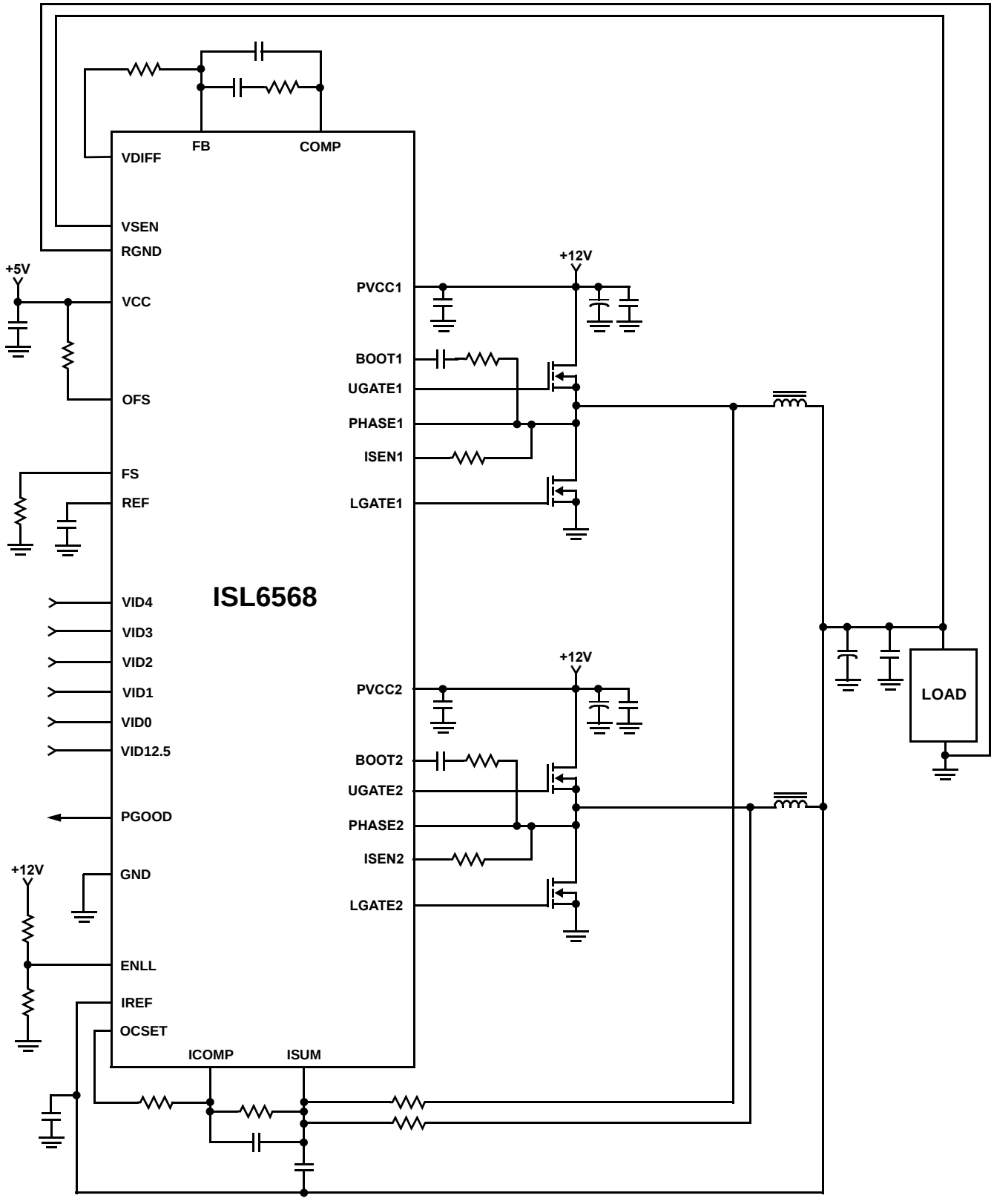
ISL6568 (QFN)
TOP VIEW



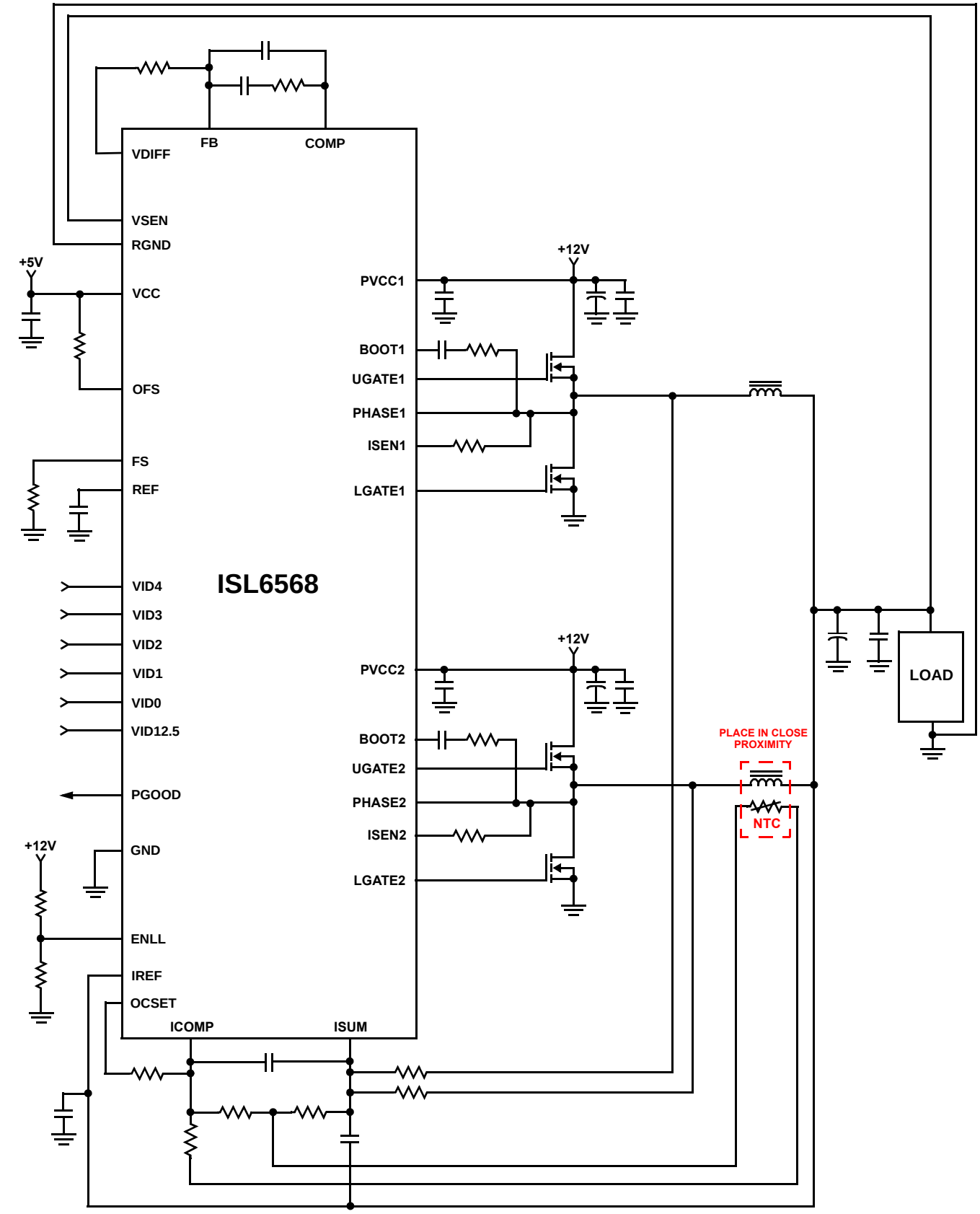
Block Diagram



Typical Application - ISL6568



Typical Application - ISL6568 with NTC Thermal Compensation



Absolute Maximum Ratings

Supply Voltage, VCC . . . . . -0.3V to +6V
Supply Voltage, PVCC . . . . . -0.3V to +15V
Absolute Boot Voltage, V_{BOOT} . . . . . GND - 0.3V to GND + 36V
Phase Voltage, V_{PHASE} . . . . . GND - 0.3V to 15V (PVCC = 12)
GND - 8V (<400ns, 20µJ) to 24V (<200ns, $V_{BOOT-PHASE}$ = 12V)
Upper Gate Voltage, V_{UGATE} . . . . V_{PHASE} - 0.3V to V_{BOOT} + 0.3V
V_{PHASE} - 3.5V (<100ns Pulse Width, 2µJ) to V_{BOOT} + 0.3V
Lower Gate Voltage, V_{LGATE} . . . . . GND - 0.3V to PVCC + 0.3V
GND - 5V (<100ns Pulse Width, 2µJ) to PVCC+ 0.3V
Input, Output, or I/O Voltage . . . . . GND - 0.3V to VCC + 0.3V
ESD Classification . . . . . Class I JEDEC STD

Recommended Operating Conditions

VCC Supply Voltage . . . . . +5V ±5%
PVCC Supply Voltage . . . . . +5V to 12V ±5%
Ambient Temperature (ISL6568CR, ISL6568CRZ) . . . . 0°C to 70°C
Ambient Temperature (ISL6568IR, ISL6568IRZ) . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 1, 2)	35	5

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stress above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
BIAS SUPPLY AND INTERNAL OSCILLATOR					
Input Bias Supply Current	I_{VCC}; ENLL = high	-	15	20	mA
Gate Drive Bias Current	I_{PVCC}; ENLL = high	-	1.5	-	mA
VCC POR (Power-On Reset) Threshold	VCC Rising	4.25	4.38	4.50	V
	VCC Falling	3.75	3.88	4.00	V
PVCC POR (Power-On Reset) Threshold	PVCC Rising	4.25	4.38	4.50	V
	PVCC Falling	3.60	3.88	4.00	V
Oscillator Ramp Amplitude (Note 3)	V_{PP}	-	1.50	-	V
Maximum Duty Cycle (Note 3)		-	66.6	-	%
Oscillator Frequency, F_{SW}	R_T = 100kΩ (± 0.1%)	225	250	275	kHz
CONTROL THRESHOLDS					
ENLL Rising Threshold		-	0.66	-	V
ENLL Hysteresis		-	100	-	mV
COMP Shutdown Threshold	COMP Falling	0.2	0.3	0.4	V
REFERENCE AND DAC					
System Accuracy (VID = 1.0V - 1.850V)		-0.5	-	0.5	%
System Accuracy (VID = 0.8V - 1.0V)		-0.8	-	0.8	%
DAC Input Low Voltage (VR9, VR10)		-	-	0.4	V
DAC Input High Voltage (VR9, VR10)		0.8	-	-	V
DAC Input Low Voltage (AMD)		-	-	0.6	V
DAC Input High Voltage (AMD)		1.0	-	-	V
OFS Sink Current Accuracy (Negative Offset)	R_{OFS} = 30kΩ from OFS to VCC	47.5	50.0	52.5	µA
OFS Source Current Accuracy (Positive Offset)	R_{OFS} = 10kΩ from OFS to GND	47.5	50.0	52.5	µA

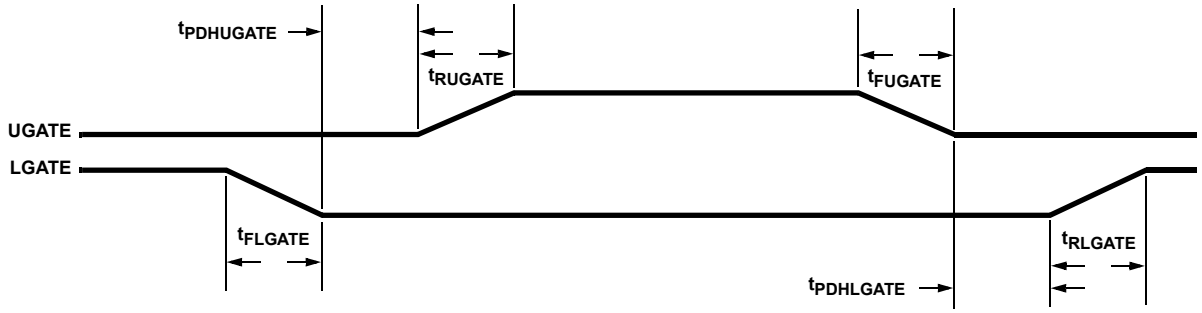
Electrical Specifications Recommended Operating Conditions, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ERROR AMPLIFIER					
DC Gain (Note 3)	R_L = 10K to ground	-	96	-	dB
Gain-Bandwidth Product (Note 3)	C_L = 100pF, R_L = 10K to ground	-	20	-	MHz
Slew Rate (Note 3)	C_L = 100pF, Load = $\pm$400μA	-	8	-	V/μs
Maximum Output Voltage	Load = 1mA	3.90	4.20	-	V
Minimum Output Voltage	Load = -1mA	-	0.85	1.0	V
OVERCURRENT PROTECTION					
OCSET trip current		93	100	107	μA
OCSET Accuracy	OCSET and ISUM Difference	-5	0	5	mV
ICOMP Offset		-5	0	5	mV
PROTECTION					
Undervoltage Threshold	VSEN falling	80	82	84	%VID
Undervoltage Hysteresis	VSEN Rising	-	3	-	%VID
Overvoltage Threshold while IC Disabled	V_{OVP}, VRM9.0 Configuration	1.92	1.97	2.02	V
	V_{OVP}, Hammer and VRM10.0 Configurations	1.62	1.67	1.72	V
Overvoltage Threshold	VSEN Rising	VID + 125mV	VID + 150mV	VID + 175mV	V
Overvoltage Hysteresis	VSEN Falling	-	50	-	mV
Open Sense-Line Protection Threshold	IREF Rising and Falling	VDIFF + 0.9V	VDIFF + 1V	VDIFF + 1.1V	V
SWITCHING TIME (Note 3)					
UGATE Rise Time	t_{RUGATE}; V_{PVCC} = 12V, 3nF Load, 10% to 90%	-	26	-	ns
LGATE Rise Time	t_{RLGATE}; V_{PVCC} = 12V, 3nF Load, 10% to 90%	-	18	-	ns
UGATE Fall Time	t_{FUGATE}; V_{PVCC} = 12V, 3nF Load, 90% to 10%	-	18	-	ns
LGATE Fall Time	t_{FLGATE}; V_{PVCC} = 12V, 3nF Load, 90% to 10%	-	12	-	ns
UGATE Turn-On Non-overlap	$t_{PDHUGATE}$; V_{PVCC} = 12V, 3nF Load, Adaptive	-	10	-	ns
LGATE Turn-On Non-overlap	$t_{PDHLGATE}$; V_{PVCC} = 12V, 3nF Load, Adaptive	-	10	-	ns
GATE DRIVE RESISTANCE (Note 3)					
Upper Drive Source Resistance	V_{PVCC} = 12V, 15mA Source Current	1.25	2.0	3.0	Ω
Upper Drive Sink Resistance	V_{PVCC} = 12V, 15mA Sink Current	0.9	1.65	3.0	Ω
Lower Drive Source Resistance	V_{PVCC} = 12V, 15mA Source Current	0.85	1.25	2.2	Ω
Lower Drive Sink Resistance	V_{PVCC} = 12V, 15mA Sink Current	0.60	0.80	1.35	Ω
OVER TEMPERATURE SHUTDOWN					
Thermal Shutdown Setpoint (Note 3)		-	160	-	°C
Thermal Recovery Setpoint (Note 3)		-	100	-	°C

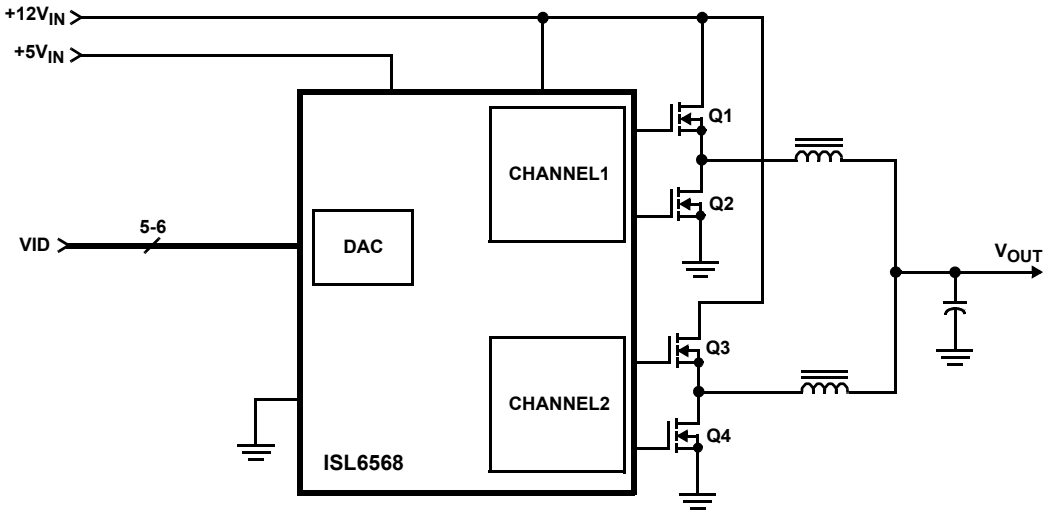
NOTE:

3. Parameter magnitude guaranteed by design. Not 100% tested.

Timing Diagram



Simplified Power System Diagram



Functional Pin Description

VCC

VCC is the bias supply for the ICs small-signal circuitry. Connect this pin to a +5V supply and locally decouple using a quality 1.0µF ceramic capacitor.

PVCC

This pin is the power supply pin for the MOSFET drivers. This pin can be connected to any voltage from +5V to +12V, depending on the desired MOSFET gate drive level.

GND

GND is the bias and reference ground for the IC.

ENLL

This pin is a threshold-sensitive (approximately 0.66V) enable input for the controller. Held low, this pin disables controller operation. Pulled high, the pin enables the controller for operation. ENLL has a internal 1.0µA pull-up to 5V.

FS

A resistor, placed from FS to ground, will set the switching frequency. Refer to Equation 34 for proper resistor calculation.

VID4, VID3, VID2, VID1, VID0, and VID12.5

These are the inputs for the internal DAC that provides the reference voltage for output regulation. These pins respond to TTL logic thresholds. The ISL6568 decodes the VID inputs to establish the output voltage; see VID Tables for correspondence between DAC codes and output voltage settings. These pins are internally pulled high, to approximately 1.2V, by 40µA (typically) internal current sources; the internal pull-up current decreases to 0 as the VID voltage approaches the internal pull-up voltage. All VID pins are compatible with external pull-up voltages not exceeding the IC's bias voltage (VCC).

The VID12.5 pin also serves as the internal DAC compliance selector. The way this pin is connected selects which of the three internal DAC codes will be used. For VRM10 codes this pin must be less that 3V. To encode the DAC with Intel VRM9.0 codes, connect the VID12.5 pin to a +5V source

through a 50kΩ resistor. To encode the DAC with AMD Hammer VID codes, connect this pin to a +5V source through a 5kΩ resistor.

VSEN and RGND

VSEN and RGND are inputs to the precision differential remote-sense amplifier and should be connected to the sense pins of the remote load.

ICOMP, ISUM, and IREF

ISUM, IREF, and ICOMP are the DCR current sense amplifier's negative input, positive input, and output respectively. For accurate DCR current sensing, connect a resistor from each channel's phase node to ISUM and connect IREF to the summing point of the output inductors, roughly Vout. A parallel R-C feedback circuit connected between ISUM and ICOMP will then create a voltage from IREF to ICOMP proportional to the voltage drop across the inductor DCR. This voltage is referred to as the droop voltage and is added to the differential remote-sense amplifier output.

NOTE: An optional 0.01μF ceramic capacitor can be placed from the IREF pin to the ISUM pin to help reduce any noise affects that may occur due to layout.

VDIFF

VDIFF is the output of the differential remote-sense amplifier. The voltage on this pin is equal to the difference between VSEN and RGND added to the difference between IREF and ICOMP. VDIFF therefore represents the output voltage plus the droop voltage.

FB and COMP

These pins are the internal error amplifier inverting input and output respectively. FB, VDIFF, and COMP are tied together through external R-C networks to compensate the regulator.

REF

The REF input pin is the positive input of the error amplifier. It is internally connected to the DAC output through a 1kΩ resistor. A capacitor is used between the REF pin and ground to smooth the voltage transition during Dynamic VID operations.

OFS

The OFS pin provides a means to program a dc current for generating an offset voltage across the resistor between FB and VDIFF. The offset current is generated via an external resistor and precision internal voltage references. The polarity of the offset is selected by connecting the resistor to GND or VCC. For no offset, the OFS pin should be left unconnected.

OCSET

This is the overcurrent set pin. Placing a resistor from OCSET to ICOMP allows a 100μA current to flow out this pin, producing a voltage reference. Internal circuitry compares the voltage at OCSET to the voltage at ISUM, and if ISUM ever exceeds OCSET, the overcurrent protection activates.

ISEN1 and ISEN2

These pins are used for balancing the channel currents by sensing the current through each channel's lower MOSFET when it is conducting. Connect a resistor between the ISEN1 and ISEN2 pins and their respective phase node. This resistor sets a current proportional to the current in the lower MOSFET during its conduction interval.

UGATE1 and UGATE2

Connect these pins to the corresponding upper MOSFET gates. These pins are used to control the upper MOSFETs and are monitored for shoot-through prevention purposes. Maximum individual channel duty cycle is limited to 66%.

BOOT1 and BOOT2

These pins provide the bias voltage for the corresponding upper MOSFET drives. Connect these pins to appropriately-chosen external bootstrap capacitors. Internal bootstrap diodes connected to the PVCC pins provide the necessary bootstrap charge.

PHASE1 and PHASE2

Connect these pins to the sources of the upper MOSFETs. These pins are the return path for the upper MOSFET drives.

LGATE1 and LGATE2

These pins are used to control the lower MOSFETs. Connect these pins to the corresponding lower MOSFETs' gates.

PGOOD

During normal operation PGOOD indicates whether the output voltage is within specified overvoltage and undervoltage limits. If the output voltage exceeds these limits or a reset event occurs (such as an overcurrent event), PGOOD is pulled low. PGOOD is always low prior to the end of soft-start.

Operation

Multi-Phase Power Conversion

Microprocessor load current profiles have changed to the point that the advantages of multi-phase power conversion are impossible to ignore. The technical challenges associated with producing a single-phase converter that is both cost-effective and thermally viable have forced a change to the cost-saving approach of multi-phase. The ISL6568 controller helps simplify implementation by integrating vital functions and requiring minimal external components. The block diagram on page 2 provides a top level view of multi-phase power conversion using the ISL6568 controller.

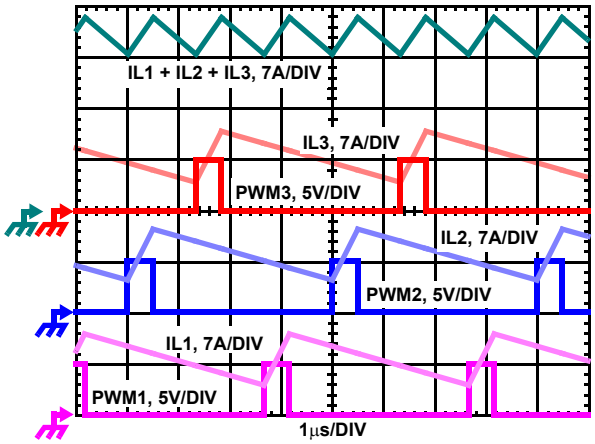


FIGURE 1. PWM AND INDUCTOR-CURRENT WAVEFORMS FOR 3-PHASE CONVERTER

Interleaving

The switching of each channel in a multi-phase converter is timed to be symmetrically out of phase with each of the other channels. In a 3-phase converter, each channel switches 1/3 cycle after the previous channel and 1/3 cycle before the following channel. As a result, the three-phase converter has a combined ripple frequency three times greater than the ripple frequency of any one phase. In addition, the peak-to-peak amplitude of the combined inductor currents is reduced in proportion to the number of phases (Equations 1 and 2). Increased ripple frequency and lower ripple amplitude mean that the designer can use less per-channel inductance and lower total output capacitance for any performance specification.

Figure 1 illustrates the multiplicative effect on output ripple frequency. The three channel currents (IL1, IL2, and IL3) combine to form the AC ripple current and the DC load current. The ripple component has three times the ripple frequency of each individual channel current. Each PWM pulse is terminated 1/3 of a cycle after the PWM pulse of the previous phase. The peak-to-peak current for each phase is about 7A, and the dc components of the inductor currents combine to feed the load.

To understand the reduction of ripple current amplitude in the multi-phase circuit, examine the equation representing an individual channel peak-to-peak inductor current.

$$I_{PP} = \frac{(V_{IN} - V_{OUT})V_{OUT}}{L f_S V_{IN}} \quad \text{(EQ. 1)}$$

In Equation 1, V_{IN} and V_{OUT} are the input and output voltages respectively, L is the single-channel inductor value, and f_S is the switching frequency.

The output capacitors conduct the ripple component of the inductor current. In the case of multi-phase converters, the capacitor current is the sum of the ripple currents from each of the individual channels. Compare Equation 1 to the expression for the peak-to-peak current after the summation of N symmetrically phase-shifted inductor currents in Equation 2. Peak-to-peak ripple current decreases by an amount proportional to the number of channels. Output-voltage ripple is a function of capacitance, capacitor equivalent series resistance (ESR), and inductor ripple current. Reducing the inductor ripple current allows the designer to use fewer or less costly output capacitors.

$$I_{C,PP} = \frac{(V_{IN} - N V_{OUT})V_{OUT}}{L f_S V_{IN}} \quad \text{(EQ. 2)}$$

Another benefit of interleaving is to reduce input ripple current. Input capacitance is determined in part by the maximum input ripple current. Multi-phase topologies can improve overall system cost and size by lowering input ripple current and allowing the designer to reduce the cost of input capacitance. The example in Figure 2 illustrates input currents from a three-phase converter combining to reduce the total input ripple current.

The converter depicted in Figure 2 delivers 1.5V to a 36A load from a 12V input. The RMS input capacitor current is 5.9A. Compare this to a single-phase converter also stepping down 12V to 1.5V at 36A. The single-phase converter has 11.9A RMS input capacitor current. The single-phase converter must use an input capacitor bank with twice the RMS current capacity as the equivalent three-phase converter.

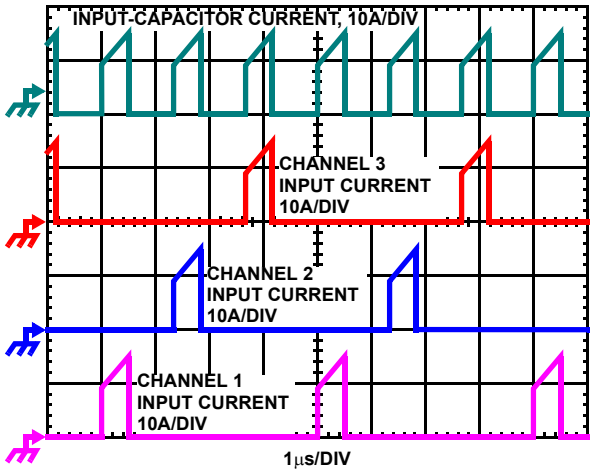


FIGURE 2. CHANNEL INPUT CURRENTS AND INPUT-CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER

Figures 22 and 23 in the section entitled *Input Capacitor Selection* can be used to determine the input-capacitor RMS current based on load current, duty cycle, and the number of channels. They are provided as aids in determining the optimal input capacitor solution.

PWM Operation

The timing of each converter leg is set by the number of active channels. The default channel setting for the ISL6568 is two. One switching cycle is defined as the time between the internal PWM1 pulse termination signals. The pulse termination signal is the internally generated clock signal that triggers the falling edge of PWM1. The cycle time of the

pulse termination signal is the inverse of the switching frequency set by the resistor between the FS pin and ground. Each cycle begins when the clock signal commands PWM1 to go low. The PWM1 transition signals the internal channel-1 MOSFET driver to turn off the channel-1 upper MOSFET and turn on the channel-1 synchronous MOSFET. In the default channel configuration, the PWM2 pulse terminates 1/2 of a cycle after the PWM1 pulse.

If the BOOT2 and PHASE2 pins are both connected to +12V single channel operation is selected.

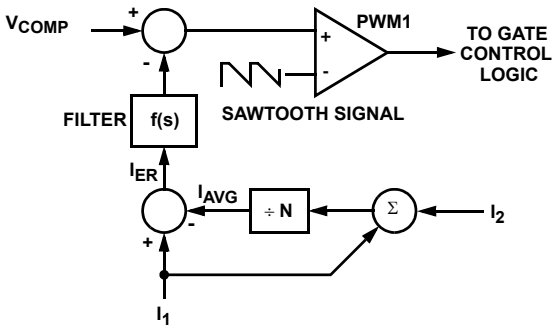
Once a PWM pulse transitions low, it is held low for a minimum of 1/3 cycle. This forced off time is required to ensure an accurate current sample. Current sensing is described in the next section. After the forced off time expires, the PWM output is enabled. The PWM output state is driven by the position of the error amplifier output signal, V_{COMP}, minus the current correction signal relative to the sawtooth ramp as illustrated in Figure 3. When the modified V_{COMP} voltage crosses the sawtooth ramp, the PWM output transitions high. The internal MOSFET driver detects the change in state of the PWM signal and turns off the synchronous MOSFET and turns on the upper MOSFET. The PWM signal will remain high until the pulse termination signal marks the beginning of the next cycle by triggering the PWM signal low.

Channel-Current Balance

One important benefit of multi-phase operation is the thermal advantage gained by distributing the dissipated heat over multiple devices and greater area. By doing this the designer avoids the complexity of driving parallel MOSFETs and the expense of using expensive heat sinks and exotic magnetic materials.

In order to realize the thermal advantage, it is important that each channel in a multi-phase converter be controlled to carry about the same amount of current at any load level. To achieve this, the currents through each channel must be sampled every switching cycle. The sampled currents, I_n, from each active channel are summed together and divided by the number of active channels. The resulting cycle average current, I_{AVG}, provides a measure of the total load-current demand on the converter during each switching cycle. Channel-current balance is achieved by comparing the sampled current of each channel to the cycle average current, and making the proper adjustment to each channel pulse width based on the error. Intersil's patented current-balance method is illustrated in Figure 3, with error correction for channel 1 represented. In the figure, the cycle average current, I_{AVG}, is compared with the channel 1 sample, I_1, to create an error signal I_{ER}.

The filtered error signal modifies the pulse width commanded by V_{COMP} to correct any unbalance and force I_{ER} toward zero. The same method for error signal correction is applied to each active channel.



NOTE: Channel 2 is optional.

FIGURE 3. CHANNEL-1 PWM FUNCTION AND CURRENT-BALANCE ADJUSTMENT

Current Sampling

In order to realize proper current-balance, the currents in each channel must be sampled every switching cycle. This sampling occurs during the forced off-time, following a PWM transition low. During this time the current-sense amplifier uses the ISEN inputs to reproduce a signal proportional to the inductor current, I_L. This sensed current, I_{SEN}, is simply a scaled version of the inductor current. The sample window opens exactly 1/6 of the switching period, t_{SW}, after the PWM transitions low. The sample window then stays open the rest of the switching cycle until PWM transitions high again, as illustrated in Figure 4.

The sampled current, at the end of the t_{SAMPLE}, is proportional to the inductor current and is held until the next switching period sample. The sampled current is used only for channel-current balance.

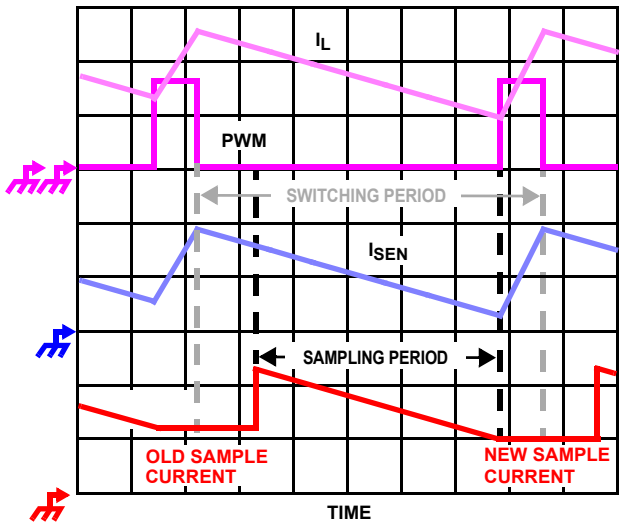


FIGURE 4. SAMPLE AND HOLD TIMING

The ISL6568 supports MOSFET $r_{DS(ON)}$ current sensing to sample each channel's current for channel-current balance. The internal circuitry, shown in Figure 5 represents channel n of an N-channel converter. This circuitry is repeated for each channel in the converter, but may not be active

depending on the status of the BOOT2 and PHASE2 pins, as described in the *PWM Operation* section.

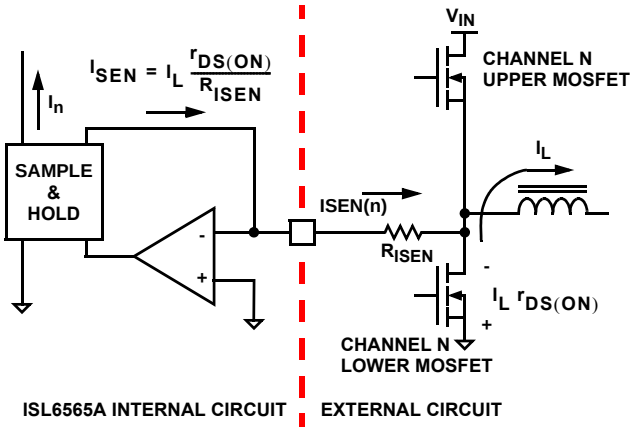


FIGURE 5. ISL6568 INTERNAL AND EXTERNAL CURRENT-SENSING CIRCUITRY FOR CURRENT BALANCE

The ISL6568 senses the channel load current by sampling the voltage across the lower MOSFET $r_{DS(ON)}$, as shown in Figure 5. A ground-referenced operational amplifier, internal to the ISL6568, is connected to the PHASE node through a resistor, R_{ISEN}. The voltage across R_{ISEN} is equivalent to the voltage drop across the $r_{DS(ON)}$ of the lower MOSFET while it is conducting. The resulting current into the ISEN pin is proportional to the channel current, I_L. The ISEN current is sampled and held as described in the *Current Sampling* section. From Figure 5, the following equation for I_n is derived where I_L is the channel current.

$$I_n = I_L \frac{r_{DS(ON)}}{R_{ISEN}} \quad \text{(EQ. 3)}$$

Output Voltage Setting

The ISL6568 uses a digital to analog converter (DAC) to generate a reference voltage based on the logic signals at the VID pins. The DAC decodes the 5 or 6-bit logic signals into one of the discrete voltages shown in Tables 2, 3, and 4. Each VID pin is pulled up to an internal 1.2V voltage by a weak current source (40µA current), which decreases to 0 as the voltage at the VID pin varies from 0 to the internal 1.2V pull-up voltage. External pull-up resistors or active-high output stages can augment the pull-up current sources, up to a voltage of 5V.

The ISL6568 accommodates three different DAC ranges: Intel VRM9.0, AMD Hammer, or Intel VRM10.0. The state of the VID12.5 pin decides which DAC version is active. Refer to Table 1 for a description of how to select the desired DAC version.

TABLE 1. ISL6568 DAC SELECT TABLE

DAC VERSION	VID12.5 PIN CONDITION
VRM10.0	Less then 3V
VRM9.0	50kΩ resistor to +5V
AMD HAMMER	5kΩ resistor to +5V

TABLE 2. AMD HAMMER VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	VDAC
1	1	1	1	1	Off
1	1	1	1	0	0.800
1	1	1	0	1	0.825
1	1	1	0	0	0.850
1	1	0	1	1	0.875
1	1	0	1	0	0.900
1	1	0	0	1	0.925
1	1	0	0	0	0.950
1	0	1	1	1	0.975
1	0	1	1	0	1.000
1	0	1	0	1	1.025
1	0	1	0	0	1.050
1	0	0	1	1	1.075
1	0	0	1	0	1.100
1	0	0	0	1	1.125
1	0	0	0	0	1.150
0	1	1	1	1	1.175
0	1	1	1	0	1.200
0	1	1	0	1	1.225
0	1	1	0	0	1.250
0	1	0	1	1	1.275
0	1	0	1	0	1.300
0	1	0	0	1	1.325
0	1	0	0	0	1.350
0	0	1	1	1	1.375
0	0	1	1	0	1.400
0	0	1	0	1	1.425
0	0	1	0	0	1.450
0	0	0	1	1	1.475
0	0	0	1	0	1.500
0	0	0	0	1	1.525
0	0	0	0	0	1.550

TABLE 3. VRM9 VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	VDAC
1	1	1	1	1	Off
1	1	1	1	0	1.100
1	1	1	0	1	1.125

TABLE 3. VRM9 VOLTAGE IDENTIFICATION CODES (Continued)

VID4	VID3	VID2	VID1	VID0	VDAC
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	12.75	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850

TABLE 4. VRM10 VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	VID12.5	VDAC
1	1	1	1	1	1	Off
1	1	1	1	1	0	Off
0	1	0	1	0	0	0.8375
0	1	0	0	1	1	0.8500
0	1	0	0	1	0	0.8625
0	1	0	0	0	1	0.8750

TABLE 4. VRM10 VOLTAGE IDENTIFICATION CODES (Continued)

VID4	VID3	VID2	VID1	VID0	VID12.5	VDAC
0	1	0	0	0	0	0.8875
0	0	1	1	1	1	0.9000
0	0	1	1	1	0	0.9125
0	0	1	1	0	1	0.9250
0	0	1	1	0	0	0.9375
0	0	1	0	1	1	0.9500
0	0	1	0	1	0	0.9625
0	0	1	0	0	1	0.9750
0	0	1	0	0	0	0.9875
0	0	0	1	1	1	1.0000
0	0	0	1	1	0	1.0125
0	0	0	1	0	1	1.0250
0	0	0	1	0	0	1.0375
0	0	0	0	1	1	1.0500
0	0	0	0	1	0	1.0625
0	0	0	0	0	1	1.0750
0	0	0	0	0	0	1.0875
1	1	1	1	0	1	1.1000
1	1	1	1	0	0	1.1125
1	1	1	0	1	1	1.1250
1	1	1	0	1	0	1.1375
1	1	1	0	0	1	1.1500
1	1	1	0	0	0	1.1625
1	1	0	1	1	1	1.1750
1	1	0	1	1	0	1.1875
1	1	0	1	0	1	1.2000
1	1	0	1	0	0	1.2125
1	1	0	0	1	1	1.2250
1	1	0	0	1	0	1.2375
1	1	0	0	0	1	1.2500
1	1	0	0	0	0	1.2625
1	0	1	1	1	1	1.2750
1	0	1	1	1	0	1.2875
1	0	1	1	0	1	1.300
1	0	1	1	0	0	1.3125
1	0	1	0	1	1	1.3250
1	0	1	0	1	0	1.3375
1	0	1	0	0	1	1.3500

TABLE 4. VRM10 VOLTAGE IDENTIFICATION CODES (Continued)

VID4	VID3	VID2	VID1	VID0	VID12.5	VDAC
1	0	1	0	0	0	1.3625
1	0	0	1	1	1	1.3750
1	0	0	1	1	0	1.3875
1	0	0	1	0	1	1.4000
1	0	0	1	0	0	1.4125
1	0	0	0	1	1	1.4250
1	0	0	0	1	0	1.4375
1	0	0	0	0	1	1.4500
1	0	0	0	0	0	1.4625
0	1	1	1	1	1	1.4750
0	1	1	1	1	0	1.4875
0	1	1	1	0	1	1.5000
0	1	1	1	0	0	1.5125
0	1	1	0	1	1	1.5250
0	1	1	0	1	0	1.5375
0	1	1	0	0	1	1.5500
0	1	1	0	0	0	1.5625
0	1	0	1	1	1	1.5750
0	1	0	1	1	0	1.5875
0	1	0	1	0	1	1.6000

Voltage Regulation

In order to regulate the output voltage to a specified level, the ISL6568 uses the integrating compensation network shown in Figure 6. This compensation network insures that the steady-state error in the output voltage is limited only to the error in the reference voltage (output of the DAC) and offset errors in the OFS current source, remote-sense and error amplifiers. Intersil specifies the guaranteed tolerance of the ISL6568 to include the combined tolerances of each of these elements.

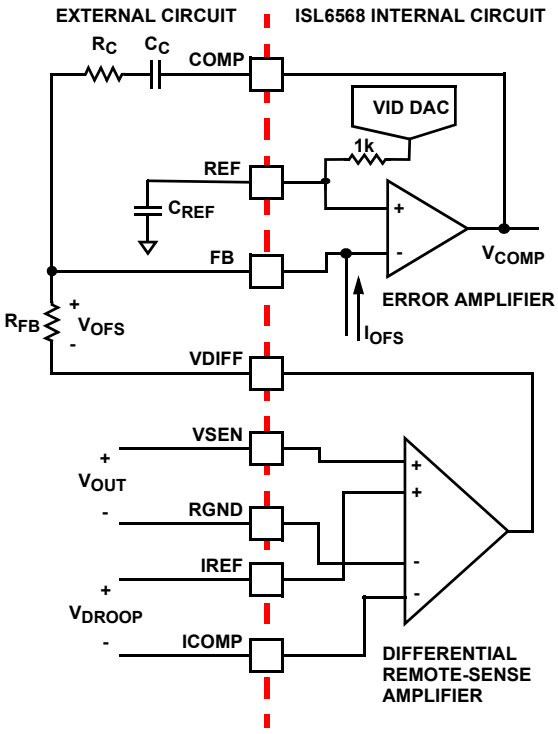


FIGURE 6. OUTPUT VOLTAGE AND LOAD-LINE REGULATION WITH OFFSET ADJUSTMENT

The ISL6568 incorporates an internal differential remote-sense amplifier in the feedback path. The amplifier removes the voltage error encountered when measuring the output voltage relative to the controller ground reference point, resulting in a more accurate means of sensing output voltage. Connect the microprocessor sense pins to the non-inverting input, VSEN, and inverting input, RGND, of the remote-sense amplifier. The droop voltage, V_{DROOP}, also feeds into the remote-sense amplifier. The remote-sense output, V_{DIFF}, is therefore equal to the sum of the output voltage, V_{OUT}, and the droop voltage. V_{DIFF} is connected to the inverting input of the error amplifier through an external resistor.

The output of the error amplifier, V_{COMP}, is compared to the sawtooth waveform to generate the PWM signals. The PWM signals control the timing of the Internal MOSFET drivers and regulate the converter output so that the voltage at FB is equal to the voltage at REF. This will regulate the output voltage to be equal to Equation 4. The internal and external circuitry that controls voltage regulation is illustrated in Figure 6.

$$V_{OUT} = V_{REF} - V_{OFS} - V_{DROOP} \quad \text{(EQ. 4)}$$

Load-Line (Droop) Regulation

Some microprocessor manufacturers require a precisely-controlled output impedance. This dependence of output voltage on load current is often termed “droop” or “load line” regulation.

As shown in Figure 6, a voltage, V_{DROOP}, proportional to the total current in all active channels, I_{OUT}, feeds into the differential remote-sense amplifier. The resulting voltage at the output of the remote-sense amplifier is the sum of the output voltage and the droop voltage. As Equation 4 shows, feeding this voltage into the compensation network causes the regulator to adjust the output voltage so that it’s equal to the reference voltage minus the droop voltage.

The droop voltage, V_{DROOP}, is created by sensing the current through the output inductors. This is accomplished by using a continuous DCR current sensing method.

Inductor windings have a characteristic distributed resistance or DCR (Direct Current Resistance). For simplicity, the inductor DCR is considered as a separate lumped quantity, as shown in Figure 7. The channel current, I_L, flowing through the inductor, passes through the DCR. Equation 5 shows the s-domain equivalent voltage, V_L, across the inductor.

$$V_L(s) = I_L \cdot (s \cdot L + DCR) \quad \text{(EQ. 5)}$$

The inductor DCR is important because the voltage dropped across it is proportional to the channel current. By using a simple R-C network and a current sense amplifier, as shown in Figure 7, the voltage drop across all of the inductors’ DCRs can be extracted. The output of the current sense amplifier, V_{DROOP}, can be shown to be proportional to the channel currents I_{L1} and I_{L2}, shown in Equation 6.

$$V_{DROOP}(s) = \frac{\left(\frac{s \cdot L}{DCR} + 1\right)}{(s \cdot R_{COMP} \cdot C_{COMP} + 1)} \cdot \frac{R_{COMP}}{R_S} \cdot (I_{L1} + I_{L2}) \cdot DCR \quad \text{(EQ. 6)}$$

If the R-C network components are selected such that the R-C time constant matches the inductor L/DCR time constant, then V_{DROOP} is equal to the sum of the voltage drops across the individual DCRs, multiplied by a gain. As Equation 7 shows, V_{DROOP} is therefore proportional to the total output current, I_{OUT}.

$$V_{DROOP} = \frac{R_{COMP}}{R_S} \cdot I_{OUT} \cdot DCR \quad \text{(EQ. 7)}$$

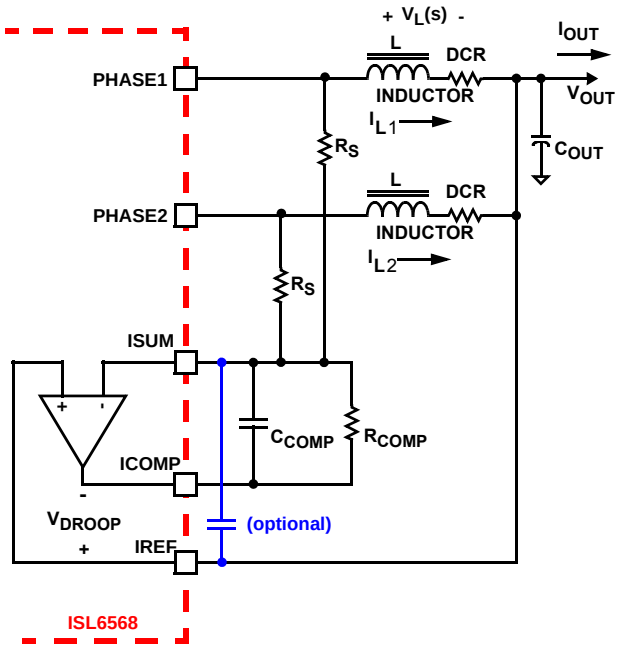


FIGURE 7. DCR SENSING CONFIGURATION

By simply adjusting the value of R_S, the load line can be set to any level, giving the converter the right amount of droop at all load currents. It may also be necessary to compensate for any changes in DCR due to temperature. These changes cause the load line to be skewed, and cause the R-C time constant to not match the L/DCR time constant. If this becomes a problem a simple negative temperature coefficient resistor network can be used in the place of R_{COMP} to compensate for the rise in DCR due to temperature.

Note: An optional 10nF ceramic capacitor from the ISUM pin to the IREF pin is recommended to help reduce any noise affects on the current sense amplifier due to layout.

Output-Voltage Offset Programming

The ISL6568 allows the designer to accurately adjust the offset voltage by connecting a resistor, R_{OFS}, from the OFS pin to VCC or GND. When R_{OFS} is connected between OFS and VCC, the voltage across it is regulated to 1.5V. This causes a proportional current (I_{OFS}) to flow into the OFS pin and out of the FB pin. If R_{OFS} is connected to ground, the voltage across it is regulated to 0.5V, and I_{OFS} flows into the FB pin and out of the OFS pin. The offset current flowing through the resistor between VDIFF and FB will generate the desired offset voltage which is equal to the product (I_{OFS} x R_{FB}). These functions are shown in Figures 8 and 9.

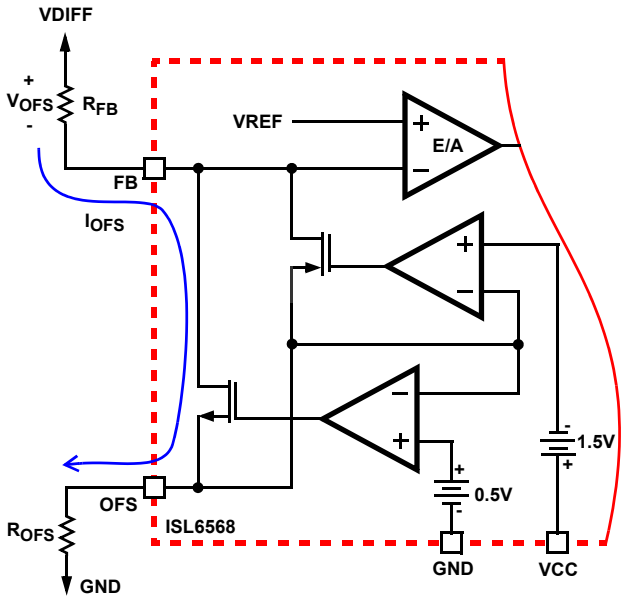


FIGURE 8. POSITIVE OFFSET OUTPUT VOLTAGE PROGRAMMING

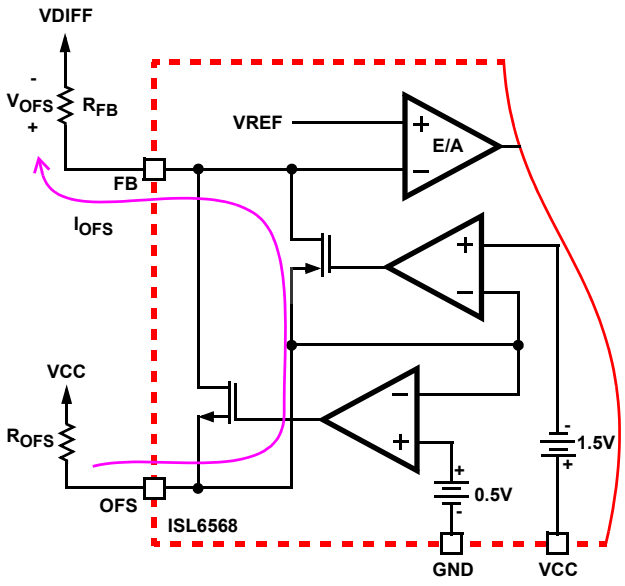


FIGURE 9. NEGATIVE OFFSET OUTPUT VOLTAGE PROGRAMMING

Once the desired output offset voltage has been determined, use the following formulas to set R_{OFS}:

For Positive Offset (connect R_{OFS} to GND):

$$R_{OFS} = \frac{0.5 \times R_{FB}}{V_{OFFSET}} \quad \text{(EQ. 8)}$$

For Negative Offset (connect R_{OFS} to VCC):

$$R_{OFS} = \frac{1.5 \times R_{FB}}{V_{OFFSET}} \quad \text{(EQ. 9)}$$

Dynamic VID

Modern microprocessors need to make changes to their core voltage as part of normal operation. They direct the core-voltage regulator to do this by making changes to the VID inputs. The core-voltage regulator is required to monitor the DAC inputs and respond to on-the-fly VID changes in a controlled manner, supervising a safe output voltage transition without discontinuity or disruption.

The DAC mode the ISL6568 is operating in determines how the controller responds to a dynamic VID change. When in VRM10 mode the ISL6568 checks the VID inputs six times every switching cycle. If a new code is established and it stays the same for 3 consecutive readings, the ISL6568 recognizes the change and increments the reference. Specific to VRM10, the processor controls the VID transitions and is responsible for incrementing or decrementing one VID step at a time. In VRM10 setting, the ISL6568 will immediately change the reference to the new requested value as soon as the request is validated; in cases where the reference step is too large, the sudden change can trigger overcurrent or overvoltage events.

In order to ensure the smooth transition of output voltage during a VRM10 VID change, a VID step change smoothing network is required for an ISL6568 based voltage regulator. This network is composed of a 1kΩ internal resistor between the output of DAC and the capacitor C_{REF}, between the REF pin and ground. The selection of C_{REF} is based on the time duration for 1 bit VID change and the allowable delay time.

Assuming the microprocessor controls the VID change at 1 bit every T_{VID}, the relationship between C_{REF} and T_{VID} is given by Equation 10.

$$C_{REF} = 0.004 \times T_{VID} \quad \text{(EQ. 10)}$$

As an example, for a VID step change rate of 5µs per bit, the value of C_{REF} is 22nF based on Equation 10.

When running in VRM9 or AMD Hammer operation, the ISL6568 responds slightly differently to a dynamic VID change than when in VRM10 mode. In these modes the VID code can be changed by more than a 1-bit step at a time. Once the controller receives the new VID code it waits half of a phase cycle and then begins slewing the DAC 12.5mV every phase cycle, until the VID and DAC are equal. Thus, the total time required for a VID change, t_{DVID}, is dependent on the switching frequency (f_S), the size of the change (ΔV_{VID}), and the time required to register the VID change. The one-cycle addition in the t_{DVID} equation is due to the possibility that the VID code change may occur up to one full switching cycle before being recognized. The approximate time required for a ISL6568-based converter in AMD Hammer configuration running at f_S =

335kHz to make a 1.1V to 1.5V reference voltage change is about 100µs, as calculated using the following equation.

$$t_{DVID} = \frac{1}{f_S}\left(\frac{\Delta V_{VID}}{0.0125} + 1.5\right) \quad \text{(EQ. 11)}$$

Advanced Adaptive Zero Shoot-Through Deadtime Control (Patent Pending)

The integrated drivers incorporate a unique adaptive deadtime control technique to minimize deadtime, resulting in high efficiency from the reduced freewheeling time of the lower MOSFET body-diode conduction, and to prevent the upper and lower MOSFETs from conducting simultaneously. This is accomplished by ensuring either rising gate turns on its MOSFET with minimum and sufficient delay after the other has turned off.

During turn-off of the lower MOSFET, the PHASE voltage is monitored until it reaches a -0.3V/+0.8V trip point for a forward/reverse current, at which time the UGATE is released to rise. An auto-zero comparator is used to correct the $r_{DS(ON)}$ drop in the phase voltage preventing false detection of the -0.3V phase level during $r_{DS(ON)}$ conduction period. In the case of zero current, the UGATE is released after 35ns delay of the LGATE dropping below 0.5V. During the phase detection, the disturbance of LGATE falling transition on the PHASE node is blanked out to prevent falsely tripping. Once the PHASE is high, the advanced adaptive shoot-through circuitry monitors the PHASE and UGATE voltages during a PWM falling edge and the subsequent UGATE turn-off. If either the UGATE falls to less than 1.75V above the PHASE or the PHASE falls to less than +0.8V, the LGATE is released to turn on.

Internal Bootstrap Device

Both integrated drivers feature an internal bootstrap schottky diode. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit. The bootstrap function is also designed to prevent the bootstrap capacitor from overcharging due to the large negative swing at the PHASE node. This reduces voltage stress on the boot to phase pins.

The bootstrap capacitor must have a maximum voltage rating above PVCC + 5V and its capacitance value can be chosen from the following equation:

$$C_{BOOT\_CAP} \geq \frac{Q_{GATE}}{\Delta V_{BOOT\_CAP}} \quad \text{(EQ. 12)}$$

$$Q_{GATE} = \frac{Q_{G1} \bullet PVCC}{V_{GS1}} \bullet N_{Q1}$$

where Q_{G1} is the amount of gate charge per upper MOSFET at V_{GS1} gate-source voltage and N_{Q1} is the number of control MOSFETs. The ΔV_{BOOT_CAP} term is defined as the allowable droop in the rail of the upper gate drive.

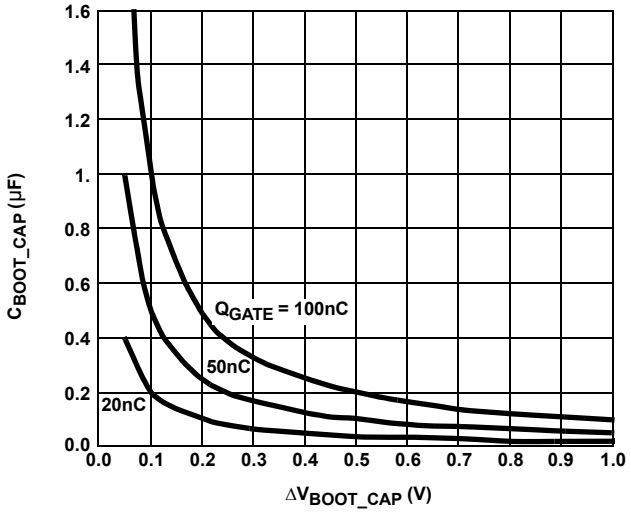


FIGURE 10. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE

Gate Drive Voltage Versatility

The ISL6568 provides the user flexibility in choosing the gate drive voltage for efficiency optimization. The controller ties the upper and lower drive rails together. Simply applying a voltage from 5V up to 12V on PVCC sets both gate drive rail voltages simultaneously.

Initialization

Prior to initialization, proper conditions must exist on the ENLL, VCC, PVCC and the VID pins. When the conditions are met, the controller begins soft-start. Once the output voltage is within the proper window of operation, the controller asserts PGOOD.

Enable and Disable

While in shutdown mode, the PWM outputs are held in a high-impedance state. This forces the drivers to short gate-to-source of the upper and lower MOSFET's to assure the MOSFETs remain off. The following input conditions must be met before the ISL6566 is released from this shutdown mode.

1. The bias voltage applied at VCC must reach the internal power-on reset (POR) rising threshold. Once this threshold is reached, proper operation of all aspects of the ISL6568 is guaranteed. Hysteresis between the rising and falling thresholds assure that once enabled, the ISL6568 will not inadvertently turn off unless the bias voltage drops substantially (see *Electrical Specifications*).

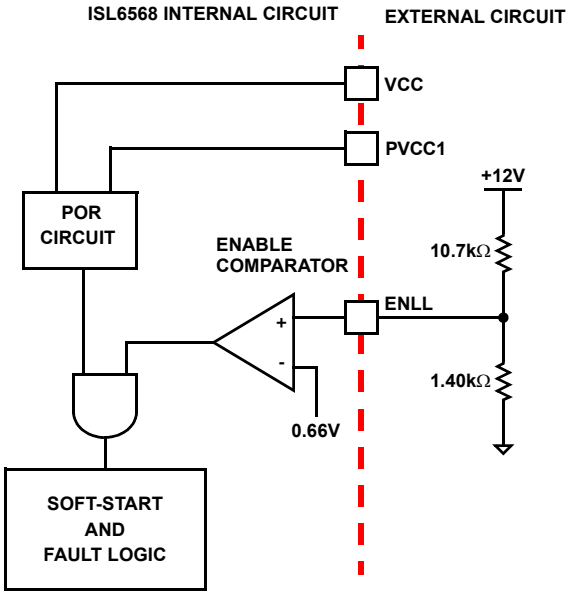


FIGURE 11. POWER SEQUENCING USING THRESHOLD-SENSITIVE ENABLE (ENLL) FUNCTION

2. The voltage on ENLL must be above 0.66V. The EN input allows for power sequencing between the controller bias voltage and another voltage rail. The enable comparator holds the ISL6568 in shutdown until the voltage at ENLL rises above 0.66V. The enable comparator has 60mV of hysteresis to prevent bounce.
3. The driver bias voltage applied at the PVCC pin must reach the internal power-on reset (POR) rising threshold. Hysteresis between the rising and falling thresholds assure that once enabled, the ISL6568 will not inadvertently turn off unless the PVCC bias voltage drops substantially (see *Electrical Specifications*).
4. The VID code must not be 111111 or 111110 in VRM10 mode or 11111 in AMD Hammer or VRM9 modes. These codes signal the controller that no load is present. The controller will enter shut-down mode after receiving either of these codes and will execute soft-start upon receiving any other code. These codes can be used to enable or disable the controller but it is not recommended. After receiving one of these codes, the controller executes a 2-cycle delay before changing the overvoltage trip level to the shut-down level and disabling PWM. Overvoltage shutdown cannot be reset using one of these codes.

When each of these conditions is true, the controller immediately begins the soft-start sequence.

SOFT-START

The soft-start function allows the converter to bring up the output voltage in a controlled fashion, resulting in a linear ramp-up. Following a delay of 16 PHASE clock cycles between enabling the chip and the start of the ramp, the output voltage progresses at a fixed rate of 12.5mV per each 16 PHASE clock cycles.

Thus, the soft-start period (not including the 16 PHASE clock cycle delay) up to a given voltage, V_{DAC}, can be approximated by the following equation

$$T_{SS} = \frac{V_{DAC} \cdot 1280}{f_S} \quad \text{(EQ. 13)}$$

where V_{DAC} is the DAC-set VID voltage, and f_S is the switching frequency.

The ISL6568 also has the ability to start up into a pre-charged output, without causing any unnecessary disturbance. The FB pin is monitored during soft-start, and should it be higher than the equivalent internal ramping reference voltage, the output drives hold both MOSFETs off. Once the internal ramping reference exceeds the FB pin potential, the output drives are enabled, allowing the output to ramp from the pre-charged level to the final level dictated by the DAC setting. Should the output be pre-charged to a level exceeding the DAC setting, the output drives are enabled at the end of the soft-start period, leading to an abrupt correction in the output voltage down to the DAC-set level.

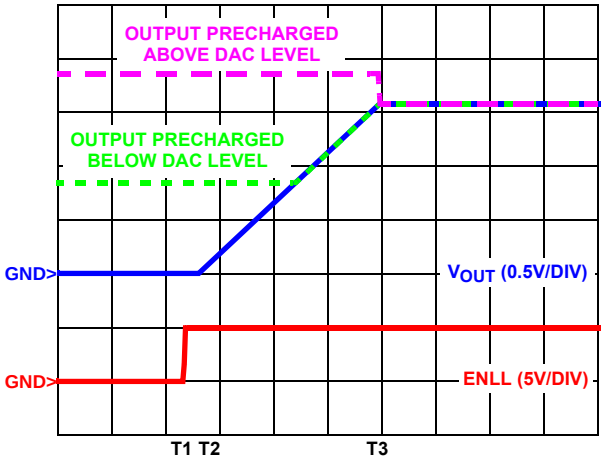


FIGURE 12. SOFT-START WAVEFORMS FOR ISL6568-BASED MULTI-PHASE CONVERTER

Fault Monitoring and Protection

The ISL6568 actively monitors output voltage and current to detect fault conditions. Fault monitors trigger protective measures to prevent damage to a microprocessor load. One common power good indicator is provided for linking to external system monitors. The schematic in Figure 13 outlines the interaction between the fault monitors and the power good signal.