## Low Voltage Fuel Gauge

The ISL6295 is a cost-effective, highly accurate IC that measures, stores, and reports all of the critical parameters required for rechargeable battery monitoring with a minimum of external components. It precisely measures charge/discharge current as well as voltage and temperature of a battery pack. In addition, the ISL6295 accurately accumulates both charge and discharge current as independent parameters. Temperature history can also be maintained for calculating self-discharge effects.

The ISL6295 integrates a highly accurate 16-bit (15-bit plus sign) integrating A/D converter that performs calibrated current measurement to within ±0.5% error. On-chip counters precisely track battery charge/discharge and temperature history. Also included are an on-chip voltage regulation circuit, non-crystal time base, and on-chip temperature sensor. The operating voltage range of the ISL6295 is optimized to allow a direct interface to a single cell Li-Ion/Li-Poly pack. 256 bytes of general-purpose nonvolatile EEPROM storage are provided to store factory programmed, measured, and user defined parameters.

Efficient communication is provided through an industry standard SMBus/I$^2$C™ compatible 2-wire communications interface. This interface allows the host to determine accurate battery status for effective system power management and for communication to the end user. A battery management solution utilizing the ISL6295 delivers both space and total system component cost savings for a wide variety of battery operated applications.

## Ordering Information

| PART NUMBER | PART MARKING | TEMP RANGE (°C) | PACKAGE | PKG. DWG. # |
|---|---|---|---|---|
| ISL6295CV | 6295CV | -20°C to 85 | 8 Ld TSSOP | M8.173 |
| ISL6295CV-T | 6295CV | -20°C to 85 | 8 Ld TSSOP | M8.173 |
| ISL6295CVZ (Note) | 6295CVZ | -20°C to 85 | 8 Ld TSSOP (Pb-free) | M8.173 |
| ISL6295CVZ-T (Note) | 6295CVZ | -20°C to 85 | 8 Ld TSSOP (Pb-free) | M8.173 |

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
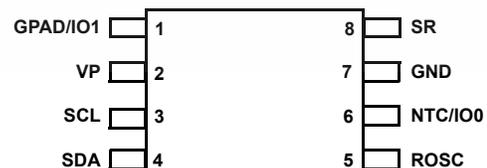
## Features

- Measures, maintains, and reports all critical rechargeable battery parameters with high accuracy

- Supports Lithium Ion and Lithium Polymer battery packs

- Current measurement with 16-bit (15-bit plus sign) integrating A/D accurate to less than ±0.5% error

- Calibrated temperature measurement accurate to within ±3°C absolute using on-chip temp sensor or external thermistor

- Accumulation of charge current, discharge current, temperature, and voltage in independent 32-bit registers

- 256-byte nonvolatile EEPROM stores factory programmed, measured, and user-defined parameters

- In-system offset calibration compensates for offset error in current measurement

- Industry standard SMBus/I$^2$C™ compatible 2-wire communications interface
  - SMBus V1.1 with PEC/CRC-8 communication

- -20°C to +85°C operating temperature range

- NTC pin can be configured as a thermistor input or GPIO

- GPAD pin can be configured as an independent A/D input or GPIO

- Flexible power operating modes allow low-power monitoring of battery conditions during system full operating and standby conditions:
  - Run: Continuous Conversion; 85µA typ.
  - Sample: Sample interval from 0.5-64s @ 45µA typ.
  - Sample-Sleep: Sample interval from 0.5-138s min. @ 20µA typ.

- Shelf-Sleep mode reduces power consumption to pack storage conditions to 300nA typ., with automatic wake-up upon pack insertion.

- Pb-free plus anneal available (RoHS compliant)

## Applications

- Notebook PC, PDAs, Hand Held Devices

## Pinout

**ISL6295 (TSSOP)**
TOP VIEW

| | | |
|---|---|---|
| GPAD/IO1 | 1 | 8 | SR |
| VP | 2 | 7 | GND |
| SCL | 3 | 6 | NTC/IO0 |
| SDA | 4 | 5 | ROSC |

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

# ISL6295

## Absolute Maximum Ratings

Supply Voltage $V_P$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . -0.5V to 10V
Input Voltage or IO Voltage . . . . . . . . . . . . . . . . . . . . . . -0.5V to 7V

## Recommended Operating Conditions

Ambient Temperature Range. . . . . . . . . . . . . . . . . . . .-20°C to 85°C
Operating Supply Voltage (VP Pin) . . . . . . . . . . . . . . . . 2.8V to 7V

## Thermal Information

| Thermal Resistance (Typical, Note 1) | $\theta_{JA}$ (°C/W) |
|---|---|
| TSSOP Package . . . . . . . . . . . . . . . . . . . . . . . . . . . | 115 |

Maximum Junction Temperature (Plastic Package) . . . . . . . .120°C
Maximum Storage Temperature Range. . . . . . . . . . .-35°C to 120°C
Maximum Lead Temperature (Soldering 10s) . . . . . . . . . . . .300°C

*CAUTION: Stress above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.*

NOTE:

1. $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

**Electrical Specifications** Typical Values Are Tested at $V_P$ = 5V and ambient temperature is at 25°C, All Maximum and Minimum Values Are Guaranteed Under the Recommended Operating Conditions., Unless Otherwise Noted.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | |
| Supply Voltage | $V_P$ | For SMBus and register access | 2.8 | | 7.0 | V |
| | | For EEPROM write | 3.3 | | 7.0 | V |
| | | For guaranteed analog parametrics | 3.0 | | 7.0 | V |
| Supply Current Run Mode | $I_{DD}$ | A/D Active (Note 1) | | 85 | 120 | µA |
| Supply Current Sample Mode | $I_{DDINS}$ | A/D Inactive (Notes 1, 2) | | 45 | 85 | µA |
| Supply Current Sample - Sleep Mode | $I_{DDSLP}$ | Sample -Sleep Mode (Note 1) | | 20 | 40 | µA |
| Supply Current Shelf Sleep Mode | $I_{DDSSLP}$ | Shelf Sleep Mode (Note 1) | | 400 | 800 | nA |
| Input Low Voltage IO0, IO1 | $V_{IL}$ | | | | 0.6 | V |
| Input High Voltage IO0, IO1 | $V_{IH}$ | | 2.4 | | | V |
| GPIO Input Low Current Pull-up mode | $I_{IL-IO0PU}$ | | | 7 | | µA |
| Leakage Current IO pin programmed as outputs or inputs without pullup | $I_{L-IO}$ | | | 1 | 600 | nA |
| Output low voltage for IO0, IO1 | $V_{OL-IO}$ | $I_{OL}$ = 0.5mA | | | 0.4 | V |
| Output high voltage for IO0 configured as push-pull | $V_{OH-IO}$ | $I_{OH}$ = 100µA | 2.1 | | | V |
| Thermistor Output Current | $I_{NTC}$ | ROSC = 221kΩ ± 0.1% | 8 | 13 | 16 | µA |
| Input Low Voltage for SMBus pins | $V_{IL-SMB}$ | | | | 0.8 | V |
| Input High Voltage for SMBus pins | $V_{IH-SMB}$ | | 2.0 | | 5.5 | V |
| Output Low Voltage for SMBus pins | $V_{OL-SMB}$ | $I_{PULLUP}$ = 4mA | | | 0.4 | V |
| Output High Voltage for SMBus pins | $V_{OH-SMB}$ | (Note 3) | 2.1 | | 5.5 | V |
| Input leakage current  SMBus pins | $I_{LEAK-SMB}$ | | -5.0 | | +5.0 | µA |
| **AC CHARACTERISTICS**  ($T_A$ = -20°C to +85°C; $V_P$ = 3.0V to 7.0V; ROSC = 221kΩ ± 0.1%) | | | | | | |
| Internal main oscillator frequency | $f_{RC}$ | ROSC = 221kΩ ± 0.1% | 130.8 | 131.5 | 132.2 | kHz |
| Internal auxiliary oscillator frequency | $f_{AUX}$ | | 118 | 131 | 144 | kHz |
| Accumulator Time Base Accuracy (internal 2Hz clock) | $f_{ACC}$ | During Run and Sample mode (Note 3) | -0.6 | | +0.6 | % |
| | | During Sample-Sleep mode (Note 3) | -10 | | +10 | % |
| Internal A/D operating clock | $f_{A/D}$ | (Note 3) | | $f_{RC}$/4 | | kHz |
| Power-on-Reset Threshold | $V_{POR}$ | Voltage at VP | 2.4 | | 2.75 | V |
| Delay to entry of Shelf-Sleep mode | $t_{SHELF}$ | (Shent = 1 or VP < VPtrip) and (SDA and SCL go low) | | 10 | | ms |

**Electrical Specifications** Typical Values Are Tested at $V_P$ = 5V and ambient temperature is at 25°C, All Maximum and Minimum Values Are Guaranteed Under the Recommended Operating Conditions., Unless Otherwise Noted. **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **A/D CONVERTER CHARACTERISTICS** ($T_A$ = -20°C to +85°C; $V_P$ = 3.0V to 7.0V, Note 3, 4) | | | | | | |
| A/D Converter Resolution | N | Magnitude only (Note 5) | 8 | | 15 | bits |
| A/D Conversion Measurement Time | tconv | N-bit + sign | | $2^{(N+1)}/f_{A/D}$ | | s |
| A/D Converter Input Voltage Range (internal) | $V_{ADIN}$ | Differential | -152 | | +152 | mV |
| | | Single-Ended | 0 | | 309 | mV |
| Internal Temperature Accuracy | $T_{ACC}$ | | -3 | | 3 | °K |
| Calibrated Voltage Measurement Gain Error | $E_{VGAIN}$ | Max deviation over supply voltage and temperature range (assumed ideal under the calibration condition) | | | 0.60 | % |
| Calibrated Current Measurement Gain Error (with ideal ZTC current sense resistor) | $E_{IGAIN}$ | Max deviation over supply voltage and temperature range (assumed ideal under the calibration condition) | | | 0.50 | % |
| Calibrated Temperature Measurement Gain Error (internal sensor) | $E_{TEMP}$ | Max deviation over supply voltage and temperature range (assumed ideal under the calibration condition) | | | 0.60 | % |
| Calibrated ADC Offset Error | $E_{VOFFSET}$ | Max deviation over supply voltage and temperature range (assumed ideal under the calibration condition) | | | | |
| | | $V_{REF}$ = 170mV | | | 0.30 | % |
| | | $V_{REF}$ = 340mV | | | 0.15 | % |
| Integrated Nonlinearity Error | $E_{INL}$ | | | | 0.01 | % |

NOTES:

1. Does not include current consumption due to external loading on pins. No EEPROM access.

2. Sample mode current is specified during an A/D inactive cycle. Sample mode average current can be calculated using the formula: Average Sample Mode Supply Current = (IDDRUN + (n-1)*IDDINS)/Ns; where Ns is the programmed sample rate.

3. Guaranteed by characterization or correlation to other test.

4. The max calibrated gain and offset errors are based on a 15-bit calibration procedure to generate the calibration factors. These calibration factors are then applied to correct the ADC results.

5. Voltage is internal at A/D converter inputs. VSR is measured directly. VP and GPAD inputs are measured using internal level-translation circuitry that scales the input voltage range appropriately for the converter.
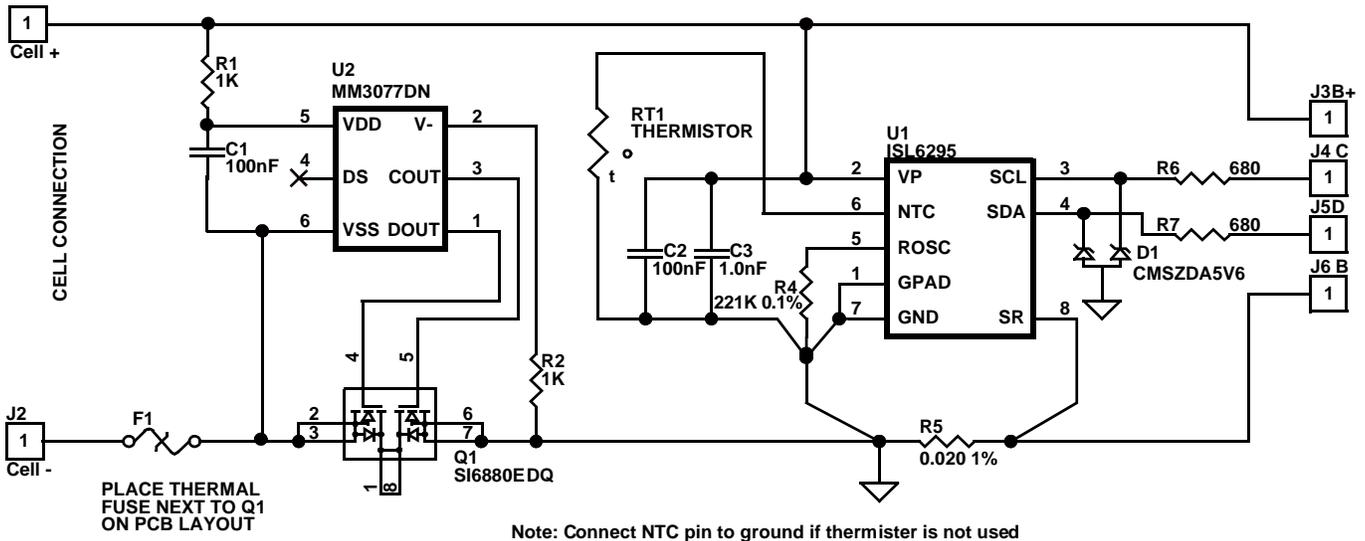
**Note: Connect NTC pin to ground if thermister is not used**

**FIGURE 1. ISL6295 APPLICATIONS SCHEMATIC**

## Functional Pin Descriptions

### GPAD/IO1 (Pin 1)

General purpose A/D input or general purpose input/output pin. Grounded if not used.

### VP (Pin 2)

Cell input connection for the positive terminal of the Li-Ion cell. Connects to the positive terminal of 1-cell series packs. VP serves as the power supply input for the ISL6295.

### SCL (Pin 3)

SMBus/I$^2$C™ clock line connection

### SDA (Pin 4)

SMBus/I$^2$C™ data line connection

### ROSC (Pin 5)

External bias resistor. 221kΩ (±0.1%) oscillator reference setting resistor connected between this pin and GND.

### NTC/IO0 (Pin 6)

Connection for an external temperature sensor using a thermistor. Can also be configured as an open drain general purpose input/output pin. Grounded if not used.

### GND (Pin 7)

Analog and digital ground

### SR (Pin 8)

Current measurement A/D input. Connects to the other terminal of a grounded current sense resistor.

## Theory of Operation

The ISL6295 contains a complete analog "front-end" for battery monitoring as well as digital logic for control, measurement accumulation, timing, and communications. Major functions within the ISL6295 include:

- Voltage Regulator
- Precision Time Base
- Temperature Sensor
- 256 Byte NV-EEPROM
- 32 Byte general purpose SRAM
- Analog-to-Digital (A/D) Converter
- 32-bit Accumulators/Timers
- SMBus/I$^2$C™ Communications Interface

Figure 2 is a block diagram of the internal circuitry of the ISL6295. Figure 1 is a schematic diagram that depicts the ISL6295 in a typical single cell Lithium-ion application. The function of each of the blocks listed above is summarized in the following sections.
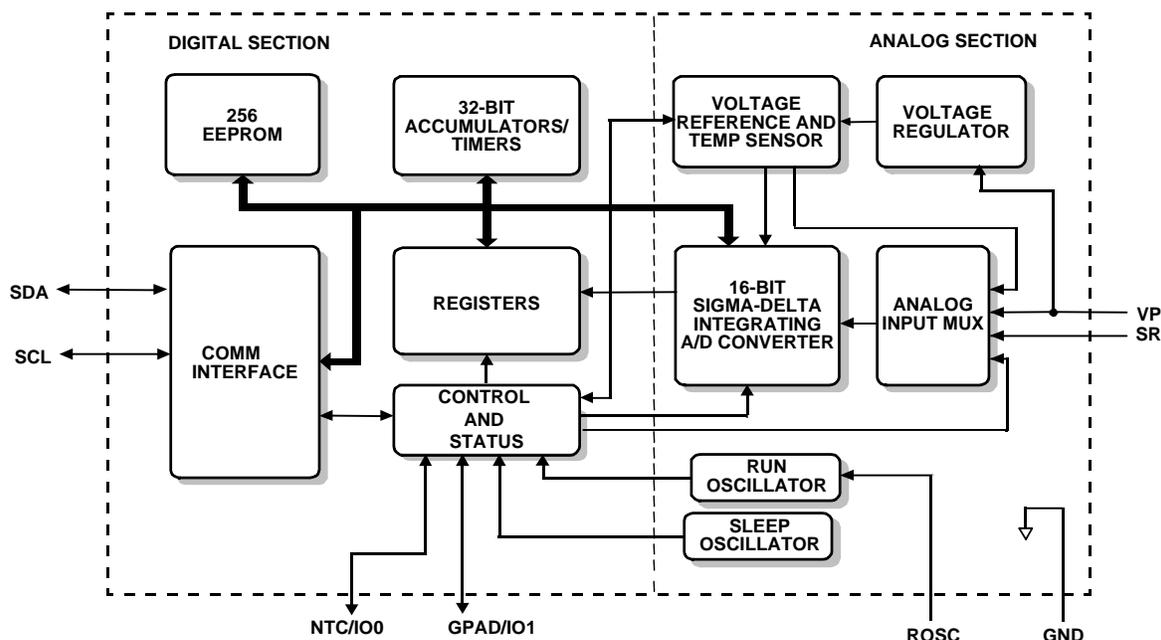
**FIGURE 2. BLOCK DIAGRAM**

### *Internal Voltage Regulator*

The ISL6295 incorporates an internal voltage regulator that supports 1-cell series lithium pack configurations. The internal regulator draws power directly from the VP input. No other external components are required to regulate circuit voltage.

### *Precision Time Base*

The integrated precision time base is a highly accurate RC oscillator that provides precise timing for the sigma-delta A/D and for the on-chip elapsed time counters without the need for an external crystal. This time base is trimmed during manufacturing to a nominal frequency of 131.072kHz.

### *Temperature Sensor*

An integrated temperature sensor is provided that can eliminate the need for an external thermistor. As an option, a connection is provided for an external thermistor for applications where the battery pack is physically located at a distance from the ISL6295.

### *EEPROM*

256 bytes of EEPROM memory is incorporated for storage of non-volatile parameters such as cell models for use with Intersil's host driver firmware. An an initialization block with values that are loaded into ISL6295 registers following a power on condition. Included in this block is 16 bytes for battery ID information.

### *RAM*

32 bytes of general purpose RAM memory are provided for storage of temporary parameters.

### *A/D Converter*

The ISL6295 incorporates an integrating sigma-delta A/D converter together with an analog MUX that has inputs for charge and discharge currents, pack voltage, GPAD voltage, the on-chip temperature sensor, and an off-chip thermistor. The converter can be programmed to perform a conversion with magnitude resolution of 8- to 15-bits while using either a single 170mV or 340mV reference.

### *32-Bit Accumulator/Timers*

The ISL6295 incorporates four 32-bit accumulators and four 32-bit elapsed time counters. The Discharge Current Accumulator (DCA) and the Charge Current Accumulator (CCA) are intended to record discharge and charge capacity values. The Discharge Time Counter (DTC) and the Charge Time Counter (CTC) are intended to maintain the total discharge time and charge time. Accumulated charge and discharge values can be used to determine state of charge of the battery as well as cycle count information. With information provided by the elapsed time counters, average charge and discharge currents over an extended period of time can be calculated.

### *SMBus/$I^2C$™ Communications Interface*

This communications port for the ISL6295 is a 2-wire industry-standard SMBus/$I^2C$™ interface. All commands, status, and data is read or written from the host system via this interface.

### *A/D and Accumulator/Timer Operation*

#### A/D CONVERSION CYCLE

When the A/D converter is enabled and active, it repeatedly performs a cycle of 1 to 8 conversions as programmed by

the user through 8 A/D control registers. These registers determine the input source, conversion resolution, reference voltage, and sequence of conversions during an A/D conversion cycle. During the cycle, the A/D logic accesses each register in sequence and performs the conversion specified by the bits within the registers. Each register contains an enable bit, a resolution field, a select bit for single-ended (340mV reference) or differential (170mV reference) conversion, and a select field for the analog input multiplexer. The result from each conversion is stored in one of eight corresponding 16-bit result registers.

If the "Enable" bit is set within a control register, a conversion will be performed. If it is disabled, that conversion will be skipped and the logic will move on to the next register. In this manner, the user can specify a sequence of conversions that will be performed during each A/D cycle.

As stated above, the input source for each of the registers is programmable. The 3-bit MUX field within each control register selects one of seven possible input sources for the A/D conversion. The list of input sources is as follows:

• Charge/discharge Current (Voltage from SR pin to GND)

• Internal temperature sensor

• External thermistor (Constant current source on NTC pin)

• Battery pack voltage

• Reserved

• General purpose A/D voltage

• ADC offset (Conversion performed with ADC input internally shorted to ground) to determine offset error associated with the converter

However, the accumulator/timer functions are "hard-wired" to specific A/D result registers. For this reason, the control/result registers are given names which indicate their primary intended usage:

| A/D REGISTER | CONTROL REGISTER | RESULT REGISTER | INTENDED INPUT SOURCE |
|---|---|---|---|
| 0 | Ictrl | Ires | Battery Pack Current (via sense resistor) |
| 1 | ITctrl | ITres | Internal Temperature Sensor |
| 2 | ETctrl | ETres | External Temperature Sensor |
| 3 | VPctrl | VPres | Battery Pack Voltage |
| 4 | Reserved | | |
| 5 | GPADctrl | GPADres | General Purpose A/D Input |
| 6 | OFFSctrl | OFFSres | Internal ADC offset voltage (with input grounded) |
| 7 | AUXctrl | AUXres | Any |

The 3-bit "resolution" field in each A/D control register determines the magnitude resolution of the conversion, from a minimum of 8-bits to a maximum of 15-bits. The time required to complete the conversion is a function of the number of bits of resolution selected. The conversion time can be calculated as follows:

$T_{ADC} = 30.52\mu s * 2^{(N+1)}$

where "N" is the number of bits of magnitude resolution selected

The "Ref" bit selects either a differential or single-ended conversion. For differential conversions, the 170mV reference is used. For single-ended conversion the 340mV reference is selected. Single-ended conversions would be used for measurements of pack voltage while a differential conversion is required for current measurement.

The value of the LSB in the result register is as follows:

For single-ended conversion,
A/D LSB = 340 mV/$2^{15}$ = 10.38μV

For differential conversion,
A/D LSB = 170 mV/$2^{15}$ = 5.19μV

For both differential and single-ended conversions, the result value is given in sign-magnitude format (i.e. a sign bit and 15 magnitude bits). When N less than 15 is selected, the conversion result is padded with trailing zeroes. Note that

| 15 | 14 | 0 |
|---|---|---|
| S | Magnitude | |

the single-ended reference should not be used for a negative measurement. Though the sign-magnitude value presented may still look valid, the accumulator will not be able to interpret the result for proper accumulation.

**CURRENT MEASUREMENT**

Charge and discharge currents are measured using a 5 to 600mΩ sense resistor that is connected between the SR and GND pins. The sense resistor value chosen must accommodate the system's lowest and highest expected charge and discharge currents, including suspend and standby currents, while maintaining a voltage of no more than ±152mV presented at the SR pin.

In order to perform charge and discharge current measurements, the Ictrl register must be programmed with the SR pin as the analog input source. If charge and discharge accumulation is desired, the Ictrl and corresponding Ires registers should be used to select current measurement since the DCA, DTC, CCA, and CTC registers are updated by the measurement results from the Ires register.

When a 20mΩ sense resistor is used, the value of the LSB in units of current is:

5.19μV/20mΩ = 259.5μA

Ictrl programming in a typical application is as follows:

| BIT(s) | NAME | VALUE | FUNCTION |
|--------|------|-------|----------|
| 7 | EN | 1 | ENABLES A/D CONVERSION |
| 6-4 | Res | 111 | Selects 15-bit resolution |
| 3 | Ref | 0 | Selects 170mV Reference |
| 2-0 | Sel | 000 | Selects VSR as ADC input |

## VOLTAGE MEASUREMENTS

An analog multiplexer and divider network is provided to support measurement of battery pack voltages. The A/D control registers VPctrl and GPADctrl are used to specify the measurement to be made. In typical applications, voltage measurement a pack level is done using the 340mV reference and a 10-bit magnitude resolution.

The value of the LSB in a pack voltage measurement using the 340mV reference voltage and 15 bit resolution is given by the formula:

$V_{PACK}$ LSB = $10.2V/2^{15}$ = 311.3µV

VPctrl programming in a typical application is as follows:

| BIT(s) | NAME | VALUE | FUNCTION |
|--------|------|-------|----------|
| 7 | En | 1 | Enables A/D conversion |
| 6-4 | Res | 010 | Selects 10-bit resolution |
| 3 | Ref | 1 | Selects 340mV Reference |
| 2-0 | Sel | 011 | Selects Vpack (VP) as ADC input |

The input source fields for the VPctrl, and GPADctrl registers must be programmed to select the pack voltage VP and the general purpose A/D input voltage GPAD in order for these registers to control their intended measurements.

The measurable input range for VP is from 2.8V to 7V. The measurable input range for GPAD is from 0V to 6.2V.

## TEMPERATURE MEASUREMENTS

A/D input channels are provided for temperature measurement using either the internal temperature sensor or an external thermistor.

Defined within the ITctrl register is settings for the reference utilized and the resolution desired for measurement of temperature using the internal temperature sensor. Due to the voltage output range of the temperature sensor, the 340mV reference must be selected.

The temperature measurement given by the internal temperature sensor is derived using the following equation:

IT(°C) = (ITres – 22421)/78.95 °C

Typically, 10-bit resolution is selected, which results in the following temperature measurement resolution:

IT($\Delta$) = 0.405°C/LSB

For temperature measurement using an external sensor, the NTC pin sources a current of 12.5µA. For proper operation, an industry standard 10k$\Omega$ at 25°C negative temperature coefficient (NTC) device with a proper resistance range should be connected between the NTC and GND pins. The NTC reference output is only enabled during an external temperature measurement in order to minimize power consumption.

Defined within the ETctrl register are settings for the reference utilized and the resolution desired for measurement of temperature using the external temperature sensor. The accuracy of temperature measurement using the external thermistor is directly determined by the characteristic of the NTC device used. It is suggested that temperature measurements be thoroughly characterized to extract the best-fit equation for temperature determination.

Internal to the ISL6295, a voltage inverter is provided to translate the NTC voltage to a PTC voltage so that a larger A/D conversion result would correspond to a higher temperature reading. The actual voltage presented to the ADC is as follows:

$V_{ADC}$ = $V_{REF}$ - $V_{NTC}$

where $V_{REF}$ is the reference voltage selected.

For typical NTC devices, the 340mV reference should be used to cover the expected operational temperature range of the battery pack. For a NTC with a 10k$\Omega$ resistance at 25°C, the voltage at the NTC pin will be 125mV, which corresponds to an ADC input of (340-125)mV = 215mV. The expected conversion result would be $215/340 * 2^{15}$ = 20721.

## OFFSET COMPENSATION

The host software can perform offset compensation by using an offset measurement value read from the ISL6295. When the offset calibration is enabled within the OFFSctrl register, the converter input is internally shorted to ground and an A/D conversion is performed at the specified resolution. The offset value is stored in the OFFSres register.

## ACCUMULATION/TIMING

The ISL6295 incorporates four 32-bit accumulators and four 32-bit elapsed time counters. The Discharge Current Accumulator (DCA) and the Charge Current Accumulator (CCA) are intended to record discharge and charge capacity values. The Discharge Time Counter (DTC) and the Charge Time Counter (CTC) are intended to maintain the total discharge time and charge time. Accumulated charge and discharge values can be used to determine state of charge of the battery as well as cycle count information. With information provided by the elapsed time counters, average charge and discharge currents over an extended period of time can be calculated.

Each of the four 32-bit accumulator registers is assigned a fixed "source" A/D result register. When the accumulator is

enabled, it is updated every 0.5s by adding the contents of the assigned result register value to the previous accumulated value. The accumulators are listed below with their assigned source registers:

| ABBR. | ACCUMULATOR NAME | SOURCE |
|---|---|---|
| DCAIres | Discharge Current Accumulator | Ires (Sign bit = 1) |
| CCA | Charge Current Accumulator | Ires (Sign bit = 0) |
| TA | Temperature Accumulator | ITres or ETres |
| GPADA | GPAD Accumulator | GPADres |

The measurement resolution of the accumulated value is equal to that selected for the associated conversion, up to a converter resolution of 15-bits. If a 15-bit A/D value is being accumulated, then the accumulator resolution in microvolt seconds is:

Accumulator LSB (µVs) = $(V_{REF}/2^{15})$ µV * 0.5s

When the 170mV reference is selected, this value equates to 2.59µVs per LSB.

## CHARGE/DISCHARGE ACCUMULATORS

The DCA accumulator is intended to accumulate discharge current, and the CCA accumulator is intended to accumulate charge current. Both accumulators use the Ires register as its source. For this reason, the lres register should be programmed for current measurement by selecting the SR pin as the multiplexed ADC input source.

During charging, the voltage at the SR pin will be negative. This translates to a positive voltage measurement with the sign bit set to '0'. Whenever the sign bit equals '0', the measured result will be added to the CCA register contents and the sum is returned to CCA. In this way, total charge current is accumulated in the CCA.

Similarly, during discharge, a positive voltage will exist at the SR pin. In this case, the conversion will result in the sign bit being set to '1' in the Ires register, indicating a negative value or discharge current condition. Under this condition, the DCA register will be updated with the discharge current measured during that conversion.

The value stored in the DCA or CCA register can be interpreted as illustrated in the following example. Using a 20mΩ sense resistor, the LSB can expressed in units of current as follows:

Accumulator LSB (µAs) = Voltage LSB/$R_{SENSE}$
$$= 129.5µAs$$

The "Accum" bit in the AccumCtrl register must be enabled for accumulation to occur in both the CCA and DCA registers.

## CHARGE/DISCHARGE TIME COUNTERS

The Charge Time Counter (CTC) will increment at the rate of 2 counts every second as long as a negative voltage is measured at the SR pin. The CTC can thereby maintain a

time count representing the total time that charge current has flowed into the battery.

The Discharge Time Counter (DTC) will increment at the rate of 2 counts every second as long as a positive voltage is measured at the SR pin. The DTC can thereby maintain a time count representing the total time that discharge current has flowed from the battery.

### *Power Modes*

The ISL6295 has five operational power modes: Power-on Reset, Run, Sample, Sample-Sleep, and Shelf-Sleep. Each consumes power according to the configuration settings as described below:

### POWER-ON RESET

When power is first applied to the V input, the ISL6295 automatically executes a Power-on Reset sequence. The device is held in a RESET state while the voltage is below the minimum operating threshold, $V_{POR}$. When the voltage on the VP pin rises above the $V_{POR}$ threshold, the ISL6295 will initialize itself by loading the internal counters, data and control registers with default values pre-written into the non-volatile EEPROM memory. Please refer to "Register Initialization" and "Factory Register Initialization" sections for a detailed description of the register initialization operation. When this is complete, the ISL6295 will enter the Run Mode.

### RUN MODE

During Run mode, the ISL6295 performs continuous A/D conversion cycles per the programming of the A/D conversion cycle described in the "A/D Conversion Cycle" section. During each cycle, one to eight conversions are performed, and the respective accumulators/time counters are updated at 0.5s interval using the most recent A/D conversion results.

Run Mode is entered following a Power-on Reset when the pack voltage ($V_{PACK}$) applied to the VP pin rises above the $V_{POR}$ threshold. Run Mode can also be entered from the Sample, Sample-Sleep, and Shelf-Sleep modes as to be described.

The ISL6295 will remain in RUN mode as long as the pack voltage is above the $V_{POR}$ threshold and Sample, Sample-Sleep, and Shelf-Sleep modes are not active.

### SAMPLE MODE

In Sample Mode, A/D measurements are not continuously performed as in Run Mode. Instead, they are performed at a user selectable rate. The purpose of Sample Mode is to reduce power consumption during periods of low rate change (charge or discharge). The power advantage of Sample Mode comes from the reduction in frequency of A/D measurements. The accumulation counters and timers will continue to run at the rate of 0.5s per update.

Sample Mode is entered by programming the "Samp" bit to '1' in the A/D Configuration register. The ISL6295 will remain

in Sample mode as long as "Samp" bit equals '1', the VP voltage is above the $V_{POR}$ threshold, and the Sample-Sleep and Shelf-Sleep modes are not active. Run mode will be resumed when the Samp bit is cleared to '0'.

The Sample mode rate is selected using the "SampDiv" bits within the A/D Configuration Register. The sample interval is given by ($2^{SampDiv}$ x 0.5) sec. The possible sample rate intervals are as follows:

| "SAMPDIV" | SAMPLE INTERVAL |
|---|---|
| Value = 0 | 0.5s |
| Value = 1 | 1.0s |
| Value = 2 | 2.0s |
| Value = 3 | 4.0s |
| Value = 4 | 8.0s |
| Value = 5 | 16.0s |
| Value = 6 | 32.0s |
| Value = 7 | 64.0s |

In Sample mode, much of the analog circuitry remains on. Therefore, the power savings is not as great as in Sample-Sleep Mode described below.

### SAMPLE-SLEEP MODE

In Sample-Sleep Mode, the ISL6295 goes into sleep mode and wakes up at a user-programmed interval to perform a set of conversions as programmed for the A/D cycle. The purpose of Sample-Sleep is to achieve the minimum power consumption possible while periodically measuring specified parameters.

While the ISL6295 is in the sleep portion of the Sample-Sleep interval, all of the analog circuitry is shut off, and the Sleep interval time is derived from a less accurate ultra low power on-chip oscillator that is separate from the primary oscillator. During the active portion of Sample-Sleep Mode, a single set of conversions is performed and RUN mode current will be consumed for the duration of the measurements. While in Sample-Sleep mode, the accumulation counters and timers will still continue to run at an uninterrupted rate of 0.5s per update.

Sample-Sleep Mode is invoked by one of the following actions:

1. Cell voltage on VP drops below the trip point programmed in the VCtrip register with the corresponding "VPent" bit set in the TRIPctrl register (If GPAD is grounded). This action can be used to prevent excessive battery discharge in the event of a dangerously low cell voltage.

2. If GPAD is used for other analog input, the GPAD voltage drops below the trip ponit programmed in the VCtrip register with the corresponding "GPADent" bit set in the TRIPctrl register.

3. Setting the "SSLP" bit in the OpMode register. The host can take this action when the system is entering a low power standby condition, and it is desireable to periodically update measurements for current, voltage, and/or temperature accumulation.

4. Magnitude of current measurement is less than the I-trip register value when "Ient" bit is set in the Tripctrl register.

The Sample-Sleep interval is determined by the programming of the "SampDiv" bits within the ADconfig register, together with the "SSLPdiv" bits within the OpMode register. The sample interval is $2^{SampDiv}$x $2^{SSLPdiv}$x 0.5sec. The possible Sample-Sleep interval time therefore ranges from a minimum of 0.5sec to over 136 minutes.

Exit from Sample-Sleep Mode to Run mode can be accomplished by clearing the "SSLP" bit or by programming a wake up based on pack voltage or current. Wake up based on charge current will occur when the "Iex" bit is set in the TRIPcntl register and the charging current value is above the threshold programmed in the I+trip register. Wake up based on pack voltage will occur when the "VPex" bit is set in the TRIPctrl register and the pack voltage rises above the threshold programmed in the VPtrip register.

### SHELF-SLEEP MODE

Shelf-Sleep Mode is the lowest power mode and is intended to preserve battery capacity when the battery pack is shipped or stored or if the battery voltage drops below a specified threshold. While in Shelf-Sleep mode, no ADC measurement is taken, no accumulation is performed, and no SMBus communications are recognized. In addition, volatile memory is not maintained.

Entry to Shelf-Sleep Mode is enabled by programming the "SHELF" bit in the OPmode register to '1' or "Shent" bit in the TRIPctrl register to '1' and when VP is less than SStrip. The Shelf Sleep mode will then be entered when the SMBus pins (both SDA and SCL) drop from a high to a low level for a minimum time period specified by $t_{SHELF}$. This action will also occur if the battery pack is physically disconnected from the system.

Exit from the Shelf-Sleep mode back to Run mode will occur when the SMBus pins (both SDA and SCL) are both pulled from a low to a high state, and remain high for a minimum time of $t_{WAKE}$ to signify system activity or connection of the pack to the host.

### *General Purpose Input/Output*

The NTC and GPAD pins have alternate functions of general purpose I/O. IO0 and IO1 respectively. These pins can be configured as digital General Purpose Inputs/Outputs if their normal application functions of temperature and voltage monitoring are not needed. Their configuration is controlled in the GPIOctrl register.

The NTC/IO0 pin may be configured as a push-pull output, an open-drain driver with internal pull-up, or as a three-stated pin. When configured as a push-pull or open drain output, the output high voltage is equal to the internally regulated supply voltage, which is nominally at 3.3V. When the output function is disabled, an external circuit may drive the pin as an input with a voltage range of 0-3.3V. The input function may be used whether or not the pin is driven by the ISL6295. In addition, the input function may be disabled, in which case, the input buffer is

powered down to prevent static current drain if the NTC pin rests at an intermediate level.

The GPAD/IO1 pin is similar to that of the NTC/IO0 except it is an open train only output with no resistive pull-up. Therefore, if the output is set to a logic 1, the internal pull-down is turned off and the pin is three-stated. The input function is the same as IO0.

NOTE: If the IO0 and/or IO1 pins are being used for their analog functions, their respective GPIO output and input functions must be disabled. The GPIO function may be totally disabled by clearing the appropriate GPIOctrl bit.

### General Purpose A/D Input

The GPAD/IO1 pin can be used as a general purpose A/D input as needed. The configuration is controlled in the GPAD A/D control register similar to the VP A/D control register. This pin should be connected to ground if not used.

### SMBus/I$^2$C™ Interface

The ISL6295 supports a 2-wire bidirectional bus and data transmission protocol that is fully compatible with the industry-standard SMBus V1.1 Packet Error Checking (PEC) CRC-8 error correction protocols based on the I$^2$C™ interface. This interface is used to read and write data from/to the on-chip registers and EEPROM. The device responds to the same SMBus slave address for access to all functions. The following is a brief overview of the SMBus/I$^2$C™ operational implementation in the ISL6295. Please refer to the SMBus V1.1 specification for complete operational details of this industry standard interface. This specification can be obtained at the SMBus Implementer's Forum web site at www.smbus.org.

### SMBus OVERVIEW

SMBus is a two-wire multi-master bus, meaning that more than one device capable of controlling the bus can be connected to it. A master device initiates a bus transfer and provides the clock signals. A slave device can receive data provided by the master or can in return provide data to the master.

Since more than one device may attempt to take control of the bus as a master, SMBus provides an arbitration mechanism, based on I$^2$C™ and relying on the wired-AND connection of all SMBus devices residing on the bus. If two or more masters try to place information on the bus, the first to produce a "ONE" when the other(s) produce a "ZERO" loses arbitration and has to release the bus.

The clock signals during arbitration are a wired-AND combination of all the clocks provided by SMBus masters. Bus clock signals from a master can only be altered by clock stretching or by other masters and only during a bus arbitration situation. In addition to bus arbitration, SMBus implements the I$^2$C™ method of clock low extending in order to accommodate devices of different speeds on the same bus.

SMBus version 1.1 can be implemented at any voltage between 3V and 5V $\pm$10%. Devices can be powered by the bus VDD or by their own power source (such as Smart Batteries)

and they will inter-operate flawlessly as long as they adhere to the SMBus electrical specifications.

### SMBus DATA TRANSFERS

A device that sends data onto the SMBus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a "master". The devices that are controlled by the master are "slaves". The SMBus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates START and STOP conditions. The ISL6295 operates as a slave on the two-wire bus. Connections to the bus are made via the open drain I/O lines SDA and SCL.

SMBus operates according to the following bus protocol:

- Data transfer may be initiated only when the bus is not busy.

- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high will be interpreted as control signals.

The SMBus specification defines the following bus conditions:

| | |
|---|---|
| **Bus Not Busy** | Both data and clock lines remain HIGH. |
| **Start Data Transfer** | A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition. |
| **Stop Data Transfer** | A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines a STOP condition. |
| **Data Valid** | The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit. |
| **Acknowledge** | Each receiving device, when addressed, is obliged to generate an Acknowledge bit after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit. |
| | A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition. |
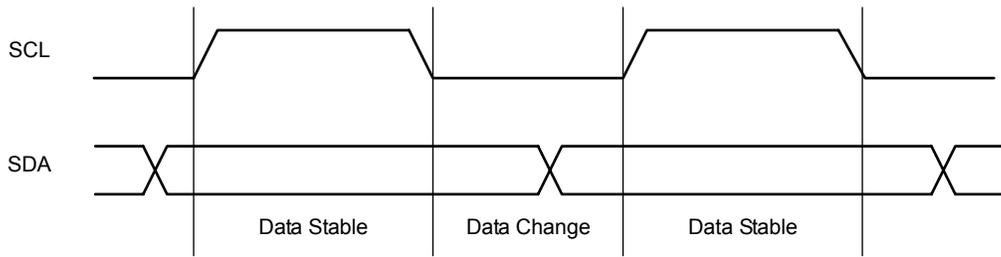
**FIGURE 3. VALID DATA CHANGES ON THE SDA BUS**
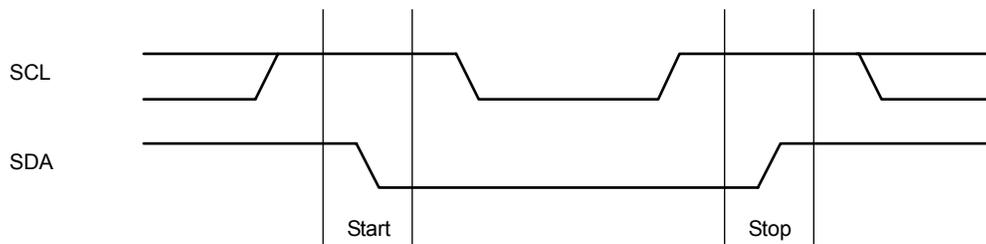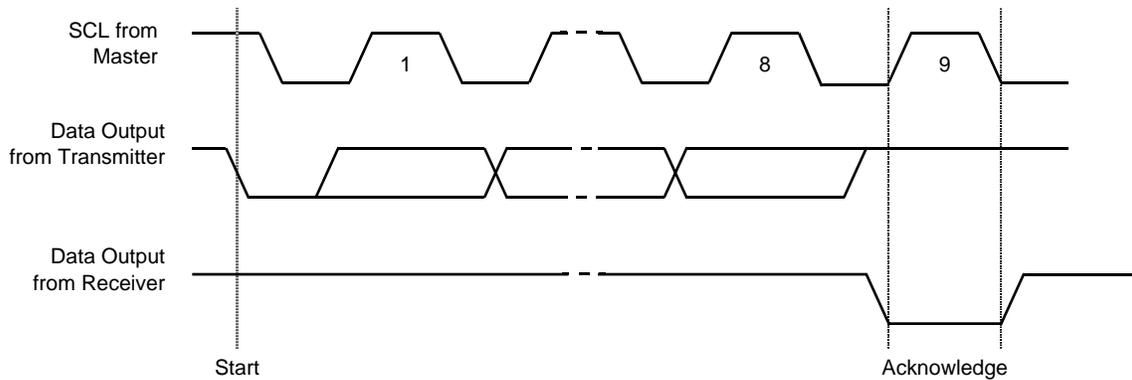


**FIGURE 4. VALID START AND STOP CONDITIONS**
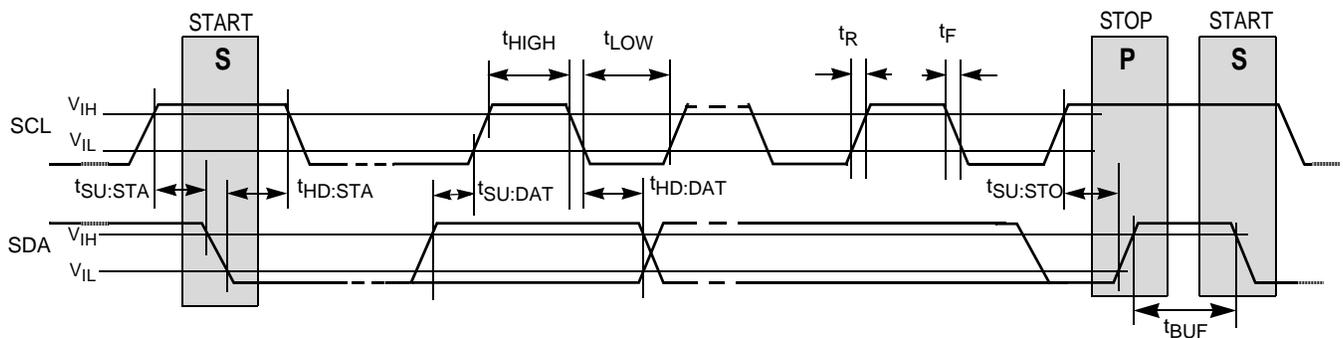


**FIGURE 5. ACKNOWLEDGE RESPONSE FROM RECEIVER**



**FIGURE 6. BUS TIMING**

Figures 3 through 6 detail how data transfer is accomplished on the SMBus. Depending upon the state of the R/W bit, two types of data transfer are possible:

1. **Data transfer from a master transmitter to a slave receiver:** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an Acknowledge bit after each received byte.

2. **Data transfer from a slave transmitter to a master receiver:** The first byte (slave address) is transmitted by the master. The slave then returns an Acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an Acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a 'Not Acknowledge' is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a Repeated START condition. Since a Repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The ISL6295 may operate in the following two modes:

1. **Slave receiver mode:** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.

2. **Slave transmitter mode:** The first byte is received and handled as in the Slave Receiver mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the ISL6295 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.



**Legend:**

| | |
|---|---|
| **S** | -Start |
| **P** | - Stop |
| **RS** | - Repeated start |
| **A** | - Acknowdedge |
| **$\overline{A}$** | - Negative Acknowledge (terminates transaction) |
| **BT** | - Block mode indicator bit |
| **Bank** | - Controls selection of bank: |
| |     00: EEPROM    10: Reserved |
| |     01: RAM / Registers    11: Reserved |
| **PEC** | - Packet Error Code |
| **AH** | - High order address bits (2) |
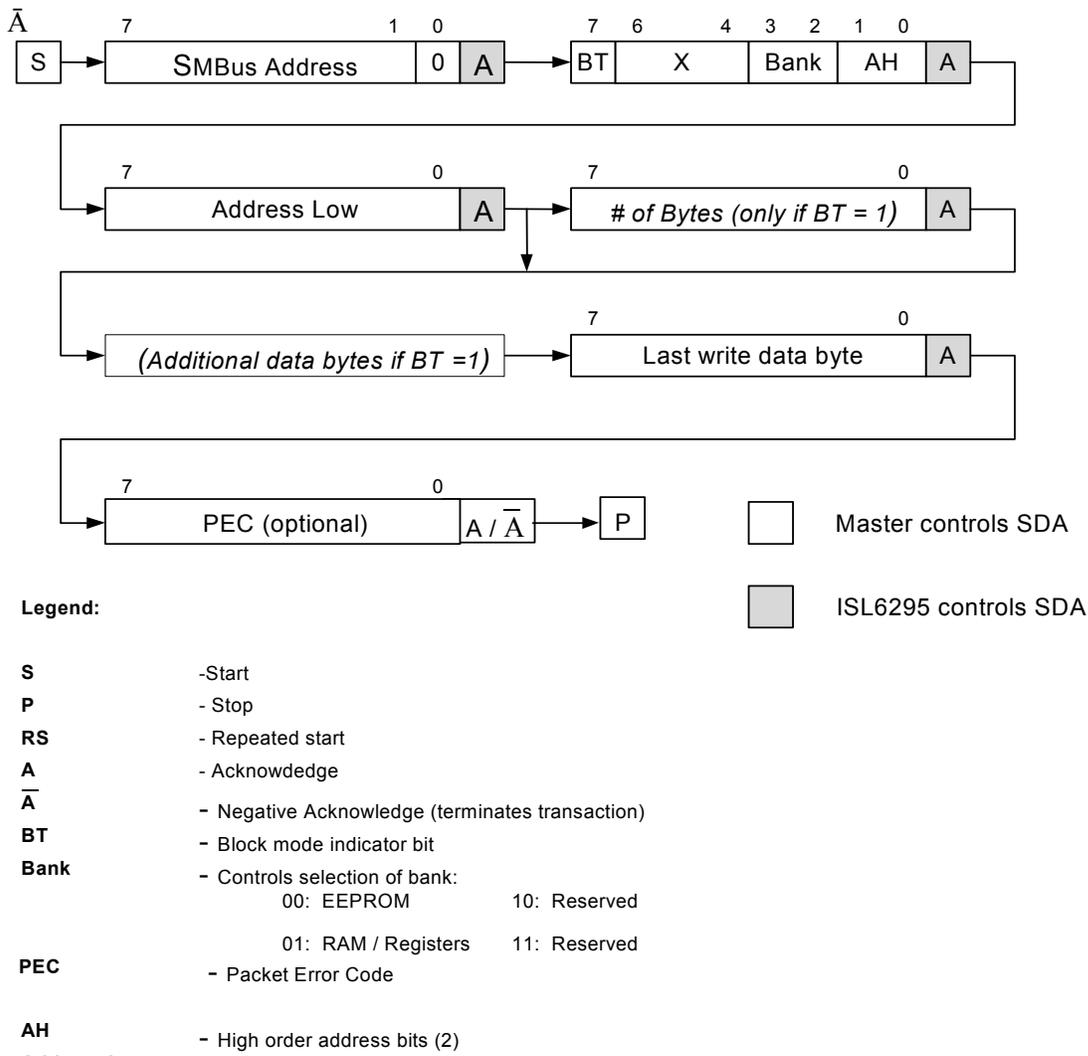
**FIGURE 7. ISL6295 SMBus WRITE TRANSACTION**

**Legend:**

| | |
|---|---|
| **S** | - Start |
| **P** | - Stop |
| **RS** | - Repeated start |
| **A** | - Acknowdedge |
| **$\overline{A}$** | - Negative Acknowledge (terminates transaction) |
| **BT** | - Block mode indicator bit |
| **Bank** | - Controls selection of bank: |

        00: EEPROM      10: Test Mode Registers
        01: RAM / Registers  11: Reserved

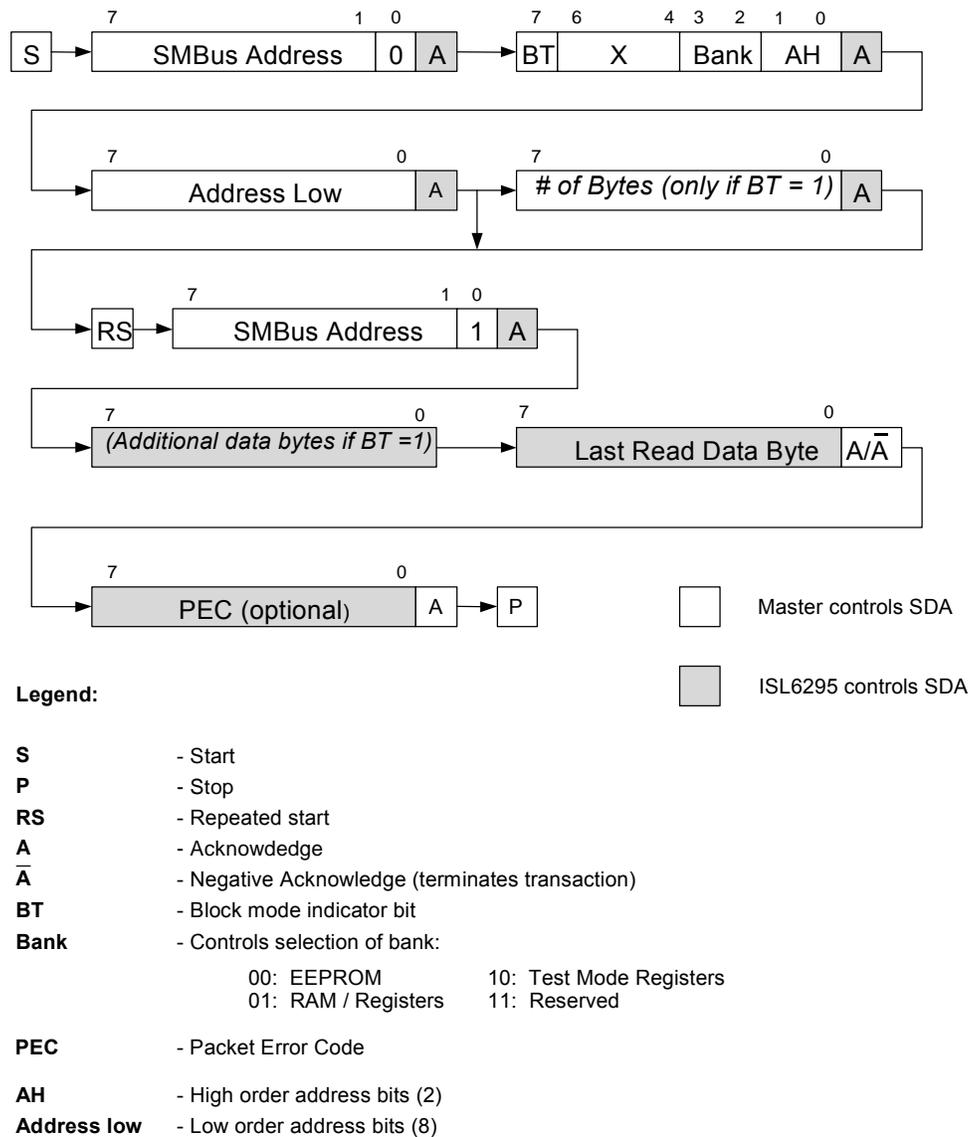| | |
|---|---|
| **PEC** | - Packet Error Code |
| **AH** | - High order address bits (2) |
| **Address low** | - Low order address bits (8) |

**FIGURE 8. ISL6295 SMBus READ TRANSACTION**

## Memory/Operational Register Description

### Memory/Register Map

The ISL6295 internal structure is accessible on a strict memory mapped basis. The only action directly taken by the ISL6295 in response to an SMBus command is to read or write registers, SRAM, or EEPROM locations. Any actions taken by ISL6295 happen as a result of values written to internal control registers.

Addressing in ISL6295 consists of 10 bits plus two bank select bits. Therefore, there are a total of 4K byte locations that are addressable within the ISL6295, organized as 4 banks of 1024 locations each. Bank 0 is dedicated for the EEPROM. Bank 1 contains the general-purpose SRAM and the data, status and control registers. Bank 2 contains test registers, and Bank 3 is reserved.

Table 1 describes the ISL6295 memory map. The notation is y:0xzzz where y is the bank number and zzz is the register address in HEX.

### EEPROM

The 256 byte EEPROM is located in bank 0 and occupies address 0:0x000 to 0:0x0FF. The EEPROM can be read using Byte or Block transfer modes, but can only be written a byte at a time. Writing the EEPROM takes approximately 4ms/byte. An EEPROM write cycle command from the SMBus is immediately acknowledged by the ISL6295 if no other EEPROM write cycles are in progress. If an EEPROM read or write cycle is attempted while a previous request to write is in progress, a negative Acknowledge will be returned until the previous write cycle is completed.

A read or write to a register or SRAM location will not be affected by an EEPROM write cycle in progress.

### General Purpose SRAM

32 bytes of General Purpose SRAM are provided as temporary storage and is located in Bank 1 at 1:0x000 through 1:0x01F. The RAM may be read or written using either the Byte or Block transfer modes.

### Operational Registers

The following is a detailed description of all registers within the ISL6295 including all control, status and result bits, and fields that are contained therein.

#### DCA - DISCHARGE COUNT ACCUMULATOR

The DCA is a 32-bit register that holds the total accumulated current discharged from the battery. While current accumulation is enabled, the DCA is updated every 0.5s by adding the magnitude of the latest current conversion result to the previous accumulated value as long as the sign bit of the Ires register is '1', indicating a discharge condition. When the sign bit is '0', no accumulation is performed by the DCA.

The DCA register will rollover if it is allowed be updated beyond 0xFFFFFFFF, so proper register maintenance by the host system is necessary. The DCA register may be cleared by setting the "CLR0" bit in the ACCclr register.

#### DTC - DISCHARGE TIME COUNT REGISTER

The DTC records the length of time that the battery is in a discharge condition. This register is incremented at a rate of 2Hz for as long as current accumulation is enabled and the sign bit of the Ires register returns a '1' following a current conversion.

Time accumulation in the DTC register is not expected to rollover over the life of the battery pack. If desired, the DTC register may be cleared by setting the "CLR1" bit in the ACCclr register.

#### CCA - CHARGE COUNT ACCUMULATOR

The CCA is a 32-bit register that holds the total accumulated charging current delivered to the battery. While current accumulation is enabled, the CCA is updated every 0.5s by adding the magnitude of the latest current conversion result to the previous accumulated value as long as the sign bit of the Ires register is '0', indicating a charge condition. When the sign bit is '1', no accumulation is performed by the CCA.

The CCA register will rollover if it is allowed to be updated beyond 0xFFFFFFFF, so proper register maintenance by the host system is necessary. The CCA register may be cleared by setting the "CLR2" bit in the ACCclr register.

#### CTC - CHARGE TIME COUNT REGISTER

The CTC records the length of time that the battery is in a charge condition. This register is incremented at a rate of 2Hz for as long as current accumulation is enabled and the sign bit of the Ires register returns a '0' following a current conversion.

Time accumulation in the CTC register is not expected to rollover over the life of the battery pack. If desired, the CTC register may be cleared by setting the "CLR3" bit in the ACCclr register.

#### TA - TEMPERATURE ACCUMULATOR

TA is the accumulated 32-bit value of temperature measurements from the internal or external temperature sensor. TA is updated by the Itres or Etres register. Selection of the internal temperature sensor or external thermistor for temperature accumulation is made through the "tsel" bit in the AccumCtrl register.

The TA register will rollover if it is allowed be updated beyond 0xFFFFFFFF, so proper register maintenance by the host system is necessary. The TA register may be cleared by setting the "CLR4" bit in the ACCclr register.

#### TAT - TEMPERATURE TIME COUNT REGISTER

The TAT register records the length of time that the ISL6295 is sensing temperature and accumulating the value in register TA. TAT is incremented at a rate of 2Hz for as long as temperature accumulation is enabled.

Time accumulation in the TAT register is not expected to rollover over the life of the battery pack. If desired, the TAT register may be cleared by setting the "CLR5" bit in the ACCclr register.

**TABLE 1.  ISL6295 MEMORY MAP**

| FUNCTION | BYTE 3 | BYTE 2 | BYTE 1 | BYTE 0 | BANK:ADDRESS (BYTE 0) |
|---|---|---|---|---|---|
| EEPROM | ↓↓↓ Battery Pack Information (unassigned)  ↓↓↓ | | | | 0:0x000 |
| | // | // | | | // |
| | ↑↑↑ Battery Pack Information (unassigned)  ↑↑↑ | | | | 0:0x01C |
| | ↓↓↓ Operational Registers Initialization Values  ↓↓↓ | | | | 0:0x020 |
| | // | // | | | // |
| | ↑↑↑ Operational Registers Initialization Values  ↑↑↑ | | | | 0:0x078 |
| | | | | | 0:0x07C |
| | Cal / Set-up Register 1 Initialization Values | | | | 0:0x080 |
| | Cal / Set-up Register 2 Initialization Values | | | | 0:0x084 |
| | ↓↓↓ Cell Look-up Tables (unassigned)  ↓↓↓ | | | | 0:0x088 |
| | // | // | | | // |
| | ↑↑↑ Cell Look-up Tables (unassigned)  ↑↑↑ | | | | 0:0x0FC |
| General Purpose SRAM | | | | | 1:0x000 |
| | // | // | | | // |
| | | | | | 1:0x01C |
| Operational Registers: Accumulators, Timers, A/D Registers and Mode Control | DCA | | | | 1:0x020 |
| | DTC | | | | 1:0x024 |
| | CCA | | | | 1:0x028 |
| | CTC | | | | 1:0x02C |
| | TA | | | | 1:0x030 |
| | TAT | | | | 1:0x034 |
| | GPADA | | | | 1:0x038 |
| | GPADT | | | | 1:0x03C |
| | ADconfig | Ictrl (ADc0) | Ires (ADr0) | | 1:0x040 |
| | Reserved 0x00h | ITctrl (ADc1) | ITres (ADr1) | | 1:0x044 |
| | | ETctrl (ADc2) | Etres (ADr2) | | 1:0x048 |
| | | VPctrl (ADc3) | VPres (ADr3) | | 1:0x04C |
| | GPIOctrl | Reserved | Reserved | | 1:0x050 |
| | Reserved 0x00h | GPADctrl (ADc5) | GPADres (ADr5) | | 1:0x054 |
| | | OFFSctrl (ADc6) | OFFSres (ADr6) | | 1:0x058 |
| | | AUXctrl (ADc7) | AUXres (ADr7) | | 1:0x05C |
| | ACCctrl | ACCclr | I+trip | | 1:0x060 |

**TABLE 1. ISL6295 MEMORY MAP  (Continued)**

| FUNCTION | BYTE 3 | BYTE 2 | BYTE 1 | BYTE 0 | BANK:ADDRESS (BYTE 0) |
|---|---|---|---|---|---|
| Operational Registers: Accumulators, Timers, A/D Registers and Mode Control **(Continued)** | Reserved 0x00h | Reserved 0x00h | I-trip | | 1:0x064 |
| | | | VPtrip | | 1:0x068 |
| | | | VCtrip | | 1:0x06C |
| | | | SStrip | | 1:0x070 |
| | | TRIPctrl | Reserved 0x00h | | 1:0x074 |
| | | OPmode | | | 1:0x078 |
| | | Reserved | | | 1:0x07C |
| Reserved | | // | // | | 2:0x000 |
| | | | | | // |
| | | | | | 2:0x0FC |
| Cal/Setup Registers | MOSCT | VREFT | VBGT | SMBaddr | 2:0x080 |
| | Reserved | AOSCT | TestMuxSel | ClkTM | 2:0x084 |

## GPADA - GPAD ACCUMULATOR

GPADA is a 32 bit register that holds the total accumulated value measured on the GPAD/IO1 pin. GPADA is incremented by the value in GPADres every 0.5s as long as the function is enabled by the AccV bit in the AccumCtrl register.

The GAPDA register will rollover if it is allowed to count beyond 0xFFFFFFFF, so proper register maintenance by the host system is necessary. The GAPDA register may be cleared by setting the "CLR6" bit in the ACCclr register.

## GPADT - GPAD TIME COUNT REGISTER

GPADT records elapsed time for which measurements are taken on the GPAD pin. GPADT is incremented at a rate of 2Hz for as long as GPAD accumulation is enabled.

Time accumulation in the GPADT register is not expected to rollover over the life of the battery pack. If desired, the GPADT register may be cleared by setting the "CLR7" bit in the ACCclr register.

## A/D CONFIGURATION REGISTER – ADconfig
### (Address - 43 Hex/67 Decimal)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ADEN | Samp | Reserved | | | SampDiv (2:0) | | |

**ADEN** Master A/D enable:  When set to a '1', A/D conversions can be performed. All A/D conversions are disabled when it is cleared to '0'.

**Samp** Sample Mode enable:  This bit controls the enabling of Sample mode when the ISL6295 is not in a Power-on Reset, Sample-Sleep, or Shelf-Sleep mode. When set to '1', Sample Mode is enabled and conversions will be performed at a periodic rate determined by the programming of the "SampDiv" bits. When cleared, Sample Mode is disabled and the ISL6295 will operate in Run Mode.

**Reserved** Reserved bit.

**SampDiv** The SampDiv bits define the time interval between executing an A/D conversion cycle sequence during Sample mode. The time interval between each conversion cycle is defined by: $2^{\wedge}(SampDiv) * 0.5s$

Note that if the time taken to complete an A/D conversion cycle is more than the defined interval, the time-overlapped pending conversion cycle(s) will be skipped until the previous conversion cycle is complete. For example, if SampDiv = 2, but the time taken to complete a conversion cycle is 5s, then the effective conversion time interval will be 6s.

## ACCUMULATOR CONTROL REGISTER – AccCtrl
### (Address - 63 Hex/99 Decimal)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Accum | AccI | AccT | AccV | tsel | Reserved | | |

**Accum** Accumulator Master Enable:  Master enable control for all accumulators. If any combination of "AccI", "AccT" and "AccV" are enabled, "Accum" must also be enabled to permit accumulation. If "Accum" is '0', no accumulation will occur regardless of the settings of "AccI", "AccT" and "AccV".

**AccI** Current Accumulation enable:  When set to '1', current accumulation is enabled. The DCA and CCA registers will periodically add the value of the Ires register to its accumulated result. Also, the DTC and CTC elapsed time counters will count during discharge and charge respectively. When "AccI" is cleared to '0', current accumulation is disabled.

**AccT** Temperature Accumulation enable:  When set to '1', accumulation will be enabled in the TA. TA will accumulate results from either ITres or ETres register, depending on the setting of the "tsel" bit. While enabled, the TAT eapsed time counter will increment. When "AccT" is cleared to '0', TA accumulation will be disabled.

**AccV** GPAD Voltage Accumulation enable:  When set to '1', accumulation in GPADA will be updated by results from the GPADres register. While enabled, the GPADT elapsed time counter will increment. When "AccV" is cleared to '0', GPADA accumulation will be disabled.

**tsel** Temperature Accumulation selection:  Selects temperature sensing source used for accumulation.
    0 = internal temperature sensor is used
    1 = external temperature sensor is used

**Reserved** Reserved bit.

## A/D CONTROL REGISTERS

The eight A/D control registers are defined as follows:

| A/D Reg | NAME | FUNCTION | Addr |
|---|---|---|---|
| ADc0 | Ictrl | Current measurement control | 42h |
| ADc1 | Itctrl | Internal temperature measurement control | 46h |
| ADc2 | Etctrl | External temperature measurement control | 4Ah |
| ADc3 | VPctrl | Pack voltage measurement control | 4Eh |
| ADc4 | Reserved | | 52h |
| ADc5 | GPADctrl | GPAD voltage measurement control | 56h |
| ADc6 | OFFSctrl | Offset measurement control | 5Ah |
| ADc7 | AUXctrl | Auxiliary measurement control | 5Eh |

The eight A/D control registers contain the following bits:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Enable | Resolution | | | Reference | | Select | |

**Enable**   A/D Measurement enable:  Setting this bit enables the A/D measurements defined by bits 0-6.

**Resolution**   A/D Resolution selection:  These 3 bits control the magnitude resolution of the A/D measurement performed for the corresponding A/D result register as follows:

| RESOLUTION | # BIT CONVERSION |
|---|---|
| 0 | 8-bit conversion |
| 1 | 9-bit conversion |
| 2 | 10-bit conversion |
| 3 | 11-bit conversion |
| 4 | 12-bit conversion |
| 5 | 13-bit conversion |
| 6 | 14-bit conversion |
| 7 | 15-bit conversion |

**Reference**   A/D Reference selection:  Selects the reference voltage used for the pending A/D conversion.
   0 = 170mV reference (for differential conversion)
   1 = 340mV reference (for single-ended conversion)

**Select**   A/D Input selection:  Selects the analog multiplexer input for the pending A/D conversion as follows:

   Select = 0:  Current (SR pin voltage)

   Select = 1:  Internal temperature sensor

   Select = 2:  External temperature sensor (NTC pin voltage)

   Select = 3:  Pack Voltage

   Select = 4:  Reserved

   Select = 5:  GPAD Voltage

   Select = 6:  Offset voltage

   Select = 7:  Offset voltage

In order for the A/D control registers to function according to their names, their select fields should be programmed as follows:

| A/D REG. # | NAME | SELECT VALUE |
|---|---|---|
| ADc0 | Ictrl | 0 |
| ADc1 | Itctrl | 1 |
| ADc2 | Etctrl | 2 |
| ADc3 | VPctrl | 3 |
| ADc4 | Rsvd | |
| ADc5 | GPADctrl | 5 |
| ADc6 | OFFSctrl | 6 |
| ADc7 | AUXctrl | X |

## A/D RESULT REGISTERS

The eight 16-bit A/D result registers are defined as follows:

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Sign | Magnitude | | | | | | | | | | | | | | |

| A/D REG | NAME | FUNCTION | ADDR |
|---|---|---|---|
| ADr0 | Ictrl | Current measurement result | 40h |
| ADr1 | Itctrl | Internal temperature measurement result | 44h |
| ADr2 | Etctrl | External temperature measurement result | 48h |
| ADr3 | VPctrl | Pack voltage measurement result | 4Ch |
| ADr4 | Reserved | | |
| ADr5 | GPADctrl | GPAD Voltage measurement result | 54h |
| ADr6 | OFFSctrl | Offset measurement result | 58h |
| ADr7 | AUXctrl | Auxiliary measurement result | 5Ch |

The eight A/D result registers contain the following:

**Magnitude** Magnitude of A/D output: Reports the magnitude value of the A/D measurement with 00h representing a zero value and 7Fh representing full scale (magnitude of ADC input voltage equals $V_{REF}$). The magnitude value is left-justified, meaning that result from a N-bit conversion, as defined by the resolution specified within the A/D Control register, will occupy bit locations from bit 14 to bit (15-N).

**Sign** Polarity of the A/D measurement: The sign bit shows the polarity of the A/D measurement.
  0 = positive value
  1 = negative value

## GPIO CONTROL REGISTER - GPIOctrl
### (Address 53 Hex/83 Decimal)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PP0 | OE0 | IE1 | IE0 | OUT1 | OUT0 | IN1 | IN0 |

These GPIO control bits are relevent only when the respective GPIO enable bit (contained within the VREFT register) is set.

**PP0** IO0 Push-Pull Output mode: Setting this bit to '1' will configure the IO0 pin as a push-pull digital output. If set to '0', the IO0 pin will become an open drain output with a 300kΩ pull-up to the internal regulated supply. To be used in conjunction with the "OE0" bit.

**OE0** IO0 Output Enable: Setting this bit to '1' will configure the IO0 pin to be either a push-pull output (when PP0 = '1') or open drain output (when PP0 = '0'). If "OE0" is reset to '0', the IO0 pin is three-stated (when PP0 = '1') or pulled up to the internal regulated supply through a 300kΩ resistor (when PP0 = '0').

**IE1** IO1 Input enable: Setting this bit to '1' enables the IO1 pin to be used as a digital input. If reset to '0', the digital input buffer on IO1 is powered down and the "IN1" bit will always read logic 0.

**IE0** IO0 Input enable: Setting this bit to '1' enables the IO0 pin to be used as a digital input. If reset to '0', the digital input buffer on IO0 is powered down and the "IN0" bit will always read logic 0.

**OUT1** IO1 Output Data: Controls the open drain pull-down device. When "0" is written, the pull-down device is enabled and the IO1 pin outputs a logic 0. When set to "1", the pull-down device is disabled and the IO1 is three-stated.

**OUT0** IO0 Output Data: Sets the logic level driven on the IO0 pin. Relevant only when Output Enable bit "OE0" is set.

**IN1** IO1 Input Data: Current logic state of the IO1 pin (read- only).

**IN0** IO0 Input Data: Current logic state of the IO0 pin (read- only).

## ACCUMULATOR CLEAR REGISTER - ACCclr
### (Address - 62 Hex/98 Decimal)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CLR7 | CLR6 | CLR5 | CLR4 | CLR3 | CLR2 | CLR1 | CLR0 |

A '1' in any of the "CLRn" bits will clear the associated accumulator. Following the clear operation, all of the bits in the AccClr register will be reset to 0.

**CLR7** Clear GPADT Timer

**CLR6** Clear GPADA Accumulator

**CLR5** Clear TAT Timer

**CLR4** Clear TA Accumulator

**CLR3** Clear CTC Timer

**CLR2** Clear CCA Accumulator

**CLR1** Clear DTC Timer

**CLR0** Clear DCA Accumulator

## TRIP POINT VALUE REGISTERS

There are 5 registers that are utilized to set up Trip Point Values. These registers are used when enabled by the TRIPctrl register to enter or exit various power modes. Three of these trip point value registers contain voltage values and two contain current values. Locations of the trip point detection enable bit and the corresponding compare and trip point value registers are listed below:

| TPV REGISTER | LOCATION | COMPARISON REGISTER | ENABLE BIT |
|---|---|---|---|
| I+trip | 60h | Ires | Iex |
| I-trip | 64h | Ires | Ient |
| VPtrip | 68h | VPres | VPex |
| VCtrip | 6Ch | VPres or GPADres | VPent or GPADent |
| SStrip | 70h | VPres | Shent |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Sign | Magnitude | | | | | | | | | | | | | | |

VPtrip, VCtrip and SStrip are used as voltage values to be compared to VPres, GPADres and VPres respectively for transitioning in and out of various power modes. I+trip and I-trip are used as current values to be compared to Ires for transitioning in and out of various power modes. The data format in these registers is left justified. For the purpose of trip point detection, only magnitude is compared and the sign is ignored.

## OPERATION MODE CONTROL REGISTER - OPmode
**(Address 7A Hex/122 Decimal)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SSLP | RESERVED | SSLPdiv | | | SHELF | POR | sPOR |

**SSLP** Sample-Sleep Mode enable: Setting this bit to '1' immediately enables Sample-Sleep Mode. Clearing this bit immediately disables Sample-Sleep mode.

**Reserved** Reserved bit.

**SSLPdiv** Sample-Sleep Divider setting: Sets the interval between executing an A/D conversion cycle during Sample-Sleep mode. The time interval between each conversion cycle is defined by:

$$2^{(SampDiv)} * 2^{(SSLPdiv)} * 0.5 \text{ sec}$$

Note that if the time taken to complete an A/D conversion cycle is more than the defined interval, the time-overlapped pending conversion cycle(s) will be skipped until the previous conversion cycle is complete.

**SHELF** Shelf-Sleep Mode enable: Setting this bit to '1' will prepare the device for Shelf-Sleep mode. The Shelf-Sleep mode will not be entered until a SMBus Stop condition occurs, when both SDA and SCL pins go low.

**POR** Power-on Reset Flag: This bit will read a '1' when a Power-on Reset has occurred. Writing a '0' to this bit will clear the POR flag.

**sPOR** Soft Reset: Writing a '1' to this bit will cause the device to re-initialize by reloading EEPROM contents into all working registers. This function has the same effect as the initial Power-on Reset.

## TRIP CONTROL REGISTER - TRIPctrl
**(Address 76 Hex/118 Decimal)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Iex | Ient | VPex | VPent | GPADent | Shent | Rsvd | Oflow |

**Iex** Note1 Exit from Sample-Sleep Mode on current: A '1' in this bit will enable an exit from Sample-Sleep Mode upon the following condition: |current| >I+Trip

**Ient** Enter Sample-Sleep Mode on current: A '1' in this bit will enable entry to Sample-Sleep Mode under the following condition: |current| <I-Trip

**VPex** Note1 Exit from Sample-Sleep Mode on Pack voltage: A '1' in this bit will enable an exit from Sample-Sleep Mode upon the following condition: VP > VPtrip

**VPent** Enter Sample-Sleep Mode on Pack voltage: (Use VPent only if GPAD is not used and grouned) A '1' in this bit will enable entry to Sample-Sleep Mode upon the following condition: VP < VCtrip

**GPADent** Enter Sample-Sleep Mode on GPAD voltage: A '1' in this bit will enable entry to Sample-Sleep Mode upon the following condition: GPAD < VCtrip

**Shent** Enter Shelf-Sleep Mode on Pack voltage: A '1' in this bit will enable entry to Shelf-Sleep mode upon the following condition: VP < SStrip

**Rsvd** Reserved bit.

**Oflow** ADC Overflow flag: This bit is set when the ADC input voltage is beyond the designed voltage range of the ADC. This bit will remain set until a '0' is written to it.

Note1: The exit conditions are verifyed by design but not tested in production.

## Register Initialization

During the Power-on Reset sequence, all registers are loaded with initial values from EEPROM locations 0x020-0x087. These EEPROM locations are reserved to contain register initialization values. In a battery pack application, a Power-on Reset typically happens only at the time of pack manufacture, when the cells are first connected to the battery monitoring PCB containing the ISL6295.

Data in the EEPROM locations 0:0x020-0:0x07F will be loaded into the corresponding register locations 1:0x020-1:0x07F in Bank 1. Data in the EEPROM locations, 0:0x080-0:0x087 will be loaded into the corresponding Cal/Setup register locations 2:0x080-2:0x087 in Bank 2. In all cases, EEPROM register initialization locations corresponding to "Reserved" register locations must contain the value of 0x00h in order to insure proper operation following a Power-on Reset.

## Factory Register Initialization

The EEPROM register initialization locations are programmed with a set of default values at the time that the ISL6295 is manufactured. This programming results in the following operational state following a Power-on Reset:

- All Accumulators and Time Counters disabled and reset to zero

- All A/D Conversion disabled

- A/D registers programmed with zeroes

- Sample and Shelf-Sleep modes disabled

- All Sample-Sleep mode entry methods disabled and trip point values reset to zero

- GPIO mode disabled on GPAD and NTC pins

- SMBus address = 0x26

- Factory calibrated trim values for bandgap, voltage reference, and main and auxiliary oscillators.

Table 2 lists in detail the values that are programmed into the EEPROM register initialization locations.

*CAUTION: Some critical calibration and initialization data is programmed into the EEPROM locations with default values at the time of the ISL6295 manufacture. Any modification to these values may cause incorrect operation or malfunction of the part. The following table sumarises the critical control registers where the default settings must be kept.*

### TABLE 2. CRITICAL CONTROL REGISTERS

| Name | Address | Default Setting |
|---|---|---|
| SMB Address | 0x80 | 0x26 (Bits 0-7) (0 0 1 0 0 1 1 0) 7           0 |
| Band Gap Trim | 0x81 | Factory Trimmed Value |
| Voltage Reference Trim | 0x82 | Factory Trimmed Value |
| Main Oscillator | 0x83 | Factory Trimmed Value |
| clkTM (Clock Test Mode) | 0x84 | 0x00 |
| Test Mux | 0x85 | 0x00 |
| Aux Oscillator | 0x86 | Factory Trimmed Value |

**TABLE 3. ISL6295 REGISTER INITIALIZATION**

| FUNCTION | BYTE 3 | BYTE 2 | BYTE 1 | BYTE 0 | BANK:ADDRESS (BYTE 0) |
|---|---|---|---|---|---|
| **Operational Registers:**<br><br>**Accumulators, Timers, A/D Registers and Mode Control** | DCA: 0x00000000 | | | | 1:0x020 |
| | DTC: 0x00000000 | | | | 1:0x024 |
| | CCA: 0x00000000 | | | | 1:0x028 |
| | CTC: 0X00000000 | | | | 1:0x2C |
| | TA: 0X00000000 | | | | 1:0x30 |
| | GPADA: 0X00000000 | | | | 1:0x34 |
| | GPADT: 0X00000000 | | | | 1:0x38 |
| | CTC: 0x00000000 | | | | 1:0x3C |
| | ADconfig: 00000000b = 0x00 | Ictrl (ADc0): 01110000b = 0x70 | Ires (ADr0): 0x0000 | | 1:0x040 |
| | Reserved 0x00 | ITctrl (ADc1): 00101001b = 0x29 | ITres (ADr1): 0x0000 | | 1:0x044 |
| | | ETctrl (Adc2): 00101010b = 0x2A | Etres (ADr2): 0x0000 | | 1:0x048 |
| | | VPctrl (ADc3): 00101011b = 0x2B | VPres (ADr3): 0x0000 | | 1:0x04C |
| | Reserved: 0x00 | GPADctrl (ADc5): 00100101b = 0x25 | GPADres (ADr5): 0x0000 | | 1:0x054 |
| | | OFFSctrl (ADc6): 01110110b = 0x76 | OFFSres (ADr6): 0x0000 | | 1:0x058 |
| | | AUXctrl (ADc7): 00000110b = 0x06 | AUXres (ADr7): 0x0000 | | 1:0x05C |
| | ACCctrl: 00000000b = 0x00 | ACCclr: 00000000b = 0x00 | I+trip: 0x0000 | | 1:0x060 |
| | Reserved: 0x00 | Reserved: 0x00 | I-trip: 0x0000 | | 1:0x064 |
| | | | VPtrip: 0x0000 | | 1:0x068 |
| | | | VCtrip | | 1:0x06C |
| | | | SStrip: 0x0000 | | 1:0x070 |
| | | TRIPctrl: 00000000b = 0x00 | Reserved: 0x00 | | 1:0x074 |
| | | OPmode: 00000000b = 0x00 | | | 1:0x078 |
| | | Reserved: 0x00 | | | 1:0x07C |
| **Cal/Setup Registers** | MOSCT: 0xxxxxxxb ('xxxxxxx' = factory trim value) | VREFT: 00xxxxxxb ('xxxxxx' = factory trim value) | VBGT 0000xxxxb ('xxxx' = factory trim value) | SMBaddr: 00100110b | 2:0x080 |
| | Reserved: 0x00 | AOSCT: 000xxxxxb ('xxxxx' = factory trim value) | TestMuxSel: 00000000b | clkTM: 00000000b | 2:0x084 |

## Cal/Setup Mode AND Registers

Cal/Setup mode allows the pack designer to re-program the default SMBus address and/or change the calibration parameters programmed at the factory for bandgap, voltage reference, and oscillators trim values.

Entering Cal/Setup requires the host to request three consecutive and specific incorrect SMBus addresses with no interruptions between requests. These addresses are:

Addr1          hex 50
Addr2          hex 52
Addr3          hex 74

After each address is sent, the ISL6295 will NACK the address. Once the sequence is complete, the ISL6295 will enter Cal/Setup mode and allow access to the test mode registers located in memory bank 2.

To exit Cal/Setup mode, re-enter the same address sequence or power down the device. The ISL6295 will always power up with test mode disabled.

The following registers are only available in test mode.

### SMBUS ADDRESS REGISTERS - SMBaddr
**(Address 80 Hex/128 Decimal)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SMBadd | | | | | | | Reserved |

**SMBAdd**    SMBus Address:  Defines the SMBus address for this device.

**Reserved**    Reserved bit

### BAND-GAP TRIM REGISTER - VBGT
**(Address 81 Hex/129 Decimal)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | Vbgt | | | |

**Reserved**    Reserved bits

**Vbgt**    Band-gap Voltage trim setting:
Nominal setting = 0111
LSB voltage step = 4mV

### VOLTAGE REFERENCE TRIM REGISTER - VREFT
**(Address 82Hex/130 Decimal)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| GPIOen1 | GPIOen0 | Vreft | | | | | |

**GPIOen1**  '  IO1 pin GPIO enable:  Setting this bit to '1' configures the GPAD/IO1 pin to be used as a GPIO. When enabled as GPIO, the GPAD accumulation function in the ACCctrl register and the trip function in the TRIPctrl register must be disabled.

**GPIOen0**    IO0 pin GPIO enable:  Setting this bit to '1' configures the NTC pin to be used as a GPIO. When enabled as GPIO, the external temperature accumulation function in the ACCctrl register must be disabled.

**Vreft**    Voltage Reference trim setting:
Nominal setting = 011111
LSB voltage step = 0.2%

### MAIN OSCILLATOR TRIM REGISTER - MOSCT
**(Address 83 Hex/131 Decimal)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | MOsct | | | | | | |

**Reserved**    Reserved bit. Must be set to '0'.

**MOsct**    Main Oscillator trim setting:
Nominal setting = 0111111
LSB frequency step = 0.25%

### CLOCK TEST MODE REGISTER - clkTM
**(Address 84 Hex/132 Decimal)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Revision | | | | | ExtClk | clkTM | |

**Revision**    This is a read-only register identifying the silicon revision number of the device.

**ExtClk**    External Clock enable:  When set, the clock input to the accumulators and digital control logic within the ISL6295 is taken from the NTC pin.

For production test only. Must be set to '0' during normal operation.

**clkTM**    Clock Test Mode control:  These bits can be used to speed up testing of the clock divider chain used to generate the internal 2Hz accumulator clock (Tacc). This test mode can also be used to speed up the accumulator clock for faster accumulator test time. During normal operation, the 2Hz clock is derived by dividing the main 131kHz reference clock through a 16-bit divider chain. The divider chain can be bypassed as follows:

clkTM = 00: Normal operation (Tacc = 2Hz)

clkTM = 01: Use only divider bits 0-5
(Tacc = 2kHz)

clkTM = 10: Use only divider bits 6-11
(Tacc = 2kHz)

clkTM = 11: Use only divider bits 12-15
(Tacc = 8.2kHz)

For production test only. Must be set to '00' during normal operation.

## Fuel Gauge Operation

The operation overview diagram in Figure 9 illustrates the fuel gauge operation of the ISL6295. The ISL6295 incorporates four 32-bit accumulators and four 32-bit elapsed time counters. The Charge Current Accumulator (CCA) and Discharge Current Accumulator (DCA)

accumulate a measure of charge and discharge currents for the capacity calculation and cycle count. The Charge Time Counter (CTC) and Discharge Time Counter (DTC) are intended to maintain the total charge time and discharge time for the self-discharge, average charge, and discharge currents over an extended period of time.
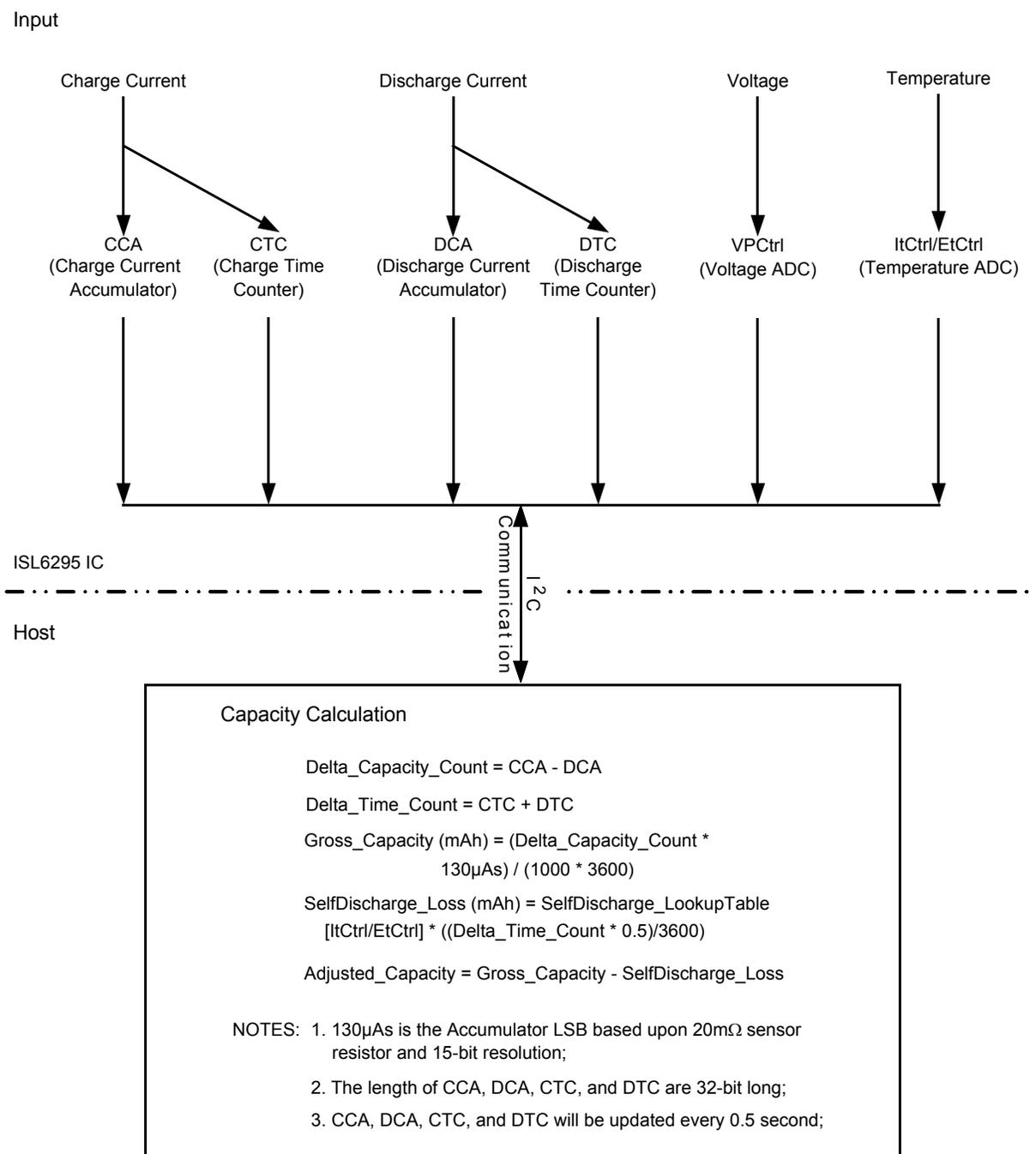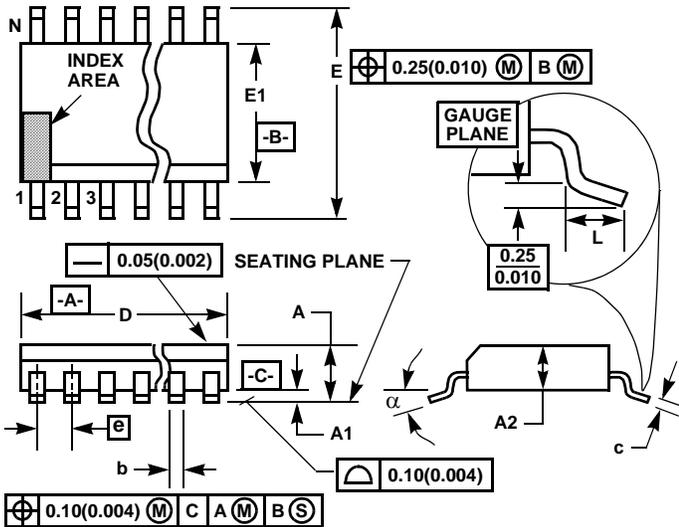
Input

| Charge Current | Discharge Current | Voltage | Temperature |
|---|---|---|---|
| CCA (Charge Current Accumulator) CTC (Charge Time Counter) | DCA (Discharge Current Accumulator) DTC (Discharge Time Counter) | VPCtrl (Voltage ADC) | ItCtrl/EtCtrl (Temperature ADC) |

ISL6295 IC

Host

Communication $I^2C$

Capacity Calculation

Delta_Capacity_Count = CCA - DCA

Delta_Time_Count = CTC + DTC

Gross_Capacity (mAh) = (Delta_Capacity_Count * 130µAs) / (1000 * 3600)

SelfDischarge_Loss (mAh) = SelfDischarge_LookupTable [ItCtrl/EtCtrl] * ((Delta_Time_Count * 0.5)/3600)

Adjusted_Capacity = Gross_Capacity - SelfDischarge_Loss

NOTES:  1. 130µAs is the Accumulator LSB based upon 20mΩ sensor resistor and 15-bit resolution;

2. The length of CCA, DCA, CTC, and DTC are 32-bit long;

3. CCA, DCA, CTC, and DTC will be updated every 0.5 second;

**FIGURE 9. FUEL GAUGE OPERATION**

## Thin Shrink Small Outline Plastic Packages (TSSOP)



**M8.173**
**8 LEAD THIN SHRINK NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|--------|--------|--------|-------------|--------|-------|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.047 | - | 1.20 | - |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 | - |
| A2 | 0.031 | 0.051 | 0.80 | 1.05 | - |
| b | 0.0075 | 0.0118 | 0.19 | 0.30 | 9 |
| c | 0.0035 | 0.0079 | 0.09 | 0.20 | - |
| D | 0.116 | 0.120 | 2.95 | 3.05 | 3 |
| E1 | 0.169 | 0.177 | 4.30 | 4.50 | 4 |
| e | 0.026 BSC | | 0.65 BSC | | - |
| E | 0.246 | 0.256 | 6.25 | 6.50 | - |
| L | 0.0177 | 0.0295 | 0.45 | 0.75 | 6 |
| N | 8 | | 8 | | 7 |
| $\alpha$ | $0^O$ | $8^O$ | $0^O$ | $8^O$ | - |

Rev. 1 12/00

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.

2. Dimensioning and tolerancing per ANSI Y14.5M-1982.

3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.

4. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.

5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.

6. "L" is the length of terminal for soldering to a substrate.

7. "N" is the number of terminal positions.

8. Terminal numbers are shown for reference only.

9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).

10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

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