



I²C LCD Module Calibrator

The VCOM voltage of an LCD panel needs to be adjusted to remove flicker. This part provides a digital interface to control the sink-current output that attaches to an external voltage divider. The increase in output sink current lowers the voltage on the external divider, which is applied to an external VCOM buffer amplifier. The desired VCOM setting is loaded from an external source via a standard 2 wire I²C serial interface. At power up the part automatically comes up at the last programmed EEPROM setting.

An external resistor attaches to the SET pin, and sets the full-scale sink current that determines the lowest voltage of the external voltage divider.

The ISL45041 is available in an 8 Ld 3mm x 3mm Thin DFN package with a maximum thickness of 0.8mm for ultra thin LCD panel design.

An evaluation kit complete with software to control the DCP from a computer is available. Reference Application note AN1207 and Ordering Information.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL45041IRZ	041Z	0 to 85	8 Ld Thin 3x3 DFN	L8.3X3A
ISL45041IRZ-T	041Z	0 to 85	8 Ld Thin 3x3 DFN Tape and Reel	L8.3X3A
ISL45041EVAL1	Evaluation Board			

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

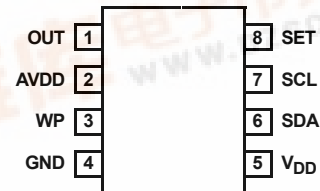
- 128-Step Adjustable Sink Current Output
- 2.25V to 3.3V Logic Supply Voltage Operating Range (2.6V Minimum Programming Voltage)
- Analog Supply Voltage Range 4.5V to 18V for VDD from 2.6V to 3.6V; 4.5V to 13V for VDD from 2.25V to 3.6V
- I²C Interface (Slave and Transmitter) - Address: 1001111
- On-Board 7-Bit EEPROM
- Output Adjustment SET Pin
- Output Guaranteed Monotonic Over Temperature
- Thin 8 Ld 3mm x 3mm DFN (0.8mm max)
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- LCD Panels

Pinout

ISL45041 (THIN DFN)
TOP VIEW



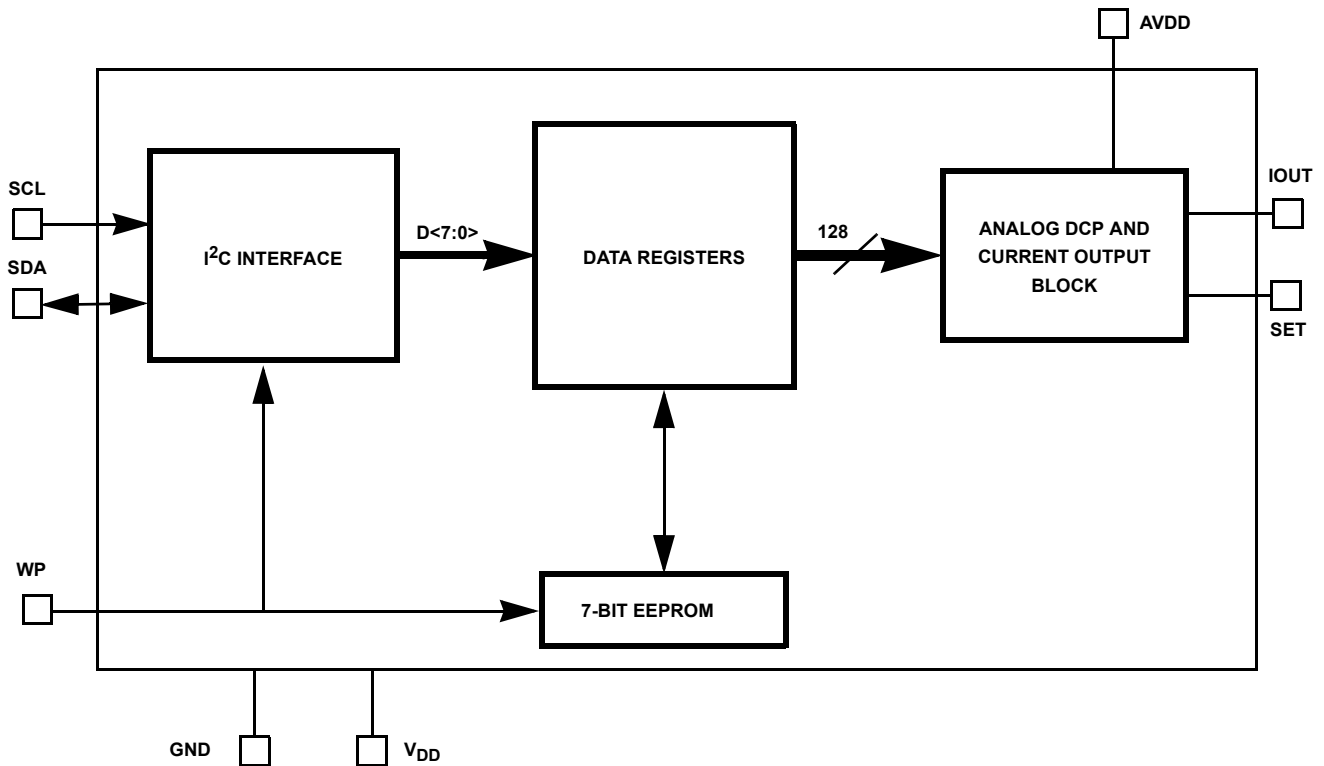
ISL45041

Pin Descriptions

PIN	TYPE	PULL U/D	FUNCTION
OUT	Output		Adjustable Sink Current Output Pin. The current sinks into the OUT pin is equal to the DAC setting times the maximum adjustable sink current divided by 128. See SET pin function description for the maxim adjustable sink current setting.
AVDD	Supply		High-Voltage Analog Supply. Bypass to GND with 0.1 μ F capacitor.
WP	Input	Pull Down	Write Protect. Active Low. To enable programming, connect to 0.7*VDD supply or greater.
GND	Supply		Ground connection.
VDD	Supply		System power supply input. Bypass to GND with 0.1 μ F capacitor.
SDA	In/Out		I ² C Serial Data Input
SCL	Input		I ² C Clock Input
SET	Analog		Maximum Sink Current Adjustment Point. Connect a resistor from SET to GND to set the maximum adjustable sink current of the OUT pin. The maximum adjustable sink current is equal to (AVDD/20) divided by RSET.

Block Diagram

ISL45041



ISL45041

Absolute Maximum Ratings

V _{DD} to Ground	+4V
Input Voltages to GND	
SET	-0.3V to +4V
AVDD	-0.3V to +20V
Output Voltages to GND	
OUT	-0.3V to +20V
ESD Rating	
HBM for Device	.2kV
HBM for Input Pins (SCL, SDA)	.4kV

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
8 Ld Thin DFN Package	170
Moisture Sensitivity (see Technical Brief TB363)	
All Packages	Level 2
Maximum Junction Temperature (Plastic Package)	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C
(Lead Tips Only)	

Operating Conditions

Temperature Range	
ISL45041IR	0°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications Test Conditions: V_{DD} = 3V, AVDD = 10V, OUT = 5V, R_{SET} = 24.9k Ω ; Unless Otherwise Specified.
Typicals are at T_A = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
V _{DD} Supply Range - Operating	V _{DD}		Full	2.25	-	3.6	V
V _{DD} Supply Range - EEPROM Programming	V _{DD}		Full	2.6	-	3.6	V
V _{DD} Supply Current	I _{DD}	(Note 4)	Full	-	-	50	μ A
AVDD Supply Range	AVDD	VDD range 2.6V - 3.6V	Full	4.5	-	18	V
		VDD range 2.25V - 3.6V		4.5	-	13	V
AVDD Supply Current	IAVDD	(Note 2)	Full	-	-	25	μ A
SET Voltage Resolution	SET _{VR}		Full	7	7	7	Bits
SET Differential Nonlinearity	SET _{DN}	Monotonic over temperature	Full	-	-	\pm 1	LSB
SET Zero-Scale Error	SET _{ZSE}		Full	-	-	\pm 2	LSB
SET Full-Scale Error	SET _{FSE}		Full	-	-	\pm 8	LSB
SET Current	ISET	Through R _{SET} (Note 5)	Full	-	20	-	μ A
SET External Resistance	SET _{ER}	To GND, AVDD = 20V	Full	10	-	200	k Ω
		To GND, AVDD = 4.5V	Full	2.25	-	45	k Ω
AVDD to SET Voltage Attenuation	AVDD to SET	(Note 3)	Full	-	1:20	-	V/V
OUT Settling Time	OUT _{ST}	to \pm 0.5 LSB Error Band (Note 3)	Full	-	8	-	μ s
OUT Voltage Range	V _{OUT}		Full	VSET + 0.5V	-	13	V
SET Voltage Drift	SET _{VD}	(Note 3)	25 to 55	-	<10	-	mV
SDA, SCL, WP Input Logic High	VIH		Full	0.7*VDD	-	-	V
SDA, SCL, WP Input Logic Low	VIL		Full	-	-	0.3*VDD	V
SDA, SCL, WP Hysteresis		(Note 3)	Full	-	0.22 * VDD	-	V
WP IL	IL _{WPN}		Full	15	25	35	μ A
SDA, SCL Output Logic High	VOH _S	@ 3mA	Full	0.4	-	-	V
SDA, SCL Output Logic Low	VOL _S	@ 3mA	Full	-	-	0.4	V

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Electrical Specifications Test Conditions: VDD = 3V, AVDD = 10V, OUT = 5V, RSET = 24.9kΩ; Unless Otherwise Specified.
Typicals are at T_A = 25°C (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
I²C							
SCL Clock Frequency	F _{SCL}		Full	0	-	400	kHz
I ² C Clock High Time	t _{SCH}		Full	0.6	-	-	μs
I ² C Clock Low Time	t _{SCL}		Full	1.3	-	-	μs
I ² C Spike Rejection Filter Pulse Width	t _{DSP}		Full	0	-	50	ns
I ² C Data Set-up Time	t _{SDS}		Full	100	-	-	ns
I ² C Data Hold Time	t _{SDH}		Full	0	-	900	ns
I ² C SDA, SCL Input Rise Time	t _{ICR}	Dependent on Load (Note 6)	Full	-	20 + 0.1* Cb	1000	ns
I ² C SDA, SCL Input Fall Time	t _{ICF}	(Note 6)	Full	-	20 + 0.1* Cb	300	ns
I ² C Bus Free Time Between Stop and Start	t _{BUF}		Full	1.3	-	-	μs
I ² C Repeated Start Condition Set-up	t _{STS}		Full	0.6	-	-	μs
I ² C Repeated Start Condition Hold	t _{STH}		Full	0.6	-	-	μs
I ² C Stop Condition Set-up	t _{SPS}		Full	0.6	-	-	μs
I ² C Bus Capacitive Load	C _b		Full	-	-	400	pF
Capacitance on SDA	C _{SDA}		Full	-	-	10	pF
Capacitance on SCL	C _S	WP = 0	Full	-	-	10	pF
		WP = 1		-	-	22	
Write Cycle Time	T _W		Full	-	-	100	ms

NOTES:

2. Tested at AVDD = 20V.
3. Simulated and Determined via Design and NOT Directly Tested.
4. Simulated Maximum Current Draw when Programming EEPROM is 23mA, should be considered when designing Power Supply.
5. A Typical Current of 20μA is Calculated using the AVDD = 10V and RSET = 24.9kΩ. The maximum suggested SET Current should be 120μA.
6. Simulated and Designed According to I²C Specifications.

Application Information

This device provides the ability to reduce the flicker of an LCD panel by adjustment of the VCOM voltage during production test and alignment. A 128-step resolution is provided under digital control, which adjusts the sink current of the output. The output is connected to an external voltage divider, so that the device will have the capability to reduce the voltage on the output by increasing the output sink current.

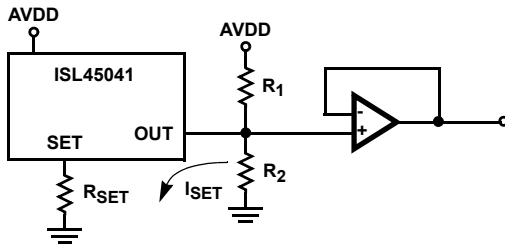


FIGURE 1. OUTPUT CONNECTION CIRCUIT EXAMPLE

The adjustment of the output is provided by the 2 wire I²C serial interface.

Expected Output Voltage

The ISL45041 provides an output sink current which lowers the voltage on the external voltage divider (VCOM output voltage). Equation 1 and Equation 2 can be used to calculate the output current (I_{OUT}) and output voltage (V_{OUT}) values.

$$I_{OUT} = \frac{\text{Setting}}{128} \times \frac{AVDD}{20(R_{SET})} \quad (\text{EQ. 1})$$

$$V_{OUT} = \left(\frac{R_2}{R_1 + R_2} \right) AVDD \left(1 - \frac{\text{Setting}}{128} \times \frac{R_1}{20(R_{SET})} \right) \quad (\text{EQ. 2})$$

NOTE: Where setting is an integer between 1 and 128.

Table 1 gives the calculated value of V_{OUT} for the eval board using the on board resistors values of: R_{SET} = 24.9k, R₁ = 200k, R₂ = 243k, and AVDD = 10V.

TABLE 1.

SETTING VALUE	VOUT
1	5.468
10	5.313
20	5.141
30	4.969
40	4.797
50	4.625
60	4.453
70	4.281
80	4.109
90	3.936
100	3.764
110	3.592
128	3.282

R_{SET} Resistor

The external R_{SET} resistor sets the full-scale sink current that determines the lowest voltage of the external voltage divider R₁ and R₂ (Figure 1). The maximum I_{SET} current has to be less than 120μA. The minimum R_{SET} resistor with AVDD equal to 10V is 4.17kΩ (10V/(20*120μA)). Typical applications with AVDD equal to 10V set R_{SET} equal to 24.9kΩ for a set current equal to 20μA.

Ramp-Up of the VDD Power Supply

It is required that the ramp-up from 10% VDD to 90% VDD level be achieved in less than or equal to 10 ms to assure that the EEPROM and Power-on-reset circuits are synchronized and the correct value is read from the EEPROM Memory.

I²C Timing Diagram

Figure 2 shows the I²C timing diagram and expected scope photos of SCL and SDA when writing all zeros or all ones.

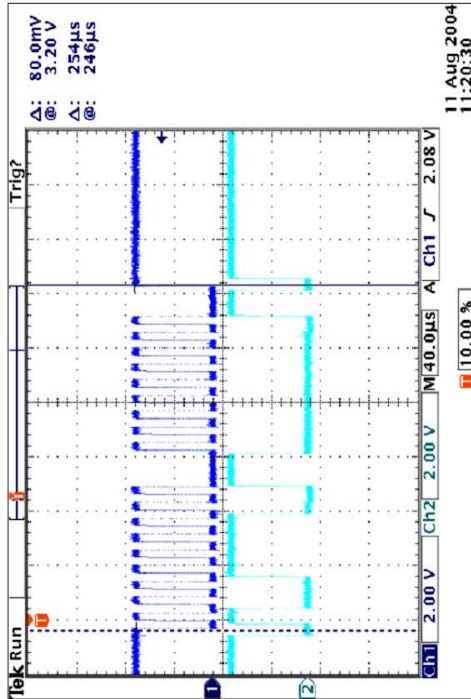
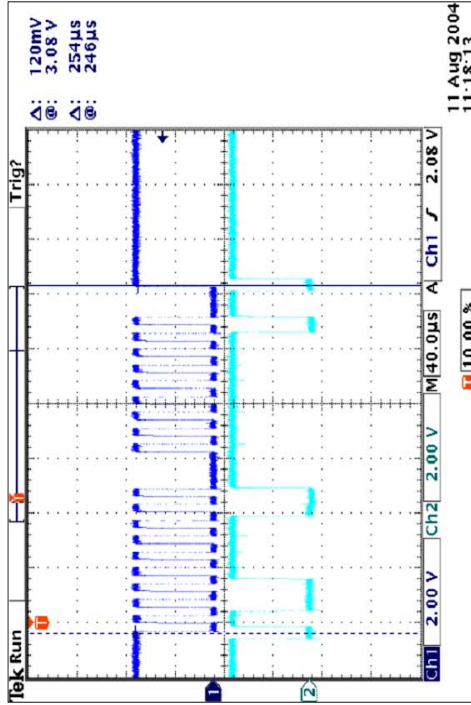
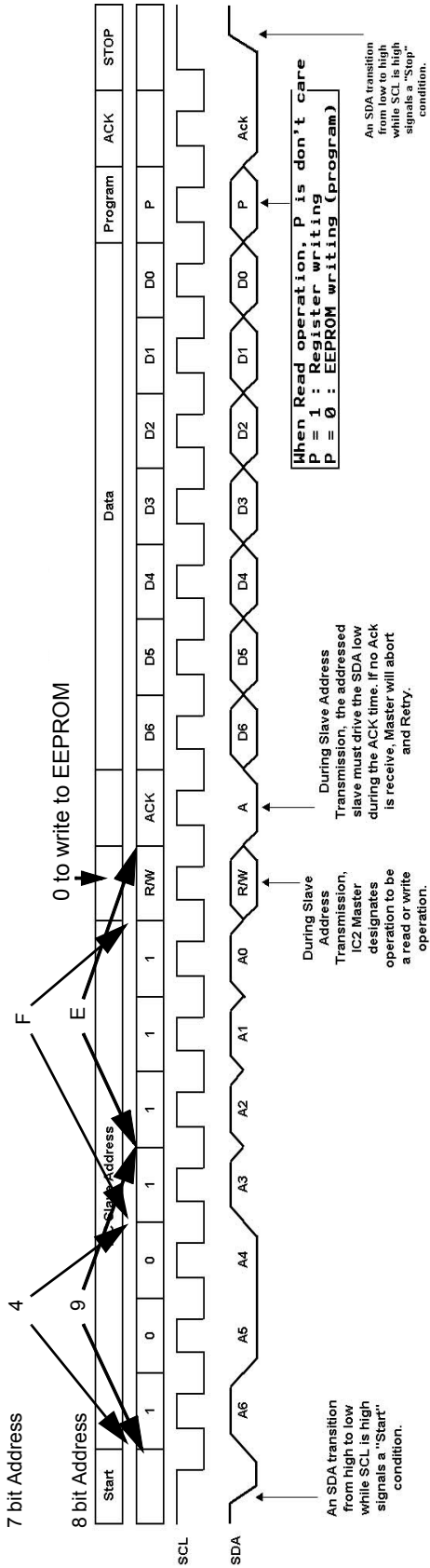
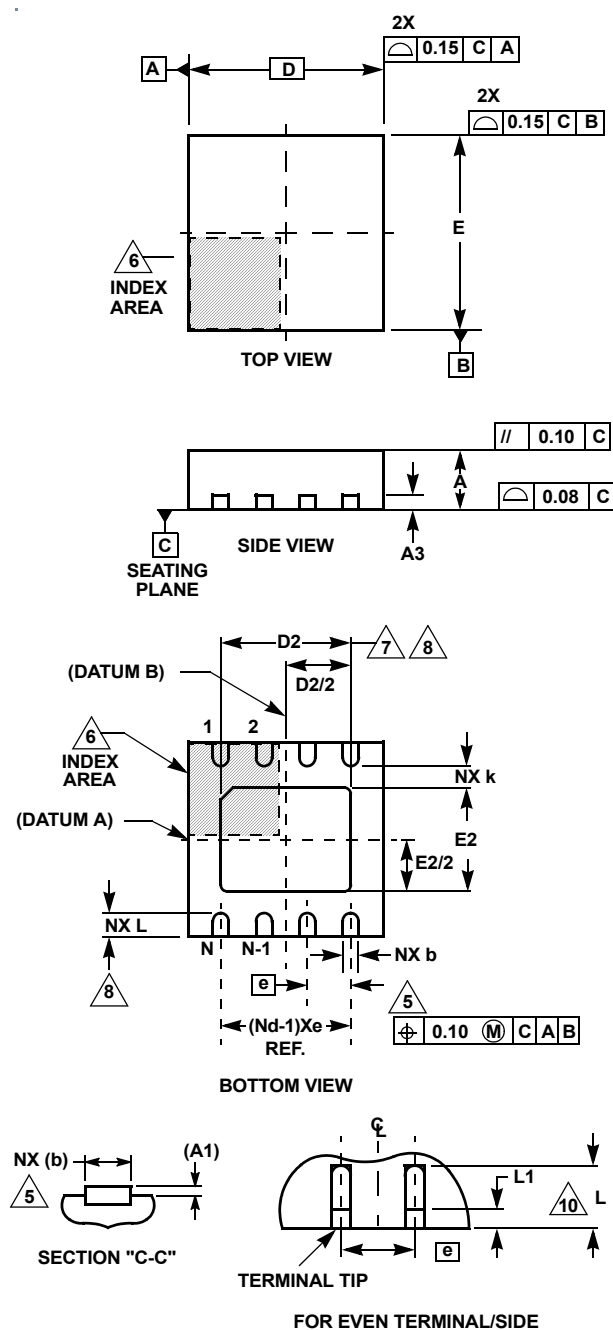


FIGURE 2. ISL45041 I²C TIMING DIAGRAM

ISL45041

Thin Dual Flat No-Lead Plastic Package (TDFN)



L8.3x3A 8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	0.02	0.05	-
A3	0.20 REF			-
b	0.25	0.30	0.35	5, 8
D	3.00 BSC			-
D2	2.20	2.30	2.40	7, 8, 9
E	3.00 BSC			-
E2	1.40	1.50	1.60	7, 8, 9
e	0.65 BSC			-
k	0.25	-	-	-
L	0.20	0.30	0.40	8
N	8			2
Nd	4			3

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Compliant to JEDEC MO-WEEC-2 except for the "L" min dimension.

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