1.4MHz, Low Power CMOS Operational Amplifiers

The ICL761X series is a family of CMOS operational amplifiers. These devices provide the designer with high performance operation at low supply voltages and selectable quiescent currents, and are an ideal design tool when ultra low input current and low power dissipation are desired.

The basic amplifier will operate at supply voltages ranging from ±1V to ±8V, and may be operated from a single Lithium cell.

A unique quiescent current programming pin allows setting of standby current to 1mA, 100µA, or 10µA, with no external components. This results in power consumption as low as 20µW. The output swing ranges to within a few millivolts of the supply voltages.

Of particular significance is the extremely low (1pA) input current, input noise current of $0.01pA/\sqrt{Hz}$, and $10^{12}\Omega$ input impedance. These features optimize performance in very high source impedance applications.

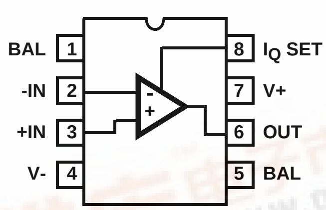
The inputs are internally protected. Outputs are fully protected against short circuits to ground or to either supply.

AC performance is excellent, with a slew rate of 1.6V/µs, and unity gain bandwidth of 1MHz at I_Q = 1mA.

Because of the low power dissipation, junction temperature rise and drift are quite low. Applications utilizing these features may include stable instruments, extended life designs, or high density packages.

Pinouts

ICL7611, ICL7612
(PDIP, SOIC)
TOP VIEW



Features

- Wide Operating Voltage Range . . . . ±1V to ±8V
- High Input Impedance . . . . $10^{12}\Omega$
- Programmable Power Consumption . . . . . Low as 20µW
- Input Current Lower Than BIFETs . . . . 1pA (Typ)
- Output Voltage Swing . . . . V+ and V-
- Input Common Mode Voltage Range Greater Than Supply Rails (ICL7612)
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Portable Instruments
- Telephone Headsets
- Hearing Aid/Microphone Amplifiers
- Meter Amplifiers
- Medical Instruments
- High Impedance Buffers

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ICL7611DCBA	0 to 70	8 Ld SOIC - D Grade	M8.15
ICL7611DCBAZ (Note)	0 to 70	8 Ld SOIC - D Grade (Pb-free)	M8.15
ICL7611DCBA-T	0 to 70	8 Ld SOIC - D Grade Tape and Reel	M8.15
ICL7611DCBAZ-T (Note)	0 to 70	8 Ld SOIC - D Grade Tape and Reel (Pb-free)	M8.15
ICL7611DCPA	0 to 70	8 Ld PDIP - D Grade	E8.3
ICL7611DCPAZ (Note)	0 to 70	8 Ld PDIP - D Grade* (Pb-free)	E8.3
ICL7612BCPA	0 to 70	8 Ld PDIP - B Grade	E8.3
ICL7612DCBA	0 to 70	8 Ld SOIC - D Grade	M8.15
ICL7612DCBAZ (Note)	0 to 70	8 Ld SOIC - D Grade (Pb-free)	M8.15
ICL7612DCBA-T	0 to 70	8 Ld SOIC - D Grade Tape and Reel	M8.15
ICL7612DCBAZ-T (Note)	0 to 70	8 Ld SOIC - D Grade Tape and Reel (Pb-free)	M8.15
ICL7612DCPA	0 to 70	8 Ld PDIP - D Grade	E8.3

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

Supply Voltage V+ to V- 18V
Input Voltage . . . . V- -0.3 to V+ +0.3V
Differential Input Voltage (Note 1) . . . . [(V+ +0.3) - (V- -0.3)]V
Duration of Output Short Circuit (Note 2). . . . . Unlimited

Operating Conditions

Temperature Range
ICL761XC. . . . . 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (°C/W)
PDIP Package* 130
SOIC Package 170
Maximum Junction Temperature (Plastic Package) . . . . 150°C
Maximum Storage Temperature Range . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
(SOIC - Lead Tips Only)

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Long term offset voltage stability will be degraded if large input differential voltages are applied for long periods of time.
2. The outputs may be shorted to ground or to either supply, for $V_{SUPPLY} \leq 10V$. Care must be taken to insure that the dissipation rating is not exceeded.
3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V_{SUPPLY} = \pm5V$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	ICL7611B, ICL7612B			ICL7611D, ICL7612D			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 100k\Omega$	25	-	-	5	-	-	15	mV
			Full	-	-	7	-	-	20	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \leq 100k\Omega$	-	-	15	-	-	25	-	µV/°C
Input Offset Current	I_{OS}		25	-	0.5	30	-	0.5	30	pA
			Full	-	-	300	-	-	300	pA
Input Bias Current	I_{BIAS}		25	-	1.0	50	-	1.0	50	pA
			Full	-	-	400	-	-	400	pA
Common Mode Voltage Range (Except ICL7612)	V_{CMR}	$I_Q = 10\mu A$	25	±4.4	-	-	±4.4	-	-	V
		$I_Q = 100\mu A$	25	±4.2	-	-	±4.2	-	-	V
		$I_Q = 1mA$	25	±3.7	-	-	±3.7	-	-	V
Extended Common Mode Voltage Range (ICL7612 Only)	V_{CMR}	$I_Q = 10\mu A$	25	±5.3	-	-	±5.3	-	-	V
		$I_Q = 100\mu A$	25	+5.3, -5.1	-	-	+5.3, -5.1	-	-	V
		$I_Q = 1mA$	25	+5.3, -4.5	-	-	+5.3, -4.5	-	-	V
Output Voltage Swing	V_{OUT}	$I_Q = 10\mu A$, $R_L = 1M\Omega$	25	±4.9	-	-	±4.9	-	-	V
			Full	±4.8	-	-	±4.8	-	-	V
		$I_Q = 100\mu A$, $R_L = 100k\Omega$	25	±4.9	-	-	±4.9	-	-	V
			Full	±4.8	-	-	±4.8	-	-	V
		$I_Q = 1mA$, $R_L = 10k\Omega$	25	±4.5	-	-	±4.5	-	-	V
			Full	±4.3	-	-	±4.3	-	-	V
Large Signal Voltage Gain	A_{VOL}	$V_O = \pm4.0V$, $R_L = 1M\Omega$, $I_Q = 10\mu A$	25	80	104	-	80	104	-	dB
			Full	75	-	-	75	-	-	dB
		$V_O = \pm4.0V$, $R_L = 100k\Omega$, $I_Q = 100\mu A$	25	80	102	-	80	102	-	dB
			Full	75	-	-	75	-	-	dB
		$V_O = \pm4.0V$, $R_L = 10k\Omega$, $I_Q = 1mA$	25	76	83	-	76	83	-	dB
			Full	72	-	-	72	-	-	dB

Electrical Specifications V_{SUPPLY} = ±5V, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	ICL7611B, ICL7612B			ICL7611D, ICL7612D			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Unity Gain Bandwidth	GBW	I_Q = 10µA	25	-	0.044	-	-	0.044	-	MHz
		I_Q = 100µA	25	-	0.48	-	-	0.48	-	MHz
		I_Q = 1mA	25	-	1.4	-	-	1.4	-	MHz
Input Resistance	R_{IN}		25	-	10^{12}	-	-	10^{12}	-	Ω
Common Mode Rejection Ratio	CMRR	R_S ≤ 100kΩ, I_Q = 10µA	25	70	96	-	70	96	-	dB
		R_S ≤ 100kΩ, I_Q = 100µA	25	70	91	-	70	91	-	dB
		R_S ≤ 100kΩ, I_Q = 1mA	25	60	87	-	60	87	-	dB
Power Supply Rejection Ratio (V_{SUPPLY} = ±8V to ±2V)	PSRR	R_S ≤ 100kΩ, I_Q = 10µA	25	80	94	-	80	94	-	dB
		R_S ≤ 100kΩ, I_Q = 100µA	25	80	86	-	80	86	-	dB
		R_S ≤ 100kΩ, I_Q = 1mA	25	70	77	-	70	77	-	dB
Input Referred Noise Voltage	e_N	R_S = 100Ω, f = 1kHz	25	-	100	-	-	100	-	nV/√Hz
Input Referred Noise Current	i_N	R_S = 100Ω, f = 1kHz	25	-	0.01	-	-	0.01	-	pA/√Hz
Supply Current (No Signal, No Load)	I_{SUPPLY}	I_Q SET = +5V, Low Bias	25	-	0.01	0.02	-	0.01	0.02	mA
		I_Q SET = 0V, Medium Bias	25	-	0.1	0.25	-	0.1	0.25	mA
		I_Q SET = -5V, High Bias	25	-	1.0	2.5	-	1.0	2.5	mA
Channel Separation	V_{O1}/V_{O2}	A_V = 100	25	-	120	-	-	120	-	dB
Slew Rate (A_V = 1, C_L = 100pF, V_{IN} = $8V_{P-P}$)	SR	I_Q = 10µA, R_L = 1MΩ	25	-	0.016	-	-	0.016	-	V/µs
		I_Q = 100µA, R_L = 100kΩ	25	-	0.16	-	-	0.16	-	V/µs
		I_Q = 1mA, R_L = 10kΩ	25	-	1.6	-	-	1.6	-	V/µs
Rise Time (V_{IN} = 50mV, C_L = 100pF)	t_r	I_Q = 10µA, R_L = 1MΩ	25	-	20	-	-	20	-	µs
		I_Q = 100µA, R_L = 100kΩ	25	-	2	-	-	2	-	µs
		I_Q = 1mA, R_L = 10kΩ	25	-	0.9	-	-	0.9	-	µs
Overshoot Factor (V_{IN} = 50mV, C_L = 100pF)	OS	I_Q = 10µA, R_L = 1MΩ	25	-	5	-	-	5	-	%
		I_Q = 100µA, R_L = 100kΩ	25	-	10	-	-	10	-	%
		I_Q = 1mA, R_L = 10kΩ	25	-	40	-	-	40	-	%

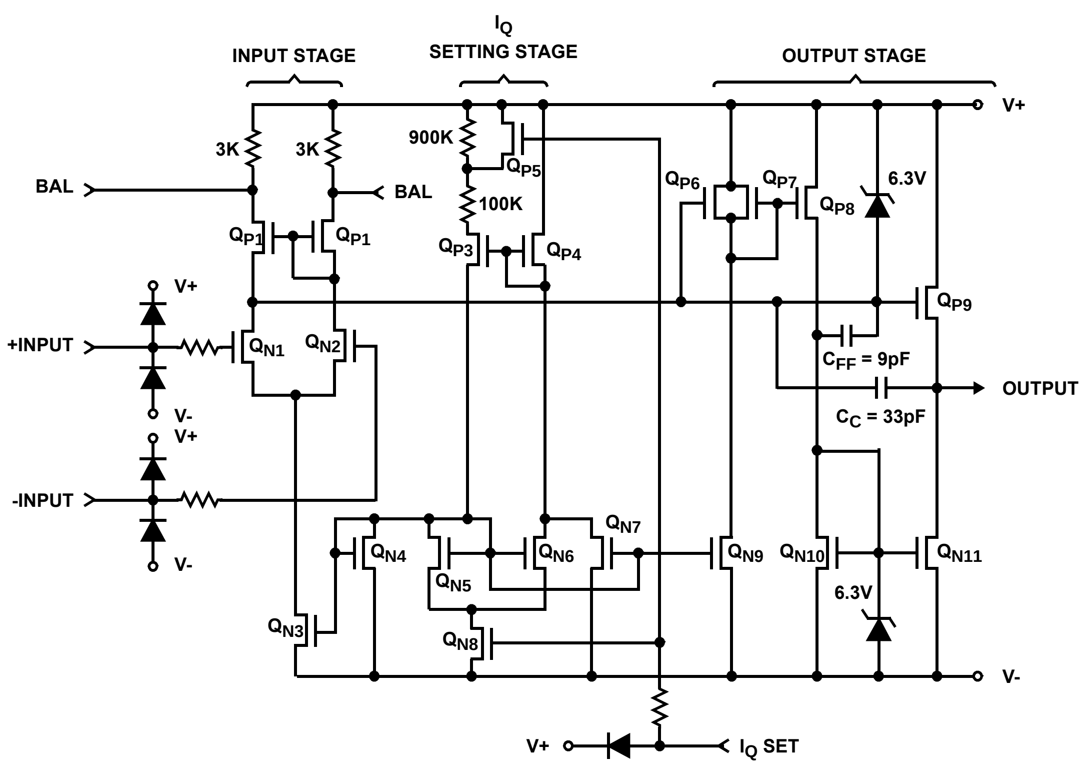
Electrical Specifications V_{SUPPLY} = ±1V, I_Q = 10µA, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	ICL7611B, ICL7612B			UNITS
				MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	R_S ≤ 100kΩ	25	-	-	5	mV
			Full	-	-	7	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	R_S ≤ 100kΩ	-	-	15	-	µV/°C
Input Offset Current	I_{OS}		25	-	0.5	30	pA
			Full	-	-	300	pA
Input Bias Current	I_{BIAS}		25	-	1.0	50	pA
			Full	-	-	500	pA
Common Mode Voltage Range (Except ICL7612)	V_{CMR}		25	±0.6	-	-	V
Extended Common Mode Voltage Range (ICL7612 Only)	V_{CMR}		25	+0.6 to -1.1	-	-	V

Electrical Specifications V_{SUPPLY} = ±1V, I_Q = 10μA, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	ICL7611B, ICL7612B			UNITS
				MIN	TYP	MAX	
Output Voltage Swing	V_{OUT}	R_L = 1MΩ	25	±0.98	-	-	V
			Full	±0.96	-	-	V
Large Signal Voltage Gain	A_{VOL}	V_O = ±0.1V, R_L = 1MΩ	25	-	90	-	dB
			Full	-	80	-	dB
Unity Gain Bandwidth	GBW		25	-	0.044	-	MHz
Input Resistance	R_{IN}		25	-	10^{12}	-	Ω
Common Mode Rejection Ratio	CMRR	$R_S \le$ 100kΩ	25	-	80	-	dB
Power Supply Rejection Ratio	PSRR	$R_S \le$ 100kΩ	25	-	80	-	dB
Input Referred Noise Voltage	e_N	R_S = 100Ω, f = 1kHz	25	-	100	-	nV/√Hz
Input Referred Noise Current	i_N	R_S = 100Ω, f = 1kHz	25	-	0.01	-	pA/√Hz
Supply Current	I_{SUPPLY}	No Signal, No Load	25	-	6	15	μA
Slew Rate	SR	A_V = 1, C_L = 100pF, V_{IN} = 0.2V_{P-P}, R_L = 1MΩ	25	-	0.016	-	V/μs
Rise Time	t_r	V_{IN} = 50mV, C_L = 100pF R_L = 1MΩ	25	-	20	-	μs
Overshoot Factor	OS	V_{IN} = 50mV, C_L = 100pF, R_L = 1MΩ	25	-	5	-	%

Schematic Diagram



Application Information

Static Protection

All devices are static protected by the use of input diodes. However, strong static fields should be avoided, as it is possible for the strong fields to cause degraded diode junction characteristics, which may result in increased input leakage currents.

Latchup Avoidance

Junction-isolated CMOS circuits employ configurations which produce a parasitic 4-layer (PNPN) structure. The 4-layer structure has characteristics similar to an SCR, and under certain circumstances may be triggered into a low impedance state resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails may be applied to any pin. In general, the op amp supplies must be established simultaneously with, or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to 2mA to prevent latchup.

Choosing the Proper I_Q

The ICL7611 and ICL7612 have a similar I_Q set-up scheme, which allows the amplifier to be set to nominal quiescent currents of 10μA, 100μA or 1mA. These current settings change only very slightly over the entire supply voltage range. The ICL7611/12 have an external I_Q control terminal, permitting user selection of quiescent current. To set the I_Q connect the I_Q terminal as follows:

I_Q = 10μA - I_Q pin to V+

I_Q = 100μA - I_Q pin to ground. If this is not possible, any voltage from V+ - 0.8 to V- +0.8 can be used.

I_Q = 1mA - I_Q pin to V-

NOTE: The output current available is a function of the quiescent current setting. For maximum peak-to-peak output voltage swings into low impedance loads, IQ of 1mA should be selected.

Output Stage and Load Driving Considerations

Each amplifiers' quiescent current flows primarily in the output stage. This is approximately 70% of the I_Q settings. This allows output swings to almost the supply rails for output loads of 1MΩ, 100kΩ, and 10kΩ, using the output stage in a highly linear class A mode. In this mode, crossover distortion is avoided and the voltage gain is maximized. However, the output stage can also be operated in Class AB for higher output currents. (See graphs under Typical Operating Characteristics). During the transition from Class A to Class B operation, the output transfer characteristic is non-linear and the voltage gain decreases.

Input Offset Nulling

Offset nulling may be achieved by connecting a 25K pot between the BAL terminals with the wiper connected to V+. At quiescent currents of 1mA and 100μA the nulling range provided is adequate for all V_{OS} selections; however with I_Q = 10μA, nulling may not be possible with higher values of V_{OS}.

Frequency Compensation

The ICL7611 and ICL7612 are internally compensated, and are stable for closed loop gains as low as unity with capacitive loads up to 100pF.

Extended Common Mode Input Range

The ICL7612 incorporates additional processing which allows the input CMVR to exceed each power supply rail by 0.1V for applications where $V_{SUPP} \geq \pm 1.5V$. For those applications where $V_{SUPP} \leq \pm 1.5V$ the input CMVR is limited in the positive direction, but may exceed the negative supply rail by 0.1V in the negative direction (e.g., for $V_{SUPPLY} = \pm 1V$, the input CMVR would be +0.6V to -1.1V).

Operation At $V_{SUPPLY} = \pm 1V$

Operation at $V_{SUPPLY} = \pm 1V$ is guaranteed at I_Q = 10μA for A and B grades only.

Output swings to within a few millivolts of the supply rails are achievable for $R_L \geq 1M\Omega$. Guaranteed input CMVR is ±0.6V minimum and typically +0.9V to -0.7V at $V_{SUPPLY} = \pm 1V$. For applications where greater common mode range is desirable, refer to the description of ICL7612 above.

Typical Applications

The user is cautioned that, due to extremely high input impedances, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup.

Note that in no case is I_Q shown. The value of I_Q must be chosen by the designer with regard to frequency response and power dissipation.

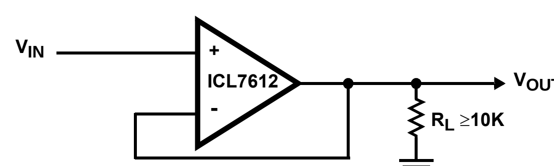
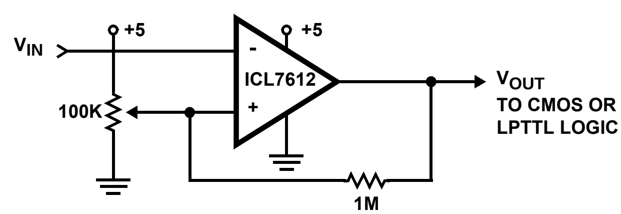


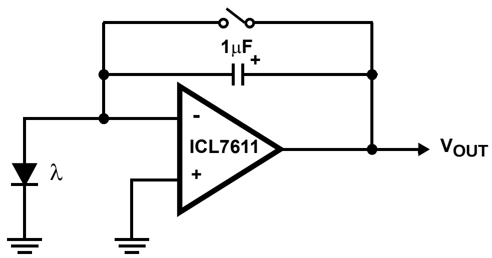
FIGURE 1. SIMPLE FOLLOWER (NOTE 4)



NOTE:

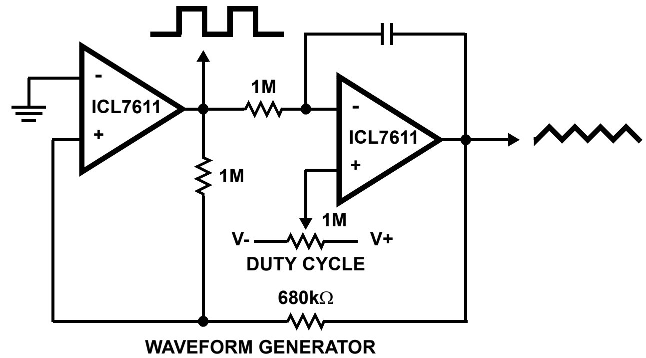
4. By using the ICL7612 in this application, the circuit will follow rail to rail inputs.

FIGURE 2. LEVEL DETECTOR (NOTE 4)



NOTE: Low leakage currents allow integration times up to several hours.

FIGURE 3. PHOTOCURRENT INTEGRATOR



NOTE: Since the output range swings exactly from rail to rail, frequency and duty cycle are virtually independent of power supply variations.

FIGURE 4. PRECISE TRIANGLE/SQUARE WAVE GENERATOR

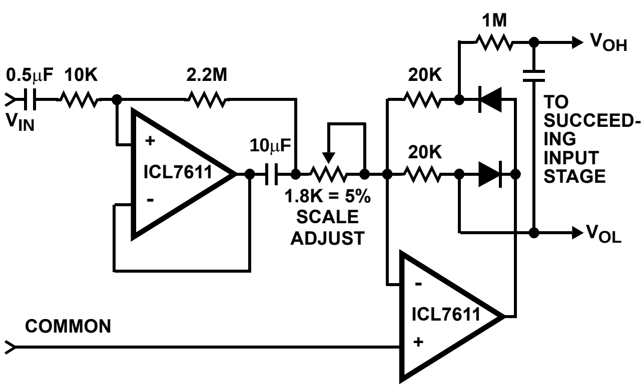


FIGURE 5. AVERAGING AC TO DC CONVERTER FOR A/D CONVERTERS SUCH AS ICL7106, ICL7107, ICL7109, ICL7116, ICL7117

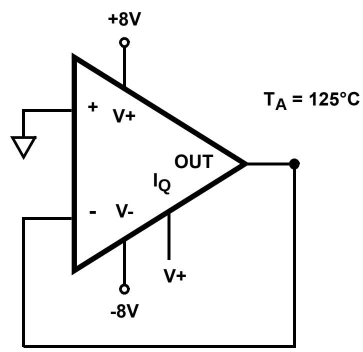


FIGURE 6. BURN-IN AND LIFE TEST CIRCUIT

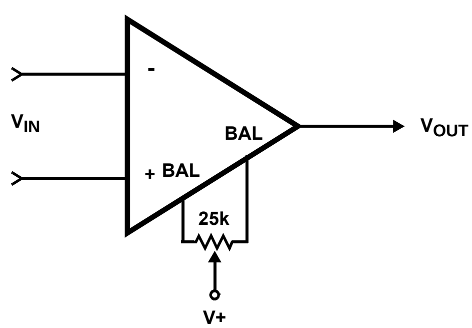
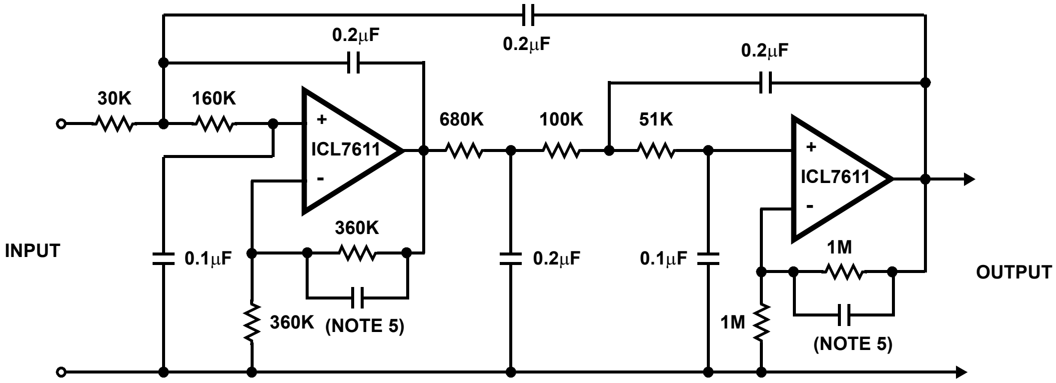


FIGURE 7. V_{OS} NULL CIRCUIT



NOTES:

5. Note that small capacitors (25pF to 50pF) may be needed for stability in some cases.
6. The low bias currents permit high resistance and low capacitance values to be used to achieve low frequency cutoff. f_C = 10Hz, A_{VCL} = 4, Passband ripple = 0.1dB.

FIGURE 8. FIFTH ORDER CHEBYCHEV MULTIPLE FEEDBACK LOW PASS FILTER

Typical Performance Curves

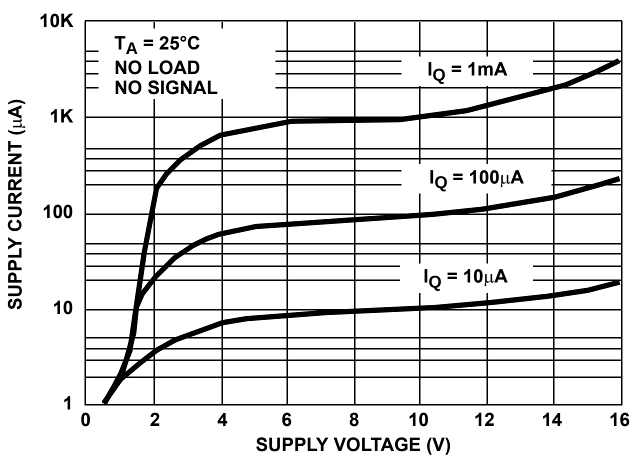


FIGURE 9. SUPPLY CURRENT PER AMPLIFIER vs SUPPLY VOLTAGE

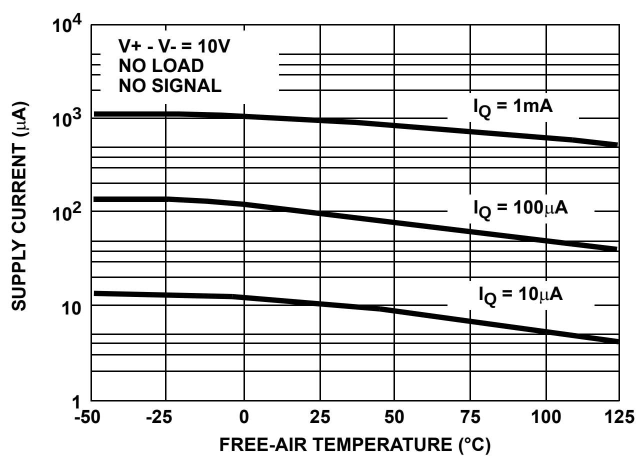


FIGURE 10. SUPPLY CURRENT PER AMPLIFIER vs FREE-AIR TEMPERATURE

Typical Performance Curves (Continued)

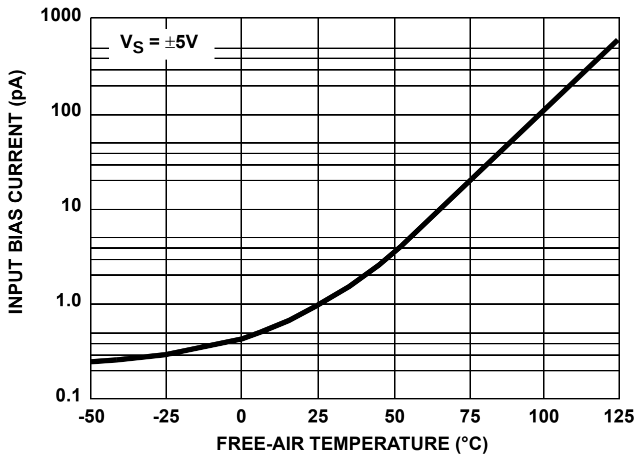


FIGURE 11. INPUT BIAS CURRENT vs TEMPERATURE

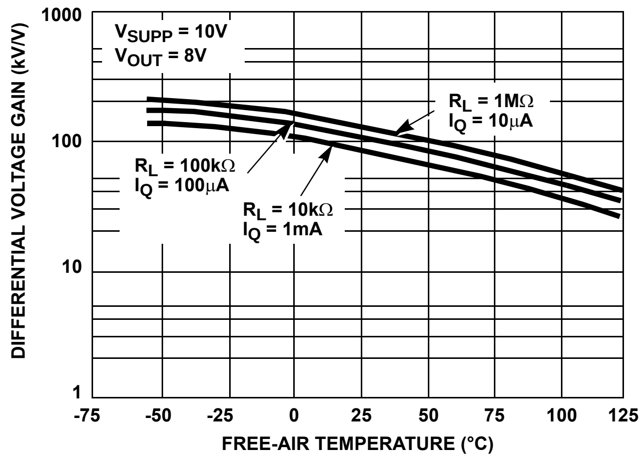


FIGURE 12. LARGE SIGNAL DIFFERENTIAL VOLTAGE GAIN vs FREE-AIR TEMPERATURE

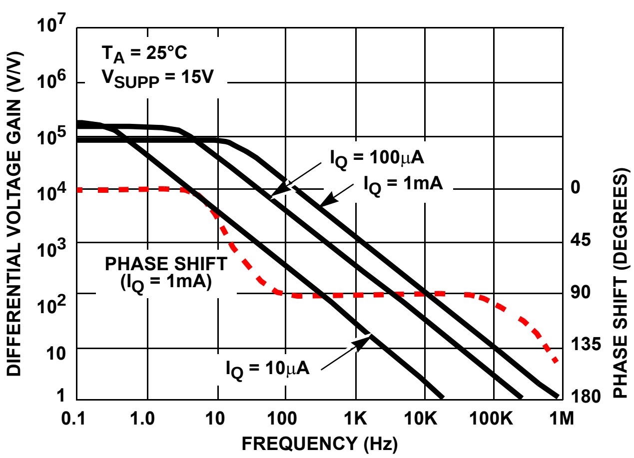


FIGURE 13. LARGE SIGNAL FREQUENCY RESPONSE

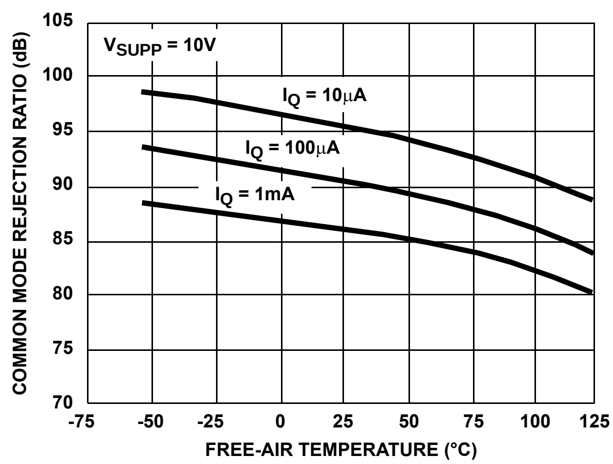


FIGURE 14. COMMON MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

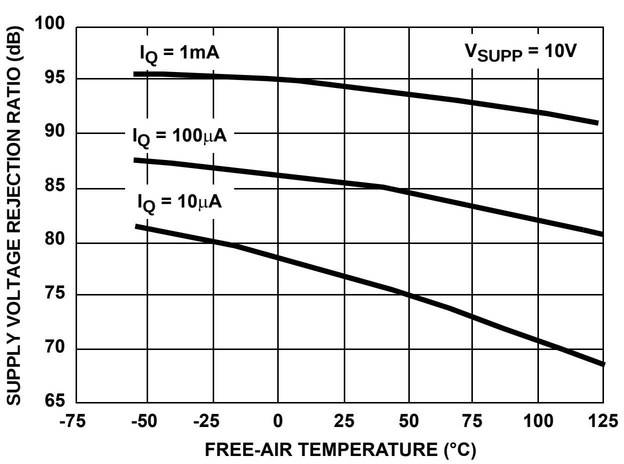


FIGURE 15. POWER SUPPLY REJECTION RATIO vs FREE-AIR TEMPERATURE

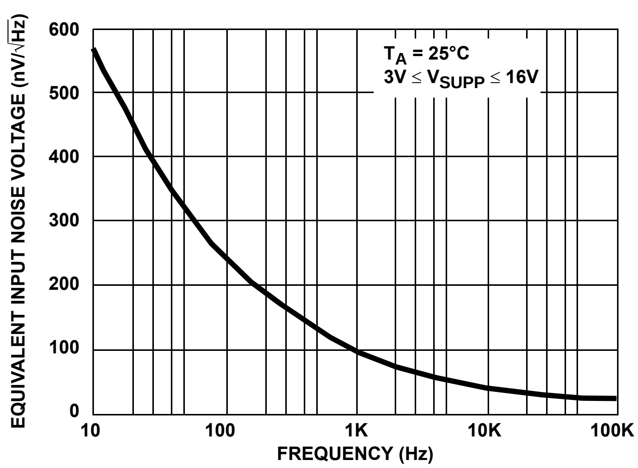


FIGURE 16. EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

Typical Performance Curves (Continued)

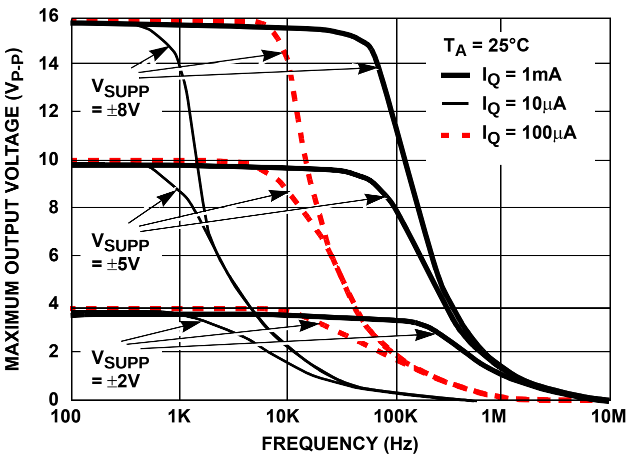


FIGURE 17. OUTPUT VOLTAGE vs FREQUENCY

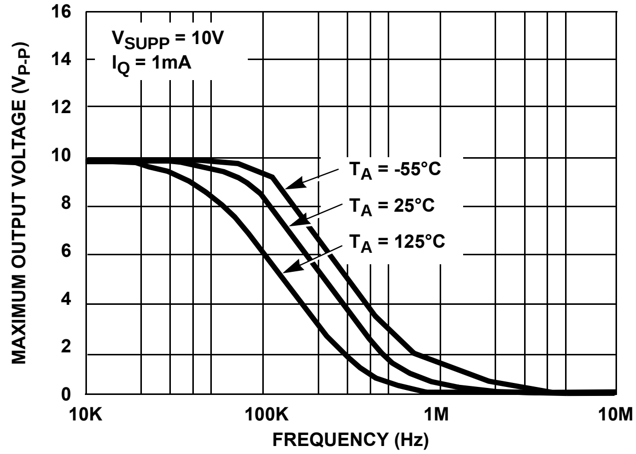


FIGURE 18. OUTPUT VOLTAGE vs FREQUENCY

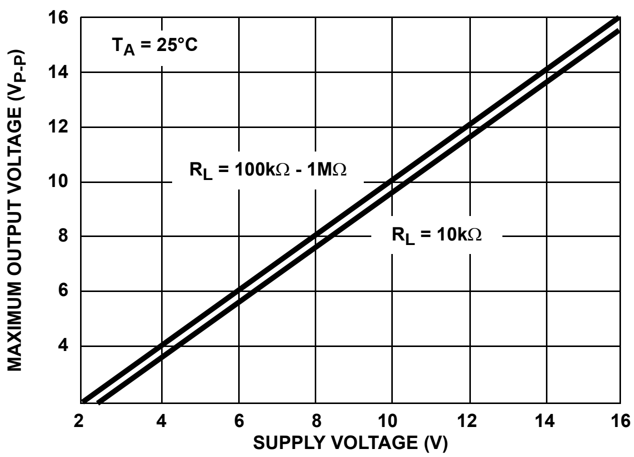


FIGURE 19. OUTPUT VOLTAGE vs SUPPLY VOLTAGE

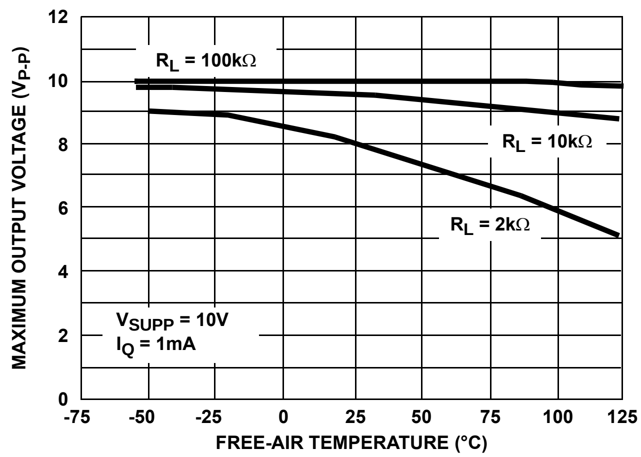


FIGURE 20. OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

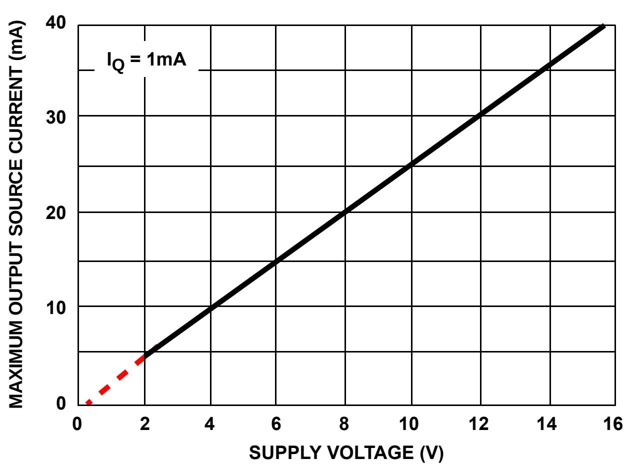


FIGURE 21. OUTPUT SOURCE CURRENT vs SUPPLY VOLTAGE

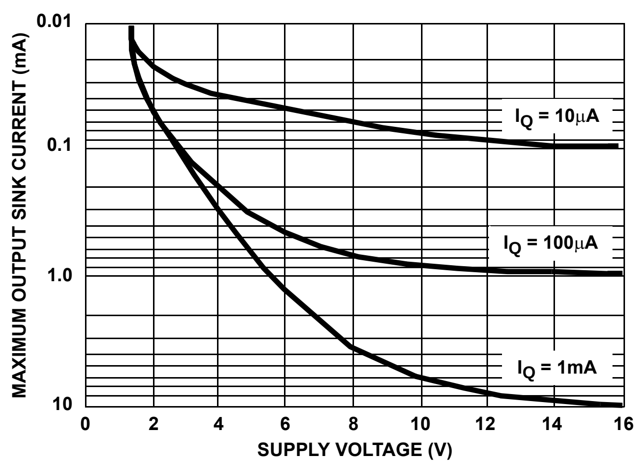


FIGURE 22. OUTPUT SINK CURRENT vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

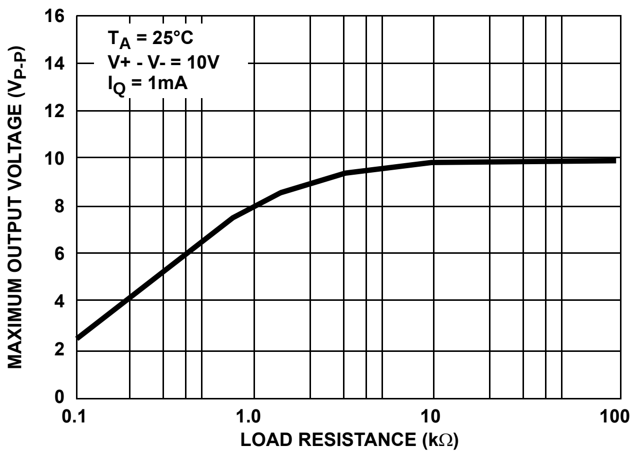


FIGURE 23. OUTPUT VOLTAGE vs LOAD RESISTANCE

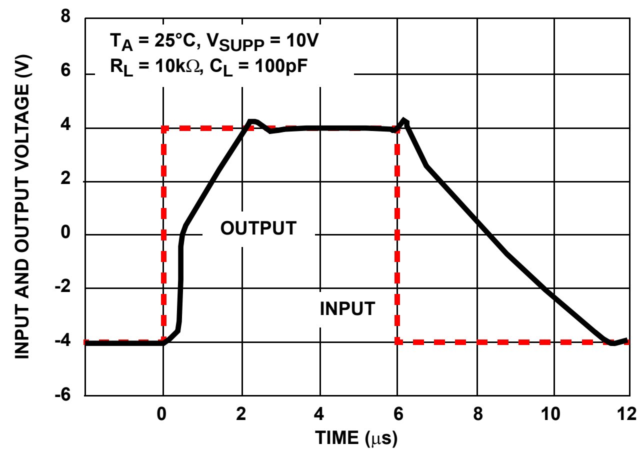


FIGURE 24. VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE (I_Q = 1mA)

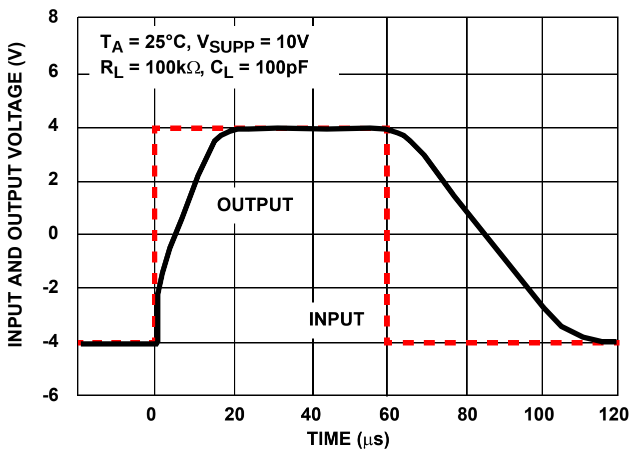


FIGURE 25. VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE (I_Q = 100μA)

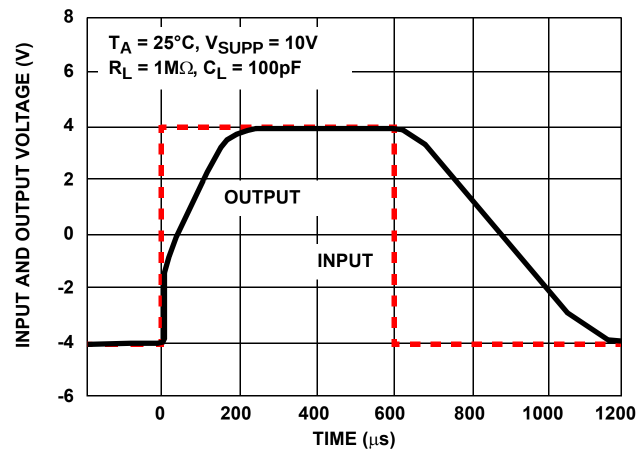


FIGURE 26. VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE (I_Q = 10μA)