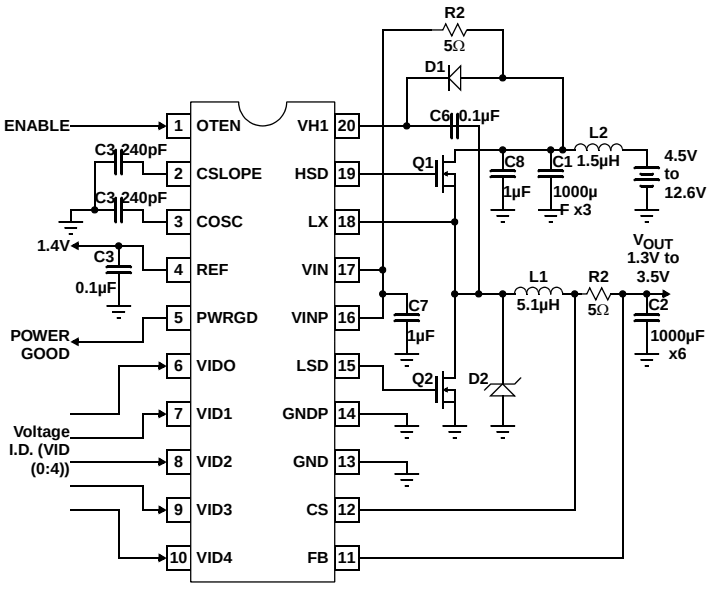
Programmable PWM Controller

The EL7571 is a flexible, high efficiency, current mode, PWM step down controller. It incorporates five bit DAC adjustable output voltage control which conforms to the Intel Voltage Regulation Module (VRM) Specification for Pentium® II and Pentium® Pro class processors. The controller employs synchronous rectification to deliver efficiencies greater than 90% over a wide range of supply voltages and load conditions. The on-board oscillator frequency is externally adjustable, or may be slaved to a system clock, allowing optimization of RFI performance in critical applications. In single supply operation, the high side FET driver supports boot-strapped operation. For maximum flexibility, system operation is possible from either a 5V rail, a single 12V rail, or dual supply rails with the controller operating from 12V and the power FETs from 5V.

Pinout



Q1, Q2: Siliconix, Si4410, x2
C1: Sanyo, 16MV 1000GX, 1000µF x3
C2: Sanyo, 6MV 1000GX, 1000µF x6
L1: Pulse Engineering, PE-53700, 5.1µH
L2: Micrometals, T30-26, 7T AWG #20, 1.5µH
R1: Dale, WSL-25-12, 15mΩ, x2
D1: BAV99
D2: IR, 32CTQ030

Features

- Pentium® II Compatible
- 5 bit DAC Controlled Output Voltage
- Greater than 90% Efficiency
- 4.5V to 12.6V Input Range
- Dual NMOS Power FET Drivers
- Fixed frequency, Current Mode Control
- Adjustable Oscillator with External Sync. Capability
- Synchronous Switching
- Internal Soft-Start
- User Adjustable Slope Compensation
- Pulse by Pulse Current Limiting
- 1% Typical Output Accuracy
- Power Good Signal
- Output Power Down
- Over Voltage Protection
- Pb-Free Available (RoHS Compliant)

Applications

- Pentium® II Voltage Regulation Modules (VRMs)
- PC Motherboards
- DC/DC Converters
- GTL Bus Termination
- Secondary Regulation

Ordering Information

PART NUMBER	PACKAGE	TAPE AND REEL	PKG. DWG. #
EL7571CM	20-Pin SO	-	MDP0027
EL7571CM-T13	20-Pin SO	13”	MDP0027
EL7571CMZ (See Note)	20-Pin SO (Pb-free)	-	MDP0027
EL7571CMZ-T13 (See Note)	20-Pin SO (Pb-free)	13”	MDP0027

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020C.

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage: . . . . . -0.5V to 14V
Input Pin Voltage:. . . . . -.03 below Ground, +0.3 above Supply
VHI. . . . . -0.5V to 27V
Storage Temperature Range:. . . . . 65°C to +150°C
Operating Temperature Range: . . . . . 0°C to +70°C
Operating Junction Temperature:. . . . . 125°C
Peak Output Current: 3A
Power Dissipation: SO20 500mW

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications

T_A = 25°C, V_{IN} = 5V, C_{OSC} = 330pF, C_{SLOPE} = 390pF, R_{SENSE} = 7.5mΩ unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range		4.5		12.6	V
$V_{UVLO\ HI}$	Input Under Voltage Lock out Upper Limit	Positive going input voltage	3.6	4	4.4	V
$V_{UVLO\ LO}$	Input Under Voltage Lock out Lower Limit	Negative going input voltage	3.15	3.5	3.85	V
$V_{OUT\ RANGE}$	Output Voltage Range	See VID table	1.3		3.5	V
$V_{OUT\ 1}$	Steady State Output Voltage Accuracy, VID = 10111	I_L = 6.5A, V_{OUT} = 2.8V	2.74	2.82	2.90	V
$V_{OUT\ 2}$	Steady State Output Voltage Accuracy, VID = 00101	I_L = 6.5A, V_{OUT} =1.8V	1.74	1.81	1.9	V
V_{REF}	Reference Voltage		1.396	1.41	1.424	V
V_{ILIM}	Current Limit Voltage	$V_{ILIM} = (V_{CS}-V_{FB})$	125	154	185	mV
V_{IREV}	Current Reversal Threshold	$V_{IREV} = (V_{CS}-V_{FB})$	-40	-5	20	mV
$V_{OUT\ PG}$	Output Voltage Power Good Lower Level	V_{OUT} = 2.05V	-18	-14	-10	%
	Output Voltage Power Good Upper Level		8	12	16	%
V_{OVP}	Over-Voltage Protection Threshold		+9	+13	+17	%
$V_{OTEN\ LO}$	Power Down Input Low Level	V_{IN} = -10uA			1.5	V
$V_{OTEN\ HI}$	Power Down Input High Level		(V_{IN}-1.5)			V
$V_{ID\ LO}$	Voltage I.D. Input Low Level				1.5	V
$V_{ID\ HI}$	Voltage I.D. Input High Level		(V_{IN}-1.5)			V
V_{OSC}	Oscillator Voltage Swing			0.85		V_{P-P}
$V_{PWRGD\ LO}$	Power Good Output Low Level	I_{OUT} = 1mA			0.5	V
$R_{DS\ ON}$	HSD, LSD Switch On-Resistance	V_{IN}, V_{INP} = 12V, I_{OUT} = 100mA, (VHI-LX) = 12V		4.8	6	Ω
R_{FB}	FB Input Impedance			9.5		kΩ
R_{CS}	CS Input Impedance			115		kΩ
I_{VIN}	Quiescent Supply Current	V_{OTEN}>(V_{IN}-0.5)V		1.2	2	mA
$I_{VIN\ DIS}$	Supply Current in Output Disable Mode	V_{OTEN}<1.5V		0.76	1	mA
$I_{SOURCE/SINK}$	Peak Driver Output Current	V_{IN},V_{INP} = 12V, Measured at HSD, LSD, (VHI-LX) = 12V		2.5		A
I_{RAMP}	C_{SLOPE} Ramp Current	High Side Switch Active	8.5	14	20	µA
$I_{OSC\ CHARGE}$	Oscillator Charge Current	1.2>V_{OSC}>0.35V		50		µA
$I_{OSC\ DISCHARGE}$	Oscillator Discharge Current	1.2>V_{OSC}>0.35V		2		mA
I_{REFMAX}	VREF Output Current				25	µA

DC Electrical Specifications T_A = 25°C, V_{IN} = 5V, C_{OSC} = 330pF, C_{SLOPE} = 390pF, R_{SENSE} = 7.5mΩ unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
I_{VID}	VID Input Pull up Current		3	5	7	µA
I_{OTEN}	OTEN Input Pull up Current		3	5	7	µA

AC Electrical Specifications T_A = 25°C, V_{IN} = 5V, C_{OSC} = 330pF, C_{SLOPE} = 390pF unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Nominal Oscillator Frequency	C_{OSC} = 330pF	140	190	240	kHz
f_{CLK}	Clock Frequency		50	500	1000	kHz
t_{OTEN}	Shutdown Delay	V_{OTEN}>1.5V		100		ns
t_{SYNC}	Oscillator Sync. Pulse Width	Oscillator i/p (COSC) driven with HCMOS gate	20		800	ns
T_{START}	Soft-start Period	V_{OUT} = 3.5V		$100/f_{CLK}$		us
D_{MAX}	Maximum Duty Cycle			97		%

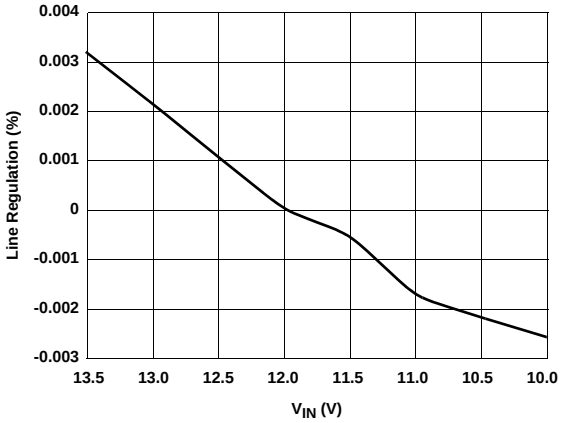
Pin Descriptions

PIN NO.	PIN NAME	PIN TYPE (NOTE 1)	FUNCTION
1	OTEN	I	Chip enable input, internal pull up (5mA typical). Active high.
2	CSLOPE	I	With a capacitor attached from CSLOPE to GND, generates the voltage ramp compensation for the PWM current mode controller. Slope rate is determined by an internal 14uA pull up and the C_{SLOPE} capacitor value. VC_{SLOPE} is reset to ground at the termination of the high side cycle.
3	COSC	I	Multi-function pin: with a timing capacitor attached, sets the internal oscillator rate f_S (kHz) = $57/C_{OSC}$ (µF); when pulsed low for a duration t_{SYNC} synchronizes device to an external clock.
4	REF	O	Band gap reference output. Decouple to GND with 0.1uF.
5	PWRGD	O	Power good, open drain output. Set low whenever the output voltage is not within ±13% of the programmed value.
6	VID0	I	Bit 0 of the output voltage select DAC. Internal pull up sets input high when not driven.
7	VID1	I	Bit 1 of the output voltage select DAC. Internal pull up sets input high when not driven.
8	VID2	I	Bit 2 of the output voltage select DAC. Internal pull up sets input high when not driven.
9	VID3	I	Bit 3 of the output voltage select DAC. Internal pull up sets input high when not driven.
10	VID4	I	Bit 4 of the output voltage select DAC. Internal pull up sets input high when not driven.
11	FB	I	Voltage regulation feedback input. Tie to V_{OUT} for normal operation.
12	CS	I	Current sense. Current feedback input of PWM controller and over current capacitor input. Current limit threshold set at +154mV with respect to FB. Connect sense resistor between CS and FB for normal operation.
13	GND	S	Ground
14	GNDP	S	Power ground for low side FET driver. Tie to GND for normal operation.
15	LSD	O	Low side gate drive output.
16	VINP	S	Input supply voltage for low side FET driver. Tie to VIN for normal operation.
17	VIN	S	Input supply voltage for control unit.
18	LX	S	Negative supply input for high side FET driver.
19	HSD	O	High side gate drive output. Driver ground referenced to LX. Driver supply may be bootstrapped to enhance low controller input voltage operation.
20	VH1	S	Positive supply input for high side FET driver.

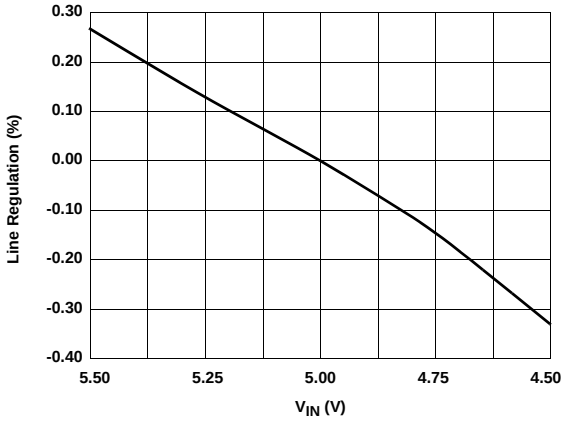
NOTE: Pin designators: I = Input, O = Output, S = Supply

Typical Performance Curves

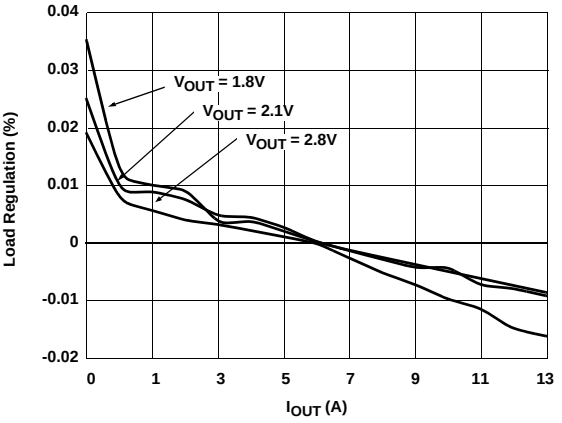
+12V Supply Sync Line Regulation



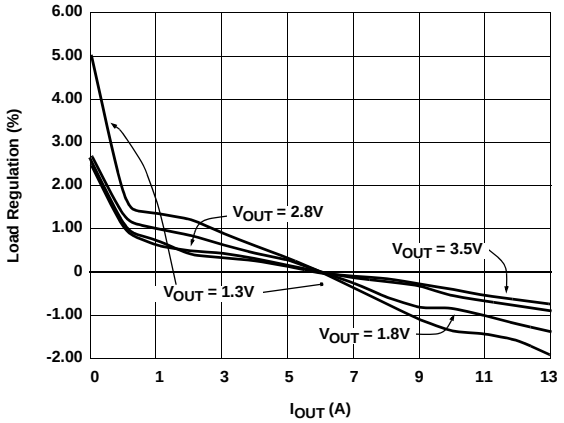
5V Supply Line Regulation



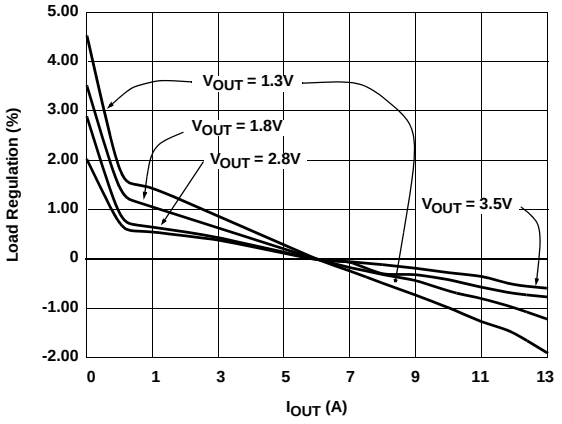
+12V Supply Sync Load Regulation



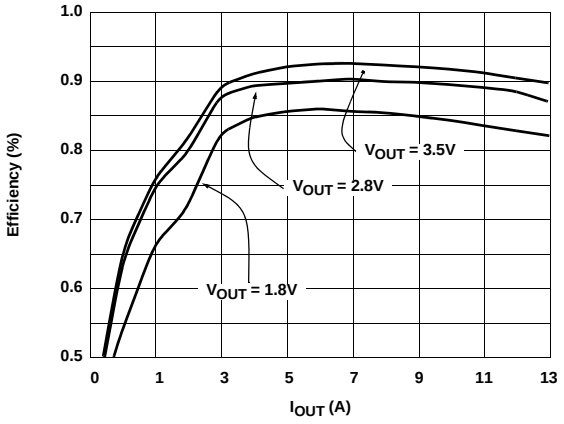
VRM +5V Supply +12V Controller Sync w/o Schottky Load Regulation



+5V Supply Non-Sync Load Regulation

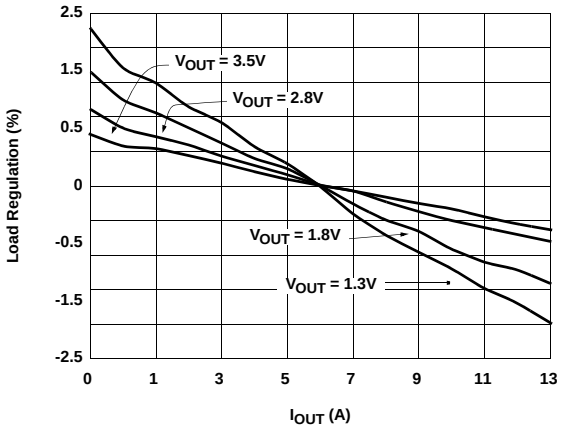


+12V Supply Sync Efficiency

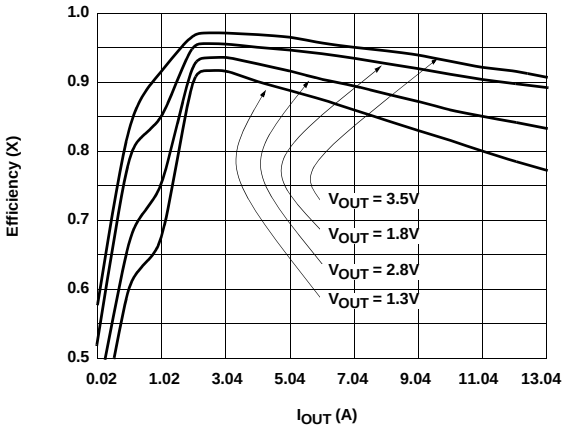


Typical Performance Curves (Continued)

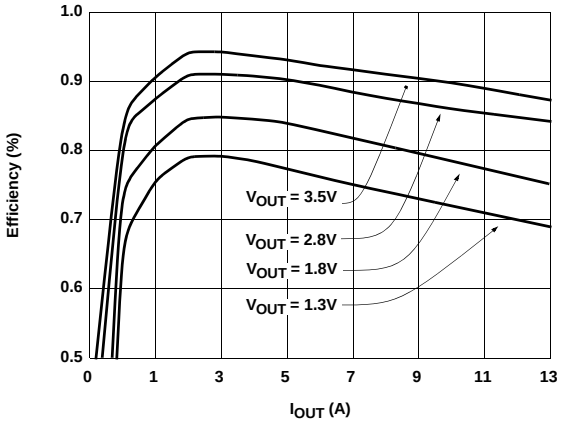
+5V Supply Sync with Schottky Load



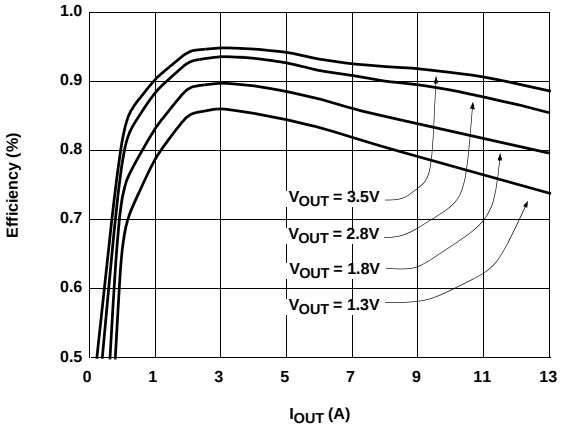
+5V Supply +12V Controller Sync w/o Schottky VRM Efficiency



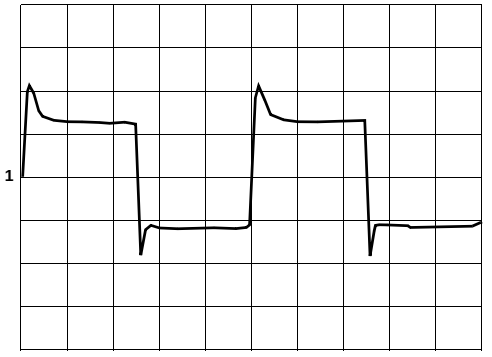
+5V Supply Non-Sync VRM Efficiency



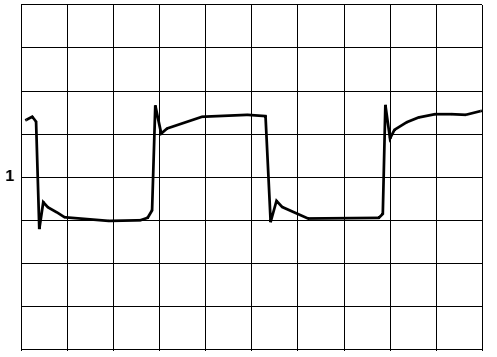
+5V Supply Sync with Schottky VRM Efficiency



12V Transient Response

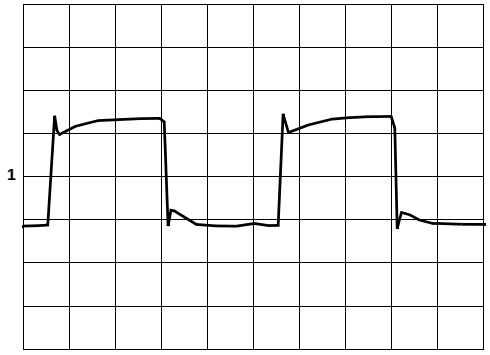


5V Non-sync Transient Response

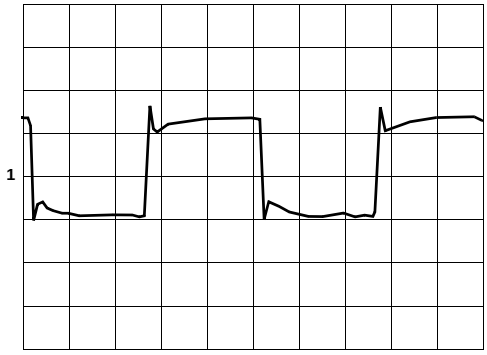


Typical Performance Curves (Continued)

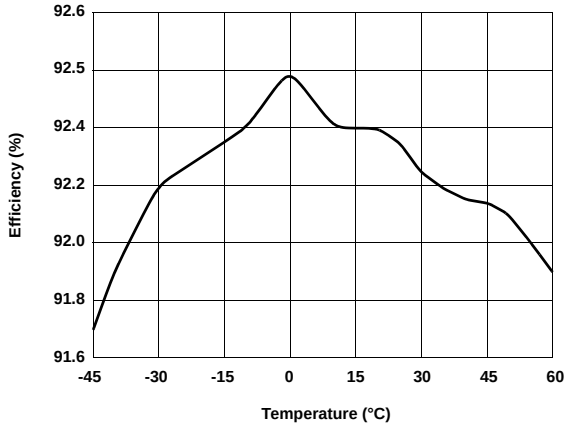
5V Sync Transient Response



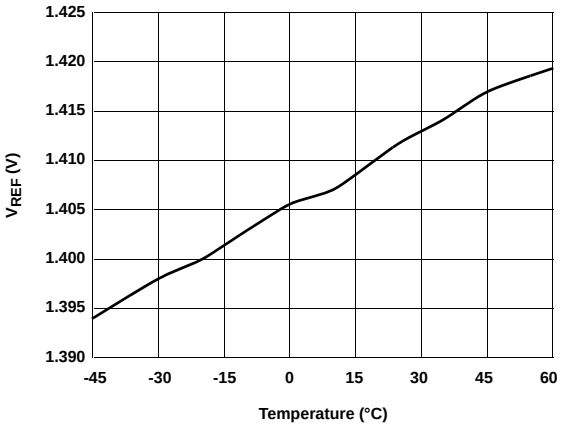
5V Input 12V Controller Transient Response



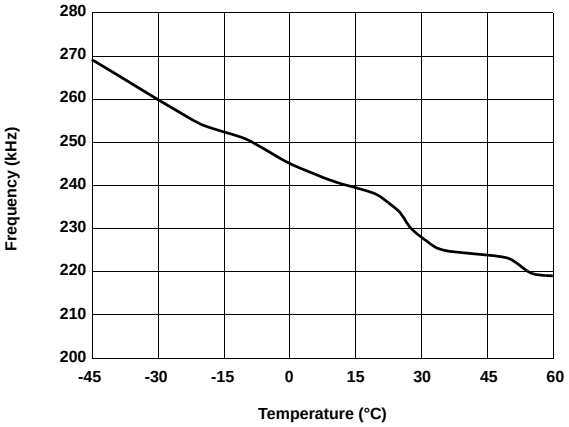
Efficiency vs Temperature



V_{REF} vs Temperature



Frequency vs Temperature



Applications Information

Circuit Description

General

The EL7571 is a fixed frequency, current mode, pulse width modulated (PWM) controller with an integrated high precision reference and a 5 bit Digital-to-Analog Converter (DAC). The device incorporates all the active circuitry required to implement a synchronous step down (buck) converter which conforms to the Intel Pentium® II VRM specification. Complementary switching outputs are provided to drive dual NMOS power FET's in either synchronous or non-synchronous configurations, enabling the user to realize a variety of high efficiency and low cost converters.

Reference

A precision, temperature compensated band gap reference forms the basis of the EL7571. The reference is trimmed during manufacturing and provides 1% set point accuracy for the overall regulator. AC rejection of the reference is optimized using an external bypass capacitor C_{REF}.

Main Loop

A current mode PWM control loop is implemented in the EL7571 (see block diagram). This configuration employs dual feedback loops which provide both output voltage and current feedback to the controller. The resulting system offers several advantages over tradititional voltage control systems, including simpler loop design, pulse by pulse current limiting, rapid response to line variaion and good load step response. Current feedback is performed by sensing voltage across an external shunt resistor. Selection of the shunt resistance value sets the level of current feedback and thereby the load regulation and current limit levels. Consequently, operation over a wide range of output currents is possible. The reference output is fed to a 5 bit DAC with step weighing conforming to the Intel VRM Specification. Each DAC input includes an internal current pull up which directly interfaces to the VID output of a Pentium® II class microprocessor. The heart of the controller is a triple-input direct summing differential comparator, which sums voltage feedback, current feedback and compensating ramp signals together. The relative gains of the comparator input stages are weighed. The ratio of voltage feedback to current feedback to compensating ramp defines the load regulation and open loop voltage gain for the system, respectively. The compensating ramp is required to maintain large system signal system stability for PWM duty cycles greater than 50%. Compensation ramp amplitude is user adjustable and is set with a single external capacitor (C_{SLOPE}). The ramp voltage is ground referenced and is reset to ground whenever the high side drive signal is low. In operation, the DAC output voltage is compared to the regulator output, which has been internally attenuated. The resulting error voltage is compared with the compensating ramp and current feedback voltage. PWM duty cycle is adjusted by the comparator output such that the combined comparator input sums to zero. A weighted comparator scheme enhances system operation over traditional voltage error amplifier loops by providing cycle-by-cycle adjustment of the PWM output voltage, eliminating the need for error amplifier compensation. The dominant pole in the loop is defined by the output capacitance and equivalent load resistance, the effect of the output inductor having been canceled due to the current feedback. An output enable (OUTEN) input allows the regulator output to be disabled by an external logic control signal.

Auxiliary Comparators

The current feedback signal is monitored by two additional comparators which set the operating limits for the main inductor current. An over current comparator terminates the PWM cycle independently of the main summing comparator output whenever the voltage across the sense resistor exceeds 154mV. For a 7.5mΩ resistor this corresponds to a nominal 20A current limit. Since output current is continuously monitored, cycle-by-cycle current limiting results. A second comparator senses inductor current reverse flow. The low side drive signal is terminated when the sense resistor voltage is less than -5mV, corresponding to a nominal reverse current of -0.67A, for a 7.5mΩ sense resistor. Additionally, under fault conditions, with the regulator output over-voltage, inductor current is prevented from ramping to a high level in the reverse direction. This prevents the parasitic boost action of the local power supply when the fault is removed and potential damage to circuitry connected to the local supply.

Oscillator

A system clock is generated by an internal relaxation oscillator. Operating frequency is simple to adjust using a single external capacitor C_{OSC}. The ratio of charge to discharge current in the oscillator is well defined and sets the maximum duty cycle for the system at around 96%.

Soft-start

During start-up, potentially large currents can flow into the regulator output capacitors due to the fast rate of change of output voltage caused during start-up, although peak inrush current will be limited by the over current comparator. However an additionally internal switch capacitor soft-start circuit controls the rate of change of output voltage during start-up by overriding the voltage feedback input of the main summing comparator, limiting the start-up ramp to around 1ms under typical operating conditions. The soft-start ramp is reset whenever the output enable (OUTEN) is reset or whenever the controller supply falls below 3.5V.

Watchdog

A system watchdog monitors the condition of the controller supply and the integrity of the generated output voltage.

Modern logic level power FET's rapidly increase in resistivity (R_{DS-ON}) as their gate drive is reduced below 5V. To prevent thermal damage to the power FET's under load, with a reduced supply voltage, the system watchdog monitors the controller supply (V_{IN}) and disables both PWM outputs (HSD, LSD) when the supply voltage drops below 3.5V. When the supply voltage is increased above 4V the watchdog initiates a soft-start ramp and enables PWM operation. The difference between enable and disable thresholds introduces hysteresis into the circuit operation, preventing start-up oscillation. In addition, output voltage is also monitored by the watchdog. As called out by the Intel Pentium® II VRM specification, the watchdog power good output (PWRGD) is set low whenever the output voltage differs from it's selected value by more than ±13%. PWRGD is an open drain output. A third watchdog function disables PWM output switching during over-voltage fault conditions, displaying both external FET drives, whenever the output voltage is greater than 13% of its selected value, thereby anticipating reverse inductor current ramping and conforming to the VRM over-voltage specification, which requires the regulator output to be disabled during fault conditions. Switching is enabled after the fault condition is removed.

Output Drivers

Complementary control signals developed by the PWM control loop are fed to dual NMOS power FET drivers via a level shift circuit. Each driver is capable of delivering nominal peak output currents of 2A at 12V. To prevent shoot-through in the external FET's, each driver is disabled until the gate voltage of the complementary power FET has fallen to less than 1V. Supply connections for both drivers are independent, allowing the controller to be configured with a boot-strapped high side drive. Employing this technique a single supply voltage may be used for both power FET's and controller. Alternatively, the application may be simplified using dual supply rails with the power FET's connected to a secondary supply voltage below the controller's, typically 12V and 5V. For applications where efficiency is less important than cost, applications can be further simplified by replacing the low side power FET with a Schottky diode, resulting in non-synchronous operation.

Applications Information

The EL7571 is designed to meet the Intel 5 bit VRM specification. Refer to the VID decode table for the controller output voltage range.

The EL7571 may be used in a number converter topologies. The trade-off between efficiency, cost, circuit complexity, line input noise, transient response and availability of input supply voltages will determine which converter topology is suitable for a given application. The following table lists some of the differences between the various configurations:

Converter Topologies

TOPOLOGY	DIAGRAM	EFFICIENCY	COST	COMPLEXITY	INPUT NOISE	TRANSIENT RESPONSE
5V only Non-synchronous	figure 1	92%	low	low	high	good
5V only Synchronous	figure 2	95%	higher	higher	high	good
5V &12V Non-synchronous	figure 3	92%	lowest	lowest	high	good
5V & 12V Synchronous	figure 4	95%	high	high	high	good
12V only Synchronous	Connection Diagram	92%	highest	highest	high	best

Circuit schematics and Bills of Material (BOMs) for the various topologies are provided at the end of this data sheet. If your application requirements differ from the included samples, the following design guide lines should be used to select the key component values. Refer to the front page connection diagram for component locations.

Output Inductor, L_1

Two key converter requirements are used to determine inductor value:

- I_{MIN}- minimum output current; the current level at which the converter enters the discontinuous mode of operation (refer to Elantec application note #18 for a detailed discussion of discontinuous mode)
- I_{MAX}- maximum output current

Although many factors influence the choice of the inductor value, including efficiency, transient response and ripple current, one practical way of sizing the inductor is to select a value which maintains continuous mode operation, i.e. inductor current positive for all conditions. This is desirable to optimize load regulation and light load transient response. When the minimum inductor ripple current just reaches zero and with the mean ripple current set to I_{MIN}, peak inductor ripple current is twice I_{MAX}, independent of duty cycle. The minimum inductor value is given by:

$$L_{1MIN} = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{1_{PEAK}} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times F_{SW} \times 2 \times I_{MIN}}$$

where:

I_{PEAK} = peak ripple current

T_{ON} = top switch on time

V_{IN} = input voltage

F_{SW} = switching frequency

V_{OUT} = output voltage

I_{MIN} = minimum load

Since inductance value tends to decrease with current, ripple current will generally be greater than $2I_{MIN}$ at higher output current.

Once the minimum output inductance is determined, an off the shelf inductor with current rating greater than the maximum DC output required can be selected. **Pulse Engineering** and **Coil Craft** are two manufactures of high current inductors. For converter designers who want to design their own high current inductors, for experimental purposes or to further reduce costs, we recommend the **Micrometals Powered Iron Cores** data sheet and applications note as a good reference and starting point.

Current Sense Resistor, R_1

Inductor current is monitored indirectly via a low value resistor R_1. The voltage developed across the current sense resistor is used to set the maximum operating current, the current reversal threshold and the system load regulation. To ensure reliable system operation it is important to sense the actual voltage drop across the resistor. Accordingly a four wire Kelvin connection should be made to the controller current sense inputs. There are two criteria for selecting the resistor value and type. Firstly, the minimum value is limited by the maximum output current. The EL7571 current limit capacitor has a typical threshold of 154mV, 125mV minimum. When the voltage across the sense resistor exceeds this threshold, the conduction cycle of the top switch terminates immediately, providing pulse by pulse current limiting. A resistor value must be selected which guarantees operation under maximum load. That is:

$$R_1 = \frac{V_{OCMIN}}{I_{MAX}}$$

where:

V_{OCMIN} = minimum over current voltage threshold

I_{MAX} = maximum output current

Secondly, since the load current passes directly through the sense resistor, its power rating must be sufficient to handle the power dissipated during maximum load (current limit) conditions. Thus:

$$P_D = I_{OUTMAX}^2 \times R_1$$

where:

P_D = power dissipated in current sense resistor

P_D must be less than the power rating of the current sense resistor. High current applications may require parallel sense resistors to dissipate sufficient power. Current Sense Resistor Table below lists some popular current sense resistors: the WLS-2512 series of Power Metal Strip Resistors from Dale Electronics, OARS series Iron Alloy resistor from IRC, and Copper Magnanin (CuNi) wire resistor from Mills Resistors. Mother board copper trace is not recommended because of its high temperature coefficient and low power dissipation. The trade-off between the different types of resistors are cost, space, packaging and performance. Although Power Metal Strip Resistors are relatively expensive, they are available in surface mount packaging with tighter tolerances. Consequently, less board space is used to achieve a more accurate current sense. Alternatively, Magnanin copper wire has looser tolerance and higher parasitic inductance. This results in a less current sense but at a much lower cost. Metal track on the PCB can also be used as current sense resistor. The trade-offs are ±30% tolerance and ±4000 ppm temperature coefficient. Ultimately, the selection of the type of current sense element must be made on an application by application basis.

Bill of Materials

MANUFACTURER	PART NO.	TOLERANCE	TEMPERATURE COEFFICIENT	POWER RATING	PHONE NO.	FAX NO.
Dale	WSL 2512	±1%	±75ppm	1W	402-563-6506	402-563-6418
IRC	OARS Series	±5%	±20ppm	1W - 5W	800-472-6467	800-472-3282
Mills Resistor	MRS1367-TBA	±10%	±20ppm	1.2W	916-422-5461	906-422-1409
PCB Trace Resistor		±30%	±4000ppm	50A/in (1oz Cu)		

Input Capacitor, C_1

In a buck converter, where the output current is greater than 10A, significant demand is placed on the input capacitor. Under steady state operation, the high side FET conducts only when it is switched “on” and conducts zero current when it is turned “off”. The result is a current square wave drawn from the input supply. Most of this input ripple current is supplied from the input capacitor C_1. The current flow through C_1’s equivalent series resistance (ESR) can heat up the capacitor and cause premature failure. Maximum input ripple current occurs when the duty cycle is 50%, a current of $I_{OUT}/2$ RMS.

Worst case power dissipation is:

$$P_D = \left(\frac{I_{OUT}}{2}\right)^2 \bullet ESR_{IN}$$

where:

ERS_{IN} = input capacitor ESR

For safe and reliable operation, P_D must be less than the capacitor’s data sheet rating.

Input Inductor, L_2

The input inductor (L_2) isolates switching noise from the input supply line by diverting buck converter input ripple current into the input capacitor. Buck regulators generate high levels of input ripple current because the load is connected directly to the supply through the top switch every cycle, chopping the input current between the load current and zero, in proportion to the duty cycle. The input inductor is critical in high current applications where the ripple current is similarly high. An exclusively large input inductor degrades the converter’s load transient response by limiting the maximum rate of change of current at the converter input. A 1.5µH input inductor is sufficient in most applications.

Output Capacitor, C_2

During steady state operation, output ripple current is much less than the input ripple current since current flow is continuous, either via the top switch or the bottom switch. Consequently, output capacitor power dissipation is less of a concern than the input capacitor’s. However, low ESR is still required for applications with very low output ripple voltage or transient response requirements. Output ripple voltage is given by:

$$V_{RIP} = I_{RIP} \times ESR_{OUT}$$

where:

I_{RIP} = output ripple current

ESR_{OUT} = output capacitor ESR

During a transient response, the output voltage spike is determined by the ESR and the equivalent series inductance (ESL) of the output capacitor in addition to the rate of change and magnitude of the load current step. The output voltage transient is given by:

$$\Delta V_{OUT} = \left(ESR_{OUT} \times \Delta I_{OUT} + ESL \times \frac{d_i}{d_t}\right)$$

where:

ESR_{OUT} = output capacitor ESR

ESL = output capacitor ESL

ΔI_{OUT} = output current step

d_i/d_t = rate of change of output current

Power MOSFET, Q_1 and Q_2

The EL7571 incorporates a boot-strap gate drive scheme to allow the usage of N-channel MOSFETs. N-channel MOSFETs are preferred because of their relative low cost and low on resistance. The largest amount of the power loss occurs in the power MOSFETs, thus low on resistance should be the primary characteristic when selecting power MOSFETs. In the boot-strap gate drive scheme, the gate drive voltage can only go as high as the supply voltage, therefore in a 5V system, the MOSFETs must be logic level type, V_{GS}<4.5V. In addition to on resistance and gate to source threshold, the gate to source capacitance is also very important. In the region when the output current is low (below 5A), switching loss is the dominant factor. Switching loss is determined by:

$$P = C \times V^2 \times F$$

where:

C is the gate to source capacitance of the MOSFET

V is the supply voltage

F is the switching frequency

Another undesirable reason for a large MOSFET gate to source capacitance is that the on resistance of the MOSFET driver can not supply the peak current required to turn the MOSFET on and off fast. This results in additional MOSFET conduction loss. As frequency increases, this loss also increases which leads to more power loss and lower efficiency.

Finally, the MOSFET must be able to conduct the maximum current and handle the power dissipation.

The EL7571 is designed to boot-strap to 12V for 12V only input converters. In this application, logic level MOSFETs are not required.

The following table below lists a few popular MOSFETs and their critical specifications.