LVD SCSI Terminator

– Ultra2/3 SCSI
– 9 Channels
– Eliminates External V_{REF} Capacitor

The IMP5245/5246 ICs are Low Voltage Differential (LVD) terminators designed to comply with the LVD termination specification in the SPI-2 document. The IMP5245/5246 are designed specifically for LVD applications. Because the IMP5245/5246 support only LVD, they have lower output capacitance than multimode terminators.

The IMP5245/5246 deliver the ultimate in SCSI bus performance while saving component cost and board area. Elimination of the external capacitors also mitigates the need for a lengthy capacitor selection process. The individual high bandwidth drivers also maximize channel separation and reduces channel-to-channel noise and cross talk. The high-bandwidth architecture insures ULTRA-2 performance, while providing a clear migration path to ULTRA-3 and beyond.

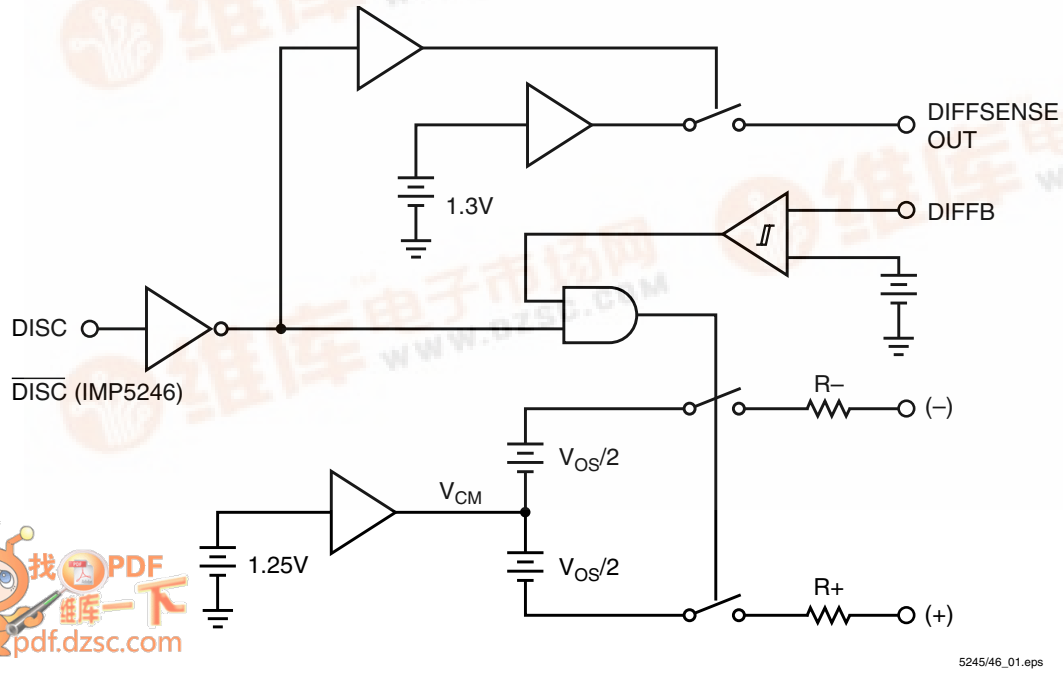
When the IMP5245/5246 are enabled, the differential sense (DIFFSENSE) pin supplies a voltage between 1.2V and 1.4V. The terminator DIFFSENSE output is connected to the system DIFFSENSE line. If there are no single ended or HVD devices attached to the system the LVD output will be enabled. If the DIFFSENSE line is LOW, indicating a single ended device, the IMP5245/5246 output will be in a high-impedance state. If the DIFFSENSE line is HIGH, indicating a high voltage differential device, the IMP5245/5246 output will also be in a high-impedance state.

The IMP5245/5246 ICs have a TTL compatible disconnect pin. The IMP5245 is active LOW and the IMP5246 is active HIGH. During sleep mode, power supply current is reduced to just 5µA. During sleep mode all outputs are in a high-impedance state. Also during sleep mode, the DIFFSENSE function is disabled and is placed in a high-impedance state.

Key Features

- 2.5pF typical disabled output capacitance
- Fast response
- No external V_{REF} capacitors required
- 5µA supply current in disconnect mode
- 20mA supply current during normal operation
- Logic command disconnects all termination lines
- Diffsense line driver
- Current limit and thermal protection
- Compatible with the pending SPI-2 LVD specification
- Pin compatible to the UCC5640

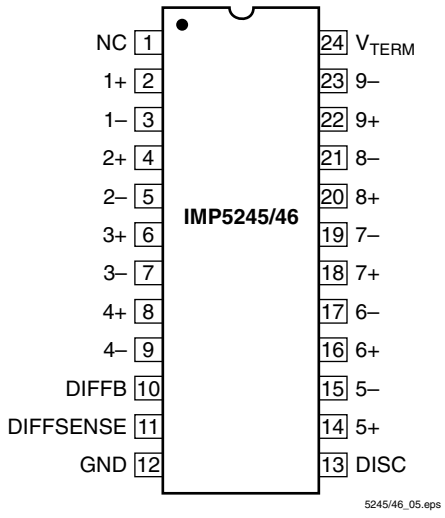
Block Diagram



5245/46_01.eps

Pin Configuration

TSSOP Package



Ordering Information

Part Number	Temperature Range	Package
IMP5245CPW	0°C to 70°C	24-Pin Plastic TSSOP
IMP5246CPW	0°C to 70°C	24-Pin Plastic TSSOP

Absolute Maximum Ratings[1]

TermPwr Voltage . . . . . +6.5V
Signal Line Voltage . . . . . 0V to 6.5V
Differential Voltage . . . . . 0V to 6.5V
Operating Junction Temperature
Plastic (PW Package) . . . . . 150°C

Storage Temperature Range . . . . . –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) . . . . . 300°C

Note: 1. Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

Thermal Data

PW Package:
Thermal Resistance Junction-to-Ambient, θ_{JA} . . . . . 100°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. No ambient airflow is assumed.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Termpwr Voltage	V_{TERM}	3.0		5.25	V
Signal Line Voltage		0		5.0	V
Disconnect Input Voltage		0		V_{TERM}	V
Operating Junction Temperature Range — IMP5245/5246		0		70	°C

Note: 2. Range over which the device is functional.

Electrical Characteristics

Unless otherwise specified, these specifications apply over the operating ambient temperature range of $0°C \le T_A \le 70°C$. TermPwr = 3.3V, DISCONNECT: IMP5245 = LOW, IMP5246 = HIGH. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
LVD Terminator Section						
TermPwr Supply Current		All term lines = Open		20	25	mA
Power Down Mode		DISCONNECT: IMP5245 = HIGH, IMP5246 = LOW		5	10	µA
Common Mode Voltage	V_{OM}		1.125	1.25	1.375	V
Offset Voltage	V_{OS}	Open circuit between – and + (see Note 3)	100	112	125	mV
Differential Terminator Impedance		V_{OD} = –1V to 1V	100	105	110	Ω
Common Mode Impedance		0V to 2.5V	100	200	300	Ω
Output Capacitance		DISCONNECT: IMP5245 = HIGH, IMP5246 = LOW		2.5		pF
Output Leakage		DISCONNECT: IMP5245 = HIGH, IMP5246 = LOW, V_{LINE} = 0 to 4V, T_A = 25°C		0	2	µA
		DISCONNECT: IMP5245 = HIGH, IMP5246 = LOW, V_{TERM} = 0V, V_{LINE} = 2.7V		1		µA
Mode Change Delay		DIFFSENSE = 1.4V to 0V	100	150		ms
DIFFSENSE Section						
DIFFSENSE Output Voltage			1.2	1.3	1.4	V
DIFFSENSE Output Source Current		DIFFSENSE = 0V	5.0		15.0	mA
DIFFSENSE Sink Current		V_{IN} = 2.75V			200	µA
DIFFSENSE Output Leakage		DISCONNECT: IMP5245 = HIGH, IMP5246 = LOW, T_A = 25°C			10	µA
DISCONNECT Section						
DISCONNECT Threshold			0.8		2.0	V
Input Current		DISCONNECT: IMP5245 = 0V			10	µA
		$\overline{\text{DISCONNECT}}$: IMP5246 = 3.3V			10	µA

Note: 3. Open circuit failsafe voltage.

Application Information

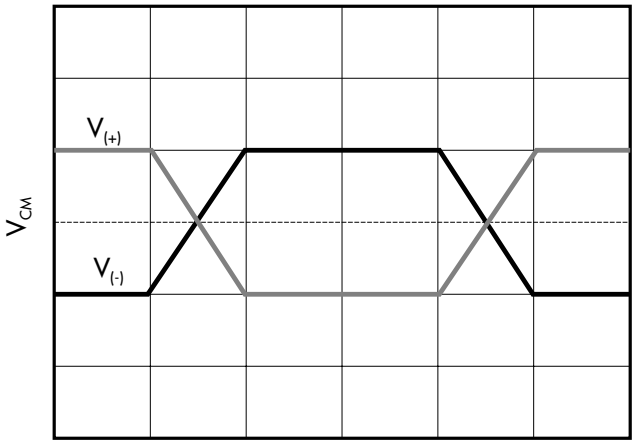


Figure 1. Bus Voltage

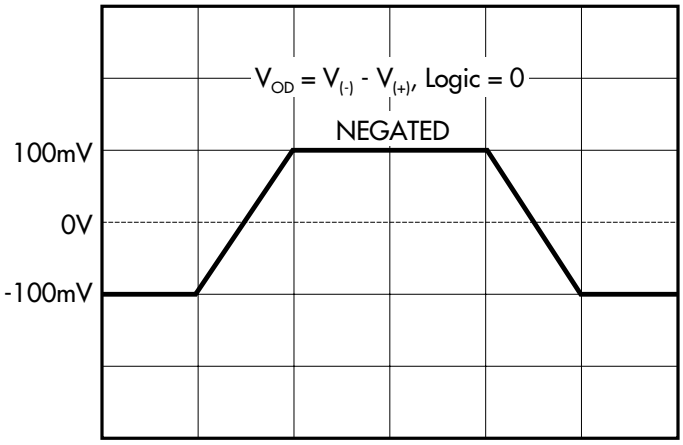


Figure 2. V_{OD}

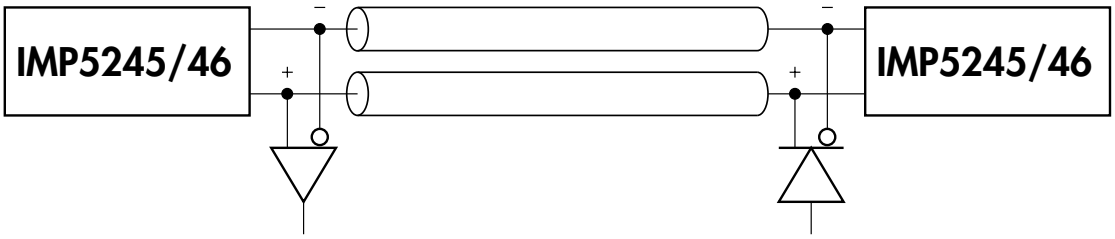


Figure 3.

Table 1. DIFFSENSE/Power Up/Power Down Function Table

IMP5245 DISCONNECT	IMP5246 $\overline{\text{DISCONNECT}}$	DIFFSENS	Outputs		Current
			Status	Type	
L	H	L < 0.5V	Disable	HiZ	2mA
L	H	0.7V to 1.9V	Enable	LVD	21mA
L	H	H > 2.4V	Disable	HiZ	2mA
H	L	X	Disable	HiZ	10µA
Open	Open	X	Disable	HiZ	10µA

Note: IMP5245 Disconnect logic is compatible with the Unitrode UCC5640.

Application Information

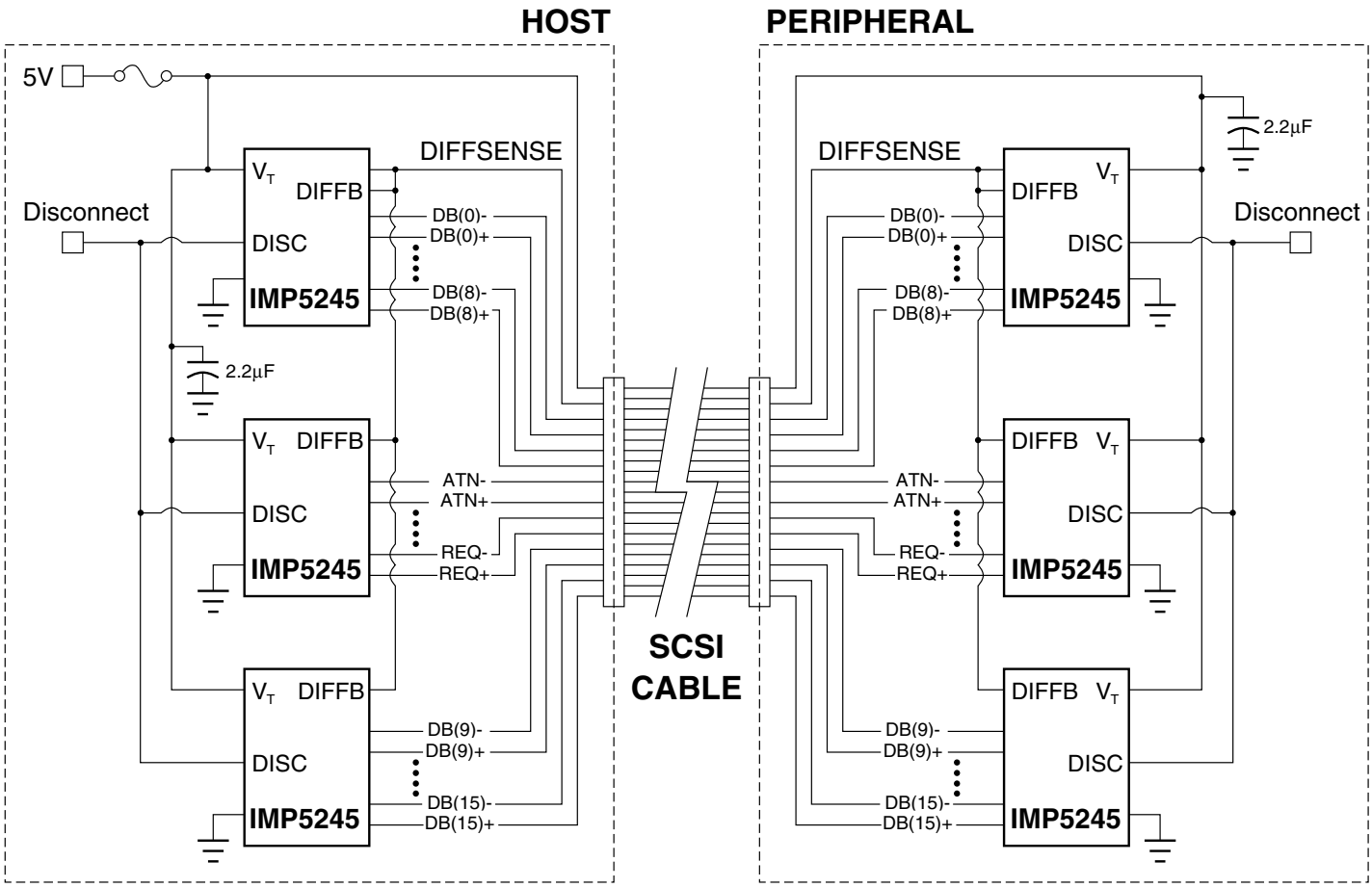


Figure 4. Application Schematic

ISO 9001 Registered

IMP, Inc.
Corporate Headquarters
2830 N. First Street
San Jose, CA 95134-2071
Tel: 408-432-9100
Fax: 408-432-1085
e-mail: info@impinc.com
http://www.impweb.com

Publication #: 7003