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ISO 9001 Registered

IMP5111/5112

DATA COMMUNICATIONS

9-Line SCSI Terminator – 35MHz Channel Bandwidth

The 9-channel IMP5111/5112 SCSI terminator is part of IMP's family of high-performance SCSI terminators that deliver true UltraSCSI performance. The BiCMOS design offers superior performance over first generation linear regulator/resistor based terminators.

IMP's new architecture employs high-speed adaptive elements for each channel, thereby providing the fastest response possible - typically 35MHz, which is 100 times faster than the older linear regulator terminator approach. The bandwidth of terminators based on the older regulator/resistor terminator architecture is limited to 500kHz since a large output stabilization capacitor is required. The IMP architecture eliminates the external output compensation capacitor and the need for transient output capacitors while maintaining pin compatibility with first generation designs. Reduced component count is inherent with the IMP5111/5112.

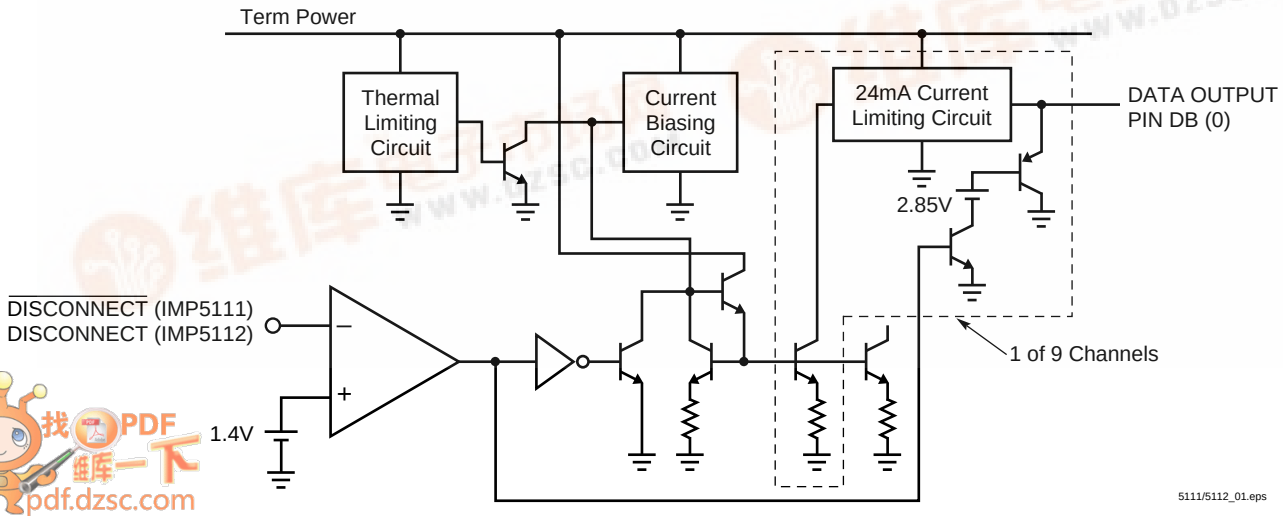
The IMP5111/5112 architecture tolerates marginal system designs. A key improvement offered by the IMP5111/5112 lies in its ability to insure reliable, error-free communications even in systems which do not adhere to recommended SCSI hardware design guidelines, such as improper cable lengths and impedance. Frequently, this situation is not controlled by the peripheral or host designer.

For portable and configurable peripherals, the IMP5111/5112 can be placed in a sleep mode with a disconnect signal. Quiescent current is less than 275µA when disabled. When disabled, the outputs are in a high impedance state with output capacitance less than 3pF.

Key Features

- Ultra-Fast response for Fast-20 SCSI applications
- 35MHz channel bandwidth
- 3.3V operation
- Less than 3pF output capacitance
- Sleep-mode current less than 275µA
- Thermally self limiting
- No external compensation capacitors
- Implements 8-bit or 16-bit (wide) applications
- Compatible with active negation drivers (60mA/channel)
- Compatible with passive and active terminations
- Approved for use with SCSI 1, 2, 3 and UltraSCSI
- Hot swap compatible
- Pin-for-pin compatible with LX5211 and UC5606 (IMP5111)
- Pin-for-pin compatible with LX5212 and UC5603/5613/5614 (IMP5112)

Block Diagrams



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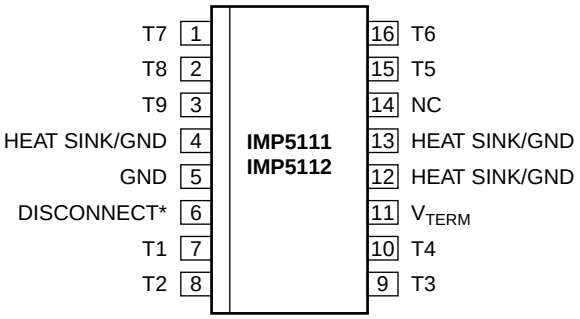
Pin Configuration

SO-16



DW Package

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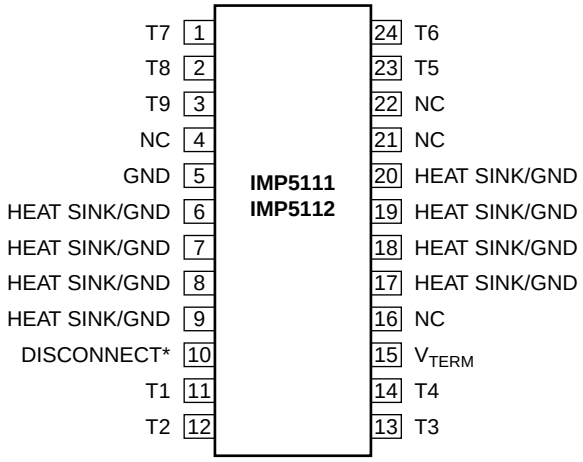
* $\overline{\text{DISCONNECT}}$ (IMP5111)
DISCONNECT (IMP5112)

TSSOP-24



PW Package

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* $\overline{\text{DISCONNECT}}$ (IMP5111)
DISCONNECT (IMP5112)

Ordering Information

Part Number	Temperature Range	Package
IMP5111CDP	0°C to 125°C	16-pin Plastic SO
IMP5111CDPT	0°C to 125°C	Tape and Reel, 16-pin Plastic SO
IMP5111CPWP	0°C to 125°C	24-pin Plastic TSSOP
IMP5111CPWPT	0°C to 125°C	Tape and Reel, 24-pin Plastic TSSOP
IMP5112CDP	0°C to 125°C	16-pin Plastic SO
IMP5112CDPT	0°C to 125°C	Tape and Reel, 16-pin Plastic SO
IMP5112CPWP	0°C to 125°C	24-pin Plastic TSSOP
IMP5112CPWPT	0°C to 125°C	Tape and Reel, 24-pin Plastic TSSOP

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Absolute Maximum Ratings[1]

TermPwr Voltage . . . . . +7V
Signal Line Voltage . . . . . 0V to +7V
Regulator Output Current 0.4A
Operating Junction Temperature
Plastic (DP, PWP Packages) . . . . . 150°C

Storage Temperature Range . . . . . -65°C to 150°C
Lead Temperature (Soldering, 10 seconds) . . . . . 300°C

Note: 1. Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

Thermal Data

DP Package:
Thermal Resistance Junction-to-Leads, θ_{JL} . . . . . 20°C / W
Thermal Resistance Junction-to-Ambient, θ_{JA} . . . . . 50°C / W
PW Package:
Thermal Resistance Junction-to-Leads, θ_{JL} . . . . . 27°C / W
Thermal Resistance Junction-to-Ambient, θ_{JA} . . . . . 100°C / W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device / pc-board system. All of the ambient airflow is assumed.

Recommended Operating Conditions[2]

Parameter		Symbol	Min	Typ	Max	Units
TermPwr Voltage		V_{TERM}	3.3		5.5	V
High Level Enable Input Voltage	IMP5111	V_{IH}	2		V_{TERM}	V
	IMP5112		0		0.8	
Low Level Disable Input Voltage	IMP5111	V_{IL}	0		0.8	V
	IMP5112		2		V_{TERM}	
Operating Junction Temperature Range			0		125	°C

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Note: 2. Recommended operating conditions indicate the range over which the device is functional.

Electrical Characteristics

Unless otherwise specified, these specifications apply at an ambient operating temperature of T_A = 25°C. TermPwr = 4.75V. Low duty cycle pulse testing techniques are used which maintain junction and case temperatures equal to the ambient temperature.

Parameter		Symbol	Conditions	Min	Typ	Max	Units
Output High Voltage		V_{OUT}		2.65	2.85		V
TermPwr Supply Current		I_{CC}	All data lines = Open		6	9	mA
			All data lines = 0.5V		215	225	
	IMP5111		$\overline{\text{DISCONNECT}}$ Pin < 0.8V		275		µA
	IMP5112		DISCONNECT Pin > 2.0V		275		
Output Current		I_{OUT}	V_{OUT} = 0.5V	–21	–23	–24	mA
DISCONNECT Input Current	IMP5111	I_{IN}	$\overline{\text{DISCONNECT}}$ Pin = 4.75V		10		nA
			$\overline{\text{DISCONNECT}}$ Pin = 0V		–90		µA
DISCONNECT Input Current	IMP5112	I_{IN}	DISCONNECT Pin = 0V		–90		µA
			DISCONNECT Pin = 4.75V		10		nA
Output Leakage Current	IMP5111	I_{OL}	$\overline{\text{DISCONNECT}}$ Pin < 0.8V, V_O = 0.5V		10		nA
	IMP5112		DISCONNECT Pin > 2.0V, V_O = 0.5V		10		
Capacitance in DISCONNECT Mode		C_{OUT}	V_{OUT} = 0V, Frequency = 1MHz		3		pF
Channel Bandwidth		BW			35		MHz
Termination Sink Current, per Channel		I_{SINK}	V_{OUT} = 4V		60		mA

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Application Information

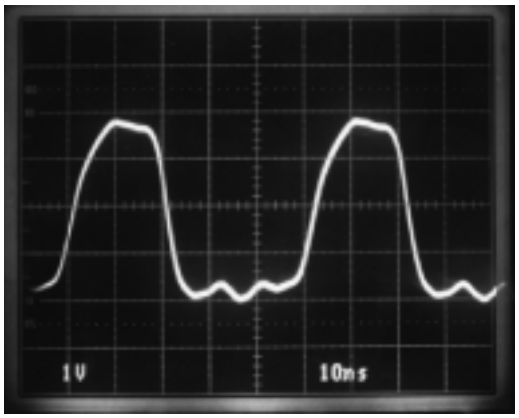

Figure 1. Receiving Waveform – 20MHz

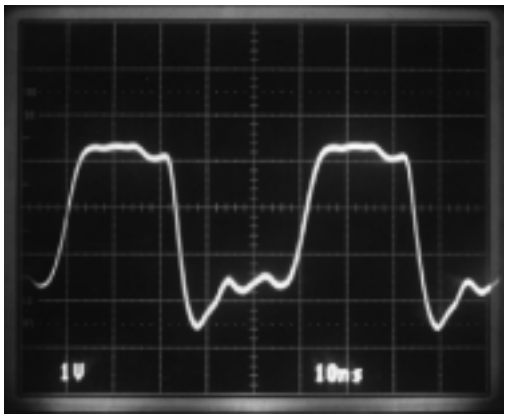

Figure 2. Driving Waveform – 20MHz

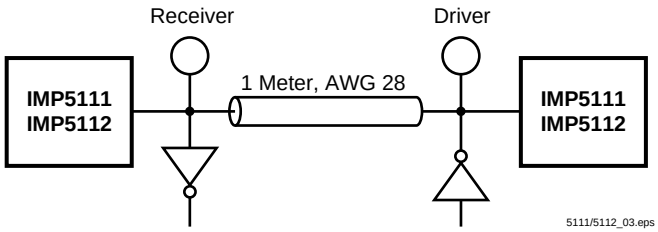

Figure 3.

IMP5111/IMP5112 Maximizes Line Current

Cable transmission theory suggests to optimize signal speed and quality, the termination should act both as an ideal voltage reference when the line is released (deasserted) and as an ideal current source when the line is active (asserted). Common active terminators which consist of linear regulators in series with resistors (typically 110Ω) are a compromise. With coventional linear terminators as the line voltage increases the amount of current decreases linearly by the equation;

$$\frac{(V_{REF} - V_{LINE})}{R} = I.$$

The IMP5111/5112, with their unique architecture, applies the maximum amount of current regardless of line voltage until the termination high threshold (2.85V) is reached.

Disable /Sleep Mode

The IMP5111 has an active LOW disconnect pin, and the IMP5112 has an active HIGH disconnect pin. The disable mode is entered if the disconnect pin on either device is left open.

When disabled the termination lines are in a high impedance state, and the power supply current drops to 275µA typically. The disable mode can be used to save power or completely eliminate the terminator from the SCSI bus.

Disabled terminators appear as distributed capacitance on the bus. The IMP5111/5112 have been optimized to have only 3pF of capacitance per output when in the disabled mode.

The IMP5111/5112 are compatible with active negation drivers. The devices will handle up to 60mA of sink current for drivers which exceed the 2.85V output high level.

Table 1. Power Up/ Power Down Function Table

$\overline{\text{IMP5111 DISCONNECT}}$	IMP5112 DISCONNECT	Outputs	Quiescent Current
H	L	Enabled	6mA
L	H	Disabled/High Impedance	275µA
Open	Open	Disabled/High Impedance	275µA

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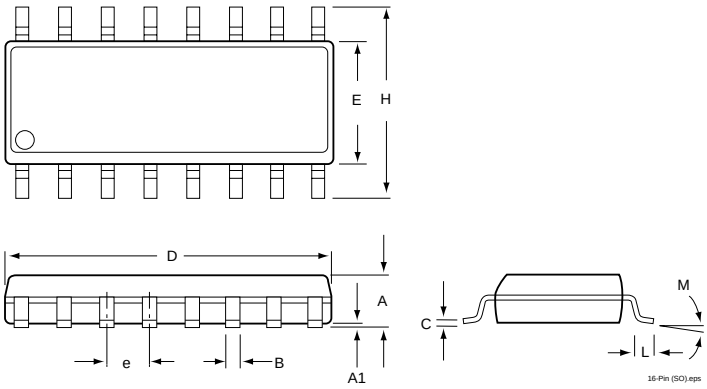
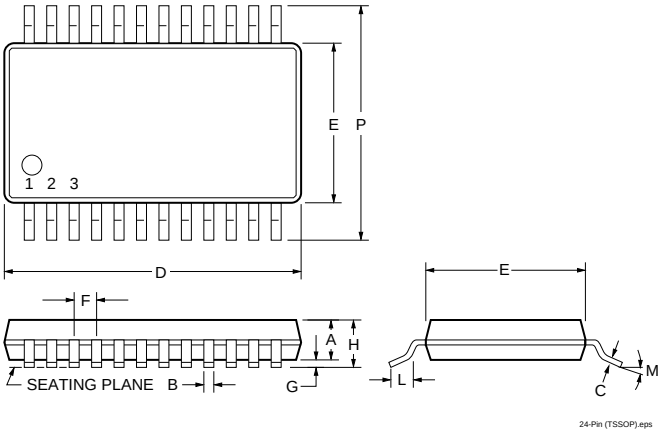
Package Dimensions

SO (16-Pin)



TSSOP (24-Pin)



	Inches		Millimeters	
	Min	Max	Min	Max
SO (16-Pin)*				
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.018	0.35	0.46
C	0.007	0.010	0.19	0.25
D	0.385	0.394	9.78	10.01
E	0.150	0.158	3.81	4.01
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.79	6.20
L	0.016	0.050	0.40	1.27
M	0°	8°	0°	8°
TSSOP (24-Pin)				
A	0.032	0.041	0.80	1.05
B	0.007	0.012	0.19	0.30
C	0.0035	0.0071	0.09	0.180
D	0.303	0.311	7.70	7.90
E	0.169	0.176	4.30	4.48
F	0.025 BSC		0.65 BSC	
G	0.002	0.005	0.05	0.15
H	—	0.0433	—	1.10
L	0.020	0.028	0.50	0.70
M	0°	8°	0°	8°
P	0.246	0.256	6.25	6.50

** JEDEC Drawing MS-012AC*

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