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Technical Data

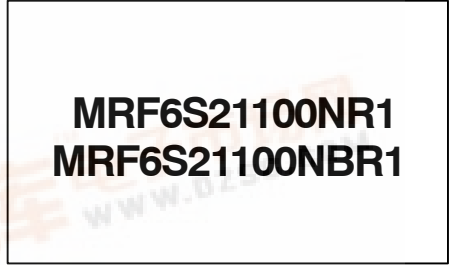
Document Number: MRF6S21100N  
Rev. 0, 6/2005

# RF Power Field Effect Transistors

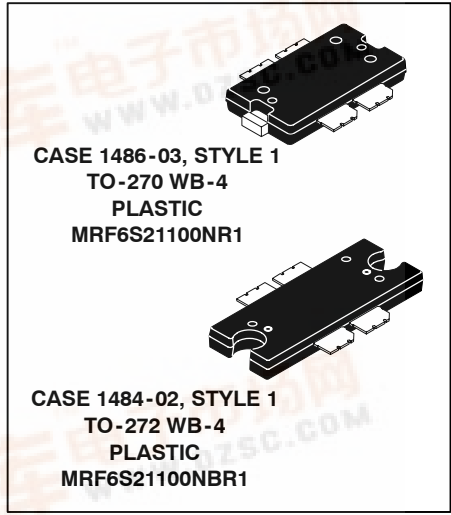
## N-Channel Enhancement-Mode Lateral MOSFETs

Designed for W-CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN - PCS/cellular radio and WLL applications.

- Typical 2-Carrier W-CDMA Performance:  $V_{DD} = 28$  Volts,  $I_{DQ} = 1050$  mA,  $P_{out} = 23$  Watts Avg., Full Frequency Band, Channel Bandwidth = 3.84 MHz, PAR = 8.5 dB @ 0.01% Probability on CCDF.  
Power Gain — 14.5 dB  
Drain Efficiency — 25.5%  
IM3 @ 10 MHz Offset — -37 dBc @ 3.84 MHz Bandwidth  
ACPR @ 5 MHz Offset — -40 dBc @ 3.84 MHz Bandwidth
- Capable of Handling 5:1 VSWR, @ 28 Vdc, 2140 MHz, 100 Watts CW Output Power
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Qualified Up to a Maximum of 32  $V_{DD}$  Operation
- Integrated ESD Protection
- N Suffix Indicates Lead-Free Terminations
- 200°C Capable Plastic Package
- Designed for Lower Memory Effects and Wide Instantaneous Bandwidth Applications
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.



**2170 MHz, 23 W AVG., 28 V**  
**2 x W-CDMA**  
**LATERAL N-CHANNEL**  
**RF POWER MOSFETs**



**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +68	Vdc
Gate-Source Voltage	$V_{GS}$	-0.5, +12	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	$P_D$	307 1.75	W W/°C
Storage Temperature Range	$T_{stg}$	-65 to +175	°C
Operating Junction Temperature	$T_J$	200	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (1,2)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 100 W CW Case Temperature 73°C, 23 W CW	$R_{\theta JC}$	0.57 0.66	°C/W

1. MTTF calculator available at <http://www.freescale.com/rf>. Select Tools/Software/Application Software/Calculators to access the MTTF calculators by product.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

**NOTE - CAUTION** - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.



**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	1B (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

**Table 4. Moisture Sensitivity Level**

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

**Table 5. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**Off Characteristics**

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 68\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**On Characteristics**

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 330\ \mu\text{Adc}$ )	$V_{GS(th)}$	1	2	3	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28\text{ Vdc}$ , $I_D = 1050\text{ mAdc}$ )	$V_{GS(Q)}$	2	2.8	4	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 3.3\text{ Adc}$ )	$V_{DS(on)}$	—	0.24	—	Vdc
Forward Transconductance ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 2.2\text{ Adc}$ )	$g_{fs}$	—	5.3	—	S

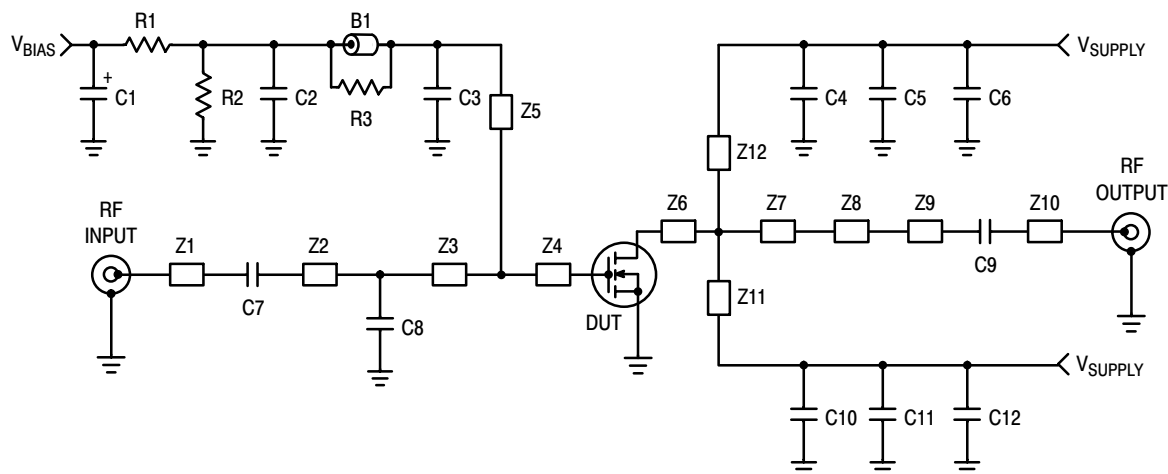
**Dynamic Characteristics<sup>(1)</sup>**

Reverse Transfer Capacitance ( $V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{rss}$	—	1.5	—	pF
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**Functional Tests** (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ} = 1050\text{ mA}$ ,  $P_{out} = 23\text{ W Avg.}$ ,  $f_1 = 2112.5\text{ MHz}$ ,  $f_2 = 2122.5\text{ MHz}$  and  $f_1 = 2157.5\text{ MHz}$ ,  $f_2 = 2167.5\text{ MHz}$ , 2-carrier W-CDMA, 3.84 MHz Channel Bandwidth Carriers, ACPR measured in 3.84 MHz Channel Bandwidth @  $\pm 5\text{ MHz}$  Offset. IM3 measured in 3.84 MHz Bandwidth @  $\pm 10\text{ MHz}$  Offset. PAR = 8.5 dB @ 0.01% Probability on CCDF.

Power Gain	$G_{ps}$	13	14.5	16	dB
Drain Efficiency	$\eta_D$	24	25.5	36	%
Intermodulation Distortion)	IM3	-47	-37	-35	dBc
Adjacent Channel Power Ratio	ACPR	-50	-40	-38	dBc
Input Return Loss	IRL	—	-12	-10	dB

1. Part is internally matched both on input and output.



Z1, Z10	0.743" x 0.084" Microstrip	Z7	0.259" x 0.880" Microstrip
Z2	0.893" x 0.084" Microstrip	Z8	0.215" x 0.230" Microstrip
Z3	0.175" x 0.084" Microstrip	Z9	0.787" x 0.084" Microstrip
Z4	0.420" x 0.800" Microstrip	Z11, Z12	1.171" x 0.120" Microstrip
Z5	1.231" x 0.040" Microstrip	PCB	Arlon AD250, 0.030", $\epsilon_r = 2.5$
Z6	0.100" x 0.880" Microstrip		

**Figure 1. MRF6S21100NR1(NBR1) Test Circuit Schematic**

**Table 6. MRF6S21100NR1(NBR1) Test Circuit Component Designations and Values**

Part	Description	Part Number	Manufacturer
B1	Ferrite Bead (0805)	25008051107Y0	Fair-Rite
C1	10 $\mu$ F, 35 V Tantalum Capacitor	T491D106K035AS	Kemet
C2	0.01 $\mu$ F Chip Capacitor (1825)	C1825C103J1GAC	Kemet
C3, C4, C10	5.1 pF 600B Chip Capacitors	600B5R1BT250XT	ATC
C5, C6, C11, C12	10 $\mu$ F, 50 V Chip Capacitors	GRM55DR61H106KA88L	Murata
C7	10 pF 600B Chip Capacitor	600B100BT250XT	ATC
C8	1.1 pF 600B Chip Capacitor	600B1R1BT250XT	ATC
C9	5.1 pF 600 B Chip Capacitor (MRF6S21100NR1) 8.2 pF 600 B Chip Capacitor (MRF6S21100NBR1)	600B5R1BT250XT 600B8R2BT250XT	ATC ATC
R1	1 k $\Omega$ , 1/4 W Chip Resistor (1206)		
R2	10 k $\Omega$ , 1/4 W Chip Resistor (1206)		
R3	10 $\Omega$ , 1/4 W Chip Resistor (1206)		

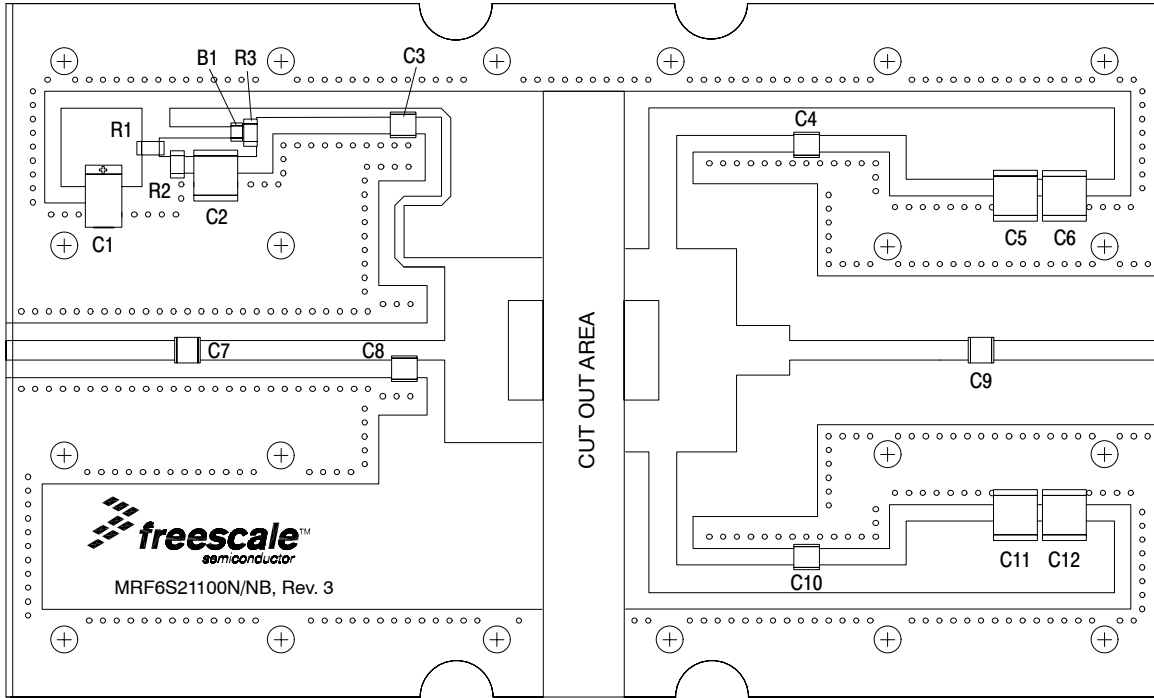


Figure 2. MRF6S21100NR1(NBR1) Test Circuit Component Layout

## TYPICAL CHARACTERISTICS

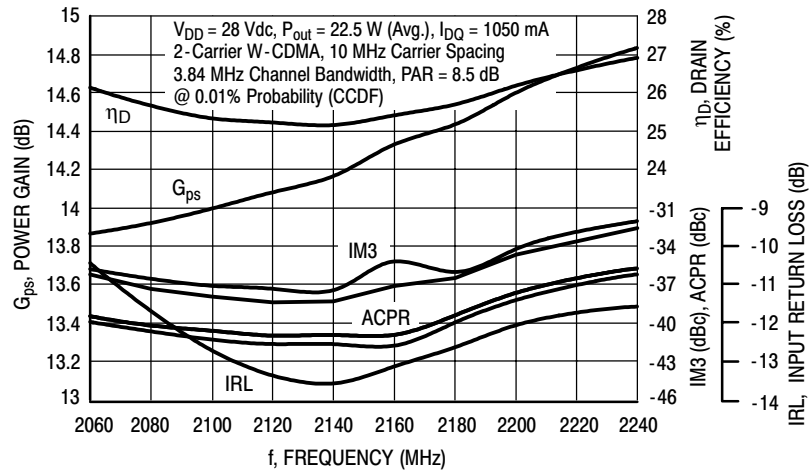


Figure 3. 2-Carrier W-CDMA Broadband Performance @  $P_{out} = 22.5$  Watts Avg.

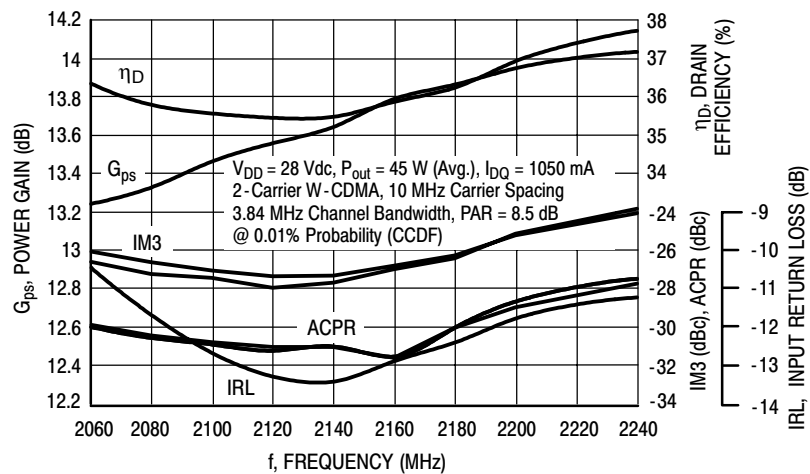


Figure 4. 2-Carrier W-CDMA Broadband Performance @  $P_{out} = 45$  Watts Avg.

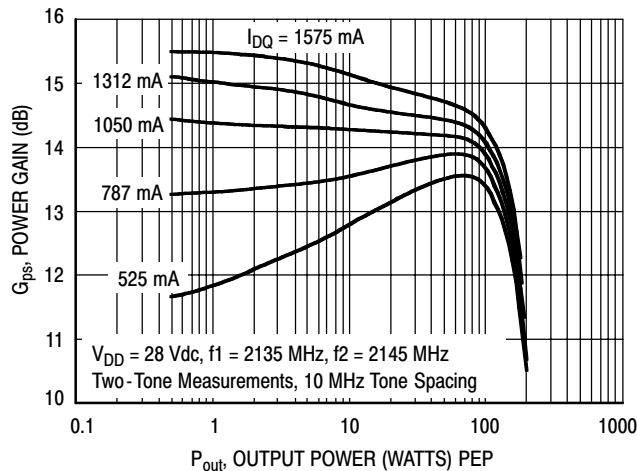


Figure 5. Two-Tone Power Gain versus Output Power

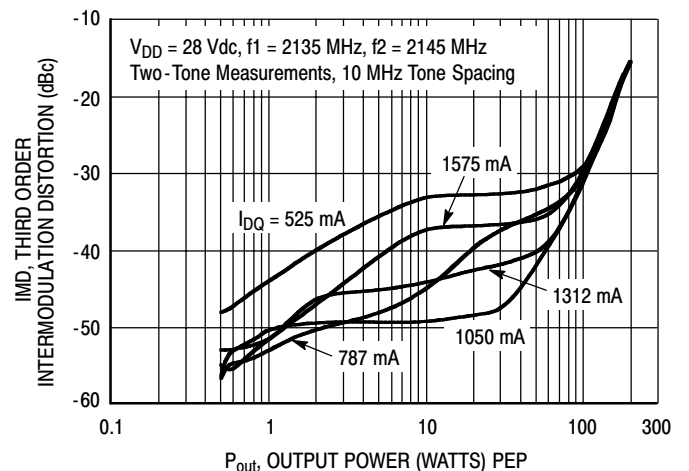
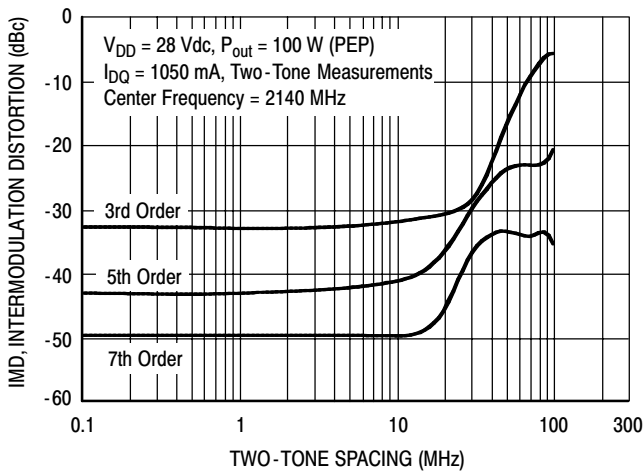
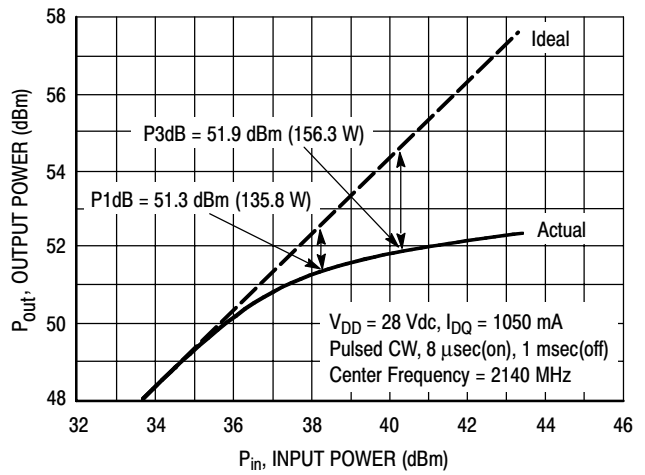


Figure 6. Third Order Intermodulation Distortion versus Output Power

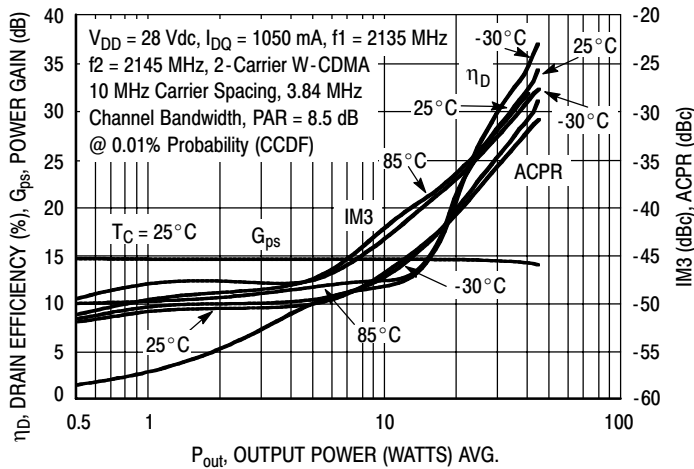
## TYPICAL CHARACTERISTICS



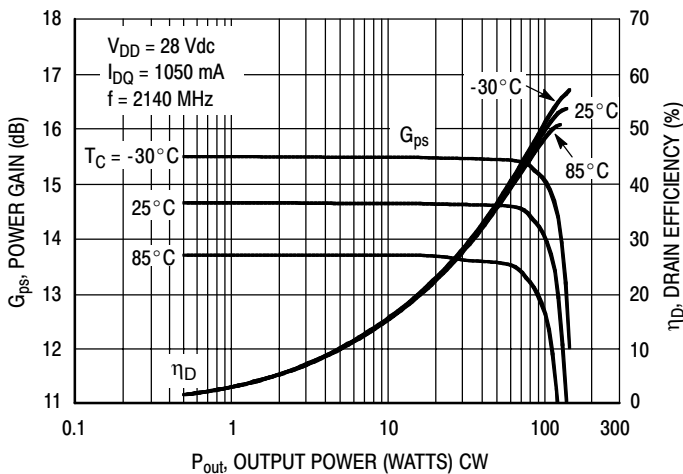
**Figure 7. Intermodulation Distortion Products versus Tone Spacing**



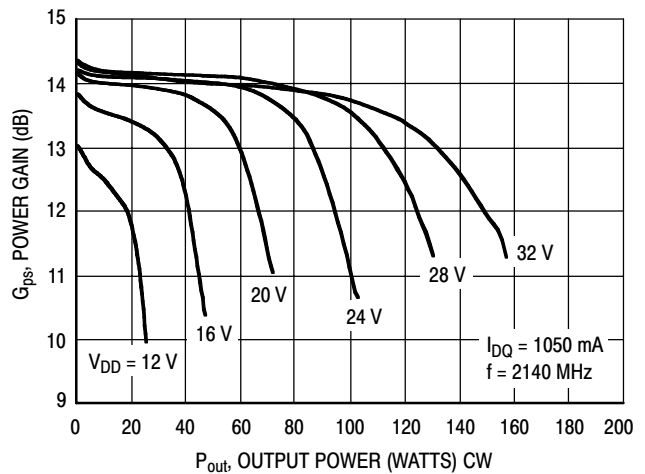
**Figure 8. Pulse CW Output Power versus Input Power**



**Figure 9. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power**

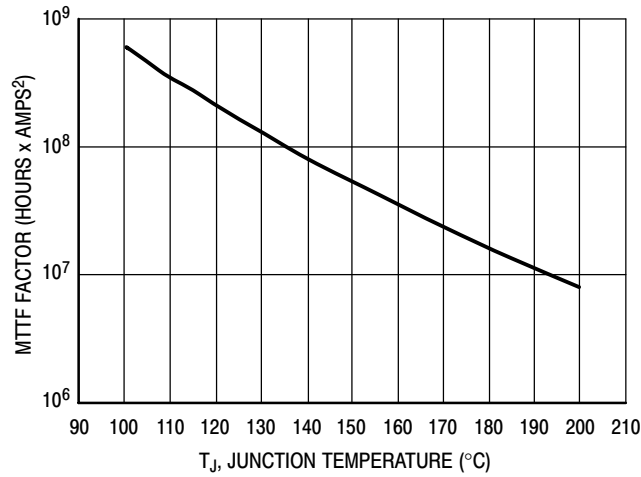


**Figure 10. Power Gain and Drain Efficiency versus CW Output Power**



**Figure 11. Power Gain versus Output Power**

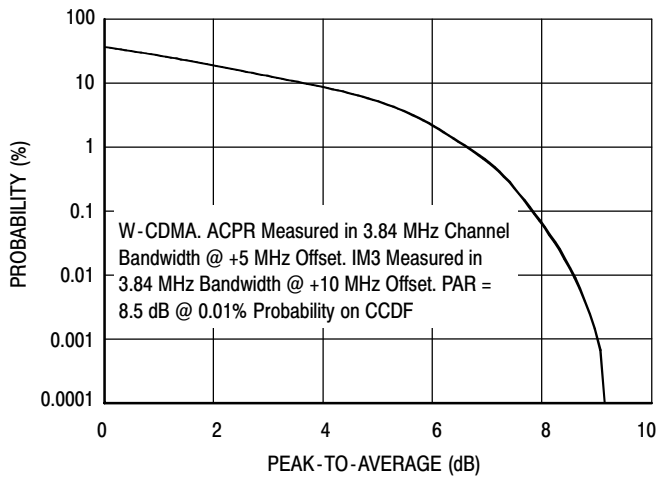
## TYPICAL CHARACTERISTICS



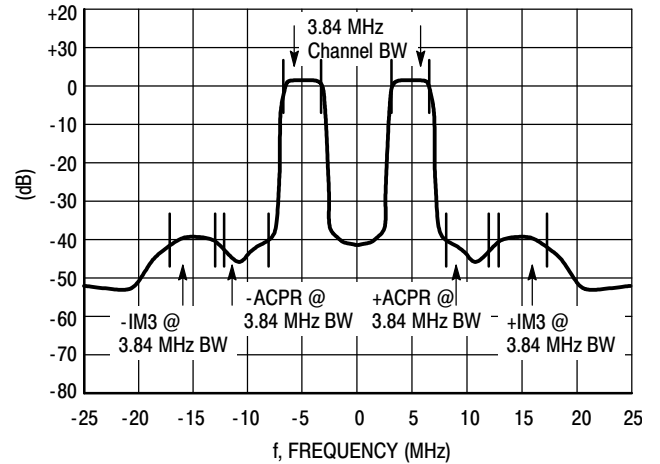
This above graph displays calculated MTTF in hours x ampere<sup>2</sup> drain current. Life tests at elevated temperatures have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTTF factor by  $I_D^2$  for MTTF in a particular application.

**Figure 12. MTTF Factor versus Junction Temperature**

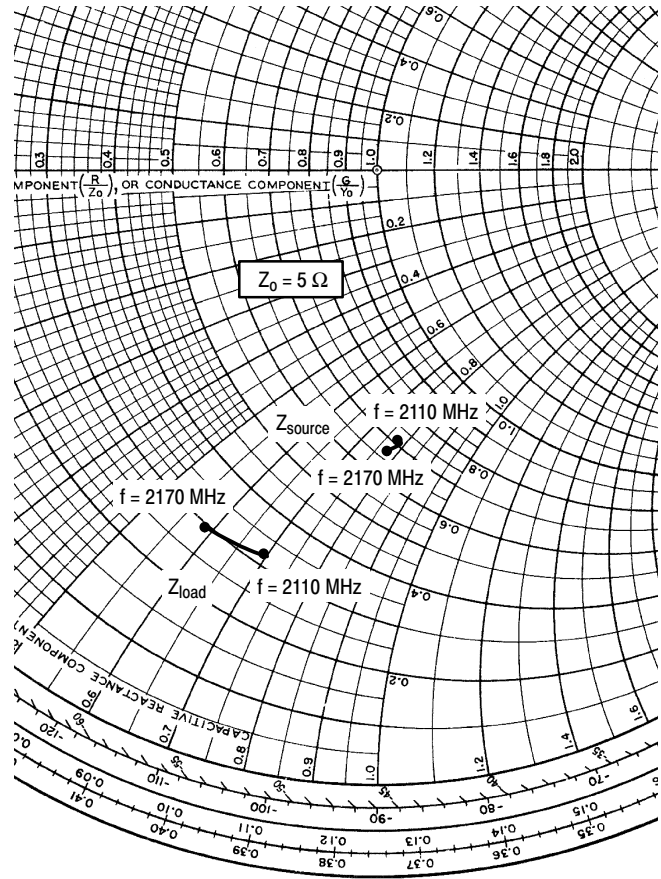
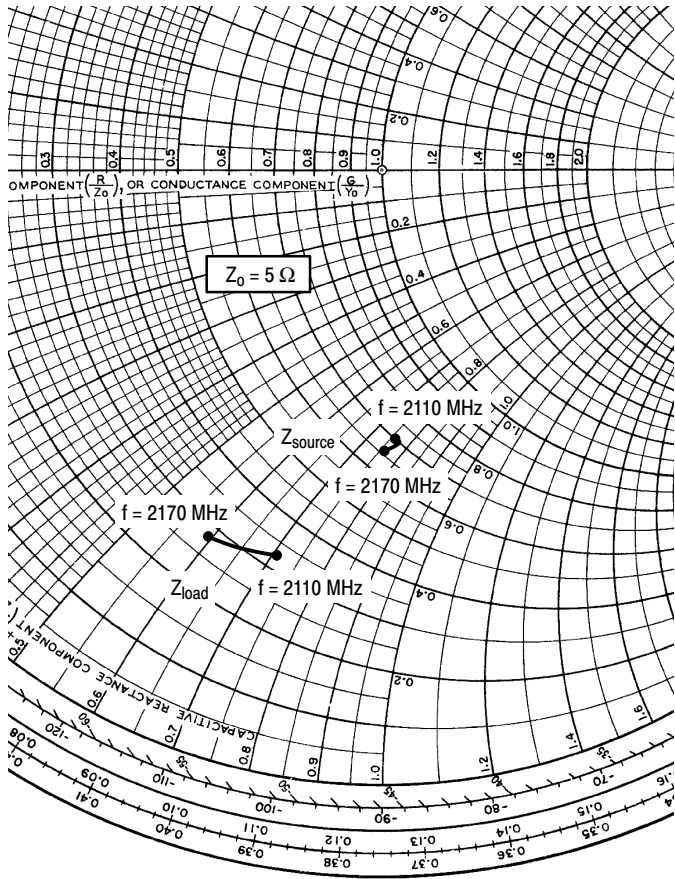
## W-CDMA TEST SIGNAL



**Figure 13. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 67% Clipping, Single-Carrier Test Signal**



**Figure 14. 2-Carrier W-CDMA Spectrum**



MRF6S21100NR1

$V_{DD} = 28$  Vdc,  $I_{DQ} = 1050$  mA,  $P_{out} = 23$  W Avg.

f MHz	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
2110	3.51 - j3.78	1.62 - j3.54
2140	3.50 - j3.83	1.51 - j3.26
2170	3.29 - j3.78	1.41 - j2.95

MRF6S21100NBR1

$V_{DD} = 28$  Vdc,  $I_{DQ} = 1050$  mA,  $P_{out} = 23$  W Avg.

f MHz	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
2110	3.56 - j3.92	1.62 - j3.47
2140	3.55 - j3.97	1.53 - j3.19
2170	3.34 - j3.90	1.44 - j2.89

$Z_{source}$  = Test circuit impedance as measured from gate to gate, balanced configuration.

$Z_{load}$  = Test circuit impedance as measured from drain to drain, balanced configuration.

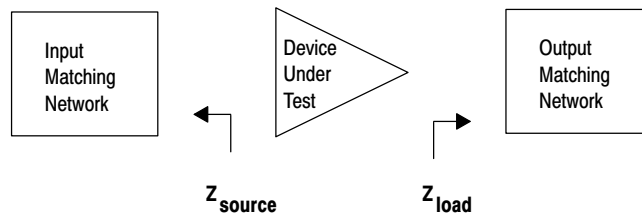


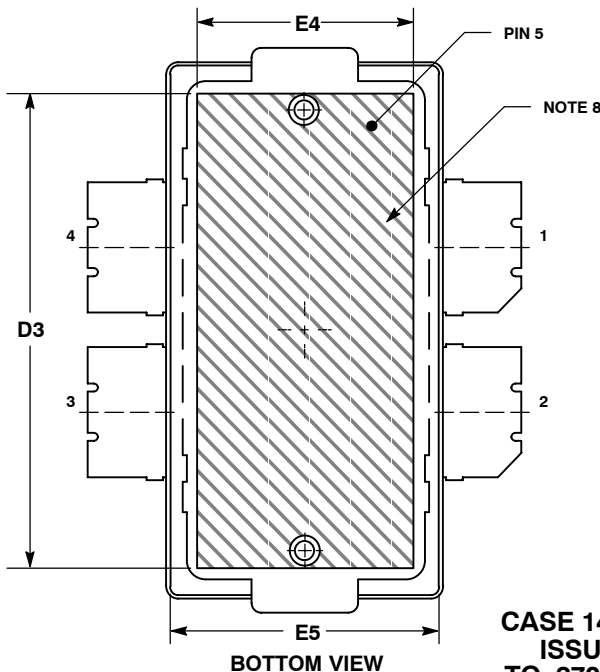
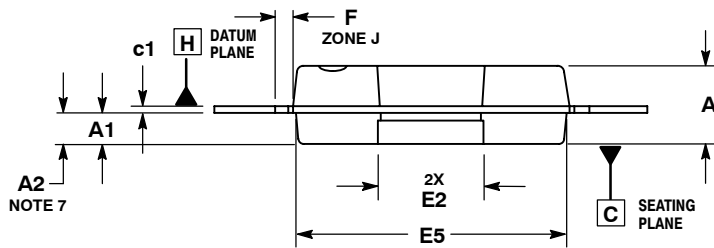
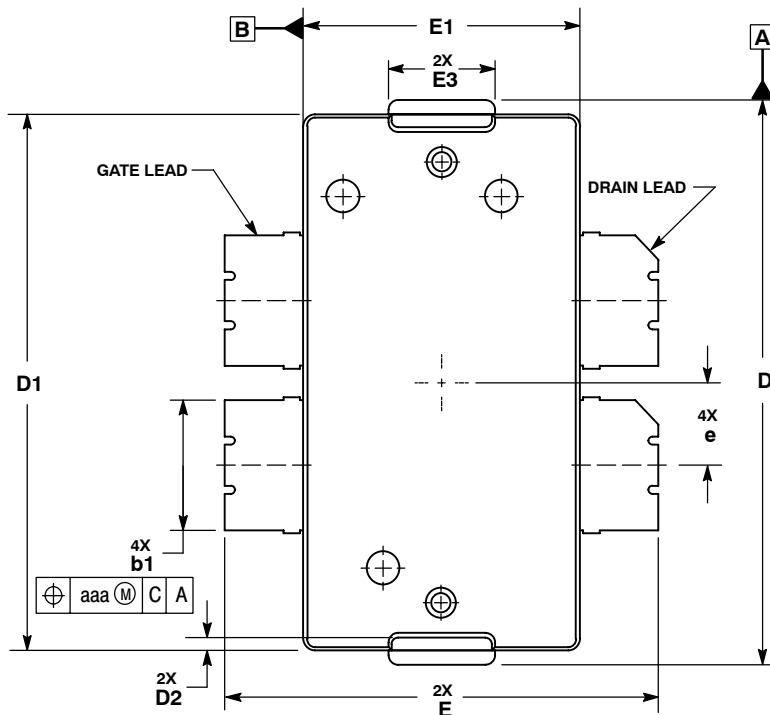
Figure 15. Series Equivalent Source and Load Impedance





## NOTES

## PACKAGE DIMENSIONS



**NOTES:**

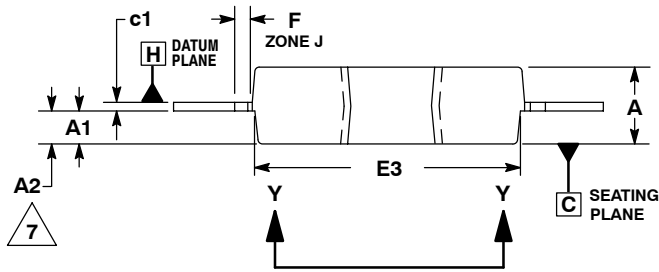
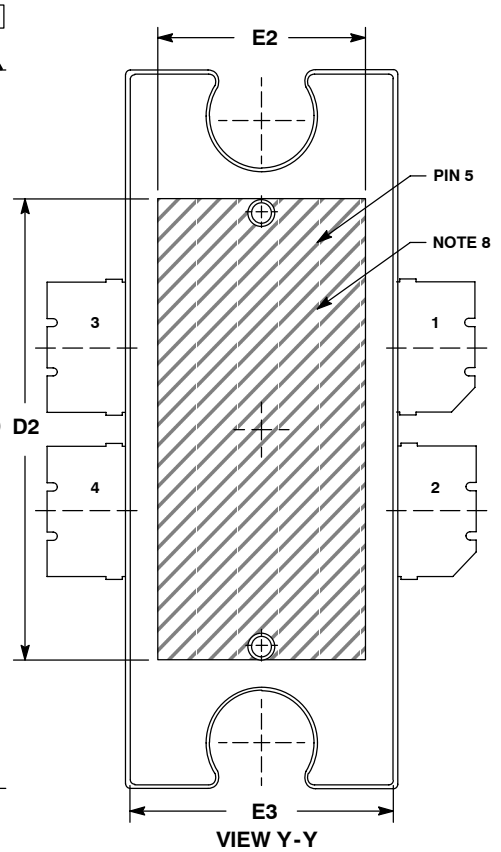
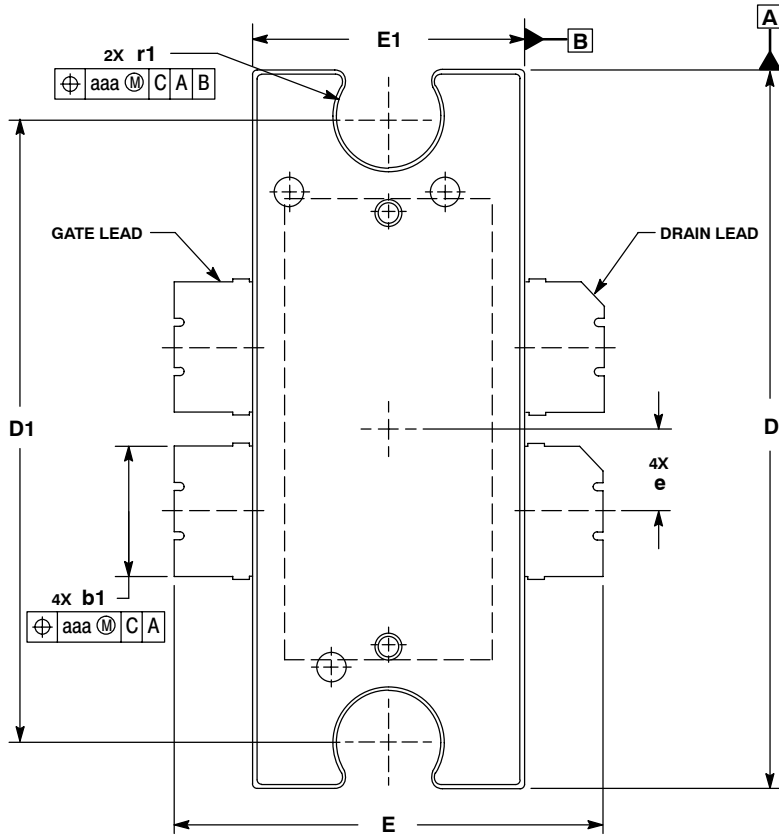
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64
A1	.039	.043	0.99	1.09
A2	.040	.042	1.02	1.07
D	.712	.720	18.08	18.29
D1	.688	.692	17.48	17.58
D2	.011	.019	0.28	0.48
D3	.600	---	15.24	---
E	.551	.559	.14	14.2
E1	.353	.357	8.97	9.07
E2	.132	.140	3.35	3.56
E3	.124	.132	3.15	3.35
E4	.270	---	6.86	---
E5	.346	.350	8.79	8.89
F	.025 BSC		0.64 BSC	
b1	.164	.170	4.17	4.32
c1	.007	.011	0.18	0.28
e	.106 BSC		2.69 BSC	
aaa	.004		0.10	

**STYLE 1:**

- PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

**CASE 1486-03  
ISSUE C  
TO-270 WB-4  
PLASTIC  
MRF6S21100NR1**



- NOTES:
1. CONTROLLING DIMENSION: INCH.
  2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
  3. DATUM PLANE - H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
  4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE - H-.
  5. DIMENSION "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
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  8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64
A1	.039	.043	0.99	1.09
A2	.040	.042	1.02	1.07
D	.928	.932	23.57	23.67
D1	.810 BSC		20.57 BSC	
D2	.600	---	15.24	---
E	.551	.559	14	14.2
E1	.353	.357	8.97	9.07
E2	.270	---	6.86	---
E3	.346	.350	8.79	8.89
F	.025 BSC		0.64 BSC	
b1	.164	.170	4.17	4.32
c1	.007	.011	.18	.28
r1	.063	.068	1.60	1.73
e	.106 BSC		2.69 BSC	
aaa	.004	---	.10	---

- STYLE 1:  
 PIN 1. DRAIN  
 2. DRAIN  
 3. GATE  
 4. GATE  
 5. SOURCE

**CASE 1484-02  
 ISSUE B  
 TO-272 WB-4  
 PLASTIC  
 MRF6S21100NBR1**

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