MC68HC05SR3
MC68HC705SR3

Technical Data

M68HC05 Microcontrollers

MC68HC05SR3D/H
Rev. 2.1
08/2005

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MC68HC05SR3
MC68HC705SR3

High-density Complementary Metal Oxide Semiconductor (HCMOS) Microcontroller Units

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Register and bit mnemonics are defined in the paragraphs describing them.

An overbar is used to designate an active-low signal, eg: $\overline{\text{RESET}}$.

Unless otherwise stated, blank cells in a register diagram indicate that the bit is either unused or reserved; shaded cells indicate that the bit is not described in the following paragraphs; ‘u’ is used to indicate an undefined state (on reset).

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1
GENERAL DESCRIPTION

The MC68HC05SR3 HCMOS microcontroller is a member of the M68HC05 family of low-cost single-chip microcontrollers. This 8-bit microcontroller unit (MCU) contains on-chip oscillator, CPU, RAM, ROM, I/O, Timer, and Analog-to-Digital Converter. The MC68HC05SR3 is pin compatible with the MC6805R3 and is provided as a low power upgrade path for MC6805R3 applications. The low power advantage of CMOS is combined with the addition of I/O and port modifications which help eliminate external components in cost sensitive applications.

The MC68HC705SR3 is an EPROM version of the MC68HC05SR3; it is available in windowed and OTP packages. All references to the MC68HC05SR3 apply equally to the MC68HC705SR3, unless otherwise stated. *References specific to the MC68HC705SR3 are italicized in the text and also, for quick reference, they are summarized in Appendix A.*

1.1 Features

- Fully static chip design featuring the industry standard 8-bit M68HC05 core
- Pin compatible with the MC6805R3
- Power saving STOP, WAIT, and SLOW modes
- 3840 bytes of user ROM with security feature in MC68HC05SR3
  3840 bytes of EPROM with security bit in MC68HC705SR3
- 192 bytes of RAM (64 bytes for stack)
- 32 bidirectional I/O lines
- Keyboard interrupts
- 8-bit count-down timer with programmable 7-bit prescaler
- On-chip crystal oscillator, with built-in capacitor for RC option
- Second software programmable external interrupt line ($\overline{\text{IRQ2}}$)
- Direct LED drive capability on all ports
- Programmable 20KΩ pull-up resistors integrated into I/O ports

- Internal 100KΩ pull-up resistors on $\overline{\mathrm{IRQ}}$ and $\overline{\mathrm{RESET}}$ pins
- Four channel 8-bit Analog to Digital Converter
- Low Voltage Reset
- Available in 40-pin PDIP, 42-pin SDIP and 44-pin QFP packages

1.2 Mask Options

The following mask options are available:

- RC or Crystal Oscillator (see Section 2.2). The default is crystal option.
- Power-On Reset delay — Table 1-1 shows available options. The default value is 4096 cycles.

Table 1-1 Power-On Reset Delay Mask Option

Power-On Reset Delay (cycles)
256
512
1024
2048
4096
8192
16384
32768

- Power-On Reset Slow mode. If enabled, the device goes into Slow mode directly upon power-on reset. The bus frequency is 16 times slower than the normal mode. Thus, the power-on reset delay will also be 16 times longer. The default setting is “Slow mode” disabled.

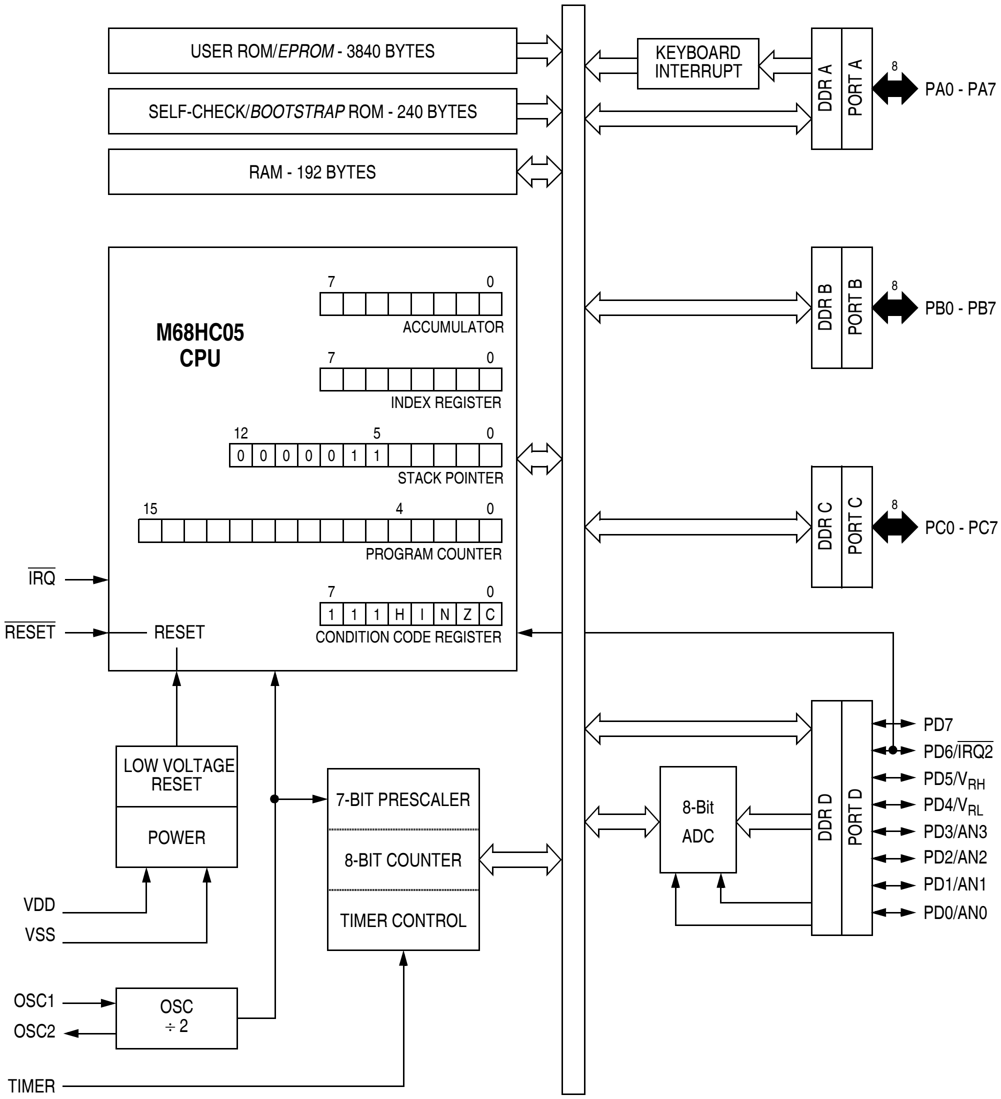

Figure 1-1 MC68HC05SR3/*MC68HC705SR3* Block Diagram

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2
PIN DESCRIPTIONS

This section provides a description of the functional pins of the MC68HC05SR3 microcontroller.

2.1 Functional Pin Descriptions

PIN NAME	40-pin PDIP PIN No.	42-pin SDIP PIN No.	44-pin QFP PIN No.	DESCRIPTION

VDD
VSS
VSS(INT)
VSS(EXT)
	4
	1
	—
	—
		5
		—
		1
		2
			10, 33
			32
			6
			7
				Power is supplied to the MCU using these pins. VDD should be connected to the positive supply. VSS, VSS(INT), and VSS(EXT) should be connected to supply ground.

VPP	*7*	*8*	*13*	*This is the EPROM programming voltage input pin on the MC68HC705SR3. On the MC68HC05SR3 part, this pin should be connected to VDD or VSS.*
$\overline{\text{IRQ}}$	3	4	9	$\overline{\text{IRQ}}$ is software programmable to provide two choices of interrupt triggering sensitivity. These options are: 1) negative-edge-sensitive triggering only, or 2) both negative-edge-sensitive and level-sensitive triggering. This pin has an integrated pull-up resistor to VDD but should be tied to VDD if not needed to improve noise immunity. The $\overline{\text{IRQ}}$ pin contains an internal Schmitt trigger as part of its input to improve noise immunity. The voltage on this pin may affect the mode of operation as described in Section 10.
$\overline{\text{RESET}}$	2	3	8	This pin can be used as an input to reset the MCU to a known start-up state by pulling it to the low state. The $\overline{\text{RESET}}$ pin contains an internal Schmitt trigger to improve its noise immunity as an input. It also has an internal pull-down device that pulls the $\overline{\text{RESET}}$ pin low during the power-on reset cycles and an integrated pull-up resistor to VDD.
TIMER	8	9	14	The TIMER pin provides an optional gating input to the timer. Refer to Section 6 for additional information.
OSC1, OSC2	5, 6	6, 7	11, 12	The OSC1 and OSC2 pins are the connections for the on-chip oscillator. See Section 2.2 for detail.

PIN NAME	40-pin PDIP PIN No.	42-pin SDIP PIN No.	44-pin QFP PIN No.	DESCRIPTION
PA0-PA7	33-40	34-41	42-44, 1-5	These eight I/O lines comprise port A. The state of any pin is software programmable. All port A lines are configured as input during power-on or external reset. PA0-PA7 are also associated with the Keyboard Interrupt function. Each pin is equipped with a programmable integrated 20KΩ pull-up resistor connected to VDD when configured as input. When programmed as output, each pin can provide a current drive of 10mA. See Section 3 for details on the I/O ports.
PB0-PB7	25-32	26-33	31, 35-41	These eight I/O lines comprise port B. The state of any pin is software programmable. All port B lines are configured as input during power-on or external reset. Each pin is equipped with a programmable integrated 20KΩ pull-up resistor connected to VDD when configured as input. When programmed as output, each pin can provide a current drive of 10mA. PB5-PB7 can also be programmed to provide a lower current drive of 2mA. See Section 3 for details on the I/O ports.
PC0-PC7	9-16	10-17	15-22	These eight I/O lines comprise port C. The state of any pin is software programmable. All port C lines are configured as input during power-on or external reset. Each pin is equipped with a programmable integrated 20KΩ pull-up resistor connected to VDD when configured as input. When programmed as output, each pin can provide a current drive of 10mA. See Section 3 for details on the I/O ports.
PD0-PD7 AN0-AN3 $\overline{\text{IRQ2}}$ VRH VRL	24-21, 20-17 24-21 18 19 20	25-22, 21-18 25-22 19 20 21	30-23 30-27 24 25 26	These eight I/O lines comprise port D. The state of any pin is software programmable. All port D lines are configured as input during power-on or external reset. Each pin is equipped with a programmable integrated 20KΩ pull-up resistor connected to VDD when configured as input. When programmed as output, each pin can provide a current drive of 10mA. PD0-PD3 become analog inputs AN0-AN3 when the ADON bit is set in the ADC Status and Control Register ($0E). PD4 and PD5 becomes VRL and VRH respectively for the ADC reference voltage inputs. PD6 is configured as $\overline{\text{IRQ2}}$ by setting IRQ2E in the Miscellaneous Control Register ($0C). See Section 3 for details on the I/O ports.

2.2 OSC1 and OSC2 Connections

The OSC1 and OSC2 pins are the connections for the on-chip oscillator — the following configurations are available:

1) A crystal or ceramic resonator as shown in Figure 2-1(a).

2) An external clock signal as shown in Figure 2-1(b).

3) RC options as shown in Figure 2-1(c) and Figure 2-1(d).

The external oscillator clock frequency, f_{OSC}, is divided by two to produce the internal operating frequency, f_{OP}.

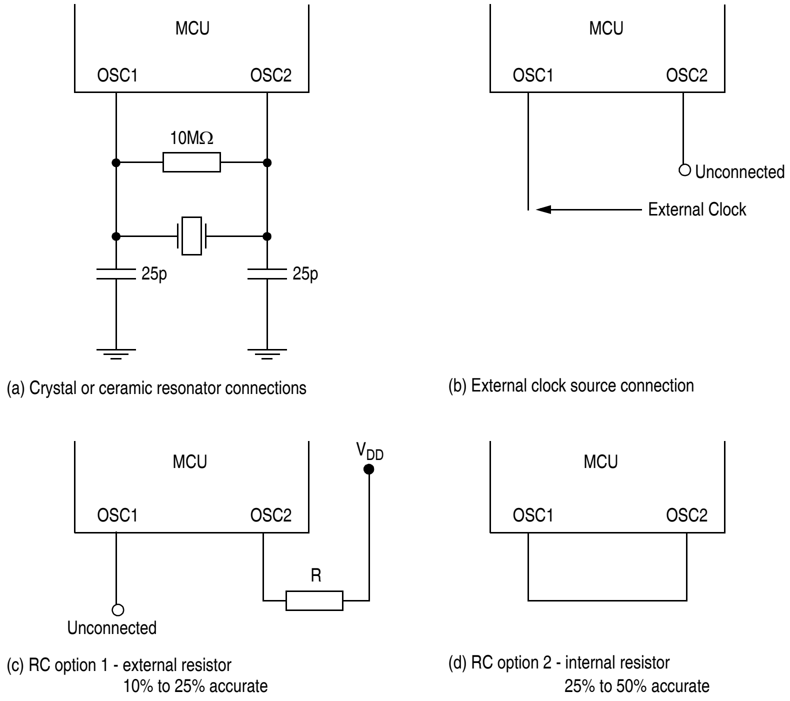
MCU
OSC1
OSC2
10MΩ
25p
25p
(a) Crystal or ceramic resonator connections
MCU
OSC1
OSC2
Unconnected
External Clock
(b) External clock source connection
MCU
OSC1
OSC2
V_{DD}
R
Unconnected
(c) RC option 1 - external resistor
10% to 25% accurate
MCU
OSC1
OSC2
(d) RC option 2 - internal resistor
25% to 50% accurate

Figure 2-1 Oscillator Connections

2.2.1 Crystal Oscillator

The circuit in Figure 2-1(a) shows a typical oscillator circuit for an AT-cut, parallel resonant crystal. The crystal manufacturer’s recommendations should be followed, as the crystal parameters determine the external component values required to provide maximum stability and reliable start-up. The load capacitance values used in the oscillator circuit design should include all stray capacitances. The crystal and components should be mounted as close as possible to the pins for start-up stabilization and to minimize output distortion. An external start-up resistor of approximately 10MΩ is needed between OSC1 and OSC2 for the crystal type oscillator.

2.2.2 External Clock

An external clock from another CMOS-compatible device can be connected to the OSC1 input, with the OSC2 input not connected, as shown in Figure 2-1(b).

2.2.3 RC Oscillator Option

This configuration is intended to be the lowest cost option in applications where oscillator accuracy is not important. An internal constant current source and a capacitor have been integrated on-chip, connected between the OSC2 pin and VSS. Thus by either connecting a resistor to VDD from OSC2 or by putting a wire strap between OSC1 and OSC2 self-oscillations at the frequency as shown in Figure 2-2 and Figure 2-3 can be induced.

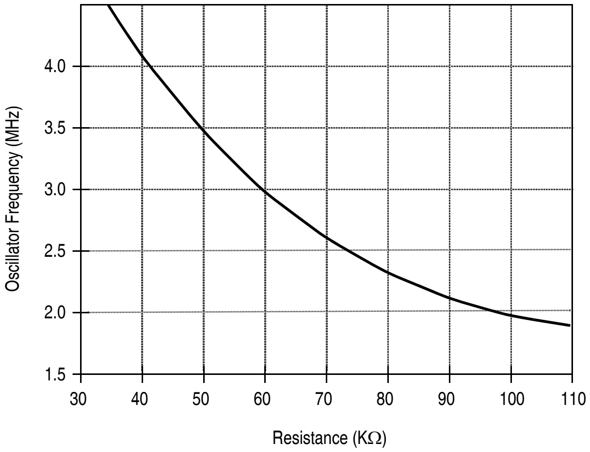

Figure 2-2 Typical Oscillator Frequency for Selected External Resistor

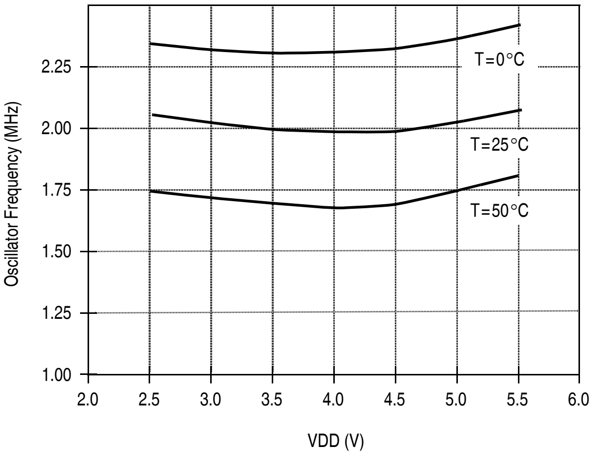

Figure 2-3 Typical Oscillator Frequency for Wire-Strap Connection

2.3 Pin Assignments

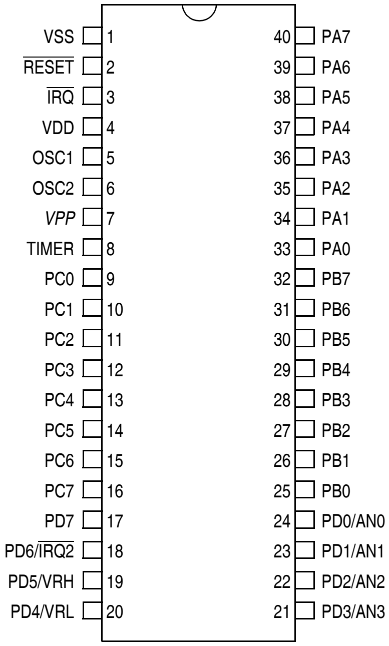

Figure 2-4 Pin Assignment for 40-pin PDIP

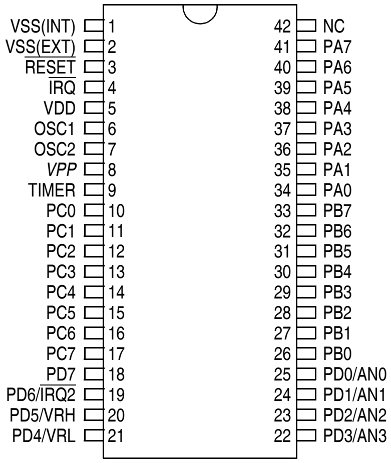

Figure 2-5 Pin Assignment for 42-pin SDIP

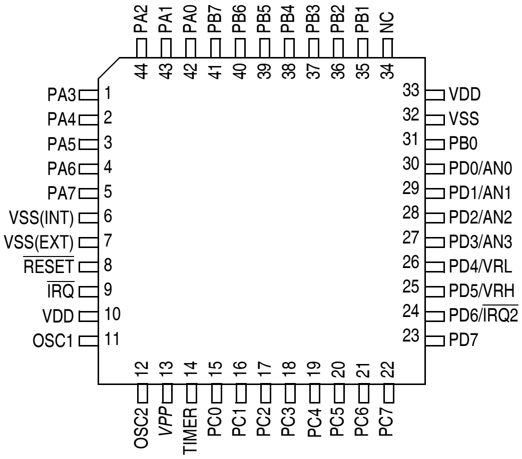

Figure 2-6 Pin Assignment for 44-pin QFP

3
INPUT/OUTPUT PORTS

The MC68HC05SR3 has 32 bidirectional I/O lines, arranged as four 8-bit I/O ports (Port A, B, C, and D). The individual bits in these ports are programmable as either inputs or outputs under software control by the Data Direction Registers (DDRs). All port pins each has an associated 20KΩ pull-up resistor, which can be connected/disconnected under software control. Also, each port pin is capable of sinking and driving a maximum current of 10mA (e.g. direct drive for LEDs). Port A can also be configured for keyboard interrupts.

3.1 Parallel Ports

Port A, B, C, and D are 8-bit bidirectional ports. Each Port pin is controlled by the corresponding bits in a Data Direction Register and a Data Register as shown in Figure 3-1. The functions of the I/O pins are summarized in Table 3-1.

Table 3-1 I/O Pin Functions

$R/\overline{W}$	DDR	I/O Pin Function
0	0	The I/O pin is in input mode. Data is written into the output data latch.
0	1	Data is written into the output data latch and output to the I/O pin.
1	0	The state of the I/O pin is read.
1	1	The I/O pin is in an output mode. The output data latch is read.

3.1.1 Port Data Registers

Each Port I/O pin has a corresponding bit in the Port Data Register. When a Port I/O pin is programmed as an output the state of the corresponding data register bit determines the state of the output pin. All Port I/O pins can drive a current of 10mA when programmed as outputs. When a Port pin is programmed as an input, any read of the Port Data Register will return the logic state of the corresponding I/O pin. The locations of the Data Registers for Port A, B, C, and D are at $00, $01, $02, and $03 respectively. The Port Data Registers are unaffected by reset.

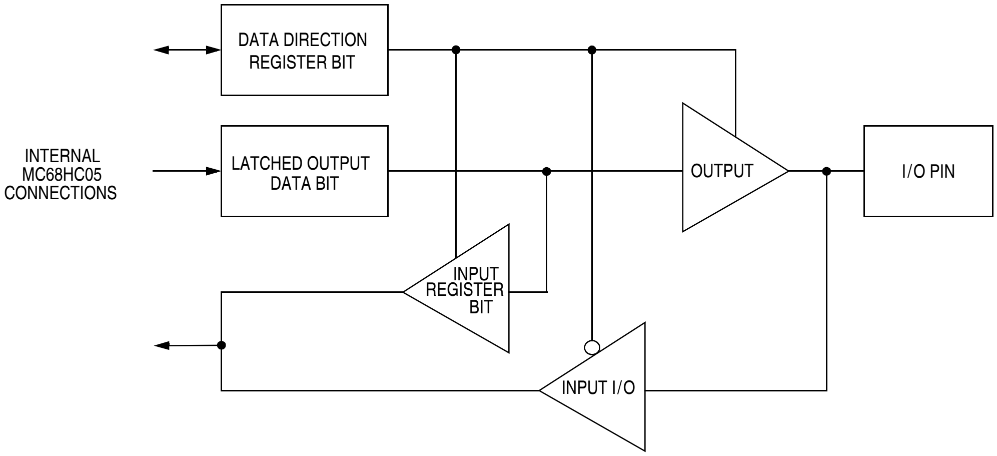

Figure 3-1 Port I/O Circuitry

3.1.2 Port Data Direction Registers

Each port pin may be programmed as an input by clearing the corresponding bit in the DDR, or programmed as an output by setting the corresponding bit in the DDR. The DDR for Port A, B, C, and D are located at $04, $05, $06 and, $07 respectively. The DDRs are cleared by reset.

Note: A “glitch” may occur on an I/O pin when selecting from an input to an output unless the data register is first preconditioned to the desired state before changing the corresponding DDR bit from a “0” to a “1”.

3.2 Port A — Keyboard Interrupts (KBI)

Port A is configured for use as keyboard interrupts when the KBIE bit is set in the Miscellaneous Control Register (MCR). Individual keyboard interrupt port pins are also maskable by setting corresponding bits in the Keyboard Interrupt Mask Register.

See Section 5.2.2.4 for details on the keyboard interrupts.

3.3 PD0:PD5 — ADC Inputs

When the ADON bit is set in the ADC Status and Control Register, PD0 to PD3 are configured as ADC inputs AN0 to AN3 respectively. PD4 and PD5 are configured as V_{RL} and V_{RH} respectively.

See Section 7 for details on the Analog to Digital Converter.

3.4 PD6 — $\overline{\text{IRQ2}}$

The port pin PD6 is configured as $\overline{\text{IRQ2}}$ by setting the IRQ2E bit in the MCR. The external interrupt $\overline{\text{IRQ2}}$ behaves similar to $\overline{\text{IRQ}}$ except it is edge-triggered only.

See Section 5.2.2.2 for details on the external interrupt $\overline{\text{IRQ2}}$.

3.5 Programmable Current Drive

All I/O ports, when programmed as outputs, can source or sink a current of 10mA for driving LEDs directly. By setting the PIL bit in the Port Option Register (at $0A), PB5-PB7 can be programmed to a low-current mode that source or sink only a current of 2mA when programmed as output. This allows a direct drive to low current LEDs.

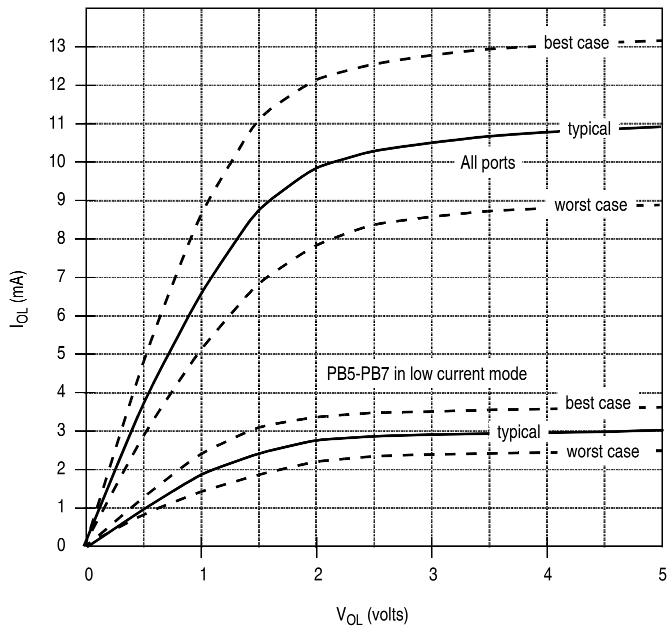

Figure 3-2 Typical I_{OL} vs V_{OL} @V_{DD}=5V

Note: Although the ports each has high current drive capability, designs should limit the total port currents to not more than 100mA.

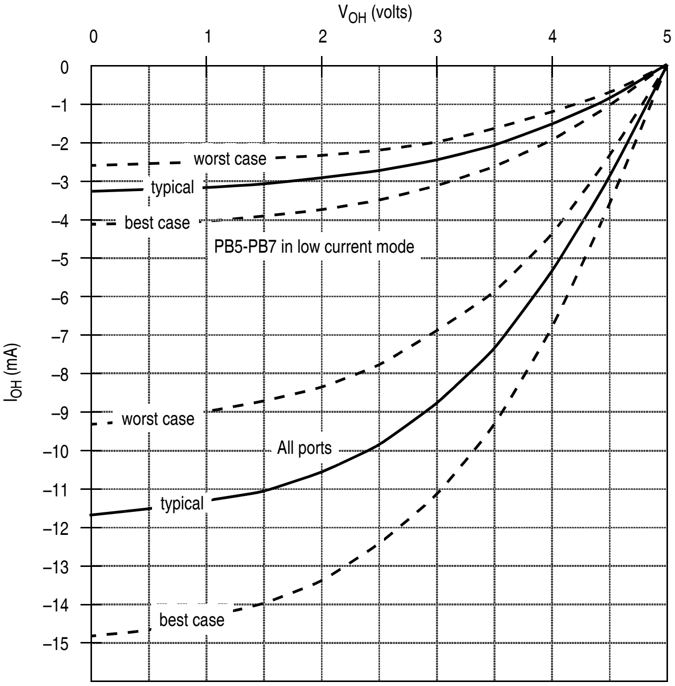

Figure 3-3 Typical I_{OH} vs V_{OH} @V_{DD}=5V

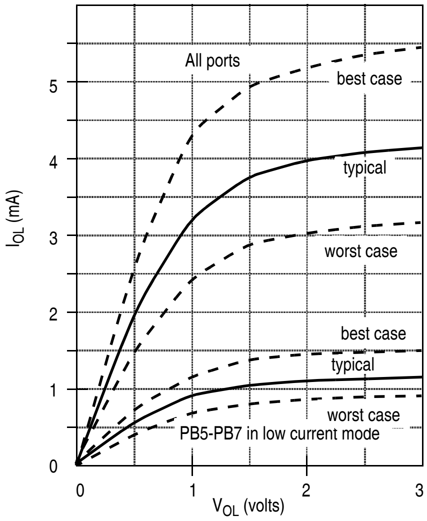

Figure 3-4 Typical I_{OL} vs V_{OL} @V_{DD}=3V

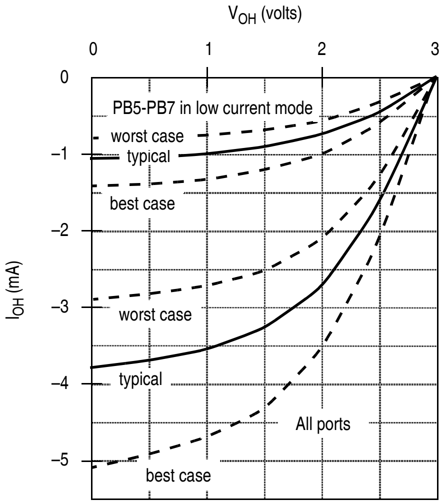

Figure 3-5 Typical I_{OL} vs V_{OL} @V_{DD}=3V

3.6 Programmable Pull-Up Devices

Ports B, C, and D have 20KΩ pull-up resistors, which can be connected or disconnected, by setting appropriate bits in the Port Option Register (at $0A).

3.6.1 Port Option Register

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port Option Register (POPR)	$0A			PIL	PDP	PCP	PBP	PB1	PB0	0000 0000

PIL — PB5:PB7 current drive select

1 (set) – PB5-PB7 are configured to 2mA drive port.

0 (clear) – PB5-PB7 are configured to 10mA drive port.

PDP — Port D Pull-up

1 (set) – The internal 20KΩ pull-up resistors are connected to the inputs of Port D.

0 (clear) – No pull-up resistor is connected to the inputs of Port D.

PCP — Port C Pull-up

1 (set) – The internal 20KΩ pull-up resistors are connected to the inputs of Port C.

0 (clear) – No pull-up resistor is connected to the inputs of Port C.

PBP — PB2:PB7 Pull-up

1 (set) – The internal 20KΩ pull-up resistors are connected to the inputs of PB2-PB7.

0 (clear) – No pull-up resistor is connected to the inputs of PB2-PB7.

PB1 — PB1 pull-up

1 (set) – The internal 20KΩ pull-up resistor is connected to the input of PB1.

0 (clear) – No pull-up resistor is connected to the input of PB1.

PB0 — PB0 pull-up

1 (set) – The internal 20KΩ pull-up resistor is connected to the input of PB0.

0 (clear) – No pull-up resistor is connected to the input of PB0.

4

MEMORY AND REGISTERS

The MC68HC05SR3/*MC68HC705SR3* has 8K-bytes of addressable memory, consisting of I/O registers, user ROM/*EPROM*, user RAM, and self-check/*bootstrap ROM*. Figure 4-1 shows the memory map for MC68HC05SR3/*MC68HC705SR3* device.

4.1 I/O Registers

The I/O, status and control registers are located within the first 16 bytes of memory, from $0000 to $000F. These are shown in the memory map in Figure 4-1; and a summary of the register outline is shown in Table 4-1. Reading from unimplemented bits will return unknown states, and writing to unimplemented bits will be ignored.

4.2 RAM

The user RAM (including the stack) consists of 192 bytes. It is separated into two blocks at locations $0010 to $008F, and $00C0 to $00FF. The stack begins at address $00FF and proceeds down to $00C0.

4.3 ROM

The user ROM consists of 3840 bytes of memory, from $1000 to $1EFF. Twelve bytes of user vectors are also available, from $1FF4 to $1FFF. *On the MC68HC705SR3, this ROM is replaced by EPROM.*

Note: Using the stack area for data storage or temporary work locations requires care to prevent the data from being overwritten due to stacking from an interrupt or subroutine call.

4.4 Memory Map

Figure 4-1 shows the memory map for MC68HC05SR3/*MC68HC705SR3* device.

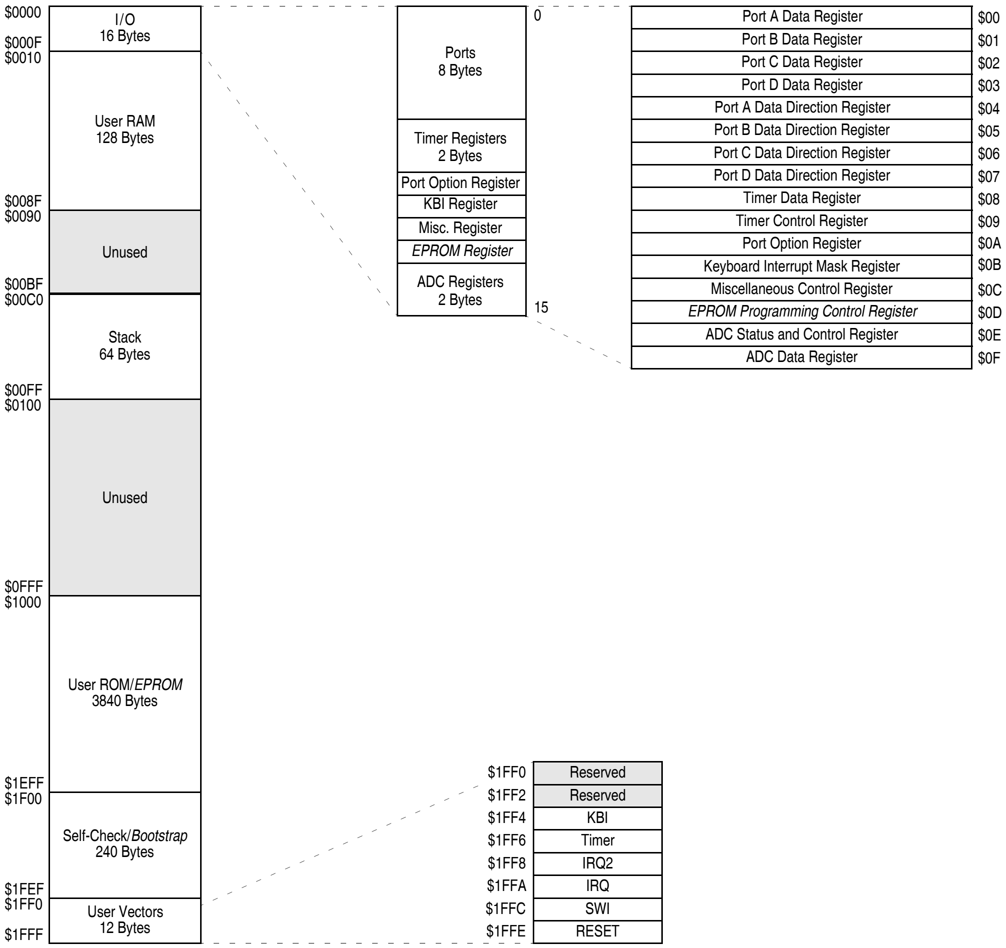

Figure 4-1 MC68HC05SR3/*MC68HC705SR3* Memory Map

4.5 I/O Registers Summary

Table 4-1 shows a summary of I/O registers for MC68HC05SR3/*MC68HC705SR3* device.

Table 4-1 MC68HC05SR3/*MC68HC705SR3* I/O Registers

Register Name	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Port A Data	$00	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	unaffected
Port B Data	$01	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	unaffected
Port C Data	$02	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	unaffected
Port D Data	$03	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	unaffected
Port A Data Direction	$04	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0	0000 0000
Port B Data Direction	$05	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0	0000 0000
Port C Data Direction	$06	DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0	0000 0000
Port D Data Direction	$07	DDRD7	DDRD6	DDRD5	DDRD4	DDRD3	DDRD2	DDRD1	DDRD0	0000 0000
Timer Data (TDR)	$08	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0	1111 1111
Timer Control (TCR)	$09	TIF	TIM	TCEX	TINE	PRER	PR2	PR1	PR0	0100 -000
Port Option (POPR)	$0A			PIL	PDP	PCP	PBP	PB1	PB0	--00 0000
KBI Mask (KBIM)	$0B	KBE7	KBE6	KBE5	KBE4	KBE3	KBE2	KBE1	KBE0	0000 0000
Miscellaneous Control (MCR)	$0C	KBIE	KBIC	INTO	INTE	LVRE	SM	IRQ2F	IRQ2E	0001 0000
EPROM Programming Control	*$0D*							*ELAT*	*PGM*	*---- --00*
ADC Status and Control (ADSCR)	$0E	COCO	ADRC	ADON			CH2	CH1	CH0	000- -000
ADC Data (ADDR)	$0F	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	uuuu uuuu

Mask Option (MOR)	*$0FFF*			*SMD*	*SEC*	*TMR2*	*TMR1*	*TMR0*	*RC*	*unaffected*

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5
RESETS AND INTERRUPTS

This section describes the reset and interrupt functions on the MCU.

5.1 RESETS

The MC68HC05SR3 can be reset in three ways:

- by initial power-on reset function, (POR),
- by an active low input to the $\overline{\text{RESET}}$ pin, ($\overline{\text{RESET}}$), and
- by a Low Voltage Reset, (LVR).

All of these resets will cause the program to go to the starting address, specified by the contents of memory locations $1FFE and $1FFF, and cause the interrupt mask (I-bit) of the Condition Code Register (CCR) to be set.

5.1.1 Power-On Reset (POR)

The power-on reset (POR) occurs on power-up to allow the clock oscillator to stabilize. The POR is strictly for power-up conditions, and should not be used to detect any drops in power supply voltage.

There is an oscillator stabilization delay of t_{PORL} internal processor bus clock cycles after the oscillator becomes active. The $\overline{\text{RESET}}$ pin will be pulled down internally during these cycles. If the $\overline{\text{RESET}}$ pin is low (by external circuit) at the end of the t_{PORL} period, the processor remains in the reset condition until $\overline{\text{RESET}}$ goes high.

5.1.2 $\overline{\text{RESET}}$ Pin

The $\overline{\text{RESET}}$ input pin is used to reset the MCU to provide an orderly software start-up procedure. When using the external reset, the $\overline{\text{RESET}}$ pin must stay low for a minimum of $1.5t_{CYC}$. The $\overline{\text{RESET}}$ pin is connected to a Schmitt Trigger circuit as part of its input to improve noise immunity.

5.1.3 Low Voltage Reset (LVR)

When the LVR function is enabled, an internal reset is generated if the supply voltage, V_{DD}, drops below V_{LVR}. (See Section 11 for value of V_{LVR}).

This LVR function is enabled by setting the LVRE bit in the Miscellaneous Control Register.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Miscellaneous Control Register	$0C	KBIE	KBIC	INTO	INTE	LVRE	SM	IRQ2F	IRQ2E	0001 0000

LVRE — Low Voltage Reset Enable

1 (set) – Low Voltage Reset function enabled.

0 (clear) – Low Voltage Reset function disabled.

Note: The LVR function should not be enabled when operating V_{DD}=3V.

5.2 INTERRUPTS

The MC68HC05SR3 MCU can be interrupted by different sources – four maskable hardware interrupt and one non-maskable software interrupt:

- Software Interrupt Instruction (SWI)
- External signal on $\overline{\text{IRQ}}$ pin
- External signal on $\overline{\text{IRQ2}}$ pin
- TImer Overflow
- Keyboard

If the interrupt mask bit (I-bit) in the Condition Code Register (CCR) is set, all maskable interrupts are disabled. Clearing the I-bit enables interrupts.

Interrupts cause the processor to save the register contents on the stack and to set the interrupt mask (I-bit) to prevent additional interrupts. The RTI instruction causes the register contents to be recovered from the stack and normal processing to resume.

Unlike reset, hardware interrupts do not cause the current instruction execution to be halted, but are considered pending until the current instruction is complete. The current instruction is the one already fetched and being operated on. When the current instruction is complete, the processor checks all pending hardware interrupts. If interrupts are not masked (CCR I-bit clear) the processor proceeds with interrupt processing; otherwise, the next instruction is fetched and executed. Table 5-1 shows the relative priority of all the possible interrupt sources. Figure 5-2 shows the interrupt processing flow.

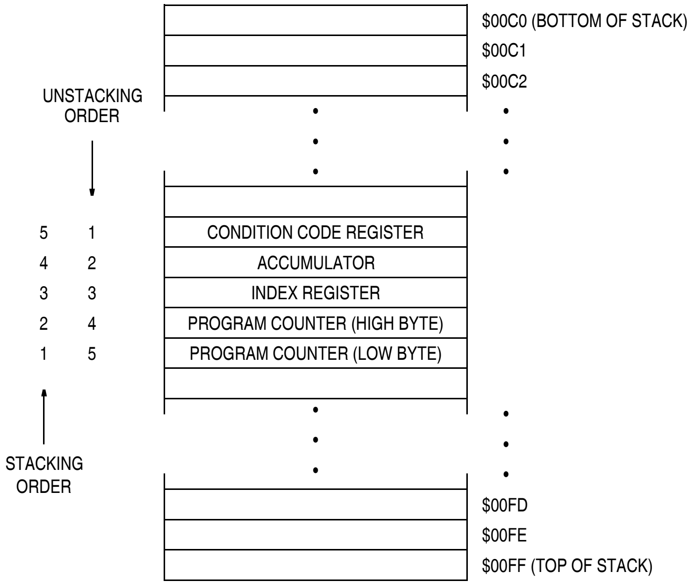


Figure 5-1 Interrupt Stacking Order

Table 5-1 Reset/Interrupt Vector Addresses

Register	Flag Name	Interrupt	CPU Interrupt	Vector Address	Priority
—	—	Reset	$\overline{\text{RESET}}$	$1FFE-$1FFF	highest ↑
—	—	Software	SWI	$1FFC-$1FFD	
—	—	External Interrupt	$\overline{\text{IRQ}}$	$1FFA-$1FFB	
—	—	External Interrupt 2	$\overline{\text{IRQ2}}$	$1FF8-$1FF9	
TCR	TIF	Timer Overflow	TIF	$1FF6-$1FF7	
—	—	Keyboard	KBI	$1FF4-$1FF5	lowest

5.2.1 Non-maskable Software Interrupt (SWI)

The software interrupt (SWI) is an executable instruction and a non-maskable interrupt: it is execute regardless of the state of the I-bit in the CCR. If the I-bit is zero (interrupt enabled), SWI is executed after interrupts that were pending when the SWI was fetched, but before interrupts generated after the SWI was fetched. The SWI interrupt service routine address is specified by the contents of memory locations $1FFC and $1FFD.

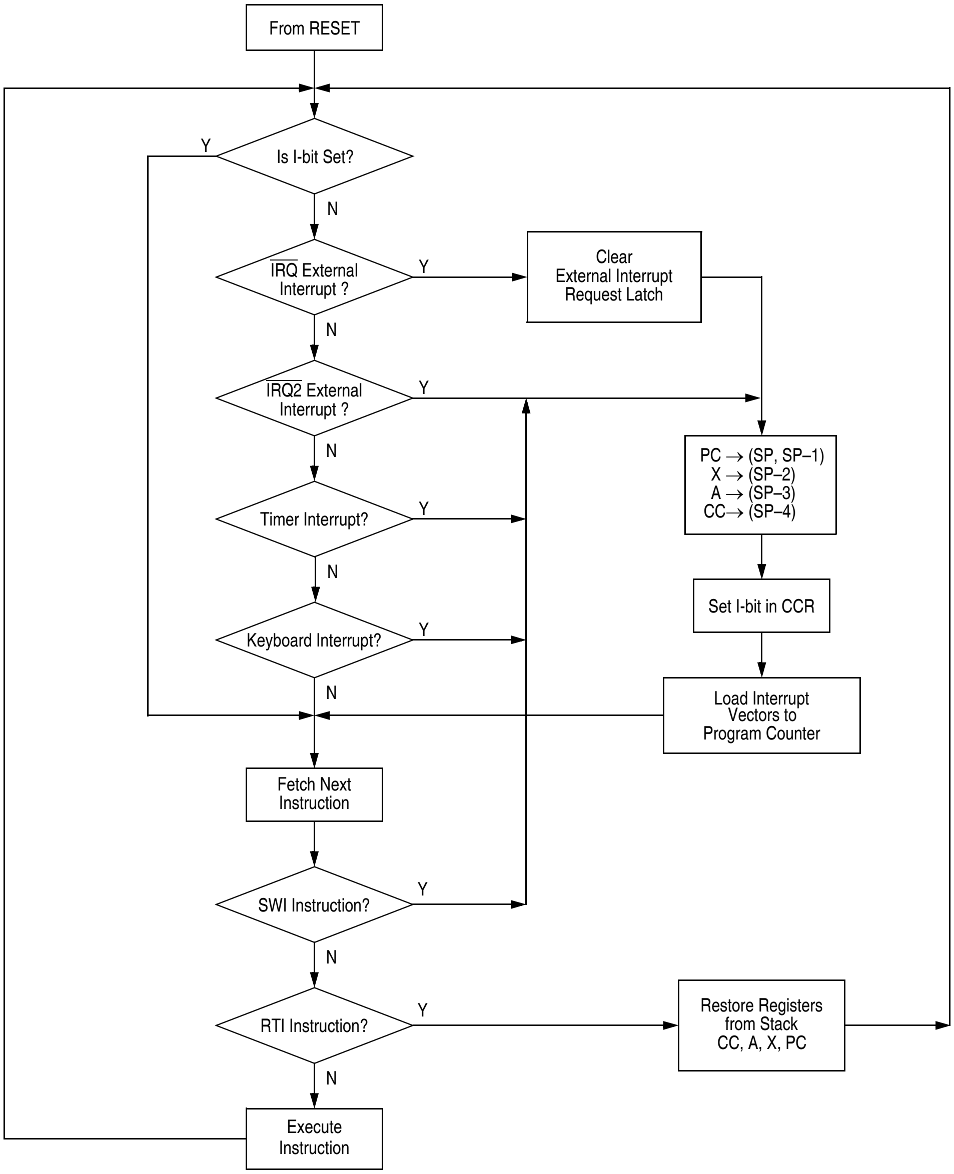


Figure 5-2 Hardware Interrupt Processing Flowchart

5.2.2 Maskable Hardware Interrupts

If the interrupt mask bit (I-bit) of the CCR is set, all maskable interrupts are masked. Clearing the I-bit allows interrupt processing to occur.

Note: The internal interrupt latch is cleared in the first part of the interrupt service routine; therefore, one external interrupt pulse could be latched and serviced as soon as the I-bit is cleared.

5.2.2.1 External Interrupt ($\overline{\text{IRQ}}$)

The external interrupt $\overline{\text{IRQ}}$ is controlled by two bits in the Miscellaneous Control Register ($0C).

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Miscellaneous Control Register	$0C	KBIE	KBIC	INTO	INTE	LVRE	SM	IRQ2F	IRQ2E	0001 0000

INTE — INTerrupt Enable

1 (set) – External interrupt $\overline{\text{IRQ}}$ is enabled.

0 (clear) – External interrupt is disabled.

The external $\overline{\text{IRQ}}$ is default enabled at power-on reset.

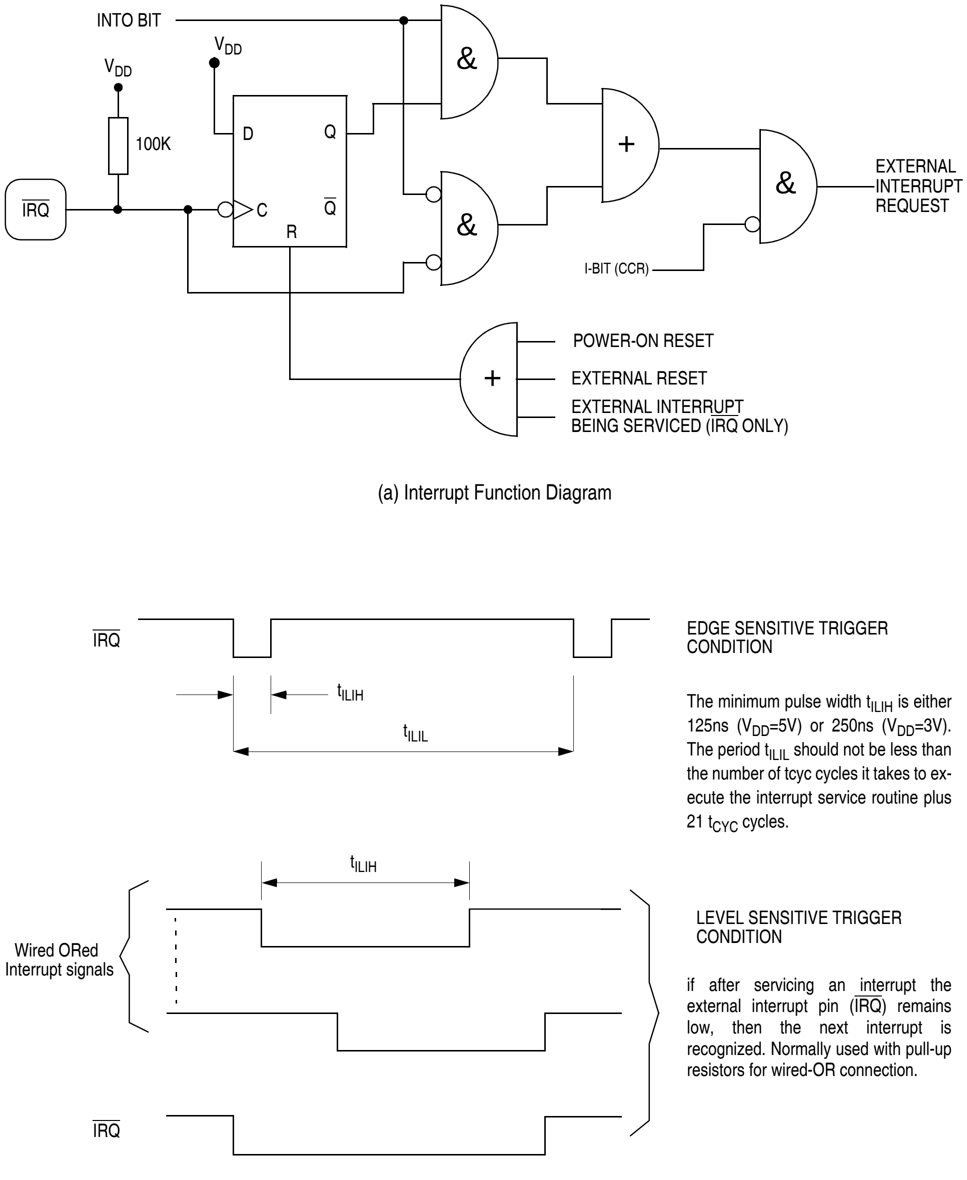
INTO — INTerrupt Option

1 (set) – Negative-edge sensitive triggering for $\overline{\text{IRQ}}$.

0 (clear) – Negative-level sensitive triggering for $\overline{\text{IRQ}}$.

When the signal of the external interrupt pin, $\overline{\text{IRQ}}$, satisfies the condition selected, an external interrupt occurs. The actual processor interrupt is generated only if the interrupt mask bit of the condition code register is also cleared. When the interrupt is recognized, the current state of the processor is pushed onto the stack and the interrupt mask bit in the Condition Code Register is set. This masks further interrupts until the present one is serviced. The service routine address is specified by the contents in $1FFA-$1FFB.

The interrupt logic recognizes negative edge transitions and pulses (special case of negative edges) on the external interrupt line. Figure 5-3 shows both a block diagram and timing for the interrupt line ($\overline{\text{IRQ}}$) to the processor. The first method is used if pulses on the interrupt line are spaced far enough apart to be serviced. The minimum time between pulses is equal to the number of cycles required to execute the interrupt service routine plus 21 cycles. Once a pulse occurs, the next pulse should not occur until the MCU software has exited the routine (an RTI occurs). The second configuration shows several interrupt lines wired-OR to perform the interrupt at the processor. Thus, if the interrupt lines remain low after servicing one interrupt, the next interrupt is recognized.



(a) Interrupt Function Diagram

EDGE SENSITIVE TRIGGER CONDITION

The minimum pulse width t_{ILIH} is either 125ns (V_{DD}=5V) or 250ns (V_{DD}=3V). The period t_{ILIL} should not be less than the number of tcyc cycles it takes to execute the interrupt service routine plus 21 t_{CYC} cycles.

LEVEL SENSITIVE TRIGGER CONDITION

if after servicing an interrupt the external interrupt pin ($\overline{IRQ}$) remains low, then the next interrupt is recognized. Normally used with pull-up resistors for wired-OR connection.

(b) Interrupt Mode Diagram

Figure 5-3 External Interrupt

5.2.2.2 External Interrupt 2 ($\overline{\text{IRQ2}}$)

The port pin PD6 is configured as $\overline{\text{IRQ2}}$ by setting the IRQ2E bit in the MCR. The external interrupt $\overline{\text{IRQ2}}$ behaves similar to $\overline{\text{IRQ}}$ except it is edge-triggered only.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Miscellaneous Control Register	$0C	KBIE	KBIC	INTO	INTE	LVRE	SM	IRQ2F	IRQ2E	0001 0000

IRQ2E — $\overline{\text{IRQ2}}$ Enable

1 (set) – External interrupt $\overline{\text{IRQ2}}$ is enabled.

0 (clear) – External interrupt $\overline{\text{IRQ2}}$ is disabled.

IRQ2F — $\overline{\text{IRQ2}}$ Flag clear

This is a write-only bit and always read as “0”.

1 (set) – Writing a “1” clears the $\overline{\text{IRQ2}}$ interrupt latch.

0 (clear) – Writing a “0” has no effect.

When a negative-edge is sensed on $\overline{\text{IRQ2}}$ pin, an external interrupt occurs. The actual processor interrupt is generated only if the I-bit in the CCR is also cleared. When the interrupt is recognized, the current state of the processor is pushed onto the stack and the I-bit in the CCR is set. This masks further interrupts until the present one is serviced. The latch for IRQ2 is cleared by reset or by writing a “1” to the IRQ2F bit in the MCR in the interrupt service routine. The interrupt service routine address is specified by the contents in $1FF8-$1FF9.

5.2.2.3 Timer Interrupt

The timer interrupt is generated by the 8-bit timer when a timer overflow has occurred. The interrupt enable and flag for the timer interrupt are located in the Timer Control Register.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Timer Control Register (TCR)	$09	TIF	TIM	TCEX	TINE	PREP	PR2	PR1	PR0	0100 -100

TIM — Timer Interrupt Mask

1 (set) – Timer interrupt is disabled.

0 (clear) – Timer interrupt is enabled.

TIF — Timer Interrupt Flag

1 (set) – A timer interrupt (timer overflow) has occurred.

0 (clear) – A timer interrupt (timer overflow) has not occurred.

The I-bit in the CCR must be cleared in order for the timer interrupt to be processed. The interrupt will vector to the interrupt service routine at the address specified by the contents in $1FF6-$0FF7.

5.2.2.4 Keyboard Interrupt (KBI)

Keyboard interrupt function is associated with Port A pins. The keyboard interrupt function is enabled by setting the keyboard interrupt enable bit KBIE (bit 7 of MCR at $0C) and the individual enable bits KBE0-KBE7 (bits 0-7 of KBIM at $0B). When the KBEx bit is set, the corresponding Port A pin will be configured as an input pin, regardless of the DDR setting, and a 20KΩ pull-up resistor is connected to the pin, as shown in Figure 5-4. When a high to low transition is sensed on the pin, a keyboard interrupt will be generated. An interrupt to the CPU will be generated if the I-bit in the CCR is cleared.

The keyboard interrupt flag should be cleared in the interrupt service routine (by writing a “1” to KBIC bit in the MCR at $0C) after the key is debounced. Debouncing will avoid spurious false triggering.

The keyboard interrupt is negative-edge sensitive only, and the interrupt service routine is specified by the contents in $1FF4-$1FF5.

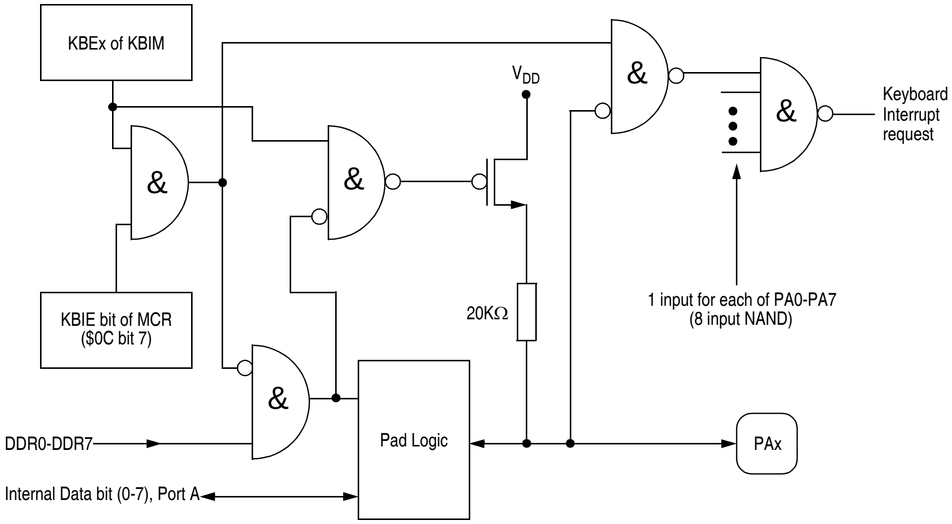

KBEx of KBIM
&
&
&
&
&
V$_{DD}$
Keyboard Interrupt request
1 input for each of PA0-PA7 (8 input NAND)
20KΩ
KBIE bit of MCR ($0C bit 7)
DDR0-DDR7
Pad Logic
PAx
Internal Data bit (0-7), Port A

Figure 5-4 Keyboard Interrupt Circuitry

The KBIE bit in the Miscellaneous Control Register controls the master enable for the keyboard interrupts.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Miscellaneous Control Register	$0C	KBIE	KBIC	INTO	INTE	LVRE	SM	IRQ2F	IRQ2E	0001 0000

KBIE — KeyBoard Interrupt Enable

1 (set) – Keyboard interrupts master enabled.

0 (clear) – Keyboard interrupts master disabled.

KBIC — KeyBoard Interrupt Clear

This is a write-only bit and always read as “0”.

1 (set) – Writing a “1” clears the keyboard interrupt latch.

0 (clear) – Writing a “0” has no effect.

The Keyboard Interrupt Mask Register (KBIMR) masks individual keyboard interrupt pins and setting of the internal pull-up resistors on port A.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
KBIMR	$0B	KBE7	KBE6	KBE5	KBE4	KBE3	KBE2	KBE1	KBE0	0000 0000

KBEx — PAx Keyboard Interrupt Enable

1 (set) – Keyboard interrupt enabled for PAx. A 20KΩ internal pull-up resistor is connected. High to low transition on PAx will cause a keyboard interrupt.

0 (clear) – Keyboard interrupt for PAx pin is masked. Any transitions on PAx will not set any flags.

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6 TIMER

This section describes the operation of the 8-bit count-down timer in the MC68HC05SR3.

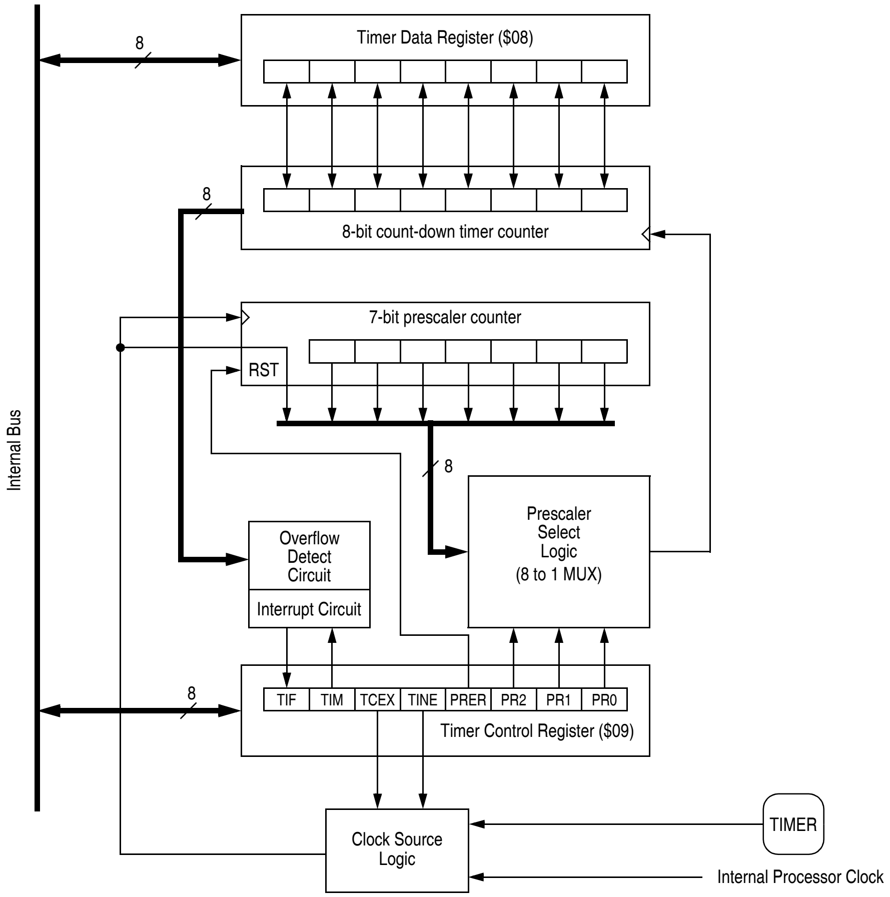
6.1 Timer Overview

The MC68HC05SR3 timer block diagram is shown in Figure 6-1. The timer contains a single 8-bit software programmable count-down counter with a 7-bit software selectable prescaler. The counter may be preset under software control and decrements towards zero. When the counter decrements to zero, the timer interrupt flag (TIF bit in Timer Control Register, TCR) is set. Once timer interrupt flag is set, an interrupt is generated to the CPU only if the TIM bit in the TCR and I-bit in the CCR are cleared. When a interrupt is recognized, after completion of the current instruction, the processor proceeds to store the appropriate registers on the stack and then fetches the timer interrupt vector from locations $1FF6 and $1FF7.

The counter continues to count after it reaches zero, allowing the software to determine the number of internal or external clocks since the timer interrupt flag was set. The counter may be read at any time by the processor without disturbing the count. The contents of the counter become stable prior to the read portion of a cycle and do not change during the read. The timer interrupt flag remains set until cleared by the software. If a write occurs before the timer interrupt is served, the interrupt is lost. The timer interrupt flag may also be used as a scanned status bit in a non-interrupt mode of operation.

The prescaler is a 7-bit divider which is used to extend the maximum length of the timer. Bit 0, 1, 2 (PR0, PR1, PR2) of TCR are programmed to choose the appropriate prescaler output which is used as the 8-bit counter clock input. The processor cannot write into or read from the prescaler; however, its contents can be cleared to all zeros by writing to the PRER bit in the TCR. This will allow for truncation-free counting.

The input clock for the timer sub-system is selectable from internal, external, or a combination of internal and external sources. The TCEX and TINE bits in the Timer Control Register selects the timer input clock.



TCEX	TINE	Clock Source
0	0	Internal clock to timer
0	1	“AND” of internal clock and TIMER pin to timer
1	0	Input clock to timer disabled
1	1	TIMER pin to timer

Figure 6-1 Timer Block Diagram

6.2 Timer Control Register (TCR)

The TCR enables the software to control the operation of the timer.

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
$09	TIF	TIM	TCEX	TINE	PRER	PRE2	PRE1	PRE0	0100 -100

TIF — Timer Interrupt Flag

1 (set) – The timer has reached a count of zero.

0 (clear) – The timer has not reached a count of zero.

The timer interrupt flag is set when the 8-bit counter decrements to zero. This bit is cleared on reset, or by writing a “0” to the TIF bit.

TIM — Timer Interrupt Mask

1 (set) – Timer interrupt request to the CPU is masked (disabled).

0 (clear) – Timer interrupt request to the CPU is not masked (enabled).

A reset sets this bit to one; it must then be cleared by software to enable the timer interrupt to the CPU. This timer interrupt mask only masks timer interrupt request to the CPU, and does not affect counting of the 8-bit counter or the setting of TIF.

TCEX — Timer Clock EXternal
TINE — Timer INput Enable

These two bits selects the source of the timer clock. Reset or power-on clears these bits to zero.

TCEX	TINE	Clock Source
0	0	Internal clock to timer
0	1	“AND” of internal clock and TIMER pin to timer
1	0	Input clock to timer disabled
1	1	TIMER pin to timer

PRER — PREscaler Reset

Writing a “1” to this write-only bit will reset the prescaler to zero, which is necessary for any new counts set by writing to the Timer Data Register.This bit always reads as zero, and is not affected by reset.

PR2:PR0

These three bits enable the program to select the division ratio of the prescaler. On reset, these three bits are set to “100”, which corresponds to a division ratio of 16.

PR2	PR1	PR0	Divide Ratio
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

6.3 Timer Data Register (TDR)

The TDR is a read/write register which contains the current value of the 8-bit count-down timer counter when read. Reading this register does not disturb the counter operation.

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
$08	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0	1111 1111

6.4 Operation during Low Power Modes

The timer ceases counting in STOP mode. When STOP mode is exited by an external interrupt ($\overline{\text{IRQ}}$ or $\overline{\text{IRQ2}}$), the internal oscillator will resume its operation, followed by internal processor stabilization delay. The timer is then cleared to zero and resumes its operation. The TIF bit in the TCR will be set. To avoid generating a timer interrupt when exiting STOP mode, it is recommended to set the TIM bit prior entering STOP mode. After exiting STOP mode TIF bit can then be cleared.

The CPU clock halts during the WAIT mode, but the timer remains active. If the interrupts are enabled, the timer interrupt will cause the processor to exit the WAIT mode.

7
ANALOG TO DIGITAL CONVERTER

The analog to digital converter system consists of a single 8-bit successive approximation converter and an 8-channel analog multiplexer. Four of the channels are available for analog inputs, and the other four channels are dedicated to internal test functions. There is one 8-bit ADC Data Register ($0F) and one 8-bit ADC Status and Control register ($0E). The reference supply, V_{RL} and V_{RH} for the converter uses two input pins (shared with PD4 and PD5) instead of the power supply lines, because drops caused by loading in the power supply lines would degrade the accuracy of the analog to digital conversion. An internal RC oscillator is available if the bus speed is low enough to degrade the ADC accuracy. An ADON bit allows the ADC to be switched off to reduce power consumption, which is particularly useful in the Wait mode.

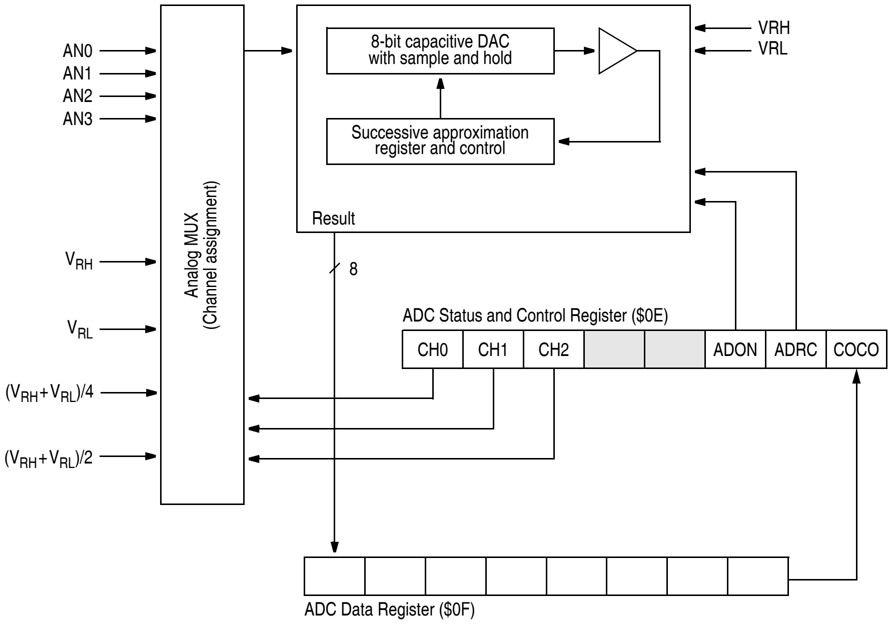


Figure 7-1 ADC Converter Block Diagram

7.1 ADC Operation

As shown in Figure 7-1, the ADC consists of an analog multiplexer, an 8-bit digital to analog capacitor array, a comparator and a successive approximation register (SAR).

There are eight options that can be selected by the multiplexer; the AN0 to AN3 input pins, V_{RH}, V_{RL}, $(V_{RH}+V_{RL})/4$, or $(V_{RH}+V_{RL})/2$. Selection is done via the CHx bits in the ADC Status and Control Register. AN0 to AN3 are input points for ADC conversion operations; the others are reference points which can be used for test purposes. The converter uses V_{RH} and V_{RL} as reference voltages. An input voltage equal to or greater than V_{RH} converts to $FF. An input voltage equal to or less than V_{RL}, but greater than V_{SS}, converts to $00. Maximum and minimum ratings must not be exceeded. Each analog input source should use V_{RH} as the supply voltage and should be referenced to V_{RL} for the ratiometric conversions. To maintain full accuracy of the ADC, the following should be noted:

1) V_{RH} should be equal to or less than V_{CC};
2) V_{RL} should be equal to or greater than V_{SS} but less than maximum specifications; and
3) $V_{RH}–V_{RL}$ should be equal to or greater than 4 Volts.

The ADC reference inputs (V_{RH} and V_{RL}) are applied to a precision internal digital to analog converter. Control logic drives this D/A converter and the analog output is successively compared with the selected analog input sampled at the beginning of the conversion. The conversion is monotonic with no missing codes.

The result of each successive comparison is stored in the successive approximation register (SAR) and, when the conversion is complete, the contents of the SAR are transferred to the read-only ADC Data Register ($0F), and the conversion complete flag, COCO, is set in the ADC Status and Control Register ($0E).

Warning: Any write to the ADC Status and Control Register will abort the current conversion, reset the conversion complete flag (COCO) and a new conversion starts on the selected channel.

At power-on or external reset, both the ADRC and ADON bits are cleared, thus the ADC is disabled.

7.2 ADC Status and Control Register (ADSCR)

The ADSCR is a read/write register containing status and control bits for the ADC.

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
$0E	COCO	ADRC	ADON			CH2	CH1	CH0	000- -000

COCO — COnversion COmplete

1 (set) – An ADC conversion has completed; ADC Data Register ($0F) contains valid conversion result.

0 (clear) – ADC conversion not completed.

This read-only status bit is set when a conversion is completed, indicating that the ADC Data Register contains a valid result. This COCO bit is cleared either by a write to the ADSCR or a read of the ADC Data Register. Once the COCO bit is cleared, a new conversion automatically starts. If the COCO bit is not cleared, conversions are initiated every 32 cycles. In this continuous conversion mode the ADC Data Register is refreshed with new data, every 32 cycles, and the COCO bit remains set.

ADRC — ADC RC Oscillator Control

1 (set) – ADC uses RC oscillator as clock source.

0 (clear) – ADC uses internal processor clock as clock source.

The RC oscillator option must be used if the internal processor is running below 1MHz. A stabilization time of typically 1ms is required when switching to the RC oscillator option.

ADON — ADC On

1 (set) – ADC is switched ON.

0 (clear) – ADC is switched OFF.

When the ADC is turned from OFF to ON, it requires a time t_{ADON} for the current sources to stabilize. During this time ADC conversion results may be inaccurate. Switching the ADC off disables the internal charge pump and RC oscillator (if selected by ADRC=1), and hence saving power.

CH2:CH0 — Channel Select Bits

These three bits selects one of eight ADC channels for the conversion. Channels 0 to 3 correspond to inputs AN0-AN3 on port pins PD0-PD3 respectively. Channels 4 and 5 are the ADC reference inputs V_{RH} and V_{RL}, on port pins PD4 and PD5 respectively. Channels 6 and 7 are used for internal reference points. Table 7-1 shows the signals selected by the channel select bits.

Table 7-1 ADC Channel Assignments

CH2	CH1	CH0	Channel	Selected Signal
0	0	0	0	AD0 on PD0
0	0	1	1	AD1 on PD1
0	1	0	2	AD2 on PD2
0	1	1	3	AD3 on PD3
1	0	0	4	V_{RH}
1	0	1	5	V_{RL}
1	1	0	6	$(V_{RH}-V_{RL}) \div 4$
1	1	1	7	$(V_{RH}-V_{RL}) \div 2$

Using a port D pin as both an analog and digital input simultaneously is prohibited. When the ADC is enabled (ADON=1) and one of channels 0 to 5 is selected, the corresponding Port D pin will appear as a logic zero when read from the Port Data Register.

7.3 ADC Data Register (ADDR)

The ADDR stores the result of a valid ADC conversion when the COCO bits is set in ADSCR.

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
$0F	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	uuuu uuuu

7.4 ADC during Low Power Modes

The ADC continues normal operation in WAIT mode. To reduce power consumption in WAIT mode, the ADON and ADRC bits in the ADSCR should be cleared if the ADC is not used. If the ADC is in use and the internal bus clock is above 1MHz, it is recommended that the ADRC bit be cleared.

In STOP mode, the ADC stops operation.

8

CPU CORE AND INSTRUCTION SET

This section provides a description of the CPU core registers, the instruction set and the addressing modes of the MC68HC05SR3.

8.1 Registers

The MCU contains five registers, as shown in the programming model of Figure 8-1. The interrupt stacking order is shown in Figure 8-2.

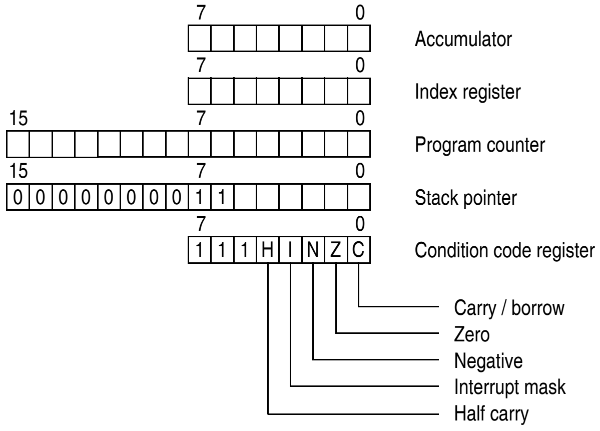


Figure 8-1 Programming model

8.1.1 Accumulator (A)

The accumulator is a general purpose 8-bit register used to hold operands and results of arithmetic calculations or data manipulations.

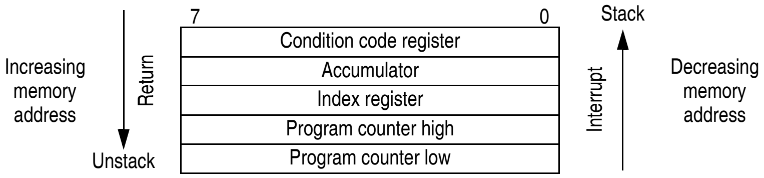


Figure 8-2 Stacking order

8.1.2 Index register (X)

The index register is an 8-bit register, which can contain the indexed addressing value used to create an effective address. The index register may also be used as a temporary storage area.

8.1.3 Program counter (PC)

The program counter is a 16-bit register, which contains the address of the next byte to be fetched.

8.1.4 Stack pointer (SP)

The stack pointer is a 16-bit register, which contains the address of the next free location on the stack. During an MCU reset or the reset stack pointer (RSP) instruction, the stack pointer is set to location $00FF. The stack pointer is then decremented as data is pushed onto the stack and incremented as data is pulled from the stack.

When accessing memory, the ten most significant bits are permanently set to 0000000011. These ten bits are appended to the six least significant register bits to produce an address within the range of $00C0 to $00FF. Subroutines and interrupts may use up to 64 (decimal) locations. If 64 locations are exceeded, the stack pointer wraps around and overwrites the previously stored information. A subroutine call occupies two locations on the stack; an interrupt uses five locations.

8.1.5 Condition code register (CCR)

The CCR is a 5-bit register in which four bits are used to indicate the results of the instruction just executed, and the fifth bit indicates whether interrupts are masked. These bits can be individually tested by a program, and specific actions can be taken as a result of their state. Each bit is explained in the following paragraphs.

Half carry (H)

This bit is set during ADD and ADC operations to indicate that a carry occurred between bits 3 and 4.

Interrupt (I)

When this bit is set, all maskable interrupts are masked. If an interrupt occurs while this bit is set, the interrupt is latched and remains pending until the interrupt bit is cleared.

Negative (N)

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was negative.

Zero (Z)

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was zero.

Carry/borrow (C)

When set, this bit indicates that a carry or borrow out of the arithmetic logical unit (ALU) occurred during the last arithmetic operation. This bit is also affected during bit test and branch instructions and during shifts and rotates.

8.2 Instruction set

The MCU has a set of 62 basic instructions. They can be grouped into five different types as follows:

- Register/memory
- Read/modify/write
- Branch
- Bit manipulation
- Control

The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables.

This MCU uses all the instructions available in the M146805 CMOS family plus one more: the unsigned multiply (MUL) instruction. This instruction allows unsigned multiplication of the contents of the accumulator (A) and the index register (X). The high-order product is then stored in the index register and the low-order product is stored in the accumulator. A detailed definition of the MUL instruction is shown in Table 8-1.

8.2.1 Register/memory Instructions

Most of these instructions use two operands. The first operand is either the accumulator or the index register. The second operand is obtained from memory using one of the addressing modes. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operand. Refer to Table 8-2 for a complete list of register/memory instructions.

8.2.2 Branch instructions

These instructions cause the program to branch if a particular condition is met; otherwise, no operation is performed. Branch instructions are two-byte instructions. Refer to Table 8-3.

8.2.3 Bit manipulation instructions

The MCU can set or clear any writable bit that resides in the first 256 bytes of the memory space (page 0). All port data and data direction registers, timer and serial interface registers, control/status registers and a portion of the on-chip RAM reside in page 0. An additional feature allows the software to test and branch on the state of any bit within these locations. The bit set, bit clear, bit test and branch functions are all implemented with single instructions. For the test and branch instructions, the value of the bit tested is also placed in the carry bit of the condition code register. Refer to Table 8-4.

8.2.4 Read/modify/write instructions

These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. The test for negative or zero (TST) instruction is an exception to this sequence of reading, modifying and writing, since it does not modify the value. Refer to Table 8-5 for a complete list of read/modify/write instructions.

8.2.5 Control instructions

These instructions are register reference instructions and are used to control processor operation during program execution. Refer to Table 8-6 for a complete list of control instructions.

8.2.6 Tables

Tables for all the instruction types listed above follow. In addition there is a complete alphabetical listing of all the instructions (see Table 8-7), and an opcode map for the instruction set of the M68HC05 MCU family (see Table 8-8).

Table 8-1 MUL instruction

Operation	**X:A ← X*A**			
Description	Multiplies the eight bits in the index register by the eight bits in the accumulator and places the 16-bit result in the concatenated accumulator and index register.			
Condition codes	H : Cleared I : Not affected N : Not affected Z : Not affected C : Cleared			
Source	MUL			
Form	Addressing mode	Cycles	Bytes	Opcode
	Inherent	11	1	$42

Table 8-2 Register/memory instructions

		Addressing modes																	
		Immediate			**Direct**			**Extended**			**Indexed (no offset)**			**Indexed (8-bit offset)**			**Indexed (16-bit offset)**		
Function	**Mnemonic**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**
Load A from memory	LDA	A6	2	2	B6	2	3	C6	3	4	F6	1	3	E6	2	4	D6	3	5
Load X from memory	LDX	AE	2	2	BE	2	3	CE	3	4	FE	1	3	EE	2	4	DE	3	5
Store A in memory	STA				B7	2	4	C7	3	5	F7	1	4	E7	2	5	D7	3	6
Store X in memory	STX				BF	2	4	CF	3	5	FF	1	4	EF	2	5	DF	3	6
Add memory to A	ADD	AB	2	2	BB	2	3	CB	3	4	FB	1	3	EB	2	4	DB	3	5
Add memory and carry to A	ADC	A9	2	2	B9	2	3	C9	3	4	F9	1	3	E9	2	4	D9	3	5
Subtract memory	SUB	A0	2	2	B0	2	3	C0	3	4	F0	1	3	E0	2	4	D0	3	5
Subtract memory from A with borrow	SBC	A2	2	2	B2	2	3	C2	3	4	F2	1	3	E2	2	4	D2	3	5
AND memory with A	AND	A4	2	2	B4	2	3	C4	3	4	F4	1	3	E4	2	4	D4	3	5
OR memory with A	ORA	AA	2	2	BA	2	3	CA	3	4	FA	1	3	EA	2	4	DA	3	5
Exclusive OR memory with A	EOR	A8	2	2	B8	2	3	C8	3	4	F8	1	3	E8	2	4	D8	3	5
Arithmetic compare A with memory	CMP	A1	2	2	B1	2	3	C1	3	4	F1	1	3	E1	2	4	D1	3	5
Arithmetic compare X with memory	CPX	A3	2	2	B3	2	3	C3	3	4	F3	1	3	E3	2	4	D3	3	5
Bit test memory with A (logical compare)	BIT	A5	2	2	B5	2	3	C5	3	4	F5	1	3	E5	2	4	D5	3	5
Jump unconditional	JMP				BC	2	2	CC	3	3	FC	1	2	EC	2	3	DC	3	4
Jump to subroutine	JSR				BD	2	5	CD	3	6	FD	1	5	ED	2	6	DD	3	7

Table 8-3 Branch instructions

		Relative addressing mode		
Function	**Mnemonic**	**Opcode**	**# Bytes**	**# Cycles**
Branch always	BRA	20	2	3
Branch never	BRN	21	2	3
Branch if higher	BHI	22	2	3
Branch if lower or same	BLS	23	2	3
Branch if carry clear	BCC	24	2	3
(Branch if higher or same)	(BHS)	24	2	3
Branch if carry set	BCS	25	2	3
(Branch if lower)	(BLO)	25	2	3
Branch if not equal	BNE	26	2	3
Branch if equal	BEQ	27	2	3
Branch if half carry clear	BHCC	28	2	3
Branch if half carry set	BHCS	29	2	3
Branch if plus	BPL	2A	2	3
Branch if minus	BMI	2B	2	3
Branch if interrupt mask bit is clear	BMC	2C	2	3
Branch if interrupt mask bit is set	BMS	2D	2	3
Branch if interrupt line is low	BIL	2E	2	3
Branch if interrupt line is high	BIH	2F	2	3
Branch to subroutine	BSR	AD	2	6

Table 8-4 Bit manipulation instructions

		Addressing modes					
		Bit set/clear			**Bit test and branch**		
Function	**Mnemonic**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**
Branch if bit n is set	BRSET n (n=0–7)				2•n	3	5
Branch if bit n is clear	BRCLR n (n=0–7)				01+2•n	3	5
Set bit n	BSET n (n=0–7)	10+2•n	2	5			
Clear bit n	BCLR n (n=0–7)	11+2•n	2	5			

Table 8-5 Read/modify/write instructions

		Addressing modes														
		Inherent (A)			Inherent (X)			Direct			Indexed (no offset)			Indexed (8-bit offset)		
Function	**Mnemonic**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**	**Opcode**	**# Bytes**	**# Cycles**
Increment	INC	4C	1	3	5C	1	3	3C	2	5	7C	1	5	6C	2	6
Decrement	DEC	4A	1	3	5A	1	3	3A	2	5	7A	1	5	6A	2	6
Clear	CLR	4F	1	3	5F	1	3	3F	2	5	7F	1	5	6F	2	6
Complement	COM	43	1	3	53	1	3	33	2	5	73	1	5	63	2	6
Negate (two’s complement)	NEG	40	1	3	50	1	3	30	2	5	70	1	5	60	2	6
Rotate left through carry	ROL	49	1	3	59	1	3	39	2	5	79	1	5	69	2	6
Rotate right through carry	ROR	46	1	3	56	1	3	36	2	5	76	1	5	66	2	6
Logical shift left	LSL	48	1	3	58	1	3	38	2	5	78	1	5	68	2	6
Logical shift right	LSR	44	1	3	54	1	3	34	2	5	74	1	5	64	2	6
Arithmetic shift right	ASR	47	1	3	57	1	3	37	2	5	77	1	5	67	2	6
Test for negative or zero	TST	4D	1	3	5D	1	3	3D	2	4	7D	1	4	6D	2	5
Multiply	MUL	42	1	11												

Table 8-6 Control instructions

		Inherent addressing mode		
Function	**Mnemonic**	**Opcode**	**# Bytes**	**# Cycles**
Transfer A to X	TAX	97	1	2
Transfer X to A	TXA	9F	1	2
Set carry bit	SEC	99	1	2
Clear carry bit	CLC	98	1	2
Set interrupt mask bit	SEI	9B	1	2
Clear interrupt mask bit	CLI	9A	1	2
Software interrupt	SWI	83	1	10
Return from subroutine	RTS	81	1	6
Return from interrupt	RTI	80	1	9
Reset stack pointer	RSP	9C	1	2
No-operation	NOP	9D	1	2
Stop	STOP	8E	1	2
Wait	WAIT	8F	1	2

Table 8-7 Instruction set

Mnemonic	Addressing modes										Condition codes				
	INH	IMM	DIR	EXT	REL	IX	IX1	IX2	BSC	BTB	H	I	N	Z	C
ADC	▨				▨				▨	▨	◊	•	◊	◊	◊
ADD	▨				▨				▨	▨	◊	•	◊	◊	◊
AND	▨				▨				▨	▨	•	•	◊	◊	•
ASL		▨		▨	▨			▨	▨	▨	•	•	◊	◊	◊
ASR		▨		▨	▨			▨	▨	▨	•	•	◊	◊	◊
BCC	▨	▨	▨	▨		▨	▨	▨	▨	▨	•	•	•	•	•
BCLR	▨	▨	▨	▨	▨	▨	▨	▨		▨	•	•	•	•	•
BCS	▨	▨	▨	▨		▨	▨	▨	▨	▨	•	•	•	•	•
BEQ	▨	▨	▨	▨		▨	▨	▨	▨	▨	•	•	•	•	•
BHCC	▨	▨	▨	▨		▨	▨	▨	▨	▨	•	•	•	•	•
BHCS	▨	▨	▨	▨		▨	▨	▨	▨	▨	•	•	•	•	•
BHI	▨	▨	▨	▨		▨	▨	▨	▨	▨	•	•	•	•	•
BHS	▨	▨	▨	▨		▨	▨	▨	▨	▨	•	•	•	•	•
BIH	▨	▨	▨	▨		▨	▨	▨	▨	▨	•	•	•	•	•
BIL	▨	▨	▨	▨		▨	▨	▨	▨	▨	•	•	•	•	•
BIT	▨				▨				▨	▨	•	•	◊	◊	•
BLO	▨	▨	▨	▨		▨	▨	▨	▨	▨	•	•	•	•	•
BLS	▨	▨	▨	▨		▨	▨	▨	▨	▨	•	•	•	•	•
BMC	▨	▨	▨	▨		▨	▨	▨	▨	▨	•	•	•	•	•
BMI	▨	▨	▨	▨		▨	▨	▨	▨	▨	•	•	•	•	•
BMS	▨	▨	▨	▨		▨	▨	▨	▨	▨	•	•	•	•	•
BNE	▨	▨	▨	▨		▨	▨	▨	▨	▨	•	•	•	•	•
BPL	▨	▨	▨	▨		▨	▨	▨	▨	▨	•	•	•	•	•
BRA	▨	▨	▨	▨		▨	▨	▨	▨	▨	•	•	•	•	•
BRN	▨	▨	▨	▨		▨	▨	▨	▨	▨	•	•	•	•	•
BRCLR	▨	▨	▨	▨	▨	▨	▨	▨	▨		•	•	•	•	◊
BRSET	▨	▨	▨	▨	▨	▨	▨	▨	▨		•	•	•	•	◊
BSET	▨	▨	▨	▨	▨	▨	▨	▨		▨	•	•	•	•	•
BSR	▨	▨	▨	▨		▨	▨	▨	▨	▨	•	•	•	•	•
CLC		▨	▨	▨	▨	▨	▨	▨	▨	▨	•	•	•	•	0
CLI		▨	▨	▨	▨	▨	▨	▨	▨	▨	•	0	•	•	•
CLR		▨		▨	▨			▨	▨	▨	•	•	0	1	•
CMP											•	•	◊	◊	◊

Address mode abbreviations

BSC	Bit set/clear	IMM	Immediate
BTB	Bit test & branch	IX	Indexed (no offset)
DIR	Direct	IX1	Indexed, 1 byte offset
EXT	Extended	IX2	Indexed, 2 byte offset
INH	Inherent	REL	Relative

▨ Not implemented

Condition code symbols

H	Half carry (from bit 3)	◊	Tested and set if true, cleared otherwise
I	Interrupt mask	•	Not affected
N	Negate (sign bit)	?	Load CCR from stack
Z	Zero	0	Cleared
C	Carry/borrow	1	Set

Table 8-7 Instruction set (Continued)

Mnemonic	Addressing modes										Condition codes				
	INH	IMM	DIR	EXT	REL	IX	IX1	IX2	BSC	BTB	H	I	N	Z	C
COM		▨		▨	▨			▨	▨	▨	•	•	◊	◊	1
CPX	▨				▨				▨	▨	•	•	◊	◊	◊
DEC		▨		▨	▨			▨	▨	▨	•	•	◊	◊	•
EOR	▨				▨				▨	▨	•	•	◊	◊	•
INC		▨		▨	▨			▨	▨	▨	•	•	◊	◊	•
JMP	▨	▨			▨				▨	▨	•	•	•	•	•
JSR	▨	▨			▨				▨	▨	•	•	•	•	•
LDA	▨				▨				▨	▨	•	•	◊	◊	•
LDX	▨				▨				▨	▨	•	•	◊	◊	•
LSL		▨		▨	▨			▨	▨	▨	•	•	◊	◊	◊
LSR		▨		▨	▨			▨	▨	▨	•	•	0	◊	◊
MUL		▨	▨	▨	▨	▨	▨	▨	▨	▨	0	•	•	•	0
NEG		▨		▨	▨			▨	▨	▨	•	•	◊	◊	◊
NOP		▨	▨	▨	▨	▨	▨	▨	▨	▨	•	•	•	•	•
ORA	▨				▨				▨	▨	•	•	◊	◊	•
ROL		▨		▨	▨			▨	▨	▨	•	•	◊	◊	◊
ROR		▨		▨	▨			▨	▨	▨	•	•	◊	◊	◊
RSP		▨	▨	▨	▨	▨	▨	▨	▨	▨	•	•	•	•	•
RTI		▨	▨	▨	▨	▨	▨	▨	▨	▨	?	?	?	?	?
RTS		▨	▨	▨	▨	▨	▨	▨	▨	▨	•	•	•	•	•
SBC	▨				▨				▨	▨	•	•	◊	◊	◊
SEC		▨	▨	▨	▨	▨	▨	▨	▨	▨	•	•	•	•	1
SEI		▨	▨	▨	▨	▨	▨	▨	▨	▨	•	1	•	•	•
STA	▨	▨			▨				▨	▨	•	•	◊	◊	•
STOP		▨	▨	▨	▨	▨	▨	▨	▨	▨	•	0	•	•	•
STX	▨	▨			▨				▨	▨	•	•	◊	◊	•
SUB	▨				▨				▨	▨	•	•	◊	◊	◊
SWI		▨	▨	▨	▨	▨	▨	▨	▨	▨	•	1	•	•	•
TAX		▨	▨	▨	▨	▨	▨	▨	▨	▨	•	•	•	•	•
TST		▨		▨	▨			▨	▨	▨	•	•	◊	◊	•
TXA		▨	▨	▨	▨	▨	▨	▨	▨	▨	•	•	•	•	•
WAIT											•	0	•	•	•

Address mode abbreviations

BSC	Bit set/clear	IMM	Immediate
BTB	Bit test & branch	IX	Indexed (no offset)
DIR	Direct	IX1	Indexed, 1 byte offset
EXT	Extended	IX2	Indexed, 2 byte offset
INH	Inherent	REL	Relative

▨ Not implemented

Condition code symbols

H	Half carry (from bit 3)	◊	Tested and set if true, cleared otherwise
I	Interrupt mask	•	Not affected
N	Negate (sign bit)	?	Load CCR from stack
Z	Zero	0	Cleared
C	Carry/borrow	1	Set

Table 8-8 M68HC05 opcode map

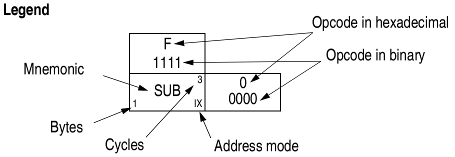
	Bit manipulation		Branch	Read/modify/write					Control		Register/memory						
	BTB	BSC	REL	DIR	INH	INH	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1	IX	
High / Low	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	High / Low
0 0000	5 BRSET0 3 BTB	5 BSET0 2 BSC	3 BRA 2 REL	5 NEG 2 DIR	3 NEGA 1 INH	3 NEGX 1 INH	6 NEG 2 IX1	5 NEG 1 IX	9 RTI 1 INH		2 SUB 2 IMM	3 SUB 2 DIR	4 SUB 3 EXT	5 SUB 3 IX2	4 SUB 2 IX1	3 SUB 1 IX	0 0000
1 0001	5 BRCLR0 3 BTB	5 BCLR0 2 BSC	3 BRN 2 REL						6 RTS 1 INH		2 CMP 2 IMM	3 CMP 2 DIR	4 CMP 3 EXT	5 CMP 3 IX2	4 CMP 2 IX1	3 CMP 1 IX	1 0001
2 0010	5 BRSET1 3 BTB	5 BSET1 2 BSC	3 BHI 2 REL		11 MUL 1 INH						2 SBC 2 IMM	3 SBC 2 DIR	4 SBC 3 EXT	5 SBC 3 IX2	4 SBC 2 IX1	3 SBC 1 IX	2 0010
3 0011	5 BRCLR1 3 BTB	5 BCLR1 2 BSC	3 BLS 2 REL	5 COM 2 DIR	3 COMA 1 INH	3 COMX 1 INH	6 COM 2 IX1	5 COM 1 IX	10 SWI 1 INH		2 CPX 2 IMM	3 CPX 2 DIR	4 CPX 3 EXT	5 CPX 3 IX2	4 CPX 2 IX1	3 CPX 1 IX	3 0011
4 0100	5 BRSET2 3 BTB	5 BSET2 2 BSC	3 BCC 2 REL	5 LSR 2 DIR	3 LSRA 1 INH	3 LSRX 1 INH	6 LSR 2 IX1	5 LSR 1 IX			2 AND 2 IMM	3 AND 2 DIR	4 AND 3 EXT	5 AND 3 IX2	4 AND 2 IX1	3 AND 1 IX	4 0100
5 0101	5 BRCLR2 3 BTB	5 BCLR2 2 BSC	3 BCS 2 REL								2 BIT 2 IMM	3 BIT 2 DIR	4 BIT 3 EXT	5 BIT 3 IX2	4 BIT 2 IX1	3 BIT 1 IX	5 0101
6 0110	5 BRSET3 3 BTB	5 BSET3 2 BSC	3 BNE 2 REL	5 ROR 2 DIR	3 RORA 1 INH	3 RORX 1 INH	6 ROR 2 IX1	5 ROR 1 IX			2 LDA 2 IMM	3 LDA 2 DIR	4 LDA 3 EXT	5 LDA 3 IX2	4 LDA 2 IX1	3 LDA 1 IX	6 0110
7 0111	5 BRCLR3 3 BTB	5 BCLR3 2 BSC	3 BEQ 2 REL	5 ASR 2 DIR	3 ASRA 1 INH	3 ASRX 1 INH	6 ASR 2 IX1	5 ASR 1 IX		2 TAX 1 INH		4 STA 2 DIR	5 STA 3 EXT	6 STA 3 IX2	5 STA 2 IX1	4 STA 1 IX	7 0111
8 1000	5 BRSET4 3 BTB	5 BSET4 2 BSC	3 BHCC 2 REL	5 LSL 2 DIR	3 LSLA 1 INH	3 LSLX 1 INH	6 LSL 2 IX1	5 LSL 1 IX		2 CLC 1 INH	2 EOR 2 IMM	3 EOR 2 DIR	4 EOR 3 EXT	5 EOR 3 IX2	4 EOR 2 IX1	3 EOR 1 IX	8 1000
9 1001	5 BRCLR4 3 BTB	5 BCLR4 2 BSC	3 BHCS 2 REL	5 ROL 2 DIR	3 ROLA 1 INH	3 ROLX 1 INH	6 ROL 2 IX1	5 ROL 1 IX		2 SEC 1 INH	2 ADC 2 IMM	3 ADC 2 DIR	4 ADC 3 EXT	5 ADC 3 IX2	4 ADC 2 IX1	3 ADC 1 IX	9 1001
A 1010	5 BRSET5 3 BTB	5 BSET5 2 BSC	3 BPL 2 REL	5 DEC 2 DIR	3 DECA 1 INH	3 DECX 1 INH	6 DEC 2 IX1	5 DEC 1 IX		2 CLI 1 INH	2 ORA 2 IMM	3 ORA 2 DIR	4 ORA 3 EXT	5 ORA 3 IX2	4 ORA 2 IX1	3 ORA 1 IX	A 1010
B 1011	5 BRCLR5 3 BTB	5 BCLR5 2 BSC	3 BMI 2 REL							2 SEI 1 INH	2 ADD 2 IMM	3 ADD 2 DIR	4 ADD 3 EXT	5 ADD 3 IX2	4 ADD 2 IX1	3 ADD 1 IX	B 1011
C 1100	5 BRSET6 3 BTB	5 BSET6 2 BSC	3 BMC 2 REL	5 INC 2 DIR	3 INCA 1 INH	3 INCX 1 INH	6 INC 2 IX1	5 INC 1 IX		2 RSP 1 INH		2 JMP 2 DIR	3 JMP 3 EXT	4 JMP 3 IX2	3 JMP 2 IX1	2 JMP 1 IX	C 1100
D 1101	5 BRCLR6 3 BTB	5 BCLR6 2 BSC	3 BMS 2 REL	4 TST 2 DIR	3 TSTA 1 INH	3 TSTX 1 INH	5 TST 2 IX1	4 TST 1 IX		2 NOP 1 INH	6 BSR 2 REL	5 JSR 2 DIR	6 JSR 3 EXT	7 JSR 3 IX2	6 JSR 2 IX1	5 JSR 1 IX	D 1101
E 1110	5 BRSET7 3 BTB	5 BSET7 2 BSC	3 BIL 2 REL						2 STOP 1 INH		2 LDX 2 IMM	3 LDX 2 DIR	4 LDX 3 EXT	5 LDX 3 IX2	4 LDX 2 IX1	3 LDX 1 IX	E 1110
F 1111	5 BRCLR7 3 BTB	5 BCLR7 2 BSC	3 BIH 2 REL	5 CLR 2 DIR	3 CLRA 1 INH	3 CLRX 1 INH	6 CLR 2 IX1	5 CLR 1 IX	2 WAIT 1 INH	2 TXA 1 INH		4 STX 2 DIR	5 STX 3 EXT	6 STX 3 IX2	5 STX 2 IX1	4 STX 1 IX	F 1111

Abbreviations for address modes and registers

BSC	Bit set/clear	IX	Indexed (no offset)
BTB	Bit test and branch	IX1	Indexed, 1 byte (8-bit) offset
DIR	Direct	IX2	Indexed, 2 byte (16-bit) offset
EXT	Extended	REL	Relative
INH	Inherent	A	Accumulator
IMM	Immediate	X	Index register

▨ Not implemented

Legend



8.3 Addressing modes

Ten different addressing modes provide programmers with the flexibility to optimize their code for all situations. The various indexed addressing modes make it possible to locate data tables, code conversion tables and scaling tables anywhere in the memory space. Short indexed accesses are single byte instructions; the longest instructions (three bytes) enable access to tables throughout memory. Short absolute (direct) and long absolute (extended) addressing are also included. One or two byte direct addressing instructions access all data bytes in most applications. Extended addressing permits jump instructions to reach all memory locations.

The term ‘effective address’ (EA) is used in describing the various addressing modes. The effective address is defined as the address from which the argument for an instruction is fetched or stored. The ten addressing modes of the processor are described below. Parentheses are used to indicate ‘contents of’ the location or register referred to. For example, (PC) indicates the contents of the location pointed to by the PC (program counter). An arrow indicates ‘is replaced by’ and a colon indicates concatenation of two bytes. For additional details and graphical illustrations, refer to the ***M6805 HMOS/M146805 CMOS Family Microcomputer/ Microprocessor User's Manual*** or to the ***M68HC05 Applications Guide****.*

8.3.1 Inherent

In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index register or accumulator, as well as the control instruction, with no other arguments are included in this mode. These instructions are one byte long.

8.3.2 Immediate

In the immediate addressing mode, the operand is contained in the byte immediately following the opcode. The immediate addressing mode is used to access constants that do not change during program execution (e.g. a constant used to initialize a loop counter).

EA = PC+1; PC ← PC+2

8.3.3 Direct

In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte. Direct addressing allows the user to directly address the lowest 256 bytes in memory with a single two-byte instruction.

EA = (PC+1); PC ← PC+2
Address bus high ← 0; Address bus low ← (PC+1)

8.3.4 Extended

In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode byte. Instructions with extended addressing mode are capable of referencing arguments anywhere in memory with a single three-byte instruction. When using the Freescale assembler, the user need not specify whether an instruction uses direct or extended addressing. The assembler automatically selects the short form of the instruction.

EA = (PC+1):(PC+2); PC ← PC+3
Address bus high ← (PC+1); Address bus low ← (PC+2)

8.3.5 Indexed, no offset

In the indexed, no offset addressing mode, the effective address of the argument is contained in the 8-bit index register. This addressing mode can access the first 256 memory locations. These instructions are only one byte long. This mode is often used to move a pointer through a table or to hold the address of a frequently referenced RAM or I/O location.

EA = X; PC ← PC+1
Address bus high ← 0; Address bus low ← X

8.3.6 Indexed, 8-bit offset

In the indexed, 8-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the unsigned byte following the opcode. Therefore the operand can be located anywhere within the lowest 511 memory locations. This addressing mode is useful for selecting the mth element in an n element table.

EA = X+(PC+1); PC ← PC+2
Address bus high ← K; Address bus low ← X+(PC+1)
where K = the carry from the addition of X and (PC+1)

8.3.7 Indexed, 16-bit offset

In the indexed, 16-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the two unsigned bytes following the opcode. This address mode can be used in a manner similar to indexed, 8-bit offset except that this three-byte instruction allows tables to be anywhere in memory. As with direct and extended addressing, the Freescale assembler determines the shortest form of indexed addressing.

EA = X+[(PC+1):(PC+2)]; PC ← PC+3
Address bus high ← (PC+1)+K; Address bus low ← X+(PC+2)
where K = the carry from the addition of X and (PC+2)

8.3.8 Relative

The relative addressing mode is only used in branch instructions. In relative addressing, the contents of the 8-bit signed byte (the offset) following the opcode are added to the PC if, and only if, the branch conditions are true. Otherwise, control proceeds to the next instruction. The span of relative addressing is from –126 to +129 from the opcode address. The programmer need not calculate the offset when using the Freescale assembler, since it calculates the proper offset and checks to see that it is within the span of the branch.

EA = PC+2+(PC+1); PC ← EA if branch taken;
otherwise EA = PC ← PC+2

8.3.9 Bit set/clear

In the bit set/clear addressing mode, the bit to be set or cleared is part of the opcode. The byte following the opcode specifies the address of the byte in which the specified bit is to be set or cleared. Any read/write bit in the first 256 locations of memory, including I/O, can be selectively set or cleared with a single two-byte instruction.

EA = (PC+1); PC ← PC+2
Address bus high ← 0; Address bus low ← (PC+1)

8.3.10 Bit test and branch

The bit test and branch addressing mode is a combination of direct addressing and relative addressing. The bit to be tested and its condition (set or clear) is included in the opcode. The address of the byte to be tested is in the single byte immediately following the opcode byte (EA1). The signed relative 8-bit offset in the third byte (EA2) is added to the PC if the specified bit is set or cleared in the specified memory location. This single three-byte instruction allows the program to branch based on the condition of any readable bit in the first 256 locations of memory. The span of branch is from –125 to +130 from the opcode address. The state of the tested bit is also transferred to the carry bit of the condition code register.

EA1 = (PC+1); PC ← PC+2
Address bus high ← 0; Address bus low ← (PC+1)
EA2 = PC+3+(PC+2); PC ← EA2 if branch taken;
otherwise PC ← PC+3

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9
LOW POWER MODES

The MC68HC05SR3 has three low-power operating modes. The WAIT and STOP instructions provide two modes that reduce the power required for the MCU by stopping various internal clocks and/or the on-chip oscillator. The flow of the STOP and WAIT modes is shown in Figure 9-1. The third low-power operating mode is the SLOW mode.

9.1 STOP Mode

Execution of the STOP instruction places the MCU in its lowest power consumption mode. In the STOP mode the internal oscillator is turned off, halting all internal processing.

When the CPU enters STOP mode the I-bit in the Condition Code Register is cleared automatically, so that any hardware interrupts ($\overline{\text{IRQ}}$, $\overline{\text{IRQ2}}$ and KBI) can “wake” the MCU. All other registers and memory contents remain unaltered. All input/output lines remain unchanged.

The MCU can be brought out of the STOP mode only by a hardware interrupt or an externally generated reset. When exiting the STOP mode the internal oscillator will resume after a pre-defined number of internal processor clock cycles, due to oscillator stabilization.

9.2 WAIT Mode

The WAIT instruction places the MCU in a low-power mode, but consumes more power than the STOP mode. In the WAIT mode the internal processor clock is halted, suspending all processor and internal bus activities. Other Internal clocks remain active, permitting interrupts to be generated from the Timer. The Timer may be used to generate a periodic exit from the WAIT mode or, in conjunction with the external Timer pin, on the occurrence of external events. Execution of the WAIT instruction automatically clears the I-bit in the Condition Code Register, so that any hardware interrupt can “wake” the MCU. All other registers, memory, and input/output lines remain in their previous states.

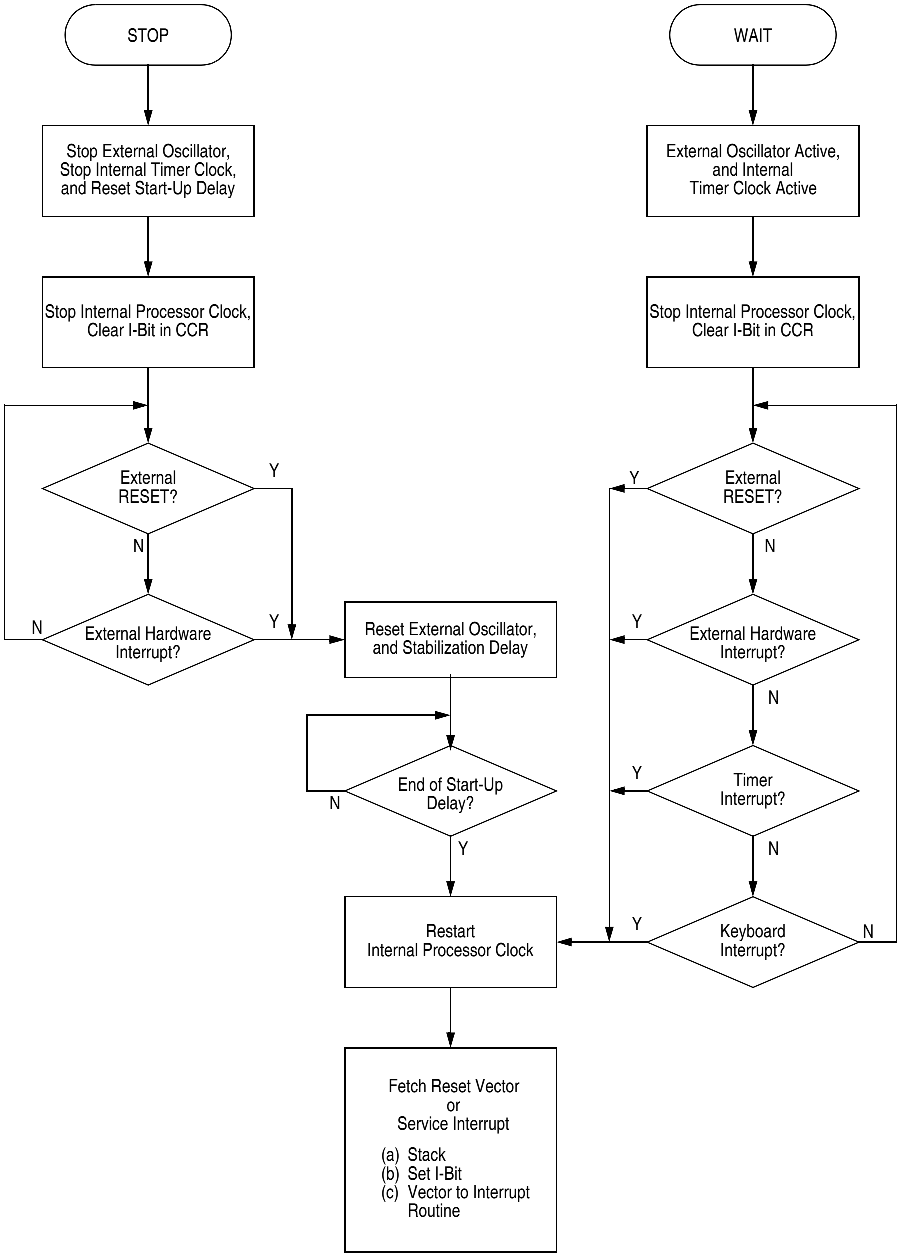
STOP
Stop External Oscillator, Stop Internal Timer Clock, and Reset Start-Up Delay
Stop Internal Processor Clock, Clear I-Bit in CCR
External RESET?
Y
N
External Hardware Interrupt?
N
Y
Reset External Oscillator, and Stabilization Delay
End of Start-Up Delay?
N
Y
Restart Internal Processor Clock
Fetch Reset Vector or Service Interrupt
(a) Stack
(b) Set I-Bit
(c) Vector to Interrupt Routine
WAIT
External Oscillator Active, and Internal Timer Clock Active
Stop Internal Processor Clock, Clear I-Bit in CCR
External RESET?
Y
N
External Hardware Interrupt?
Y
N
Timer Interrupt?
Y
N
Keyboard Interrupt?
Y
N

Figure 9-1 STOP and WAIT Mode Flowcharts

9.3 SLOW Mode

The SLOW mode function is controlled by the SM bit in the Miscellaneous Control Register. When the SM bit is set, the internal bus clock is divided by 16, resulting to a frequency equal to the oscillator frequency divide by 32. This feature permits a slow down of all the internal operations and thus reduces power consumption — particularly useful while in WAIT mode. The SM bit is automatically cleared while going to STOP mode.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Miscellaneous Control Register	$0C	KBIE	KBIC	INTO	INTE	LVRE	SM	IRQ2F	IRQ2E	0001 0000

SM — Slow Mode

1 (set) – Slow mode enabled. Internal bus frequency $f_{OP}=f_{OSC} \div 32$.

0 (clear) – Slow mode disabled. Internal bus frequency $f_{OP}=f_{OSC} \div 2$.

9.4 Data-Retention Mode

If the Low Voltage Reset function is not enabled, the contents of RAM and CPU registers are retained at supply voltages as low as 2Vdc. This is called the data-retention mode where the data is held, but the device is not guaranteed to operate. The $\overline{\text{RESET}}$ pin must be held low during data-retention mode.

The Low Voltage Reset Function is enabled/disabled by the LVRE bit in the Miscellaneous Control Register ($0C).

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Miscellaneous Control Register	$0C	KBIE	KBIC	INTO	INTE	LVRE	SM	IRQ2F	IRQ2E	0001 0000

LVRE — Low Voltage Reset Enable

1 (set) – Low Voltage Reset function enabled.

0 (clear) – Low Voltage Reset function disabled.

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10
OPERATING MODES

The MC68HC05SR3/*MC68HC705SR3* has two modes of operation: the User Mode and the Self-Check/*Bootstrap* Mode. Table 10-1 shows the conditions required for entering the two operating modes.

Table 10-1 Mode Selection

$\overline{\text{RESET}}$	V_{PP}	PB1	MODE
	V_{SS} to V_{DD}	V_{SS} to V_{DD}	USER
	V_{TST}	V_{DD}	SELF-CHECK/*BOOTSTRAP*

V_{TST}=2×V_{DD}

10.1 User Mode

The normal operating mode of the MC68HC05SR3/*MC68HC705SR3* is the User mode. This mode is entered on the rising edge of $\overline{\text{RESET}}$ when the V_{PP} and PB1 pins are between V_{SS} and V_{DD}.

10.2 Self-Check Mode

The Self-check mode is provided on the MC68HC05SR3 for the user to check device functions with an on-chip self-check program masked at location $1F00 to $1FEF under minimum hardware support. The self-check schematic is shown in Figure 10-1. Self-check mode is entered on the rising edge of $\overline{\text{RESET}}$ when the V_{PP} pin is at V_{TST} (2×V_{DD}) and PB1 pin is at V_{DD}. Once in the self-check mode, PB1 can then be used for other purposes. After entering the self-check mode, CPU branches to the self-check program and carries out the self-check. Self-check is a repetitive test, i.e. if all parts are checked to be good, the CPU will repeat the self-check again. Therefore, the LEDs attached to Port A will be flashing if the device is good; else the combination of LEDs' on-off pattern can show what part of the device is suspected to be bad. Table 10-2 lists the LEDs' on-off patterns and their corresponding indications.

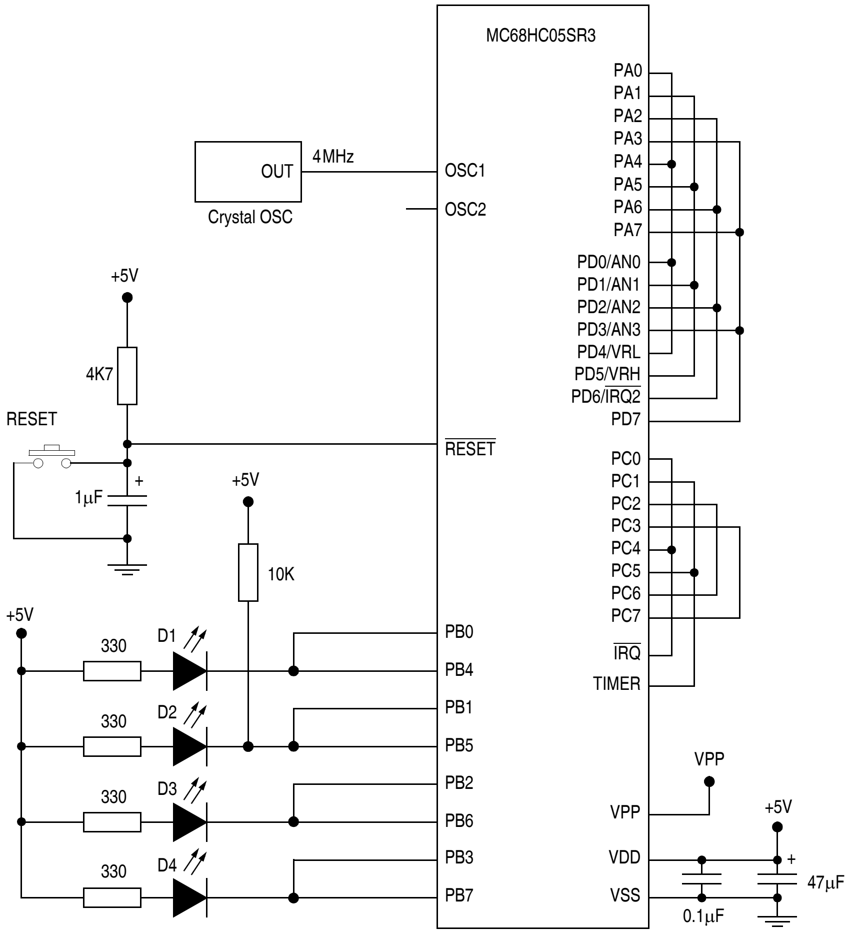

Figure 10-1 MC68HC05SR3 Self-Check Circuit

Table 10-2 Self-Check Report

D4	D3	D2	D1	REMARKS
Flashing				O.K. (self-check is on-going)
1	1	1	1	Bad port A
1	1	1	0	Bad port B
1	1	0	1	Bad port C
1	1	0	0	Bad port D
1	0	1	1	Bad RAM
1	0	1	0	Bad ROM
1	0	0	0	Bad SWI
0	1	1	1	Bad $\overline{\text{IRQ}}$

1=LED on, 0=LED off

10.3 Bootstrap Mode

The Bootstrap mode is provided in the EPROM part (MC68HC705SR3) as a mean of self-programming its EPROM with minimal circuitry. Bootstrap mode will be entered on the rising edge of $\overline{RESET}$ when the V_{PP} pin is at V_{TST} ($2 \times V_{DD}$) and PB1 pin is at V_{DD}. Once in the bootstrap mode, PB1 can then be used for other purposes. After entering the bootstrap mode, CPU branches to the bootstrap program and carries out the EPROM programming routine. The user EPROM consists of 3840 bytes, from location $1000 to $1EFF.

Refer to Appendix A for further details on MC68HC705SR3.

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11
ELECTRICAL SPECIFICATIONS

This section contains the electrical specifications for MC68HC05SR3.

11.1 Maximum Ratings

(Voltages referenced to V_{SS})

RATINGS	SYMBOL	VALUE	UNIT
Supply Voltage	V_{DD}	–0.3 to +7.0	V
Input Voltage	V_{IN}	V_{SS}–0.3 to V_{DD}+0.3	V
V_{PP} Pin	V_{IN}	V_{SS}–0.3 to 2xV_{DD}+0.3	V
Current Drain per pin excluding V_{DD} and V_{SS}	I_D	25	mA
Operating Temperature Standard Extended	T_A	T_L to T_H 0 to +70 –40 to +85	°C
Storage Temperature Range	T_{STG}	–65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

11.2 Thermal Characteristics

CHARACTERISTICS	SYMBOL	VALUE	UNIT
Thermal resistance			
DIP	θ_{JA}	60	°C/W
SOIC	θ_{JA}	60	°C/W
QFP	θ_{JA}	60	°C/W

11.3 DC Electrical Characteristics

Table 11-1 DC Electrical Characteristics for 5V Operation

(V_{DD}=5.0Vdc ±10%, V_{SS}=0Vdc, temperature range=0 to 70°C)

CHARACTERISTICS	SYMBOL	MINIMUM	TYPICAL	MAXIMUM	UNIT
Output voltage I_{LOAD} = –10µA I_{LOAD} = +10µA	 V_{OH} V_{OL}	 V_{DD}–0.1 —	 — —	 — 0.1	 V V
Output high voltage (I_{LOAD}=–0.8mA) All Ports	V_{OH}	V_{DD}–0.8	—	—	V
Output low voltage (I_{LOAD}=+1.6mA) All Ports	V_{OL}	—	0.1	0.4	V
Output high current (V_{OL}=2.5V) All ports (V_{OL}=3.0V) PB5-PB7 in low-current mode	 I_{OH} I_{OH}	 10 2	 — —	 — —	 mA mA
Output low current (V_{OL}=2.5V) All ports (V_{OL}=3.0V) PB5-PB7 in low-current mode	 I_{OL} I_{OL}	 10 2	 — —	 — —	 mA mA
Total I/O port current Either source or sink	I_{PORT}	—	100	—	mA
Input high voltage PA0-PA7, PB0, PB1, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IH}	0.7×V_{DD}	—	V_{DD}	V
Input low voltage PA0-PA7, PB0, PB1, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IL}	V_{SS}	—	0.2×V_{DD}	V
Supply current: Run Wait Stop 25°C 0°C to +70°C (Standard) –40°C to +85°C (Extended)	I_{DD}	 — — — — —	 5.0 1.3 — — —	 7.0 2.5 20 30 40	 mA mA µA µA µA
I/O ports high-Z leakage current PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7	I_{IL}	—	—	±10	µA
Input current $\overline{RESET}$, $\overline{IRQ}$, OSC1	I_{IN}	—	—	±1	µA
Capacitance Ports (as input or output) $\overline{RESET}$, $\overline{IRQ}$, OSC1, OSC2	 C_{OUT} C_{IN}	 — —	 — —	 12 8	 pF pF
Low voltage reset threshold	V_{LVR}	2.8	3.5	4.2	V
Pull-up resistor PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7 $\overline{RESET}$, $\overline{IRQ}$	R_{PU}	 14 85	 36 100	 50 176	 KΩ KΩ

Notes:

(1) All values shown reflect average measurements.

(2) Typical values at midpoint of voltage range, 25°C only.

(3) Wait I_{DD}: Only timer system active.

(4) Wait, Stop I_{DD}: All ports configured as inputs, V_{IL}=0.2Vdc, V_{IH}=V_{DD}–0.2Vdc.

(5) Run (operating) I_{DD}, Wait I_{DD}: Measured using external square wave clock source to OSC1 (f_{OSC}=2.0MHz), all inputs 0.2Vdc from rail; no DC loads, less than 50pF on all outputs, C_L=20pF on OSC2.

(6) Stop I_{DD} measured with OSC1=V_{SS}.

(7) Wait I_{DD} is affected linearly by the OSC2 capacitance.

11

Table 11-2 DC Electrical Characteristics for 3V Operation

(V_{DD}=3.0Vdc ±10%, V_{SS}=0Vdc, temperature range=0 to 70°C)

CHARACTERISTICS	SYMBOL	MINIMUM	TYPICAL	MAXIMUM	UNIT
Output voltage I_{LOAD} = –10µA I_{LOAD} = +10µA	 V_{OH} V_{OL}	 V_{DD}–0.1 —	 — —	 — 0.1	 V V
Output high voltage (I_{LOAD}=–0.8mA) All Ports	V_{OH}	V_{DD}–0.3	—	—	V
Output low voltage (I_{LOAD}=+1.6mA) All Ports	V_{OL}	—	0.1	0.3	V
Output high current (V_{OH}=1.0V) All ports	I_{OH}	2.7	3.5	4.7	mA
Output low current (V_{OL}=2.0V) All ports	I_{OL}	3.0	4.0	5.2	mA
Total I/O port current Either source or sink	I_{PORT}	—	100	—	mA
Input high voltage PA0-PA7, PB0, PB1, $\overline{\text{IRQ}}$, $\overline{\text{RESET}}$, OSC1	V_{IH}	0.7×V_{DD}	—	V_{DD}	V
Input low voltage PA0-PA7, PB0, PB1, $\overline{\text{IRQ}}$, $\overline{\text{RESET}}$, OSC1	V_{IL}	V_{SS}	—	0.2×V_{DD}	V
Supply current: Run Wait Stop 25°C 0°C to +70°C (Standard) –40°C to +85°C (Extended)	I_{DD}	 — — — — —	 2.4 0.75 — — —	 3.5 1.5 20 30 40	 mA mA µA µA µA
I/O ports high-Z leakage current PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7	I_{IL}	—	—	±10	µA
Input current $\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, OSC1	I_{IN}	—	—	±1	µA
Capacitance Ports (as input or output) $\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, OSC1, OSC2	 C_{OUT} C_{IN}	 — —	 — —	 12 8	 pF pF
Pull-up resistor PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7 $\overline{\text{RESET}}$, $\overline{\text{IRQ}}$	 R_{PU}	 14 85	 36 100	 50 176	 KΩ KΩ

Notes:
(1) All values shown reflect average measurements.

(2) Typical values at midpoint of voltage range, 25°C only.

(3) Wait I_{DD}: Only timer system active.

(4) Wait, Stop I_{DD}: All ports configured as inputs, V_{IL}=0.2Vdc, V_{IH}=V_{DD}–0.2Vdc.

(5) Run (operating) I_{DD}, Wait I_{DD}: Measured using external square wave clock source to OSC1 (f_{OSC}=2.0MHz), all inputs 0.2Vdc from rail; no DC loads, less than 50pF on all outputs, C_L=20pF on OSC2.

(6) Stop I_{DD} measured with OSC1=V_{SS}.

(7) Wait I_{DD} is affected linearly by the OSC2 capacitance.

11.4 ADC Electrical Characteristics

Table 11-3 ADC Electrical Characteristics for 5V and 3V Operation

CHARACTERISTICS	PARAMETER	MINIMUM	MAXIMUM	UNIT
Resolution	Number of bits resolved by the ADC	8	8	bits
Absolute accuracy	Difference between the actual input voltage and the full-scale equivalent of the binary code output code for all errors.[1]	— —	±1.5 (V_{DD}=5V) ±2 (V_{DD}=3.3V)	LSB LSB
Conversion range	Analog input voltage range	V_{RL}	V_{RH}	V
Power-up time	ADC power-up time delay, t_{ADON}	—	500	µs
V_{RH}	Maximum analog reference voltage	V_{RL}	V_{DD}+0.1	V
V_{RL}	Minimum analog reference voltage	V_{SS}–0.1	V_{RH}	V
Conversion time	Total time to perform a single analog to digital conversion (a) External clock (OSC1, OSC2) (b) Internal RC oscillator	— —	32 32	t_{CYC} t_{CYC}
Monotonicity	Conversion result never decreases with an increase in input voltage and has no missing codes	Inherent (within total error)		
Zero-input reading	Conversion result when V_{IN}=V_{RL}	00	—	hex
Full-scale reading	Conversion result when V_{IN}=V_{RH}	—	FF	hex
Sample acquisition time	Analog input acquisition sampling[2] (a) External clock (OSC1, OSC2) (b) Internal RC oscillator	— —	12 12	t_{CYC} µs
Input capacitance	Input capacitance on AN0-AN3	—	8	pF
Input leakage	Input leakage on ADC pins[3] AN0, AN1, AN2, AN3, V_{RL}, V_{RH}	—	±400	nA

Notes:

(1) Error includes quantization. ADC accuracy may decrease proportionately as V_{DD} is reduced below 3.0V.

(2) Source impedances greater than 10KΩ adversely affect internal RC charging time during input sampling.

(3) The external system error caused by input leakage current is approximately equal to the product of R source and input current.

11.5 Control Timing

Table 11-4 Control Timing for 5V Operation

(V_{DD}=5.0Vdc ±10%, V_{SS}=0Vdc, temperature range=0 to 70°C)

CHARACTERISTICS	SYMBOL	MINIMUM	MAXIMUM	UNIT
Frequency of operation RC oscillator Option Crystal option External clock option	f_{OSC}	 0.1 0.1 dc	 4.0 4.0 4.0	 MHz MHz MHz
Internal operating frequency (f_{OSC}/2) RC oscillator Crystal External clock	f_{OP}	 — — dc	 2.0 2.0 2.0	 MHz MHz MHz
Processor cycle time (1/f_{OP})	t_{CYC}	500	—	ns
RC oscillator stabilization time	t_{RCON}	—	1	ms
Crystal oscillator start-up time (crystal oscillator)	t_{OXOV}	—	100	ms
Stop recovery start-up time (crystal oscillator)	t_{ILCH}	—	100	ms
$\overline{\text{RESET}}$ pulse width low	t_{RL}	1.5	—	t_{CYC}
Timer resolution$^{(2)}$	t_{RESL}	See note (2)	—	t_{CYC}
Interrupt pulse width low (edge-triggered)	t_{ILIH}	125	—	ns
Interrupt pulse period	t_{ILIL}	See note (3)	—	t_{CYC}
PA0-PA7 interrupt pulse width high (edge-triggered)	t_{IHIL}	125	—	ns
PA0-PA7 interrupt pulse period	t_{IHIH}	See note (3)	—	t_{CYC}
OSC1 pulse width	t	90	—	ns
RC oscillator frequency combined stability$^{(4)}$ f_{OSC}=2.0MHz, V_{DD}=5.0Vdc±10%, t_A=-40°C to +85°C f_{OSC}=2.0MHz, V_{DD}=5.0Vdc±10%, t_A=0°C to +40°C	 Δf_{OSC} Δf_{OSC}	 – –	 ±25 ±15	 % %

Notes:

(1) V_{DD}=5.0Vdc±10%, V_{SS}=0Vdc, t_A=t_L to t_H

(2) The TIMER input pin is the limiting factor in determining timer resolution.

(3) The minimum period t_{ILIL} or t_{IHIH} should not be less than the number of cycles it takes to execute the interrupt service routine plus 19 t_{CYC}.

(4) Effects of processing, temperature, and supply voltage (excluding tolerances of external R and C).

Table 11-5 Control Timing for 3V Operation

(V_{DD}=3.0Vdc ±10%, V_{SS}=0Vdc, temperature range=0 to 70°C)

CHARACTERISTICS	SYMBOL	MINIMUM	MAXIMUM	UNIT
Frequency of operation	f_{OSC}			
RC oscillator Option		0.1	2.0	MHz
Crystal option		0.1	2.0	MHz
External clock option		dc	2.0	MHz
Internal operating frequency (f_{OSC}/2)	f_{OP}			
RC oscillator		—	1.0	MHz
Crystal		—	1.0	MHz
External clock		dc	1.0	MHz
Processor cycle time (1/f_{OP})	t_{CYC}	1000	—	ns
RC oscillator stabilization time	t_{RCON}	—	2	ms
Crystal oscillator start-up time (crystal oscillator)	t_{OXOV}	—	200	ms
Stop recovery start-up time (crystal oscillator)	t_{ILCH}	—	200	ms
$\overline{\text{RESET}}$ pulse width low	t_{RL}	1.5	—	t_{CYC}
Timer resolution(2)	t_{RESL}	See note (2)	—	t_{CYC}
Interrupt pulse width low (edge-triggered)	t_{ILIH}	250	—	ns
Interrupt pulse period	t_{ILIL}	See note (3)	—	t_{CYC}
PA0-PA7 interrupt pulse width high (edge-triggered)	t_{IHIL}	250	—	ns
PA0-PA7 interrupt pulse period	t_{IHIH}	See note (3)	—	t_{CYC}
OSC1 pulse width	t	180	—	ns
RC oscillator frequency combined stability(4)				
f_{OSC}=2.0MHz, V_{DD}=3.0Vdc±10%, t_A=–40°C to +85°C	Δf_{OSC}	—	±35	%
f_{OSC}=2.0MHz, V_{DD}=3.0Vdc±10%, t_A=0°C to +40°C	Δf_{OSC}	—	±20	%

Notes:

(1) V_{DD}=3.0Vdc±10%, V_{SS}=0Vdc, t_A=t_L to t_H

(2) The TIMER input pin is the limiting factor in determining timer resolution.

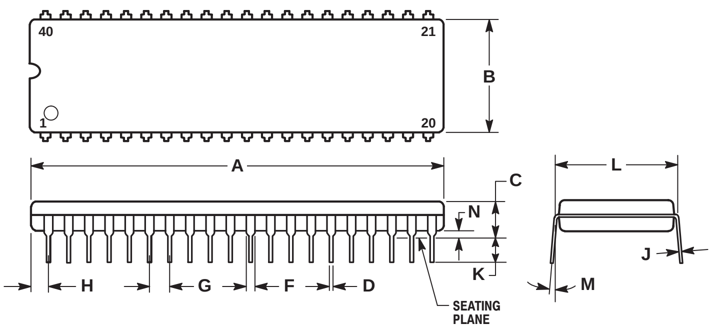
(3) The minimum period t_{ILIL} or t_{IHIH} should not be less than the number of cycles it takes to execute the interrupt service routine plus 19 t_{CYC}.

(4) Effects of processing, temperature, and supply voltage (excluding tolerances of external R and C).

12
MECHANICAL SPECIFICATIONS

This section provides the mechanical dimensions for the 40-pin DIP, 42-pin SDIP and 44-pin QFP packages for the MC68HC05SR3.

12.1 40-Pin DIP Package (Case 711-03)

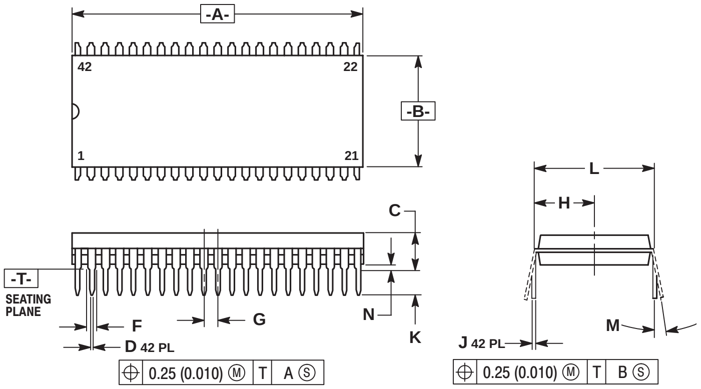


NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

Figure 12-1 40-pin DIP Package

12.2 42-Pin SDIP Package (Case 858-01)

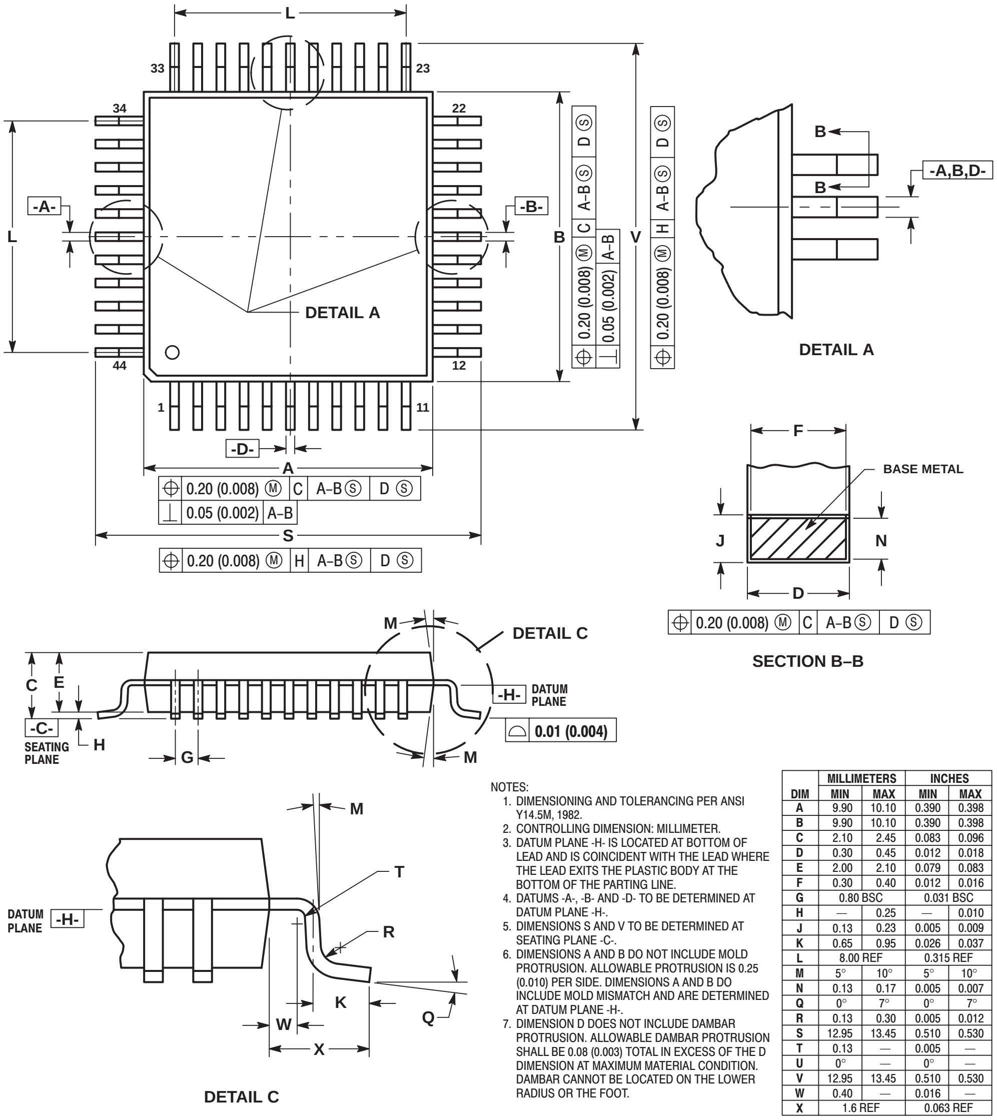


NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.435	1.465	36.45	37.21
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.56
F	0.032	0.046	0.81	1.17
G	0.070 BSC		1.778 BSC	
H	0.300 BSC		7.62 BSC	
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.600 BSC		15.24 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

Figure 12-2 42-pin SDIP Package

12.3 44-pin QFP Package (Case 824A-01)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.30	0.45	0.012	0.018
E	2.00	2.10	0.079	0.083
F	0.30	0.40	0.012	0.016
G	0.80 BSC		0.031 BSC	
H	—	0.25	—	0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	8.00 REF		0.315 REF	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13	—	0.005	—
U	0°	—	0°	—
V	12.95	13.45	0.510	0.530
W	0.40	—	0.016	—
X	1.6 REF		0.063 REF	

Figure 12-3 44-pin QFP Package

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A
MC68HC705SR3

This appendix summarizes the differences between the MC68HC05SR3 and MC68HC705SR3. The same information can also be found in appropriate sections of the book.

The MC68HC705SR3 is an EPROM version of the MC68HC05SR3. The 3840 bytes of user ROM in the MC68HC05SR3 are replaced by 3840 bytes of user EPROM.

A.1 Features

- Functionally equivalent to MC68HC05SR3
- 3840 bytes of user EPROM
- EPROM bootstrap mode replaces Self-Check mode on the MC68HC05SR3
- Available in the following packages: OTP 40-pin PDIP, windowed EPROM 40-pin Ceramic DIP, OTP 42-pin SDIP, and 44-pin QFP

A

A.2 Modes of Operation

The MC68HC705SR3 has two modes of operation – user mode and EPROM bootstrap mode. Table A-1 shows the conditions required to enter each mode on the rising edge of $\overline{\text{RESET}}$.

Table A-1 MC68HC705SR3 Operating Mode Entry Conditions

$\overline{\text{RESET}}$	V_{PP}	PB1	MODE
5V ↑	V_{SS} to V_{DD}	V_{SS} to V_{DD}	USER
	V_{TST}	V_{DD}	BOOTSTRAP

$V_{TST}=2\times V_{DD}$

A.3 User Mode

The normal operating mode of the MC68HC705SR3 is the user mode. User mode will be entered on the rising edge of $\overline{\text{RESET}}$ when the V_{PP} and PB1 pins are between V_{SS} and V_{DD}.

Warning: In the MC68HC705SR3, all vectors are fetched from EPROM in user mode; therefore, the EPROM must be programmed (via the bootstrap mode) before the device is powered up in user mode.

A.4 Bootstrap Mode

The bootstrap mode is provided as a mean of self-programming MC68HC705SR3 EPROM with minimal circuitry, and can only run in the crystal oscillator mode. Bootstrap mode will be entered on the rising edge of RESET when the V_{PP} pin is at V_{TST} ($2\times V_{DD}$) and PB1 pin is at V_{DD}. Once in the bootstrap mode, PB1 can then be used for other purposes. After entering the bootstrap mode, CPU branches to the bootstrap program and carries out the EPROM programming routine. The user EPROM consists of 3840 bytes, from location \$1000 to \$1EFF.

This program handles copying of user code from an external EPROM into the on-chip EPROM. The bootstrap function does not have to be done from an external EPROM, but it may be done from a host.

The user code must be a one-to-one correspondence with the internal EPROM addresses.

A.4.1 EPROM Programming

Programming boards are available from Freescale for programming the on-chip EPROM. Please contact your Freescale Representative.

The Programming Control register (PCR) is provided for EPROM programming. The function of the EPROM depends on the device operating mode.

A.4.2 Program Control Register (PCR)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
$0D	RESERVED						ELAT	PGM	---- --00

ELAT - EPROM Latch Control

1 (set) – EPROM address and data bus configured for programming (writes to EPROM cause address data to be latched). EPROM is in programming mode and cannot be read if ELATA is 1. This bit should not be set unless a programming voltage is applied to the V_{PP} pin.

0 (clear) – EPROM address and data bus configured for normal reads.

PGM - EPROM Program Command

1 (set) – Programming power connected to the EPROM array. If ELAT ≠ 1 then PGM = 0.

0 (clear) – Programming power disconnected from the EPROM array.

A.4.3 EPROM Programming Sequence

Programming the EPROM of the MC68HC705SR3 is as follows:

1) Set the ELAT bit.
2) Write the data to be programmed to the address to be programmed.
3) Set the PGM bit.
4) Delay for 1ms.
5) Clear the PGM and the ELAT bits.

The last action may be carried out in a single CPU write operation. It is important to remember that an external programming voltage must be applied to the V_{PP} pin while programming, but should be equal to V_{DD} during normal operation.

Example shows address $1900 is programmed with $00.

```
CLR    PCR          ;reset PCR
LDX    #$00         ;load index register with 00
BSET   1,PCR        ;set ELAT bit
LDA    #$00         ;load data=00 in to A
STA    $1900,X      ;latch data and address
BSET   0,PCR        ;program
JSR    DELAY        ;call delay subroutine for 1ms
CLR    PCR          ;reset PCR
```

A.5 Mask Option Register (MOR)

The Mask Option Register (MOR) contains programmable EPROM bits to control mask options, and cannot be changed in User mode. The erased state are zeros. This register is latched upon reset going away.

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	State on reset
Mask Option Register (MOR)	$0FFF			SMD	SEC	TMR2	TMR1	TMR0	RC	unaffected

SMD — SLOW Mode at Power-on

When programmed to “1”, this bit enables SLOW mode at power-up. Operating frequency, $f_{OP}=f_{OSC}\div2\div16=f_{OSC}\div32$.

SEC — EPROM Security

When programmed to “1”, this bit disables some functions of the Bootstrap mode, preventing external reading of EPROM content.

TMR2:TMR0 — Power-on Reset Delay

The amount Power-On Reset delay is set by programming these three bits. The delay is selected as follows:

TMR2	TMR1	TMR0	Delay (Instruction Cycles)
0	0	0	256
0	0	1	512
0	1	0	1024
0	1	1	2048
1	0	0	4096
1	0	1	8192
1	1	0	16384
1	1	1	32768

RC — RC or Crystal Oscillator Option

1 (set)	–	Resistor option selected.
0 (clear)	–	Crystal option selected.

A.6 Pin Assignments

See Section 2.3 for pin assignments for the available packages.

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