Freescale Semiconductor
Technical Data

Document order number: MC33989
Rev 9.0, 1/2006

System Basis Chip with High-Speed CAN Transceiver

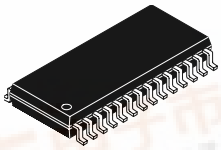
33989

SYSTEM BASIS CHIP WITH HIGH-SPEED CAN

The 33989 is a monolithic integrated circuit combining many functions frequently used by automotive Engine Control Units (ECUs), incorporating: Two voltage regulators; Four high voltage inputs, 1Mbaud CAN physical interface.

Features

- V_{DD1}: Low Drop Voltage Regulator, Current Limitation, Overtemperature Detection, Monitoring, and Reset Function
- V_{DD1}: Total Current Capability 200 mA
- V2: Tracking Function of V_{DD1} Regulator. Control Circuitry for External Bipolar Ballast Transistor for High Flexibility in Choice of Peripheral Voltage and Current Supply
- Four Operational Modes
- Low Stand-By Current Consumption in Stop and Sleep Modes
- High-Speed 1 MBaud CAN Physical Interface
- Four External High Voltage Wake-up Inputs Associated with HS1 V_{BAT} Switch
- 150 mA Output Current Capability for HS1 V_{BAT} Switch Allowing Drive of External Switches Pull-Up Resistors or Relays
- V_{SUP} Failure Detection
- Nominal DC Operating Voltage from 5.5 V to 27 V, Extended Range Down to 4.5 V
- 40 V Maximum Transient Voltage



DW SUFFIX
98ASB42345B
28-TERMINAL SOICW

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC33989DW/R2	-40°C to 125°C	28 SOICW
PC33989EG/R2		

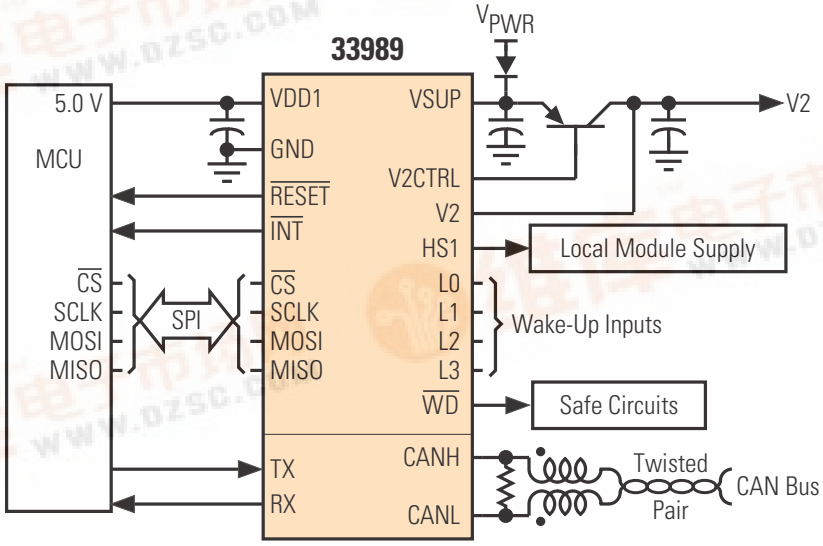


Figure 1. MC33989 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

INTERNAL BLOCK DIAGRAM

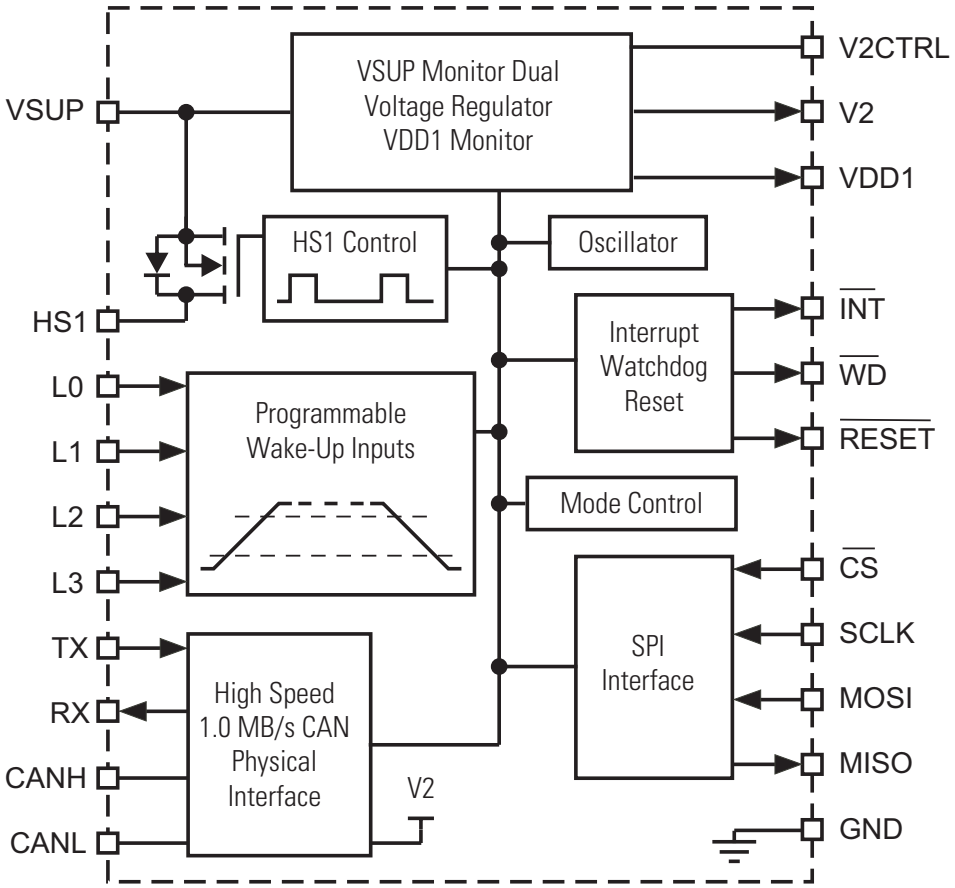


Figure 2. 33989 Simplified Internal Block Diagram

TERMINAL CONNECTIONS

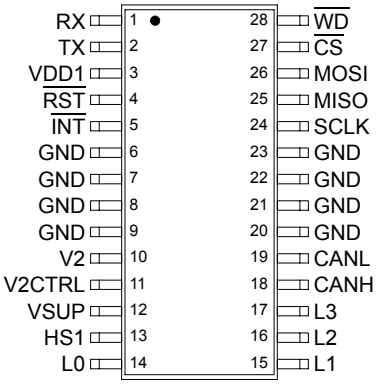


Figure 3. 33989 Terminal Connections

Table 1. 33989 Terminal Definitions

A functional description of each terminal can be found in the Functional Terminal Description section beginning on page 17.

Terminal Number	Terminal Name	Terminal Function	Formal Name	Definition
1	RX	Output	Receive Data	CAN bus receive data output terminal.
2	TX	Input	Transmit Data	CAN bus transmit data input terminal.
3	VDD1	Power Output	Voltage Digital Drain One	5.0 V regulator output terminal. Supply terminal for the MCU.
4	RST	Output	Reset	This is the device reset output terminal whose main function is to reset the MCU. This terminal has an internal pullup current source to VDD.
5	INT	Output	Interrupt	This output is asserted LOW when an enabled interrupt condition occurs. The output is a push-pull structure.
6–9 20–23	GND	Ground	Ground	These device ground terminals are internally connected to the package lead frame to provide a 33989-to-PCB thermal path.
10	V2	Input	Voltage Source Two	Sense input for the V2 regulator using an external series pass transistor. V2 is also the internal supply for the CAN transceiver.
11	V2CTRL	Power Output	Voltage Control	Output drive source for the V2 regulator connected to the external series pass transistor.
12	VSUP	Power	Voltage Supply	Supply input terminal for the 33989.
13	HS1	Output	High Side One	Output of the internal high-side switch. The output current is internally limited to 150 mA.
14–17	L0:L3	Input	Level 0: 3	Inputs from external switches or from logic circuitry.
22	CANH	Output	CAN High	CAN high output terminal.
23	CANL	Output	CAN Low	CAN low output terminal.
24	SCLK	Input	System Clock	Clock input terminal for the Serial Peripheral Interface (SPI).
25	MISO	Output	Master In/Slave Out	SPI data sent to the MCU by the 33989. When $\overline{CS}$ is HIGH, the terminal is in the high-impedance state.
26	MOSI	Input	Master Out/Slave In	SPI data received by the 33989.
27	CS	Input	Chip Select	The $\overline{CS}$ input terminal is used with the SPI bus to select the 33989.
28	WD	Output	Watch Dog	The $\overline{WD}$ output terminal is asserted LOW if the software watchdog is not correctly triggered.

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Power Supply Voltage at V_{SUP}			V
Continuous (Steady-State)	V_{SUP}	-0.3 to 27	
Transient Voltage (Load Dump)	V_{SUP}	-0.3 to 40	
Logic Inputs (Rx, Tx, MOSI, MISO, $\overline{CS}$, SCLK, RST, $\overline{WD}$, and $\overline{INT}$)	V_{LOG}	-0.3 to V_{DD1} + 0.3	V
Output Current V_{DD1}	I	Internally Limited	A
HS1			
Voltage	V	-0.3 to V_{SUP} + 0.3	V
Output Current	I	Internally Limited	A
ESD Voltage, Human Body Model (1)			kV
HS1, L0, L1, L2, L3	V_{ESDH}	- 4.0 to 4.0	
All Other Terminals		-2.0 to 2.0	
ESD Voltage Machine Model	V_{ESDM}		V
All Terminals Except CANH and CANL		±200	
L0, L1, L2, L3	V_{WUDC}		
DC Input Voltage		-0.3 to 40	V
DC Input Current		-2.0 to 2.0	mA
Transient Input Voltage with External Component (2)		-100 to 100	V
CANL and CANH Continuous Voltage	$V_{CANH/L}$	-27 to 40	V
CANL and CANH Continuous Current	$I_{CANH/L}$	200	mA
CANH and CANL Transient Voltage (Load Dump) (4)	$V_{TRH/L}$	40	V
CANH and CANL Transient Voltage (5)	$V_{TRH/L}$	-40 to 40	V
Logic Inputs (Tx and Rx)	V	-0.5 to 6.0	V
ESD Voltage (HBM 100 pF, 1.5 k) CANL, CANH	V_{ESDCH}	-4.0 to 4.0	KV
ESD Voltage Machine Model	V_{ESDCM}		V
CANH and CANL		-200 to 200	
THERMAL RATINGS			
Operating Junction Temperature	T_J	-40 to 150	°C
Storage Temperature	T_S	-55 to 165	°C
Ambient Temperature	T_A	-40 to 125	°C
Thermal Resistance Junction to GND Terminals (3)	$R_{\Theta J/P}$	20	°C/W

Notes

1. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP}=100 pF, 1.5 k).
2. According to ISO 7637 specification. See **Table 6**, page 23.
3. Ground terminals 6, 7, 8, 9, 20, 21, 22, and 23
4. Load Dump test according to ISO 7637 part 1.
5. Transient test according to ISO 7637 part 1, pulses 1, 2, 3a, and 3b according to schematic in **Table 17**, page 34.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT (V_{SUP})					
Nominal DC Supply Voltage Range	V_{SUP}	5.5	—	18	V
Extended DC Voltage Range 1 Reduced Functionality [6]	V_{SUPEX1}	4.5	—	5.5	V
Extended DC Voltage Range 2 [7]	V_{SUPEX2}	18	—	27	V
Input Voltage During Load Dump Load Dump Situation	V_{SUPLD}	—	—	40	V
Input Voltage During Jump Start Jump Start Situation	V_{SUPJS}	—	—	27	V
Supply Current in Standby Mode (Includes 10 mA at V_{DD1}) [8] [9] I_{OUT} at V_{DD1} = 10 mA CAN recessive or Sleep-Disable State	$I_{SUP(STDBY)}$	—	12	17	mA
Supply Current in Normal Mode [8] I_{OUT} at V_{DD1} = 10 mA CAN recessive or Sleep-Disable State	$I_{SUP(NORM)}$	—	12.5	17	mA
Supply Current in Sleep Mode [8] [9] V_{DD1} and V2 OFF, V_{SUP} < 12 V, Oscillator Running [10] CAN in Sleep-Disable State	$I_{SUP(SLEEP1)}$	—	72	105	µA
Supply Current in Sleep Mode [8] [9] V_{DD1} and V2 OFF, V_{SUP} < 12 V, Oscillator Not Running [10] CAN in Sleep-Disable State	$I_{SUP(SLEEP2)}$	—	57	90	µA
Supply Current in Sleep Mode [8] [9] V_{DD1} and V2 OFF, V_{SUP} > 12 V, Oscillator Running [10] CAN in Sleep-Disable State	$I_{SUP(SLEEP3)}$	—	100	150	µA
Supply Current in Stop Mode I_{OUT} V_{DD1} < 2.0 mA [8] [9] V_{DD1} ON, V_{SUP} < 12 V, Oscillator Running [10] CAN in Sleep-Disable State	$I_{SUP(STOP1)}$	—	135	210	µA
Supply Current in Stop Mode I_{OUT} V_{DD1} < 2.0 mA [9] V_{DD1} ON, V_{SUP} < 12 V, Oscillator Not Running [10] CAN in Sleep-Disable State	$I_{SUP(STOP2)}$	—	130	210	µA
Supply Current in Stop Mode I_{OUT} V_{DD1} < 2.0 mA [8] [9] V_{DD1} ON, V_{SUP} > 12 V, Oscillator Running [10] CAN in Sleep-Disable State	$I_{SUP(STOP3)}$	—	160	230	µA
BATFAIL Flag Internal Threshold	VBF	1.5	3.0	4.0	V

Notes

6. V_{DD1} > 4.0 V, Reset high, Logic terminal high level reduced, device is functional.
7. Device is fully functional. All functions are operating. All modes available and operating. Watchdog, HS1 turn ON turn OFF, CAN cell operating, L0:L3 inputs operating, SPI read/write operation. Overtemperature may occur.
8. Current measured at V_{SUP} terminal.
9. With CAN cell in Sleep-Disable state. If CAN cell is Sleep-Enabled for wake-up, an additional 60 µA must be added to specified value.
10. Oscillator running means *Forced Wake-up* or *Cyclic Sense* of *Software Watchdog is Stop mode* are not activated.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
BATFAIL Flag Hysteresis (11)	$VBF_{(HYS)}$	—	1.0	—	V
Battery Fall Early Warning Threshold In Normal and Standby Mode	BF_{EW}	5.3	5.8	6.3	V
Battery Fall Early Warning Hysteresis In Normal and Standby Mode (11)	BF_{EWH}	0.1	0.2	0.3	V
POWER OUTPUT (V_{DD1}) (12)					
V_{DD1} Output Voltage I_{DD1} from 2.0 to 200 mA T_{AMB} -40 to 125°C, 5.5 V < V_{SUP} < 27 V	V_{DD1OUT}	4.9	5.0	5.1	V
V_{DD1} Output Voltage I_{DD1} from 2.0 to 200 mA, 4.5 V < V_{SUP} < 5.5 V	$V_{DD1OUT2}$	4.0	—	—	V
Dropout Voltage I_{DD1} = 200 mA	V_{DD1DRP}	—	0.2	0.5	V
Dropout Voltage, Limited Output Current I_{DD1} = 50 mA, 4.5 V < V_{SUP}	$V_{DD1DRP2}$	—	0.1	0.25	V
I_{DD1} Output Current Internally Limited	I_{DD1}	200	285	350	mA
Junction Thermal Shutdown Normal or Standby Modes	T_{SD}	160	—	200	°C
Junction Over Temperature Pre-Warning V_{DDTEMP} Bit Set	T_{PW}	125	—	160	°C
Temperature Threshold Difference	T_{SD} - T_{PW}	20	—	40	°C
Reset Threshold 1 Selectable by SPI. Default Value After Reset.	RST_{TH1}	4.5	4.6	4.7	V
Reset Threshold 2 Selectable by SPI	RST_{TH2}	4.1	4.2	4.3	V
V_{DD1} Range for Reset Active	V_{DDR}	1.0	—	—	V
Reset Delay Time Measured at 50% of Reset Signal	t_D	4.0	—	30	µs
Line Regulation (C at V_{DD1} = 47 µF Tantal) 9.0 V V_{SUP} < 18, I_{DD} = 10 mA	LR1	—	5.0	25	mV
Line Regulation (C at V_{DD1} = 47 µF Tantal) 5.5 < V_{SUP} < 27 V, I_{DD} = 10 mA	LR2	—	10	25	mV
Load Regulation (C at V_{DD1} = 47 µF Tantal) 1.0 mA < I_{IDD} < 200 mA	LD	—	25	75	mV
Thermal Stability V_{SUP} = 13.5 V, 1 = -100 mA Not Tested (13)	$THERM_S$	—	30	50	mV

Notes

11. With CAN cell in Sleep-Disable state. If CAN cell is Sleep-Enabled for wake-up, an additional 60 µA must be added to specified value.
12. I_{DD1} is the total regulator output current. V_{DD} specification with external capacitor. Stability requirement: C > 47 µF ESR < 1.3 Ω (tantalum capacitor). In reset, normal request, normal and standby modes. Measure with C = 47 µF Tantalum.
13. Guaranteed by design; however, it is not production tested.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT (V_{DD1}) in STOP MODE (14)					
V_{DD1} Output Voltage I_{DD1} < = 2.0 mA	V_{DDSTOP}	4.75	5.00	5.25	V
V_{DD1} Output Voltage I_{DD1} < = 10 mA	$V_{DDSTOP2}$	4.75	5.00	5.25	V
I_{DD1} Stop Output Current to Wake-up SBC	I_{DD1SWU}	10	17	25	mA
I_{DD1} Over Current to Wake-up Deglitcher Time (15)	$I_{DD1DGLT}$	40	55	75	µs
Reset Threshold	RST_{STOP1}	4.5	4.6	4.7	V
Reset Threshold	RST_{STOP2}	4.1	4.2	4.3	V
Line Regulation (C at V_{DD1} = 47 µF Tantal) 5.5 V < V_{SUP} < 27 V, I_{DD} = 2.0 mA	LR_S	—	5.0	25	mV
Load Regulation (C at V_{DD1} = 47 µF Tantal) 1 mA < I_{DD} < 10 mA	LD_S	—	15	75	mV
Max Decoupling Capacitor at V_{DD1} Pin, in Stop Mode(16)	$V_{DDst-cap}$	—	—	200	µF
TRACKING VOLTAGE REGULATOR (V2) (17)					
V2 Output Voltage (C at V2 = 10 µF Tantal) I2 from 2.0 to 200 mA, 5.5 V < V_{SUP} < 27 V	V2	0.99	1.0	1.01	V_{DD1}
I2 Output Current (for information only) Depending Upon External Ballast Transistor	I2	200	—	—	mA
V2 Control Drive Current Capability Worst Case at T_J = 125°C	12_{CTRL}	0.0	—	10	mA
V2LOW Flag Threshold	$V2L_{TH}$	3.75	4.0	4.25	V
LOGIC OUTPUT TERMINAL (MISO) (18)					
Low Level Output Voltage I_{OUT} = 1.5 mA	V_{OL}	0.0	—	1.0	V
High Level Output Voltage I_{OUT} = 250 µA	V_{OH}	$V_{DD1-0.9}$	—	V_{DD1}	V
Tri-Stated MISO Leakage Current 0 V < V_{MISO} < V_{DD}	I_{HZ}	-2.0	—	2.0	µA

Notes

14. If stop mode is used, the capacitor connected at V_{DD} pin should not exceed the maximum specified by the "$V_{DDst-cap}$" parameter. If capacitor value is exceeded, upon entering stop mode, V_{DD} output current may exceed the I_{DDSWU} and prevent the device to stay in stop mode.
15. Guaranteed by design; however, it is not production tested.
16. Guaranteed by design.
17. V2 specification with external capacitor
    - Stability requirement: C > 42 µF and ESR < 1.3 Ω (Tantalum capacitor), external resistor between base and emitter required
    - Measurement conditions: Ballast transistor MJD32C, C = 10 µF Tantalum, 2.2 k resistor between base and emitter of ballast transistor
18. Push/Pull structure with tri-state condition $\overline{CS}$ high.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LOGIC OUTPUT TERMINALS (MOSI, SCLK, $\overline{CS}$)					
High Level Input Voltage	V_{IH}	0.7 V_{DD1}	—	V_{DD1} + 0.3	V
Low Level Input Voltage	V_{IL}	-0.3	—	0.3 V_{DD1}	V
High Level Input Current on $\overline{CS}$	L_{IH}	-100	—	-20	µA
Low Level Input Current on $\overline{CS}$	L_{IL}	-100	—	-20	µA
MOSI and SCLK Input Current	L_N	-10	—	10	µA
RESET TERMINAL ($\overline{RESET}$)[19]					
High Level Output Current 0 < V_{OUT} < 0.7 V_{DD}	I_{OH}	-300	-250	-150	µA
Low Level Output Voltage (I_0 = 1.5 mA) 5.5 V < V_{SUP} < 27 V	V_{OL}	0.0	—	0.9	V
Low Level Output Voltage (I_0 = 0 µA 1.0 V < V_{SUP} < 5.5 V	V_{OL}	0.0	—	0.9	V
Reset Pull Down Current V > 0.9 V	I_{PDW}	2.3	—	5.0	mA
Reset Duration After V_{DD1} High	RST_{DUR}	3.0	3.4	4.0	ms
WATCHDOG OUTPUT TERMINAL ($\overline{WD}$)[20]					
Low Level Output Voltage (I_0 = 1.5 mA) 1.0 V < V_{SUP} < 27 V	V_{OL}	0.0	—	0.9	V
High Level Output Voltage (I_0 = 250 µA)	V_{OH}	V_{DD1}-0.9	—	V_{DD1}	V
INTERRUPT TERMINAL ($\overline{INT}$) [20]					
Low Level Output Voltage (I_0 = 1.5 mA)	V_{OL}	0.0	—	0.9	V
High Level Output Voltage (I_0 = 250 µA)	V_{OH}	V_{DD1}-0.9	—	V_{DD1}	V
HIGH SIDE OUTPUT TERMINAL (HS1)					
R_{DSON} at T_J = 25°C, and I_{OUT} - 150 mA V_{SUP} > 9.0 V	RON_{25}	—	2.0	2.5	Ω
R_{DSON} at T_A = 125°C, and I_{OUT} - 150 mA V_{SUP} > 9.0 V	RON_{125}	—	—	4.5	Ω
R_{DSON} at T_A = 125°C, and I_{OUT} - 120 mA 5.5 < V_{SUP} < 9.0 V	RON_{125-2}	—	3.5	5.5	Ω
Output Current Limitation	L_{LIM}	160	—	500	mA
HS1 Overtemperature Shutdown	O_{VT}	155	—	190	°C
HS1 Leakage Current	L_{LEAK}	—	—	10	µA
Output Clamp Voltage at I_{OUT} = -10 mA No Inductive Load Drive Capability	V_{CL}	-1.5	—	-0.3	V

Notes

19. Push/Pull structure with tri-state condition $\overline{CS}$ high.
20. Output terminal only. Supply from V_{DD1}. Structure switch to ground with pull-up current source.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS (L0:L3)					
Negative Switching Threshold	V_{THN}				V
5.5 V < V_{SUP} < 6.0 V		2.0	2.5	3.0	
6.0 V < V_{SUP} < 18 V		2.5	3.0	3.6	
18 V < V_{SUP} < 27 V		2.7	3.2	3.7	
Positive Switching Threshold	V_{THP}				V
5.5 V < V_{SUP} < 6.0 V		2.7	3.3	3.8	
6.0 V < V_{SUP} < 18 V		3.0	4.0	4.6	
18 V < V_{SUP} < 27 V		3.5	4.2	4.7	
Hysteresis	V_{HYS}				V
5.5 V < V_{SUP} < 27 V		0.6	—	1.3	
Input Current	L_{IN}				µA
-0.2 V < V_{IN} < 40 V		-10	—	10	
CAN SUPPLY (V2)					
Supply Current Cell	I_{RES}				mA
Recessive State		—	1.5	3.0	
Supply Current Cell	I_{DOM}				mA
Dominant State without Bus Load		—	2.0	6.0	
Supply Current Cell, CAN in Sleep State Wake-up Enable	I_{SLEEP}				µA
V2 Regulator OFF		—	55	70	
Supply Current Cell, CAN in Sleep State Wake-up Disable	I_{DIS}				µA
V2 Regulator OFF (21)		—	—	1.0	
CANH and CANL					
Bus Terminals Common Mode Voltage	V_{CM}	-27	—	40	V
Differential Input Voltage (Common Mode Between -3.0 and 7.0 V)	V_{CANH}-V_{CANL}				mV
Recessive State at RXD		—	—	500	
Dominant State at RXD		900	—	—	
Differential Input Hysteresis (RXD)	V_{HYS}	100	—	—	mV
Input Resistance	R_{IN}	5.0	—	100	KΩ
Differential Input Resistance	R_{IND}	10	—	100	KΩ
Unpowered Node Input Current	I_{CANUP}	—	—	1.5	mA
CANH Output Voltage					V
TXD Dominant State	V_{CANHD}	2.75	—	4.5	
TXD Recessive State	V_{CANHR}	—	—	3.0	
CANL Output Voltage					V
TXD Dominant State	V_{CANLD}	0.5	—	2.25	
TXD Recessive State	V_{CANLR}	2.0	—	—	
Differential Output Voltage					
TXD Dominant State	V_{DIFFD}	1.5	—	3.0	V
TXD Recessive State	V_{DIFFR}	—	—	100	mV

Notes

21. Push/Pull structure.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CANH and CANL					
Output Current Capability (Dominant State) CANH CANL	 I_{CANH} I_{CANL}	 — 35	 —	 -35	mA
Overtemperature Shutdown	T_{SHUT}	160	180°C	—	°C
CANL Over Current Detection Error Reported in CANR	$I_{CANL/OC}$	 60	 —	 200	mA
CANH Over Current Detection Error Reported in CANR	$I_{CANH/OC}$	 -200	 —	 -60	mA
TX and RX					
TX Input High Voltage	V_{IH}	0.7 V_{DD}	—	V_{DD} + 0.4	V
TX Input Low Voltage	V_{ILP}	-0.4	—	0.3 V_{DD}	V
TX High Level Input Current, VTX = V_{DD}	L_{IH}	-10	—	10	µA
TX Low Level Input Current, VTX = 0 V	L_{IL}	-100	-50	-20	µA
RX Output Voltage High, IRX = 250 µA	V_{OH}	VDD-1	—	—	V
RX Output Voltage Low, IRX = 1.0 mA	V_{OL}	—	—	0.5	V

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
DIGITAL INTERFACE TIMING (SCLK, $\overline{CS}$, MOSI, MISO)					
SPI Operation Frequency	F_{REQ}	0.25	—	4.0	MHz
SCLK Clock Period	t_{PCLK}	250	—	N/A	ns
SCLK Clock High Time	t_{WSCLKH}	125	—	N/A	ns
SCLK Clock Low Time	t_{WSCLKH}	125	—	N/A	ns
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK	t_{LEAD}	100	—	N/A	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$	t_{LAG}	100	—	N/A	ns
MOSI to Falling Edge of SCLK	t_{SISU}	40	—	N/A	ns
Falling Edge of SCLK to MOSI	t_{SIH}	40	—	N/A	ns
MISO Rise Time (C_L = 220 pF)	t_{RSO}	—	25	50	ns
MISO Fall Time (C_L = 220 pF)	t_{FSO}	—	25	50	ns
Time from Falling or Rising Edges of $\overline{CS}$ to: MISO Low Impedance MISO High Impedance	t_{SOEN} t_{SODIS}	 — —	 — —	 50 50	ns
Time from Rising Edge of SCLK to MISO Data Valid 0.2 V1 = <MISO> = 0.8 V1, C_L = 200 pF	t_{VALID}	—	—	50	ns
STATE MACHINE TIMING ($\overline{CS}$, SCLK, MOSI, MISO, $\overline{WD}$, $\overline{INT}$)					
Delay Between $\overline{CS}$ Low to High Transition (End of SPI Stop Command) and Stop Mode Activation Detected by V2 OFF (22)	$t_{\overline{CS}STOP}$	18	—	34	µs
Interrupt Low Level Duration SBC in Stop Mode	$t_{\overline{INT}}$	7.0	10	13	µs
Internal Oscillator Frequency All Modes Except Sleep and Stop (22)	O_{SCF1}	—	100	—	kHz
Internal Low Power Oscillator Frequency Sleep and Stop Modes (22)	O_{SCF2}	—	100	—	kHz
Watchdog Period 1 Normal and Standby Modes	WD_1	8.58	9.75	10.92	ms
Watchdog Period 2 Normal and Standby Modes	WD_2	39.6	45	50.4	ms
Watchdog Period 3 Normal and Standby Modes	WD_3	88	100	112	ms
Watchdog Period 4 Normal and Standby Modes	WD_4	308	350	392	ms
Watchdog Period Accuracy Normal and Standby Modes	f_{1ACC}	-12	—	12	%

Notes

22. Guaranteed by design; however it is not production tested.

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Normal Request Mode Timeout Normal Request Modes	NR_{TOUT}	308	350	392	ms
Watchdog Period 1 - Stop Stop Mode	WD_{1STOP}	6.82	9.75	12.7	ms
Watchdog Period 2 - Stop Stop Mode	WD_{2STOP}	31.5	45	58.5	ms
Watchdog Period 3 - Stop Stop Mode	WD_{3STOP}	70	100	130	ms
Watchdog Period 4 - Stop Stop Mode	WD_{4STOP}	245	350	455	ms
Stop Mode Watchdog Period Accuracy Stop Mode	f_{2ACC}	-30	—	30	%
Cyclic Sense/FWU Timing 1 Sleep and Stop Modes	CS_{FWU1}	3.22	4.6	5.98	ms
Cyclic Sense/FWU Timing 2 Sleep and Stop Modes	CS_{FWU2}	6.47	9.25	12	ms
Cyclic Sense/FWU Timing 3 Sleep and Stop Modes	CS_{FWU3}	12.9	18.5	24	ms
Cyclic Sense/FWU Timing 4 Sleep and Stop Modes	CS_{FWU4}	25.9	37	48.1	ms
Cyclic Sense/FWU Timing 5 Sleep and Stop Modes	CS_{FWU5}	51.8	74	96.2	ms
Cyclic Sense/FWU Timing 6 Sleep and Stop Modes	CS_{FWU6}	66.8	95.5	124	ms
Cyclic Sense/FWU Timing 7 Sleep and Stop Modes	CS_{FWU7}	134	191	248	ms
Cyclic Sense/FWU Timing 8 Sleep and Stop Modes	CS_{FWU8}	271	388	504	ms
Cyclic Sense ON Time Sleep and Stop Modes Threshold and Condition to be Added	t_{ON}	200	350	500	µs
Cyclic Sense/FWU Timing Accuracy Sleep and Stop Modes	t_{ACC}	-30	—	30	%
Delay Between SPI Command and HS1 Turn ON (23)	t_{SHSON}	—	—	22	µs
Delay Between SPI Command and HS1 Turn OFF (23)	t_{SHSOFF}	—	—	22	µs
Delay Between SPI and V2 Turn ON (23) Standby Mode	tS_{V2ON}	9.0	—	22	µs
Delay Between SPI and V2 Turn OFF (23) Normal Mode	tS_{V2OFF}	9.0	—	22	µs

Notes

23. Delay starts at falling edge of clock cycle #8 of the SPI command and start of *Turn ON* or *Turn OFF* of HS1 or V2.

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Delay Between Normal Request and Normal Mode After $\overline{WD}$ Trigger Command Normal Request Mode	tS_{NR2N}	 15	 35	 70	µs
Delay Between SPI and CAN Normal Mode SBC Normal Mode [24]	tS_{CANN}	 —	 —	 10	µs
Delay Between SPI and CAN Normal Mode SBC Normal Mode [24]	tS_{CANS}	 —	 —	 10	µs
Delay Between $\overline{CS}$ Wake-up ($\overline{CS}$ Low to High) and SBC Normal Request Mode (V_{DD1} on and Reset High) SBC in Stop Mode	$tW_{\overline{CS}}$	 15	 40	 90	µs
Delay Between $\overline{CS}$ Wake-up ($\overline{CS}$ Low to High) and First Accepted API Command SBC in Stop Mode	tW_{SPI}	 90	 —	 N/A	µs
Delay Between $\overline{INT}$ Pulse and First SPI Command Accepted In Stop Mode After Wake-up	tS_{1STSPI}	20	—	 N/A	µs
INPUT TERMINNALS (L0, L1, L2, AND L3)					
Wake-up Filter Time	t_{WUF}	8.0	20	38	µs
CAN MODULE-SIGNAL EDGE RISE AND FALL TIMES (CANH, CANL)					
Dominant State Timeout	t_{DOUT}	200	360	520	µs
Propagation Loop Delay TX to RX, Recessive to Dominant Slew Rate 3 Slew Rate 2 Slew Rate 1 Slew Rate 0	t_{LRD}	 70 80 100 110	 140 155 180 220	 210 225 255 310	ns
Propagation Delay TX to CAN Slew Rate 3 Slew Rate 2 Slew Rate 1 Slew Rate 0	t_{TRD}	 20 40 60 100	 65 80 120 160	 110 150 200 300	ns
Propagation Delay CAN to RX, Recessive to Dominant	t_{RRD}	30	80	140	ns
Propagation Loop Delay TX to RX, Dominant to Recessive Slew Rate 3 Slew Rate 2 Slew Rate 1 Slew Rate 0	t_{LDR}	 70 90 100 130	 120 135 160 200	 170 180 220 260	ns
Propagation Delay TX to CAN Slew Rate 3 Slew Rate 2 Slew Rate 1 Slew Rate 0	t_{TDR}	 60 65 75 90	 110 120 150 190	 130 150 200 300	ns
Propagation Delay CAN to RX, Dominant to Recessive	t_{RDR}	20	40	60	

Notes

24. Guaranteed by design; however, it is not production tested.

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Non Differential Slew Rate (CANL or CANH)					V/µs
Slew Rate 3	t_{SL3}	4.0	19	40	
Slew Rate 2	t_{SL2}	3.0	13.5	20	
Slew Rate 1	t_{SL1}	2.0	8.0	15	
Slew Rate 0	t_{SL0}	1.0	5.0	10	

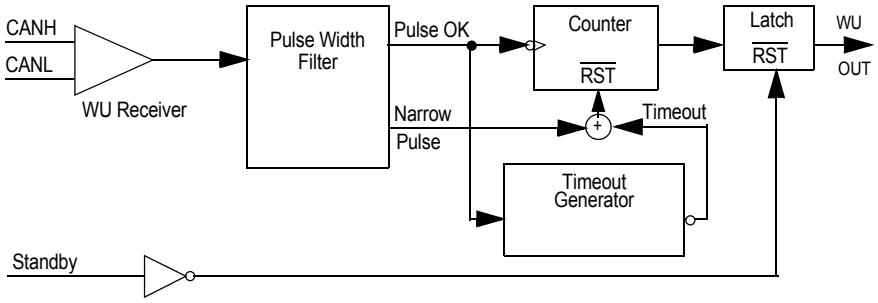
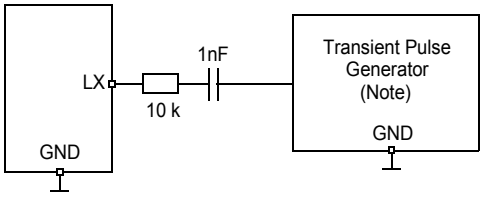


Figure 4. Wake-Up Block Diagram

The block diagram in **Figure 4** illustrates how the wake-up signal is generated. First the CAN signal is detected by a low consumption receiver (WU receiver). Then the signal passes through a pulse width filter which discards the undesired pulses. The pulse must have a width bigger than 0.5 µs and smaller than 500 µs to be accepted. When a pulse is discarded the pulse counter is reset and no wake signal is generated, otherwise when a pulse is accepted the pulse counter is incremental and after three pulses the wake signal is asserted.

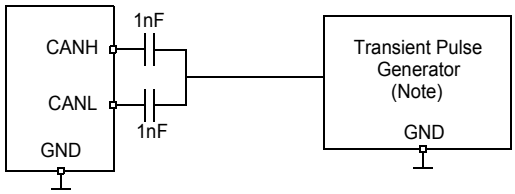


Note: Waveform in accordance to ISO 7637 part1, test pulses 1, 2, 3a and 3b.

Figure 5. Transient Test Pulse for L0:L3 Inputs

Each one of the pulses must be spaced by no more than 500 µs. In that case the pulse counter is reset and no wake signal is generated. This is accomplished by the wake timeout generator. The wake-up cycle is completed (and the wake flag reset) when the CAN interface is brought to *CAN Normal* mode.

The wake-up capability of the CAN can be disabled, refer to SPI interface and register section, CAN register.



Note: Waveform in accordance to ISO 7637 part1, test pulses 1, 2, 3a and 3b.

Figure 6. Transient Test Pulses for CANH/CANL

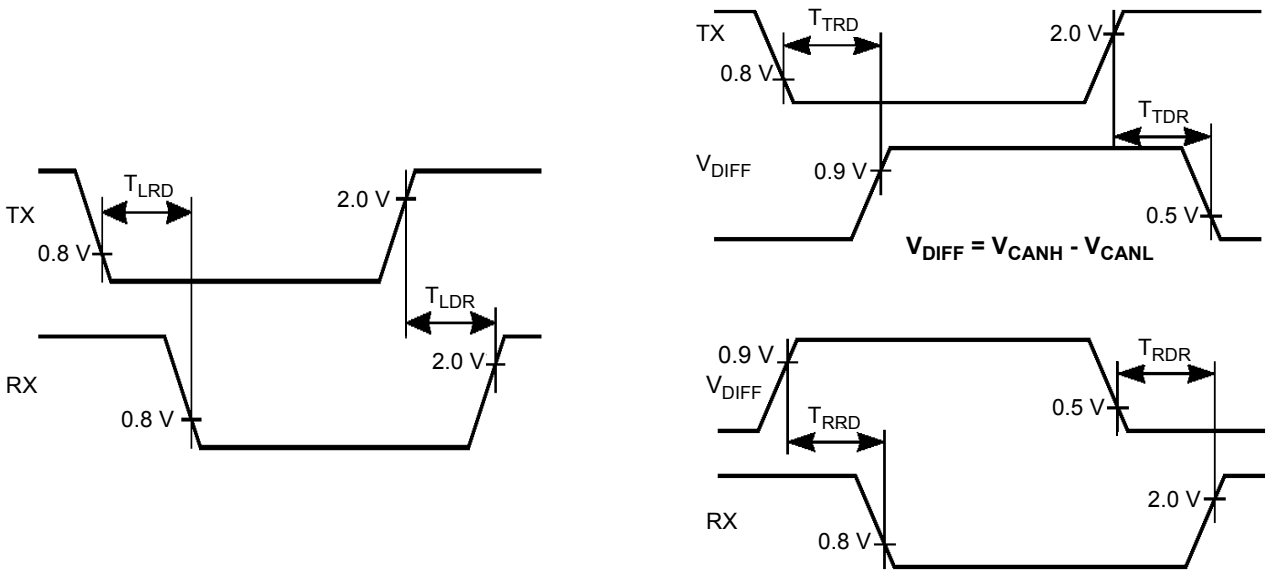
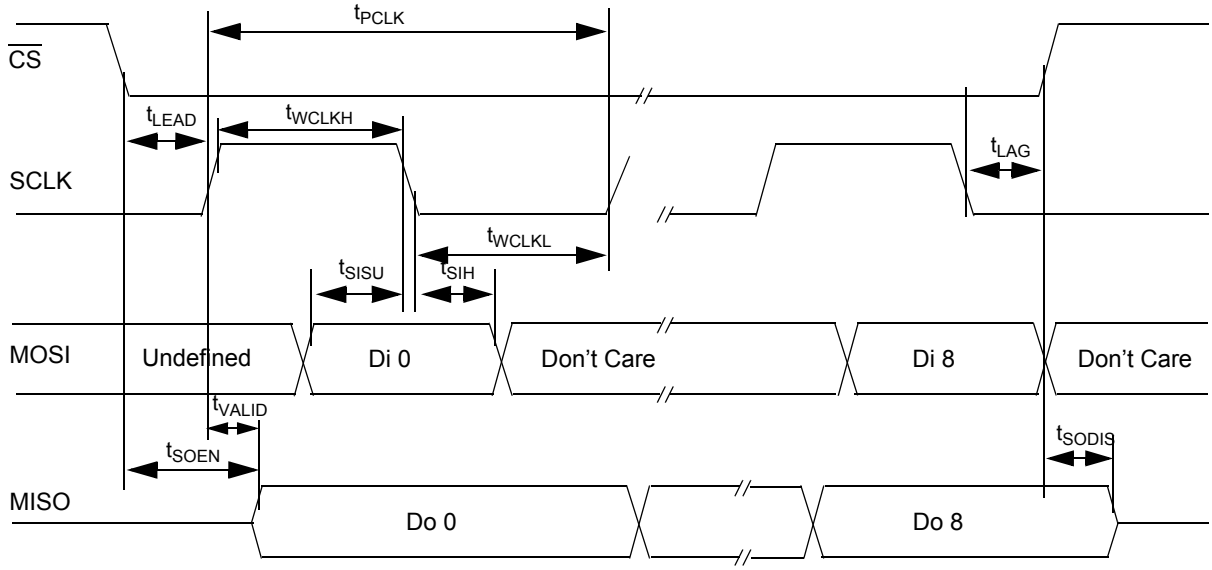


Figure 7. Transceiver AC Characteristics

TIMING DIAGRAMS



Notes:

Incoming data at MOSI terminal is sampled by the SBC at SCLK falling edge.

Outgoing data at MISO terminal is set by the SBC at SCLK rising edge (after t_{VALID} delay time).

Figure 8. SPI Timing Characteristics

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33989 is an integrated circuit dedicated to automotive applications. Its functions include:

- One full protected voltage regulator with 200 mA total output current capability available at V_{DD1} external terminal
- Driver for an external path transistor for the V2 regulator function
- Reset, programmable watchdog function, interrupt, and four operational modes
- Programmable wake-up input and Cyclic Sense wake-up
- CAN high-speed physical interface

FUNCTIONAL TERMINAL DESCRIPTION

RECEIVE AND TRANSMIT DATA (RXD AND TXD)

The RX and TX terminals (receive data and transmit data terminals, respectively) are connected to a microcontroller's CAN protocol handler. TXD is an input and controls the CANH and CANL line state (dominant when TXD is LOW, recessive when TXD is HIGH). RXD is an output and reports the bus state (RXD LOW when CAN bus is dominant, HIGH when CAN bus is recessive).

VOLTAGE DIGITAL DRAIN ONE (V_{DD1})

The V_{DD1} terminal is the output terminal of the 5.0 V internal regulator. It can deliver up to 200 mA. This output is protected against overcurrent and overtemperature. It includes an overtemperature pre-warning flag, which is set when the internal regulator temperature exceeds 130°C typical. When the temperature exceeds the overtemperature shutdown (170°C typical), the regulator is turned off.

V_{DD1} includes an undervoltage reset circuitry, which sets the $\overline{RST}$ terminal LOW when V_{DD1} is below the undervoltage reset threshold.

RESET ($\overline{RST}$)

The Reset terminal $\overline{RST}$ is an output that is set LOW when the device is in reset mode. The $\overline{RST}$ terminal is set HIGH when the device is not in reset mode. $\overline{RST}$ includes an internal pullup current source. When $\overline{RST}$ is LOW, the sink current capability is limited, allowing $\overline{RST}$ to be shorted to 5.0 V for software debug or software download purposes.

INTERRUPT ($\overline{INT}$)

The Interrupt terminal $\overline{INT}$ is an output that is set LOW when an interrupt occurs. $\overline{INT}$ is enabled using the Interrupt Register (INTR). When an interrupt occurs, $\overline{INT}$ stays LOW until the interrupt source is cleared.

$\overline{INT}$ output also reports a wake-up event by a 10 µs typical pulse when the device is in Stop mode.

VOLTAGE SOURCE TWO (V2)

The V2 terminal is the input sense for the V2 regulator. It is connected to the external series pass transistor. V2 is also the 5.0 V supply of the internal CAN interface. It is possible to connect V2 to an external 5.0 V regulator or to the V_{DD1} output when no external series pass transistor is used. In this case, the V2CTRL terminal must be left open.

VOLTAGE SOURCE 2 CONTROL (V2CTRL)

The V2CTRL terminal is the output drive terminal for the V2 regulator connected to the external series pass transistor.

VOLTAGE SUPPLY (V_{SUP})

The V_{SUP} terminal is the battery supply input of the device.

HIGH-SIDE ONE (HS1)

The HS1 terminal is the internal high-side driver output. It is internally protected against overcurrent and overtemperature.

LEVEL 0-3 INPUTS (L0:L3)

The L0:L3 terminals can be connected to contact switches or the output of other ICs for external inputs. The input states can be read by SPI. These inputs can be used as wake-up events for the SBC when operating in the Sleep or Stop mode.

CAN HIGH AND CAN LOW OUTPUTS (CANH AND CANL)

The CAN High and CAN Low terminals are the interfaces to the CAN bus lines. They are controlled by TX input level, and the state of CANH and CANL is reported through RX output. A 60 Ω termination resistor is connected between CANH and CANL terminals.

SYSTEM CLOCK (SCLK)

SCLK is the System Clock input terminal of the serial peripheral interface.

MASTER IN SLAVE OUT (MISO)

MISO is the Master In Slave Out terminal of the serial peripheral interface. Data is sent from the SBC to the microcontroller through the MISO terminal.

MASTER OUT SLAVE IN (MOSI)

MOSI is the Master Out Slave In terminal of the serial peripheral interface. Control data from a microcontroller is received through this terminal.

CHIP SELECT ($\overline{CS}$)

$\overline{CS}$ is the Chip Select terminal of the serial peripheral interface. When this terminal is LOW, the SPI port of the device is selected.

WATCHDOG ($\overline{WD}$)

The Watchdog output terminal is asserted LOW to flag that the software watchdog has not been properly triggered.

FUNCTIONAL DEVICE OPERATION

DEVICE SUPPLY

The device is supplied from the battery line through the V_{SUP} terminal. An external diode is required to protect against negative transients and reverse battery. It can operate from 4.5 V and under the jump start condition at 27 Vdc. This terminal sustains standard automotive voltage conditions such as load dump at 40 V. When V_{SUP} falls below 3.0 V typical the 33989 detects it and stores the information into the SPI register in a bit called *BATFAIL*. This detection is available in all operation modes.

The device incorporates a battery early warning function, providing a maskable interrupt when the V_{SUP} voltage is below 6.0 V typical. A hysteresis is included. Operation is only in Normal and Standby modes. V_{SUP} low is reported in the Input/Output Register (IOR).

V_{DD1} VOLTAGE REGULATOR

The V_{DD1} Regulator is a 5.0 V output voltage with output current capability up to 200 mA. It includes a voltage monitoring circuitry associated with a reset function. The V_{DD1} regulator is fully protected against overcurrent and short-circuit. It has over- temperature detection warning flags (bit V_{DDTEMP} in MCR and interrupt registers), and overtemperature shutdown with hysteresis.

V2 REGULATOR

V2 Regulator circuitry is designed to drive an external path transistor increasing output current flexibility. Two terminals are used to achieve the flexibility. Those terminals are V2 and V2 control. The output voltage is 5.0 V and is realized by a tracking function of the V_{DD1} regulator. The recommended ballast transistor is MJD32C. Other transistors can be used; however, depending upon the PNP gain an external resistor-capacitor network might be connected. The V2 is the supply input for the CAN cell. The state of V2 is reported in the IOR (bit V2LOW set to 1 if V2 is below 4.5 V typical).

HS1 V_{BAT} SWITCH OUTPUT

The HS1 output is a 2.0 Ω typical switch from the V_{SUP} terminal. It allows the supply of external switches and their associated pull-up or pull down circuitry, in conjunction with the wake-up input terminals, for example. Output current is limited to 200 mA and HS1 is protected against short-circuit and has an overtemperature shutdown (bit HS1OT in IOR and bit HS1OT-V2LOW in $\overline{\text{INT}}$ register). The HS1 output is controlled from the internal register and the SPI. Because of an internal timer, it can be activated at regular intervals in Sleep and Stop modes. It can also be permanently turned on in Normal or Standby modes to drive loads or supply peripheral components. No internal clamping protection circuit is implemented, thus a dedicated external protection circuit is required in case of inductive load drive.

BATTERY FALL EARLY WARNING

Refer to the discussion under the heading: Device Supply.

INTERNAL CLOCK

The device has an internal clock used to generate all timings (Reset, Watchdog, Cyclic Wake-up, Filtering Time, etc.). Two oscillators are implemented. A high accuracy (±12 percent) used in Normal Request, Normal and Standby modes, and a low accuracy (±30 percent) used in Sleep and Stop modes.

OPERATIONAL MODES

FUNCTIONAL MODES

The device has four primary operation modes:

1. Standby mode
2. Normal mode
3. Stop mode
4. Sleep mode

All modes are controlled by the SPI. An additional temporary mode called Normal Request mode is automatically accessed by the device after reset or wake-up from Stop mode. A Reset ($\overline{RST}$) mode is also implemented. Special modes and configuration are possible for debug and program MCU flash memory.

STANDBY MODE

Only regulator 1 is ON. Regulator 2 is turned OFF by disabling the V2 control terminal. Only the wake-up capability of the CAN interface is available. Other functions available are wake-up input reading through SPI and HS1 activation. The Watchdog is running.

NORMAL MODE

In this mode both regulators are ON. This corresponds to the normal application operation. All functions are available in this mode (Watchdog, wake-up input reading through SPI, HS1 activation, CAN communication). The software Watchdog is running and must be periodically cleared through SPI.

STOP MODE

Regulator 2 is turned OFF by disabling the V2 control terminal. The regulator 1 is activated in a special low power mode, allowing to deliver few mA. The objective is to maintain the MCU of the application supplied while it is turned into power saving condition (i.e Stop or Wait modes). In Stop mode the device supply current from V_{BAT} is very low.

When the application is in Stop mode (both MCU and SBC), the application can wake-up from the SBC side (for example: cyclic sense, forced wake-up, CAN message, wake-up inputs and over current on V_{DD1}), or the MCU side (key wake-up, etc.).

Stop mode is always selected by the SPI. In Stop mode the software Watchdog can be *running* or *idle* depending upon selection by the SPI (RCR, bit WDSTOP). To clear the watchdog, the SBC must be awakened by a $\overline{CS}$ terminal (SPI wake-up). In Stop mode, SBC wake-up capability are identical as in Sleep mode. Please refer to **Table 5**.

SLEEP MODE

Regulators 1 and 2 are OFF. The current from V_{SUP} terminal is reduced. In this mode, the device can be awakened internally by cyclic sense via the wake-up inputs terminals and HS1 output, from the *forced wake-up* function and from the CAN physical interface. When a wake-up occurs the SBC goes first into reset mode before entering Normal Request mode.

RESET MODE

In this mode, the Reset ($\overline{RST}$) terminal is low and a timer is running for a time RST_{DUR}. After this time is elapsed, the SBC enters Normal Request mode. Reset mode is entered if a reset condition occurs (V_{DD1} low, watchdog timeout or watchdog trigger in a closed window).

NORMAL REQUEST MODE

This is a temporary mode automatically accessed by the device after the reset mode, or after the SBC wake-up from Stop mode. After wake-up from the Sleep mode or after the device power-up, the SBC enters the Reset mode before entering the Normal Request mode. After a wake-up from the Stop mode, the SBC enters Normal Request mode directly.

In Normal Request mode the V_{DD1} regulator is ON, V2 is OFF, the reset terminal is high. As soon as the device enters the Normal Request mode an internal 350 ms timer is started. During these 350 ms the microcontroller of the application must address the SBC via the SPI, configuring the Watchdog register. This is the condition for the SBC to stop the 350 ms timer and to go into the Normal or Standby mode and to set the watchdog timer according to configuration.

NORMAL REQUEST ENTERED AND NO $\overline{WD}$ CONFIGURATION OCCURS

In case the Normal Request mode is entered after SBC power-up, or after a wake-up from Stop mode, and if no $\overline{WD}$ configuration occurs while the SBC is in Normal Request mode, the SBC goes to Reset mode after the 350 ms time period is expired before again going into Normal Request mode. If no $\overline{WD}$ configuration is achieved, the SBC alternatively goes from Normal Request into reset, then Normal Request modes etc.

In case the Normal Request mode is entered after a wake-up from Sleep mode, and if no $\overline{WD}$ configuration occurs while the SBC is in Normal Request mode, the SBC goes back to Sleep mode.

APPLICATION WAKE-UP FROM SBC SIDE

When an application is in Stop mode, it can wake-up from the SBC side. When a wake-up is detected by the SBC (for example, CAN, Wake-up input, etc.) the SBC turns itself into Normal Request mode and generates an interrupt pulse at the $\overline{INT}$ terminal.

APPLICATION WAKE-UP FROM MCU SIDE

When application is in Stop mode, the wake-up event may come from the MCU side. In this case the MCU signals to the SBC by a low to high transition on the $\overline{CS}$ terminal. Then the SBC goes into Normal Request mode and generates an interrupt pulse at the $\overline{INT}$ terminal.

STOP MODE CURRENT MONITOR

If the V_{DD1} output current exceed an internal threshold (I_{DD1SWU}), the SBC goes automatically into Normal Request mode and generates an interrupt at the $\overline{INT}$ terminal. The interrupt is not maskable and the interrupt register will has no flag set.

INTERRUPT GENERATION WHEN WAKE-UP FROM STOP MODE

When the SBC wakes up from Stop mode, it first enters the Normal Request mode before generating a pulse (10 µs typical) on the $\overline{INT}$ terminal. These interrupts are not maskable, and the wake-up event can be read through the SPI registers (CANWU bit in Reset Control Register (RCR) and LCTRx bit in Wake-Up Register (WUR). In case of wake-up from Stop mode over current or from forced wake-up, no bit is set. After the $\overline{INT}$ pulse the SBC accept SPI command after a time delay ($t_{S1STSPI}$ parameter).

SOFTWARE WATCHDOG IN STOP MODE

If Watchdog is enabled, the MCU has to wake-up independently of the SBC before the end of the SBC watchdog time. In order to do this the MCU must signal the wake-up to the SBC through the SPI wake-up ($\overline{CS}$ activation). The SBC then wakes up and jumps into the Normal Request mode. MCU has to configured the SBC to go to either Normal or Standby mode. The MCU can then decide to go back again to Stop mode.

When there is no MCU wake-up occurring within the watchdog timing, the SBC activates the Reset terminal, jumping into the Normal Request mode. The MCU can then be initialized.

STOP MODE ENTER COMMAND

Stop mode is entered at the end of the SPI message, and at the rising edge of the $\overline{CS}$. Please refer to the $t_{\overline{CS}STOP}$ data in Dynamic Electrical Characteristics table on page 11.

Once Stop mode is entered the SBC could wake-up from the V1 regulator over current detection. In order to allow time for the MCU to complete the last CPU instruction, allowing MCU to enter its low power mode, a deglitcher time of typical 40 µs is implemented.

Figure 9 indicates the operation to enter Stop mode.

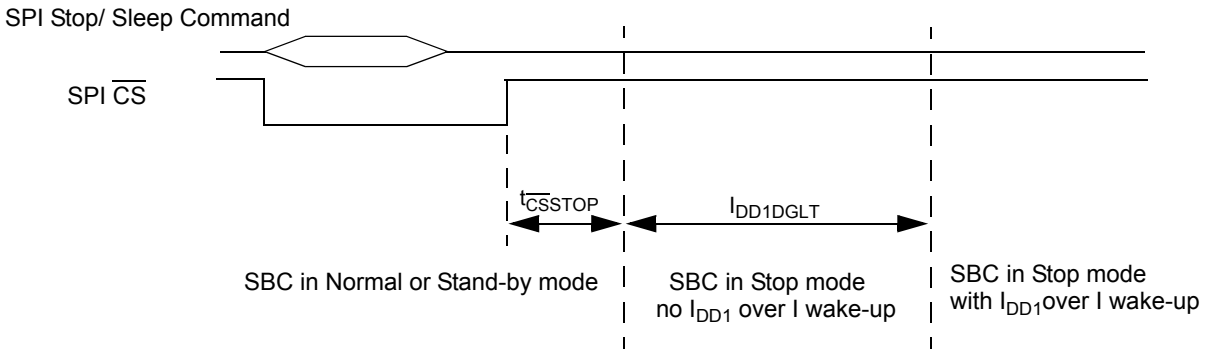


Figure 9. Operation Entering Stop Mode

RESET AND WATCHDOG TERMINALS, SOFTWARE WATCHDOG OPERATIONS

SOFTWARE WATCHDOG (SELECTABLE WINDOW OR TIMEOUT WATCHDOG)

Software watchdog uses in the SBC Normal and Standby modes is to monitor MCU. The Watchdog can be either window or timeout. This is selectable by SPI (register TIM1, bit WDW). Default is window watchdog. The period for the watchdog is selectable from the SPI from 10 ms to 350 ms (register TIM1, bits WDT0 and WDT1). When the window watchdog is selected, the closed window is the first part of the selected period, and the open window is the second part of the period. Refer to the SPI TIM register description. Watchdog can only be cleared within the open window time. An attempt to clear the watchdog in the closed window will generate a reset. Watchdog is cleared through SPI by addressing the TIM1 register.

RESET TERMINAL DESCRIPTION

A reset output is necessary and available to reset the microcontroller. Modes 1 and 2 are available for the reset terminal (please refer to **Table 5** for reset terminal operation).

Reset causes when SBC is in mode 1:

- V_{DD1} falling out of range — If V_{DD1} falls below the reset threshold (parameter R_{STTH}), the ret terminal is pulled low until V_{DD1} returns to the normal voltage.
- Power-on reset — At device power-on or at device wake-up from Sleep mode, the reset is maintained low until V_{DD1} is within its operation range.

Watchdog timeout — If watchdog is not cleared, the SBC will pull the reset terminal low for the duration of the reset time (parameter $RST_{DUR)}$.

Table 5. Reset and Watchdog Output Operation

Events	Mode	$\overline{WD}$ Output	Reset Output
Devices Power-up	1 or 2 (Safe Mode)	Low to High	Low to High
V_{DD1} Normal Watchdog Properly Triggered	1	High	High
$V_{DD1} < RST_{TH}$	1	High	Low
Watchdog Timeout Reached	1	Low (Note)	Low
V_{DD1} Normal Watchdog Properly Triggered	2 (Safe Mode)	High	High
$V_{DD1} < RST_{TH}$	2 (Safe Mode)	High	Low
Watchdog Timeout Reached	2 (Safe Mode)	Low (Note)	High

Notes
25. $\overline{WD}$ stays low until the Watchdog register is properly addressed through SPI.

In Mode 2, the reset terminal is not activated in case of Watchdog timeout. Please refer to **Table 6** for more detail.

For debug purposes at 25°C, the Reset terminal can be shorted to 5.0 V because of its internal limited current drive capability.

RESET AND WATCHDOG OPERATION: MODES1 AND 2

Watchdog and Reset functions have two modes of operation:

1. Mode 1
2. Mode 2 (also called Safe mode)

These modes are independent of the SBC modes (Normal, Standby, Sleep, and Stop). Modes 1 and 2 selection is achieved through the SPI (register MCR, bit SAFE). Default mode after reset is Mode 1.

Table 5 provides Reset and Watchdog output mode of operation. Two modes (modes 1 and 2) are available and can be selected through the SPI Safe bit. Default operation, after reset or power-up, is Mode 1.

In both modes reset is active at device power-up and wake-up.

- In mode 1–Reset is activated in case of V_{DD1} fall or watchdog not triggered. $\overline{WD}$ output is active low as soon as reset goes low. It remains low as long as the watchdog is not properly re-activated by the SPI.
- In mode 2–(Safe mode) Reset is not activated in case of watchdog fault. $\overline{WD}$ output has the same behavior as in mode 1–The Watchdog output terminal is a push-pull structure driving external components of the application for signal instance of an MCU wrong operation.

Table 6. Table of Operation

Mode	Voltage Regulator HS1 Switch	Wake-up Capabilities (if enabled)	Reset Terminal	$\overline{\text{INT}}$	Software Watchdog	CAN Cell
Normal Request	V_{DD1}:ON V2:OFF HS1:OFF	—	Low for Reset-DUR Time, then High	—	—	—
Normal	V_{DD1}:ON V2:ON HS1:Controllable	—	Normally High Active Low if $\overline{\text{WD}}$ or V_{DD1} under voltage occurs (and mode 1 selected)	If Enabled, Signal Failure (V_{DD1} Pre-Warning Temp, CAN, HS1)	Running	Tx/Rx
Standby	V_{DD1}:ON V2:OFF HS1:Controllable	—	Same as Normal Mode	Same as Normal Mode	Running	Low Power
Stop	V_{DD1}:ON (Limited Current Capability) V2:OFF HS1:OFF or Cyclic	CAN SPI L0:L3 Cyclic Sense Forced Wake-up I_{DD1} Over Current (26)	Normally High Active Low if $\overline{\text{WD}}$ (27) or V_{DD1} Under Voltage Occurs	Signal SBC Wake-up and IDD > $I_{DD1S/WU}$ (Not Maskable)	Running if Enabled Not Running if Disabled	Low Power Wake-up Capability if Enabled
Sleep	V_{DD1}:OFF V2:OFF HS1:OFF or Cyclic	CAN SPI L0:L3 Cyclic Sense Forced Wake-up	Low	Not Active	Not Running	Low Power Wake-up Capability if Enabled
Debug Normal	Same as Normal	—	Normally High Active Low if V_{DD1} Under Voltage Occurs	Same as Normal	Not Running	Same as Normal
Debug Standby	Same as Standby	—	Normally High Active Low if V_{DD1} Under Voltage Occurs	Same as Standby	Not Running	Same as Standby
Stop Debug	Same as Stop	Same as Stop	Normally High Active Low if V_{DD1} Under Voltage Occurs	Same as Stop	Not Running	Same as Stop
Flash Programming	Forced Externally	—	Not Operating	Not Operating	Not Operating	Not Operating

Notes
26. Always enable.
27. If enabled.

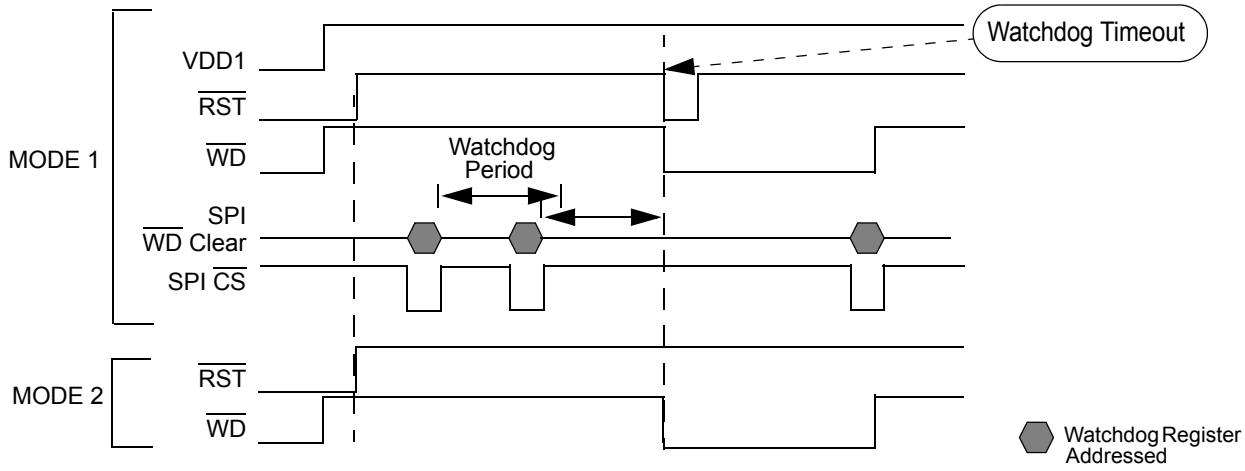


Figure 10. Reset and Watchdog Functions Diagram in Modes 1 and 2

WAKE-UP CAPABILITIES

Several wake-up capabilities are available for the device when it is in Sleep, or Stop modes. When a wake-up has occurred, the wake-up event is stored into the WUR or CAN registers. The MCU can then access to the wake-up source. The wake-up options are able to be selected through the SPI while the device is in Normal or Standby mode and prior to entering low power mode (Sleep or Stop mode). When a wake-up occurs from sleep mode the device activates V_{DD1}. It generates an interrupt if wake-up occurs from Stop mode.

WAKE-UP FROM WAKE-UP INPUTS (L0:L3) WITHOUT CYCLIC SENSE

The wake-up lines are dedicated to sense external switch states and if changes occur to wake-up the MCU (in Sleep or Stop modes). The wake-up terminals are able to handle 40 V DC. The internal threshold is 3.0 V typical and these inputs can be used as an input port expander. The wake-up inputs state are read through SPI (register WUR).

In order to select and activate direct wake-up from the LX inputs, the WUR register must be configured with the appropriate level sensitivity. Additionally, the LPC register must be configured with 0x0 data (bits LX2HS1and HS1AUTO are set at 0).

Level sensitivity is selected by WUR register. Level sensitivity is configured by a pair of Lx inputs: L0 and L1 level sensitivity are configured together while L2 and L3 are configured together.

CYCLIC SENSE WAKE-UP (CYCLIC SENSE TIMER AND WAKE-UP INPUTS L0, L1, L2, L3)

The SBC can wake-up upon state change of one of the four wake-up input lines (L0, L1, L2 and L3) while the external pull-up or pull down resistor of the switches associated to the wake-up input lines are biased with HS1 V_{SUP} switch. The HS1 switch is activated in Sleep or Stop modes from an internal timer. Cyclic Sense and Forced Wake-up are exclusive. If Cyclic Sense is enabled the forced wake-up can not be enabled.

In order to select and activate the cyclic sense wake-up from the Lx inputs the WUR register must be configured with the appropriate level sensitivity, and the LPC register must be configured with 1xx1 data (bit LX2HS1 set at 1 and bit HS1AUTO set at 1). The wake-up mode selection (direct or cyclic sense) is valid for all 4 wake-up inputs.

FORCED WAKE-UP

The SBC can wake-up automatically after a predetermined time spent in Sleep or Stop mode. Cyclic sense and Forced wake-up are exclusive. If Forced wake-up is enabled (FWU bit set to 1 in LPC register) the Cyclic Sense can not be enabled.

CAN INTERFACE WAKE-UP

The device incorporates a high-speed 1MBaud CAN physical interface. Its electrical parameters for the CANL, CANH, RX and TX terminals are compatible with ISO 11898 specification (IS0 11898: 1993(E)). The control of the CAN physical interface operation is accomplished through the SPI. CAN modes are independent of the SBC operation modes.

The device can wake-up from a CAN message if the CAN wake-up is enabled. Please refer to the CAN module description for detail of wake-up detection.

SPI WAKE-UP

The device can wake-up by the $\overline{CS}$ terminal in Sleep or Stop modes. Wake-up is detected by the $\overline{CS}$ terminal transition from low to a high level. In Stop mode, this corresponds with the condition where the MCU and SBC are in Stop mode; and when the application wake-up event comes through the MCU.

DEVICE POWER-UP, SBC WAKE-UP

After device or system power-up, or after the SBC wakes up from Sleep mode, it enters into Reset mode prior to moving into Normal Request mode.

DEBUG MODE: HARDWARE AND SOFTWARE DEBUG WITH THE SBC

When the SBC is mounted on the same printed circuit board as the microcontroller it supplies, both application software and SBC dedicated routine must be debugged. The following features allow debug of the software by allowing the possibility of disabling the SBC internal software Watchdog timer.

DEVICE POWER-UP, RESET TERMINAL CONNECTED TO V_{DD1}

At SBC power-up the V_{DD1} voltage is provided, but if no SPI communication occurs to configure the device, a reset occurs every 350 ms. In order to allow software debug and avoid MCU reset, the Reset terminal can be connected directly to V_{DD1} by a jumper.

DEBUG MODES WITH SOFTWARE WATCHDOG DISABLED THOUGH SPI (NORMAL DEBUG, STANDBY AND STOP DEBUG)

The Watchdog software can be disabled through SPI. To avoid unwanted watchdog disable while limiting the risk of disabling Watchdog during SBC normal operation, the watchdog disable must be achieved the following sequence:

- Step 1–Power down the SBC
- Step 2–Power-up the SBC (The BATFAIL bit is set, allowing the SBC to enter Normal Request mode)
- Step 3–Write to TIM1 register allowing SBC entering Normal mode
- Step 4–Write to MCR register with data 0000, enabling the Debug mode. Complete SPI byte: 000 1 0000
- Step 5–Write to MCR register normal debug (0001x101)
- Step 6–To leave the Debug mode, write 0000 to MCR register

While in Debug mode, the SBC can be used without having to clear the $\overline{WD}$ on a regular basis to facilitate software and hardware debug.

At Step 2, the SBC is in Normal Request. Steps 3, 4, and 5 should be completed consecutively and within the 350 ms time period of the Normal Request mode. If this step is not accomplished in a timely manner, the SBC will go into Reset mode, entering Normal Request again.

When the SBC is in Debug mode, and set in Stop Debug or Sleep Debug, when a wake-up occurs the SBC enters Normal Request mode for a time period of 350 ms. To avoid the SBC generating a reset (enter Reset mode) the desired next Debug mode (Normal Debug or Standby Debug) should be configured within the 350 ms time period of the Normal Request mode. For details, please refer to State Machine in Debug mode, **Figure 16**.

To avoid entering Debug mode after a power-up, first read BATFAIL bit (MCR read) and write 0000 into MCR. **Figure 15** illustrates the Debug mode enter.

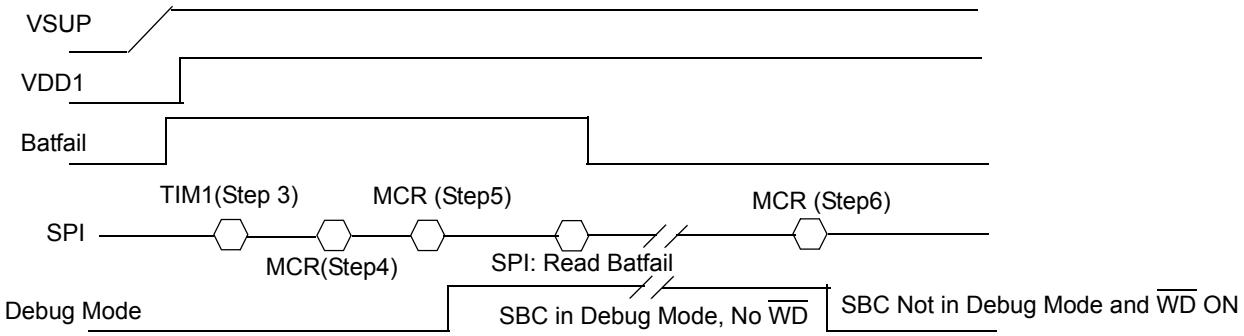


Figure 11. Debug Mode Enter

MCU FLASH PROGRAMMING CONFIGURATION

To download software into the application memory (MCU EEPROM or Flash) the SBC capabilities allows the V_{DD1} to be forced by an external power supply to 5.0 V; the reset and $\overline{WD}$ outputs by external signal sources are forced to zero or 5.0 V, both without damage. This allows, for example, supply of the complete application board by external power supply, applying the correct signal to reset terminals. No function of the SBC is operating.

Due to pass transistor from V_{DD1} to V_{SUP}, supplying the device from V_{DD1} terminal biases the V_{SUP} terminal. Therefore, V_{SUP} should not be forced to a value above 5.0 V. The Reset terminal is periodically pulled low for RST_{DUR} time (3.4 ms typical) before being pulled to V_{DD1} for 350 ms typical. During the time reset is low, the reset terminal sinks 5.0 mA maximum (L_{PDW} parameter).

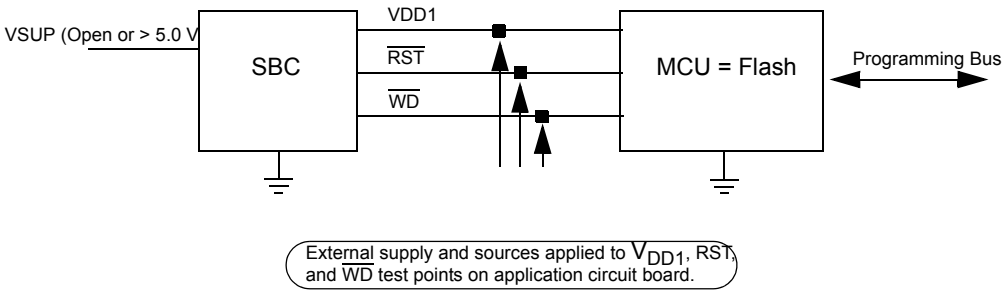
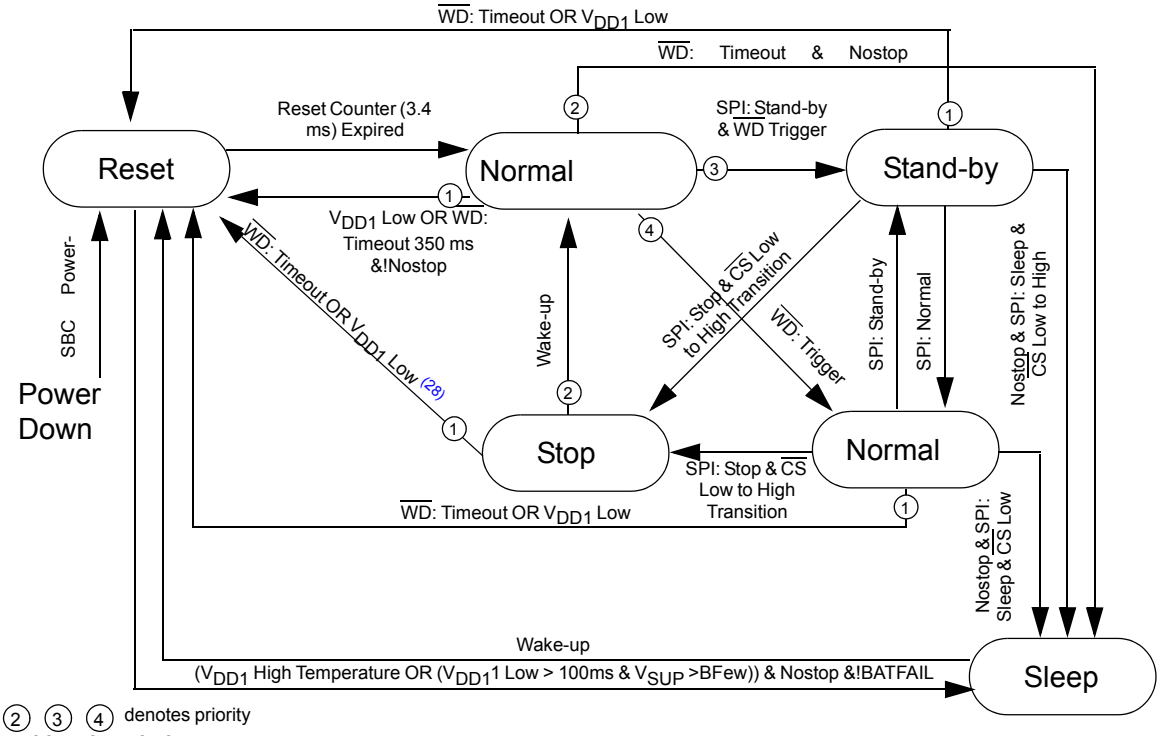


Figure 12. Simplified Schematic for Flash Programming

PACKAGE AND THERMAL CONSIDERATION

The device is proposed in a standard surface mount SOIC28 package. In order to improve the thermal performances of the SOIC28 package, eight terminals are internally connected to the lead frame and are used for heat transfer to the printed circuit board.

Table 6, page 23, describes the SBC operation modes. Normal, Stand-by, and Stop Debug modes are entered through special sequence described in the Debug mode paragraph.



State machine description:

25. Nostop = Nostop bit = 1
26. ! Nostop = Nostop bit = 0
27. BATFAIL = Batfail bit = 1
28. ! BATFAIL = Batfail bit = 0
29. V_{DD1} Over Temperature = V_{DD1} thermal shutdown occurs
30. V_{DD1} low = V_{DD1} below reset threshold
31. V_{DD1} low >100 ms = V_{DD1} below reset threshold for more than 100 ms
32. $\overline{WD}$: Trigger = TIM1 register write operation.

Figure 13. State Machine (Not Valid in Debug Modes)

Notes These two SPI commands must be sent consecutively in this sequence.

28. If $\overline{WD}$ activated.

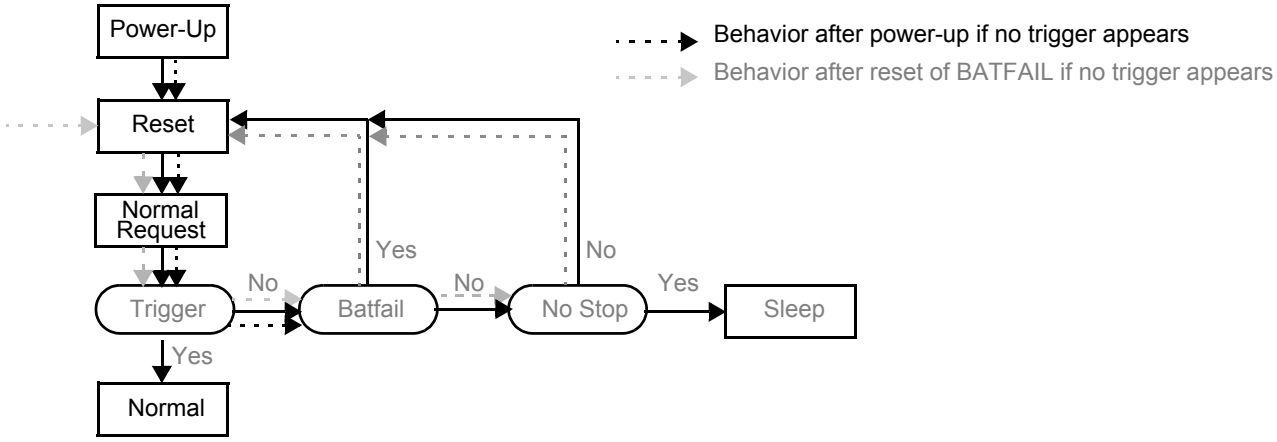


Figure 14. Behavior at SBC Power-Up

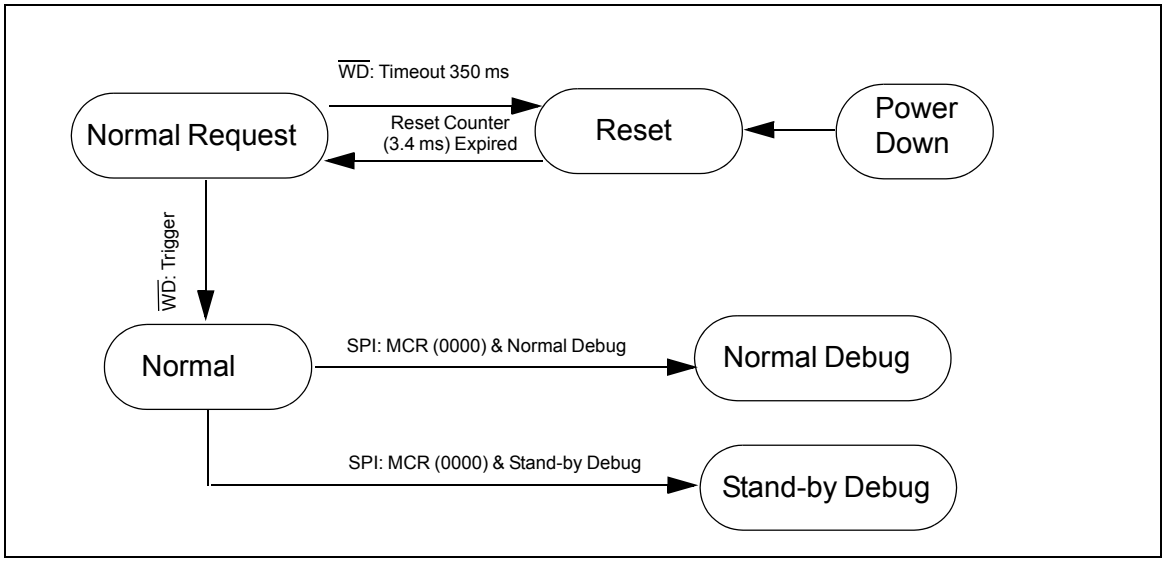
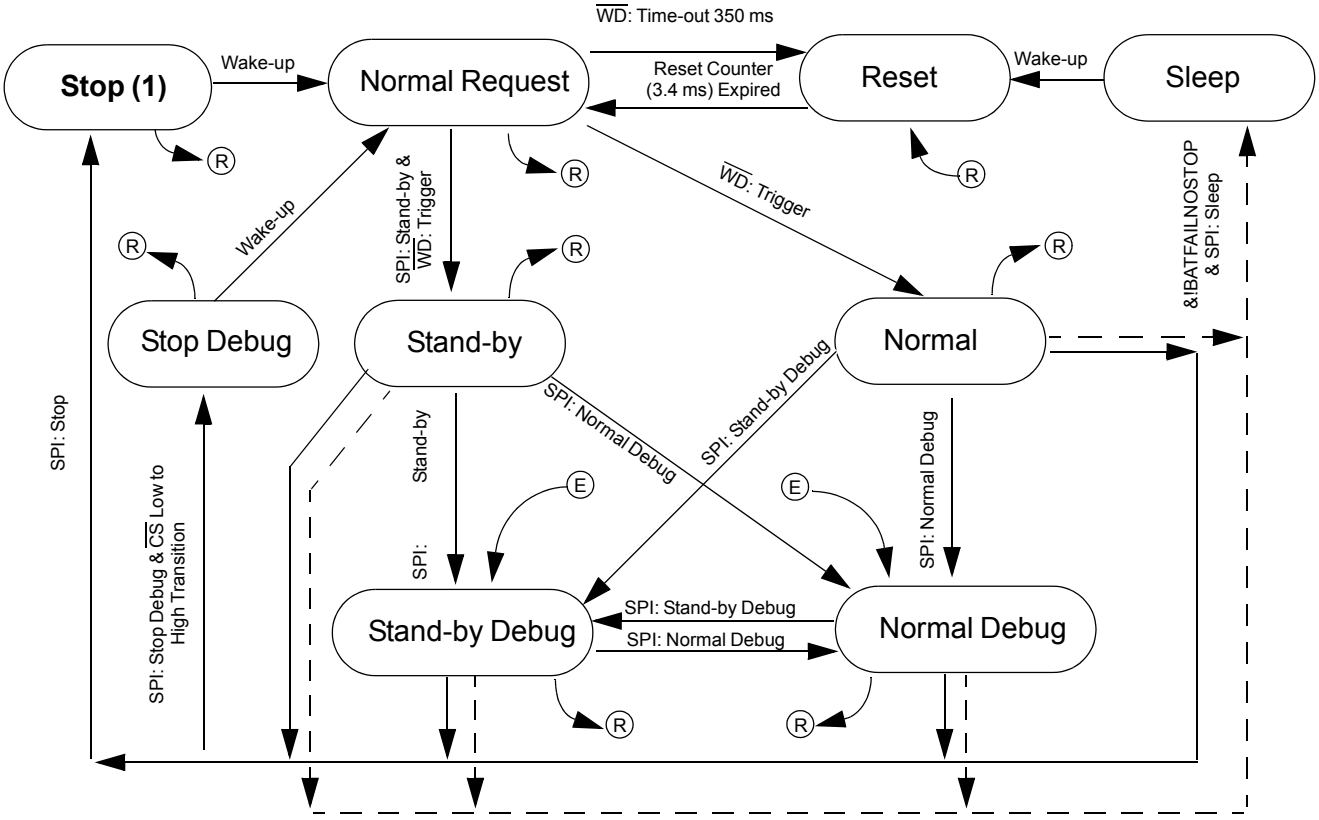


Figure 15. Transitions to Enter Debug Modes



(1) If Stop mode entered, it is entered without watchdog, no matter the WDSTOP bit.
(E) Debug mode entry point (Step 5 of the Debug mode entering sequence).
(R) Represents transitions to Reset mode due to V_{DD1} low.

Figure 16. Simplified State Machine in Debug Modes

LOGIC COMMANDS AND REGISTERS

SPI INTERFACE AND REGISTER DESCRIPTION

Table 7 illustrates a register, an 8-bit SPI. The first three bits are used to identify the internal SBC register address. Bit four is a read/write bit. The last four bits are *Data Send* from MCU to SBC, or read back from SBC to MCU.

There is no significance during write operation state of MISO.

During read operation only the final four bits of MISO have a meaning (content of the accessed register).

The following tables describe the SPI register list, and register bit meaning.

Registers reset value is also described along with the reset condition. Reset condition is the condition causing the bit to be set at the reset value.

Table 7. Data Format Description

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A2	A1	A0	R/W	D3	D2	D1	D0

Read operation: R/W Bit = 0
Write operation: R/W Bit = 1
Possible reset conditions include:

SBC Reset:	Power-On Reset POR
SBC Mode Transition:	NR2R - Normal Request to Reset Mode
	NR2N - Normal Request to Normal Mode
	NR2STB - Normal Request to Standby Mode
	N2R - Normal to Reset Mode
	STB2R - Standby to Reset Mode
	STO2R - Stop to Reset Mode
	STO2NR - Stop to Normal Request
SBC Mode:	RESET - SBC in Reset Mode

Table 8. List of Registers

Name	Address	Description	Comment and Use
MCR	$000	Mode Control Register	Write: Control of Normal, Standby, Sleep, Stop, Debug Modes Read: BATFAIL flag and other status bits and flags
RCR	$001	Reset Control Register	Write: Configuration for reset voltage level, Safe bit, Stop mode Read: CAN wake-up and CAN failure status bits
CAN	$010	CAN Control Register	Write: CAN module control: TX/RX and Sleep modes, slope control, wake enable/disable Read: CAN wake-up and CAN failure status bits
IOR	$011	I/O Control Register	Write: HS1 (High Side switch) control in Normal and Standby mode Read: HS1 over temp bit, V_{SUP} and V2 Low status
WUR	$100	Wake-up Input Register	Write: Control of wake-up input polarity Read: Wake-up input and real time LX input state
TIM	$101	Timing Register	Write: TIM1, Watchdog timing control, window, or Timeout mode Write: TIM2, Cyclic sense and force wake-up timing selection
LPC	$110	Low Power Mode Control Register	Write: Control HS1 periodic activation in Sleep and Stop modes, force wake-up
$\overline{\text{INT}}$	$111	Interrupt Register	Write: Interrupt source configuration Read: $\overline{\text{INT}}$ source

Mode Control Register (MCR)

Table 9 provides Mode Control Register data.

Table 9. MCR Register

MCR		D3	D2	D1	D0
$000B	W	—	MCTR2	MCTR1	MCTR0
	R	BATFAIL (29)	VDDTEMP	GFAIL	WDRST
Reset Value		—	0	0	0
Reset Condition		—	POR, RESET	POR, RESET	POR, RESET

Notes
29. Bit BATFAIL cannot be set by SPI. BATFAIL is set when V_{SUP} falls below 3.0 V.

Table 10. MCR Control Bits

MCTR2	MCTR1	MCTR0	SBC Mode	Description
0	0	0	Enter/Exit Debug Mode	To enter/exit Debug Mode, refer to detail Debug Mode: Hardware and Software Debug...
0	0	1	Normal	—
0	1	0	Standby	—
0	1	1	Stop, Watchdog OFF (30)	—
0	1	1	Stop, Watchdog ON (30)	—
1	0	0	Sleep (31)	—
1	0	1	Normal	No watchdog running, Debug Mode
1	1	0	Standby	
1	1	1	Stop	

Notes
30. Watchdog ON or OFF depends on RCR bit D3.
31. Before entering Sleep mode, bit BATFAIL in MCR must be previously cleared (MCR read operation), and bit NOSTOP in RCR must be previously set to 1.

Table 11. MCR Status Bits

Status Bits	Description
GFAIL	Logic OR of CAN Failure (TXF Permanent Dominant, or CAN Over Current or CAN thermal), or HS1 Over Temperature, or V2 Low
BATFAIL	Battery Fail Flag (set when V_{SUP} < 3.0 V)
VDDTEMP	Temperature Pre-Warning on V_{DD} (latched)
WDRST	Watchdog Reset Occurred

Reset Control Register (RCR)

Table 12 provides Reset Control Register data while Table 13 outlines the RCR Control Bits, and Table 14 provides RCR Status Bits data.

Table 12. RCR Register

RCR		D3	D2	D1	D0
$001B	W	WDSTOP	NOSTOP	SAFE	RSTTH
	R				
Reset Value		1	0	0	0
Reset Condition		POR,RST, STO2NR	POR, NR2N NR2STB	POR	POR

Table 13. RCR Control Bits

SAFE	$\overline{\text{WD}}$ Terminal	Reset Terminal	Condition
0 1	0	0 = > 1	Device Power-Up
0 1	1	1 1	V1 Normal, $\overline{\text{WD}}$ Properly Triggered
0 1	1 1	0 1	V1 Drops Below R_{STTH}
0 1	0	0 1	$\overline{\text{WD}}$ Timeout

Table 14. RCR Status Bits

Status Bits	Bit Value	Description
WDSTOP	0	No Watchdog in Stop Mode
	1	Watchdog Runs in Stop Mode
NOSTOP	0	Device Cannot Enter Sleep Mode
	1	Sleep Mode Allowed, Device Can Enter Sleep Mode
R_{STTH}	0	Reset Threshold 1 Selected (typ 4.6 V)
	1	Reset Threshold 2 Selected (typ 4.2 V)

CAN Register (CAN)

Table 15 provides control of the high-speed CAN module, mode, slew rate, and wake-up.

Table 15. CAN Register

CAN		D3	D2	D1	D0
$010B	W	—	SC1	SC0	MODE
	R	CANWU	TXF	CUR	THERM
Reset Value		—	0	0	0
Reset Condition		—	POR	POR	POR

High-Speed CAN Transceiver Modes

The mode bit (D0) controls the state of the CAN module, Normal or Sleep modes. Please see **Table 16**. SC0 bit (D1) defines the slew rate when the CAN module is in Normal mode, and controls the wake-up option (wake-up enable or disable) when the CAN module is in Sleep mode. CAN module modes (Normal and Sleep) are independent of the SBC modes. Please see **Table 17**.

Table 16. CAN High-Speed Transceiver Modes

SC1	SC0	MODE	CAN Mode
0	0	0	CAN Normal, Slew Rate 0
0	1	0	CAN Normal, Slew Rate 1
1	0	0	CAN Normal, Slew Rate 2
1	1	0	CAN Normal, Slew Rate 3
x	1	1	CAN Sleep and CAN Wake-up Disable
x	0	1	CAN Sleep and CAN Wake-up Enable

Table 17. CAN Status Bits

Status Bits	Description
CANWU	CAN Wake-up Occurred
TXF	Permanent Dominant TX
CUR(1)	CAN Transceiver in Current Limitation
THERM	CAN Transceiver in Thermal Shutdown

Error bits are latched in the CAN registers. Bit (1) CUR is set to 1 when the CAN interface is programmed into CAN NORMAL for the first time after V2 turn ON. To clear the CUR bit, follow this procedure:

- Turn V2 ON (SBC in Normal mode and V2 above V2 threshold) the CAN interface must be set into CAN Sleep
- Return to CAN NORMAL

Input/Output Control Register (IOR)

Table 18 provides data about HS1 control in Normal and Standby modes, while **Table 19** provides control bit data.

Table 18. IOR Register

IOR		D3	D2	D1	D0
$011B	W	—	HS1ON	—	—
	R	V2LOW	HS1OT	VSUPLOW	DEBUG
Reset Value		—	0	—	—
Reset Condition		—	POR	—	—

Table 19. IOR Control Bits

HS1ON	HS1 State
0	HS1 OFF, in Normal and Standby Modes
1	HS1 ON, in Normal and Standby Modes

When HS1 is turned OFF due to an over temperature condition, it can be turned ON again by setting the appropriate control bit to 1. Error bits are latched in the Input/Output Registers (IOR). Please see **Table 20**.

Table 20. IOR Status Bits

Status Bit	Description
V2LOW	V2 Below 4.0 V
HS1OT	High Side 1 Over Temperature
VSUPLOW	V_{SUP} Below 6.1 V
DEBUG	If Set, SBC Accepts Command to go to Debug Modes (No $\overline{WD}$)

Wake-up Input Register (WUR)

The local wake-up inputs, L0, L1, L2, and L3 can be used in both Normal and Standby modes as port expander, as well as and for waking up the SBC in Sleep or Stop modes. Please see **Table 21**.

Table 21. WUR Register

WUR		D3	D2	D1	D0
$100B	W	LCTR3	LCTR2	LCTR1	LCTR0
	R	L3WU	L2WU	L1WU	L0WU
Reset Value		0	0	0	0
Reset Condition		POR, NR2R, N2R, STB2R, STO2R			

The wake-up inputs can be configured separately, while L0 and L1 are configured together. Bits L2 and L3 are configured together. Please see **Table 22**.

Table 22. WUR Control Bits

LCTR3	LCTR2	LCTR1	LCTR0	L0/L1 Config	L2/L3 Config
x	x	0	0	Inputs Disabled	—
x	x	0	1	High Level Sensitive	
x	x	1	0	Low Level Sensitive	
x	x	1	1	Both Level Sensitive	
0	0	x	x	—	Inputs Disabled
0	1	x	x		High Level Sensitive
1	0	x	x		Low Level Sensitive
1	1	x	x		Both Level Sensitive

Table 23 provides Status bits data.

Table 23. WUR Status Bits

Status Bit	Description
L3WU	Wake-up Occurred (Sleep/Stop Modes), Logic State on Lx (Standby/Normal Modes)
L2WU	
L1WU	
L0WU	

Notes: Status bits have two functions. After SBC wake-up, they indicate the wake-up source (Example: L2WU set at 1 if wake-up source is L2 input). After SBC wake and once the WUR has been read, status bits indicates the real time state of the LX inputs (1 mean LX is above threshold, 0 means that LX input is below threshold).

If, after a wake-up from LX input, a $\overline{WD}$ timeout occurs before the first reading of the WUR register, the LXxWU bits are reset. This can occur only if SBC was in Stop mode.

Timing Register (TIM1/2)

This register is composed of two registers:

1. TIM1–controls the watchdog timing selection as well as the window or timeout option. TIM1 is selected when bit D3 is 0. Please see **Table 24**.
2. TIM2–is used to define the timing for the cyclic sense and forced wake-up function. TIM2 is selected when bit D3 is read operation it is not allowed in either TIM1 or TIM2 registers. Please see **Table 26**.

Table 24. TIM1 Register

TMI1		D3	D2	D1	D0
$101B	W	0	WDW	WDT1	WDT0
	R	—	—	—	—
Reset Value		—	0	0	0
Reset Condition		—	POR, RST	POR, RST	POR, RST

Table 25. TIM1 Control Bits

WDW	WDT1	WDT0	Timing (ms)	Parameter	
0	0	0	10	Watchdog Period 1	No Window Watchdog
0	0	1	45	Watchdog Period 2	
0	1	0	100	Watchdog Period 3	
0	1	1	350	Watchdog Period 4	
1	0	0	10	Watchdog Period 1	Window Watchdog Enabled (Window Length is Half the Watchdog Timing)
1	0	1	45	Watchdog Period 2	
1	1	0	100	Watchdog Period 3	
1	1	1	350	Watchdog Period 4	

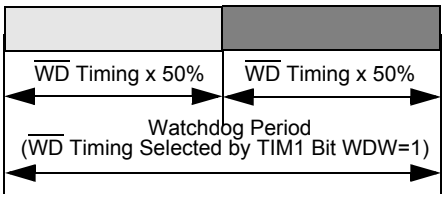


Figure 17. Window Watchdog

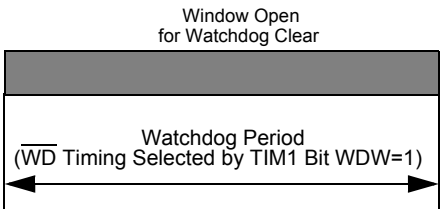


Figure 18. Timeout Watchdog

Table 26. TIM2 Register

TMI2		D3	D2	D1	D0
$101B	W	1	CSP2	CSP1	CSP0
	R	—	—	—	—
Reset Value		—	0	0	0
Reset Condition		—	POR, RST	POR, RST	POR, RST

Table 27. TIM1 Control Bits

CSP2	CSP1	CSP0	Cyclic Sense Timing (ms)	Parameter
0	0	0	5	Cyclic Sense/FWU Timing 1
0	0	1	10	Cyclic Sense/FWU Timing 2
0	1	0	20	Cyclic Sense/FWU Timing 3
0	1	1	40	Cyclic Sense/FWU Timing 4
1	0	0	75	Cyclic Sense/FWU Timing 5
1	0	1	100	Cyclic Sense/FWU Timing 6
1	1	0	200	Cyclic Sense/FWU Timing 7
1	1	1	400	Cyclic Sense/FWU Timing 8

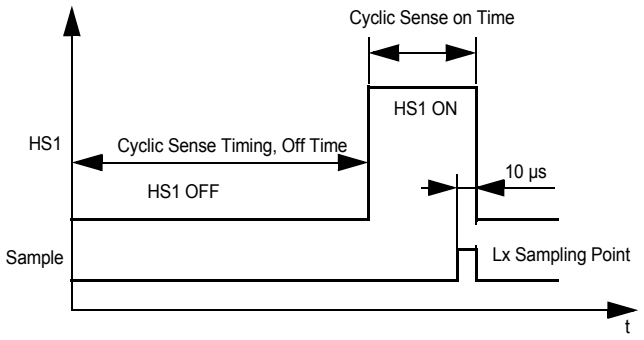


Figure 19. HS1 Operation when Cyclic Sense is Selected

Low Power Mode Control Register (LPC)

This register controls:

- The state of HS1 in Stop and Sleep mode (HS1 permanently off or HS1 cyclic)
- Enable or disable the forced wake-up function (SBC automatic wake-up after time spend in Sleep or Stop modes, time is defined by the TIM2 register)
- Enable or disable the sense of the wake-up inputs (Lx) at sampling point of the Cyclic Sense period (LX2HS1 bit).

Table 28. LPC Register

LPC		D3	D2	D1	D0
$110B	W	LX2HS1	FWU	—	HS1AUTO
	R	—	—	—	—
Reset Value		0	0	—	0
Reset Condition		POR, NR2R N2R,STB2RSTO2R	POR, NR2R N2R,STB2RSTO2R	—	POR, NR2R N2R,STB2RSTO2R

Please refer to the *Cyclic Sense Wake-up* discussion for details of the LPC register setup required for proper Cyclic Sense or direct wake-up operation.

Table 29. LX2HS1 Control Bits

LX2HS1	Wake-Up Inputs Supplied by HS1
0	No
1	Yes, Lx Inputs Sensed at Sampling Point

Table 30. HS1AUTO Control Bits

HS1AUTO	Auto Timing HS1 in Sleep and Stop Modes
0	OFF
1	ON, HS1 Cyclic, Period Defined in TIM2 Register

Interrupt Register ($\overline{\text{INT}}$)

This register allows masking or enabling the interrupt source. A read operation informs about the interrupt source.

Table 31. $\overline{\text{INT}}$ Register

$\overline{\text{INT}}$		D3	D2	D1	D0
$111B	W	VSUPLOW	HS1OT-V2LOW	VDDTEMP	CANF
	R	VSUPLOW	HS1OT	VDDTEMP	CANF
Reset Value		0	0	0	0
Reset Condition		POR, RST	POR, RST	POR, RST	POR, RST

Table 32. $\overline{\text{INT}}$ Control Bits

Control Bit	Description
CANF	Mask Bit for CAN Failures
V_{DDTEMP}	Mask Bit for V_{DD} Medium Temperature (Pre-Warning)
HS1OT - V2LOW	Mask Bit for HS1 Over Temperature AND V2 Below 4.0 V
V_{SUPLOW}	Mask Bit for V_{SUP} Below 6.1 V

When the mask bit is set, $\overline{\text{INT}}$ terminal goes low if the appropriate condition occurs.

Table 33. $\overline{\text{INT}}$ Status Bits

Status Bit	Description
CANF	CAN Failure
V_{DDTEMP}	V_{DD} Medium Temperature (pre-warning)
HS1OT	HS1 Over Temperature
V_{SUPLOW}	V_{SUP} Below 6.1 V

If $HS1_{OT}$ - $V2_{LOW}$ interrupt is only selected (only bit D2 set in $\overline{\text{INT}}$ register), reading $\overline{\text{INT}}$ register bit D2 leads to two possibilities:

1. Bit D2 = 1: $\overline{\text{INT}}$ source is HS1OT
2. Bit D2 = 0: $\overline{\text{INT}}$ source is V2LOW

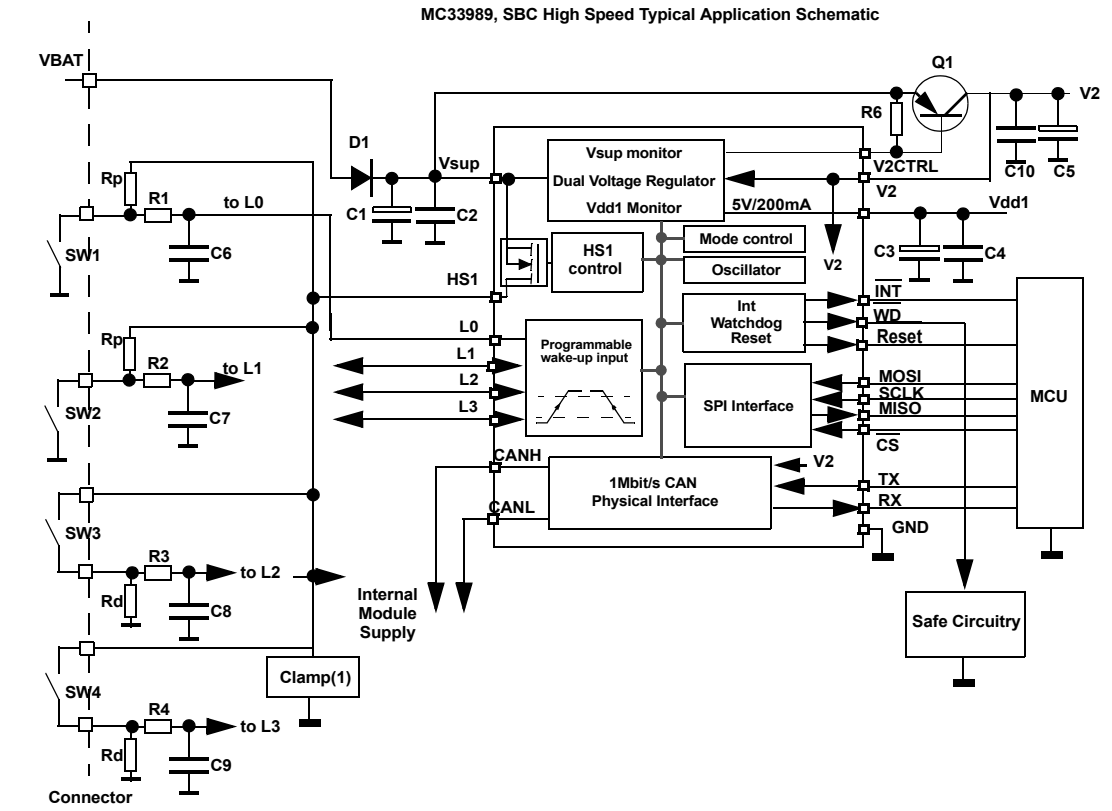
$HS1_{OT}$ and $V2_{LOW}$ bits status are available in IOR.

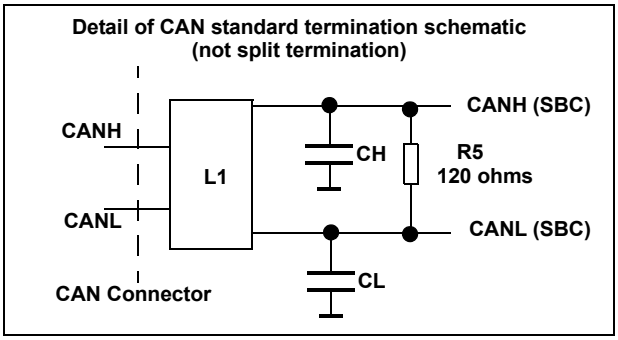
Upon a wake-up condition from Stop mode due to over current detection ($I_{DD1SW-U1}$ or $I_{DD1S-WU2}$), an $\overline{\text{INT}}$ pulse is generated; however, $\overline{\text{INT}}$ register content remains at 0000 (not bit set into the $\overline{\text{INT}}$ register).

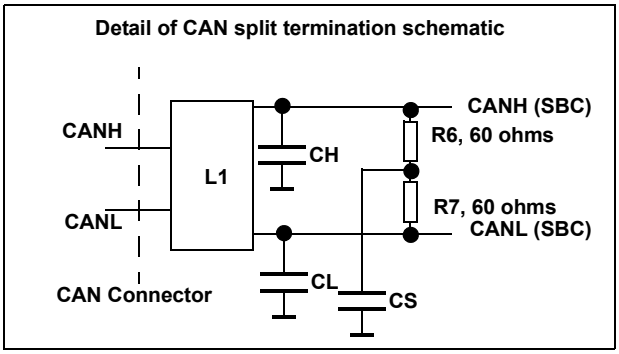
The status bit of the $\overline{\text{INT}}$ register content is a copy of the IOR and CAN registers status content. To clear the $\overline{\text{INT}}$ register bit the IOR and/or CAN register must be cleared (read register). Once this operation is done at IOR and CAN register the $\overline{\text{INT}}$ register is updated.

Errors bits are latched in the CAN register and IOR.

TYPICAL APPLICATIONS







Component values:

D1:
Q1: MJD32C
R1,R2,R3,R4: 10k
R5: 120
Rp, Rd:
R6: 2.2k
C1: 10uF
C2: 100nF
C3: 47uF
C4: 100nF
C5: 47uF tantal
C6,C7,C8,C9,C10: 100nF
CL, CH: 220 pF

Figure 20. Typical Application Diagram

SUPPLEMENTAL APPLICATION NOTES

GENERAL INFORMATION

The parameters given in the application section are for information only. Reference the electrical tables beginning on page 4 for actual operating parameters.

MC33989 device supply

The MC33989 is supplied from the battery line. A serial diode is necessary to protect the device against negative transient pulses and from reverse battery situation. This is illustrated in the device typical application schematic.

Voltage Regulator

The MC33989 contains two 5 V regulators: The V1 regulator, fully integrated and protected, and the V2 regulator which operates with an external ballast transistor. This is illustrated in the following device typical application schematic.

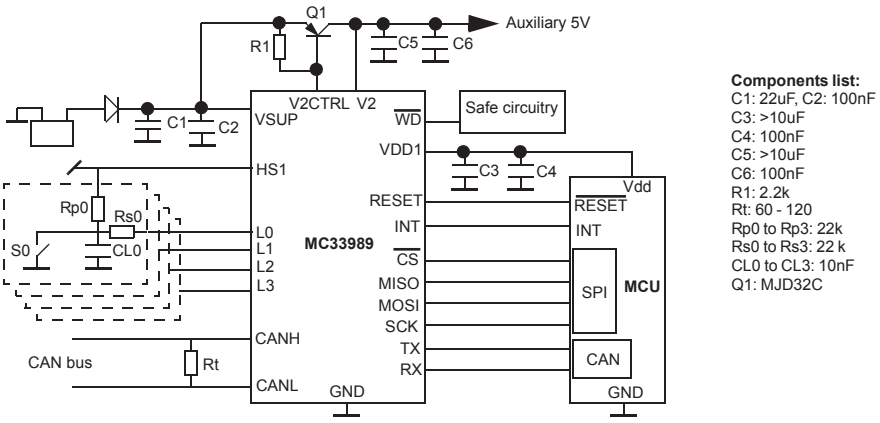


Figure 21. Device Typical Application Schematic

V1 Regulator

The V1 regulator is 5 V output, 2% accuracy with current capability of 200 mA max. It requires external decoupling and

stabilizing capacitors. The minimum recommended value are:

- C4: 100 nF
- C3: 10 µF < C3 < 22 µF, esr < 1 ohms. 22 µF < C3 < 47 µF, esr < 5 ohms. C3 > = 47 µF, esr < 10 ohms

V2 Regulator: Operation with External Ballast Transistor

The V2 regulator is a tracking regulator of the V1 output. Its accuracy relative to V1 is ±1%. It requires external decoupling and stabilizing capacitors. The recommended value are: 22 µF esr < 5 ohms, and 47 µF esr < 10 ohms.

The V2 terminal has two functions: sense input for the V2 regulator and 5 V power supply input to the CAN interface. Ballast transistor selection: PNP or PMOS transistors can be used. A resistor between base and emitter (or source and drain) is necessary to ensure proper operation and optimized performances. Recommended bipolar transistor is MJD32C.

V2 Regulator: Operation without Ballast Transistor

The external ballast transistor is optional. If the application does not requires more than the maximum output current capability of the V1 regulator, then the ballast transistor can be omitted. The thermal aspects must be analyzed as well.

The electrical connections are shown in **Figure 22**.

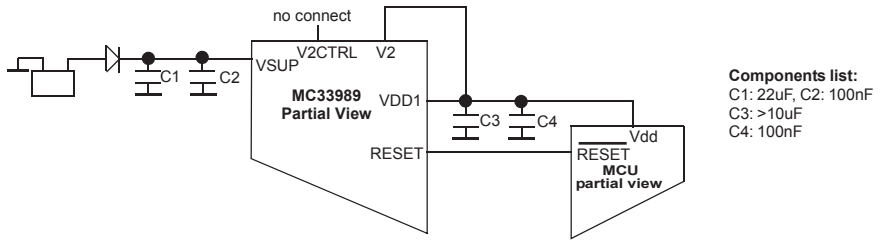


Figure 22. V2 Regulator Operation

Failure on V_{DD1}, Watchdog, Reset, INT Terminals

The paragraphs below describe the behavior of the device and of the INT, RESET, and WDOG terminals at power up and under failure of V_{DD1}.

Power Up and SBC Entering Normal Operation

After a power-up the SBC enters in Normal request mode (CAN interface is in TX/RX mode): V_{DD1} is on, V2 is off. After 350 ms if no watchdog is written (no TIM1 register write) a reset occurs, and the SBC returns to normal request mode.During this sequence WD is active (low level).

Once watchdog is written the SBC goes to normal mode: V_{DD1} is still on and V2 turns on, WD is no longer active and the reset terminal is high. If the watchdog is not refreshed, the SBC generates a reset and returns to Normal request mode.

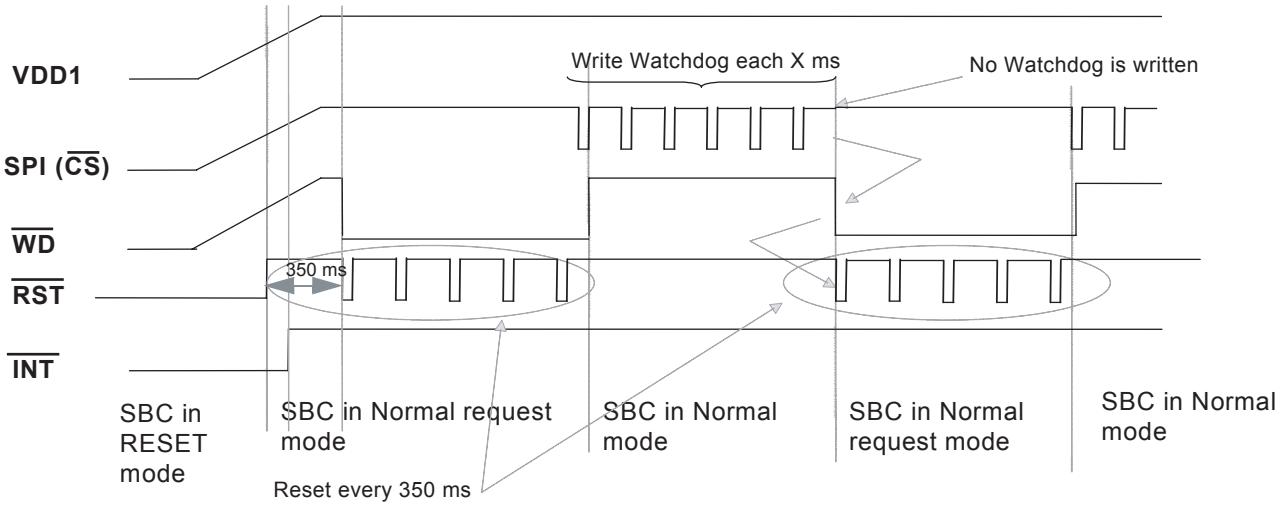


Figure 23. Power Up and SBC Entering Normal Operation

Power Up and V_{DD1} Going Low with Stop Mode as Default Low Power Mode Selected

The first part of the following figure is identical to the above. If V_{DD1} is pulled below the V_{DD1} under voltage reset (typ 4.6 V) for instance by an overcurrent or short circuit (ex short to 4 V), and if a low power mode previously selected was stop mode, the SBC enters reset mode (reset terminal is active). The terminal WD stays high, but the high level (V_{OH}) follows the V_{DD1} level. The interrupt terminal goes low.

When the V_{DD1} overload condition is removed, the SBC restarts in Normal request mode.

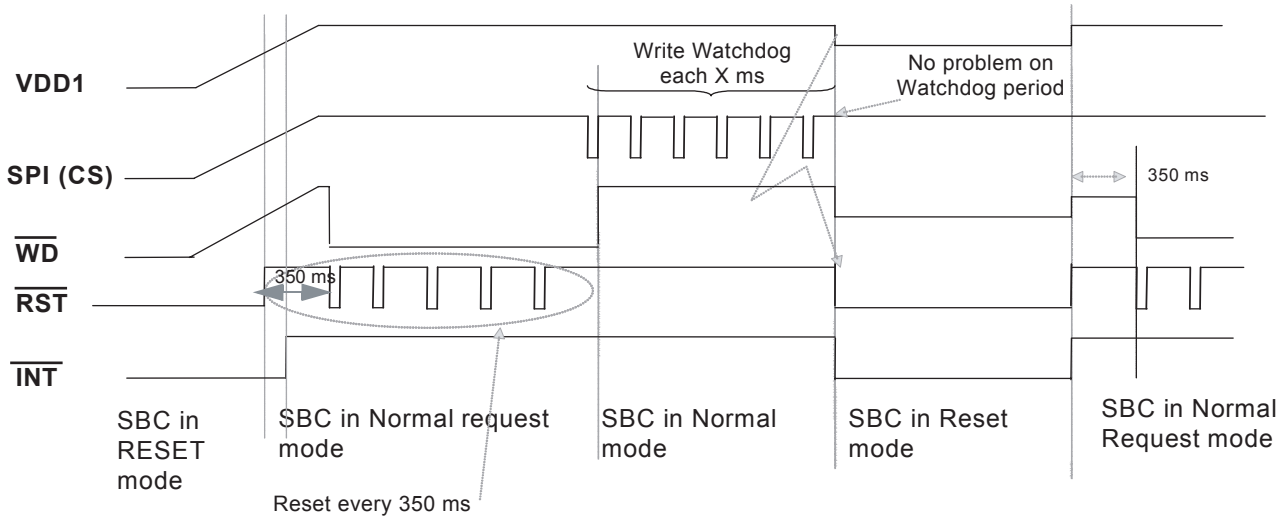


Figure 24. Power Up and V_{DD1} Going Low with Stop Mode as Default Low Power Mode Selected

Power Up and V_{DD1} Going Low with Sleep Mode as Default Low Power Mode Selected

The first part of the graph is the same as the previous figure. If V_{DD1} is pulled below the V_{DD1} under voltage reset (typ 4.6 V) for instance by an over current or short circuit (ex short to 4 V), and if the low power mode previously selected was sleep mode and if the BATFAIL flag has been cleared, the SBC enters reset mode for a time period of 100 ms. The terminal $\overline{WD}$ stays high, but the high level (V_{OH}) follows the V_{DD1} level.The reset and interrupt terminals are low. After the 100 ms, the SBC goes into sleep mode. V_{DD1} and V2 are off (The following figure is an example where V_{DD1} is shorted to 4 V, and after 100 ms the SBC enters sleep mode.

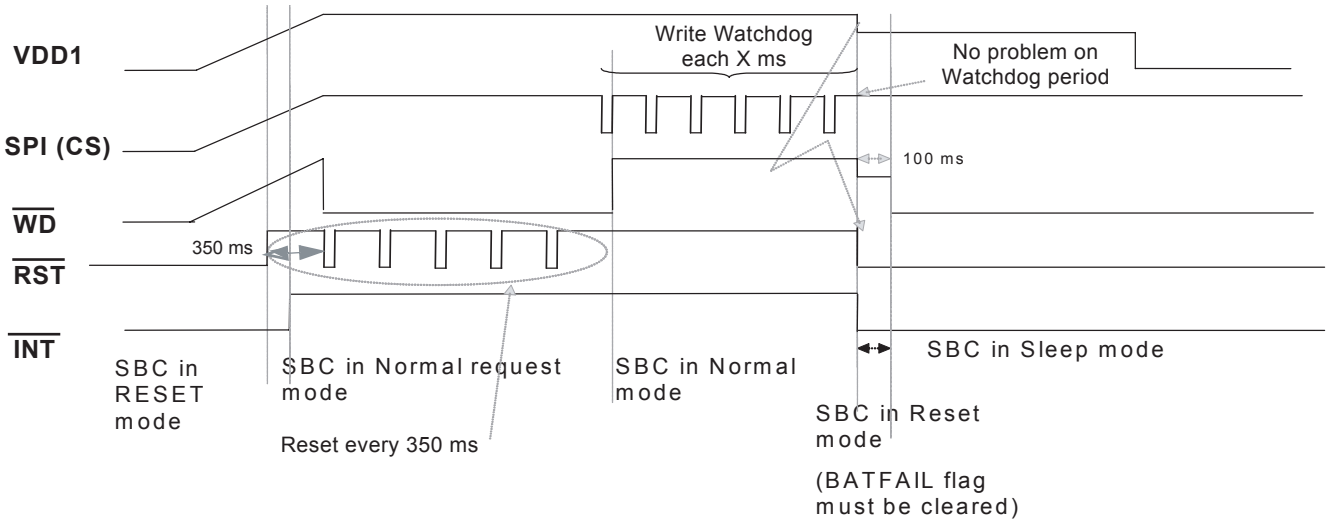


Figure 25. Power up and V_{DD1} Going Low with Sleep Mode as Default Low Power Mode Selected

WAKE-UP TIMINGS — SLEEP MODE

The paragraphs below describe the wake-up events from sleep mode, and the sequence of the signals at the SBC level. The wake-up time described is the time from the wake-up event to the SBC reset terminal release. The wake-up time is the sum of several timings: wake-up signal detection, V_{DD1} regulator start-up and decoupling capacitor charge, and reset time. At the end of the reset time, the reset terminal goes from low to high and the MCU is ready to start software operations.

LX Wakes up SBC from Sleep Mode

Below is the case where the SBC is in sleep mode and is awaked by LX positive edge.

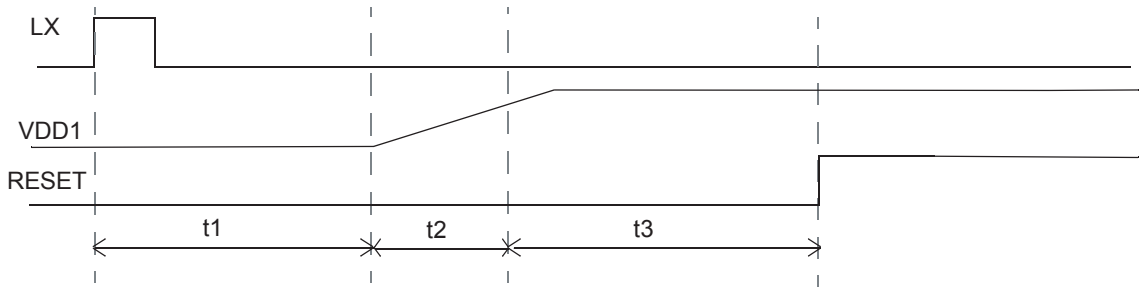


Figure 26.

- T1 (LX high level to V_{DD1} turn on): typ 100 µs.
- T2: V_{DD1} rising time is dependent on the capacitor and the load connected to V_{DD1}. It can be approximated by the capacitor charging time with the regulator output current limitation: T2 = (C x U)/I. With C = 100 mF, I_{DD1} = 200 mA min., U = 5 V so T2 = 2.5 ms).
- T3 (VDD1>RST-TH (4.6 V by default) to reset high): parameter Rest dur: 4 ms max.
- The total time is 6.6 ms in this example.

CAN Wake-Up

The following case describes the signal for CAN wake up. Refer to page 48 for more details on CAN wake up signals and the TCAN analysis.

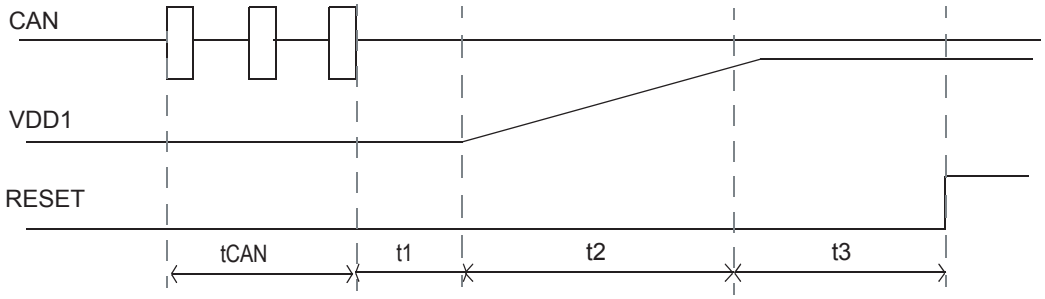


Figure 27. CAN Wake-Up

- T1(third valid CAN dominant pulse to V_{DD1} turn on): typ 80 µs.
- T2 and T3 identical to page 38 above
- The total time is 6.58 ms in this example.

LX with Cyclic Sense

The case below is a description of the wake-up by LX input associated with the cyclic sense function.

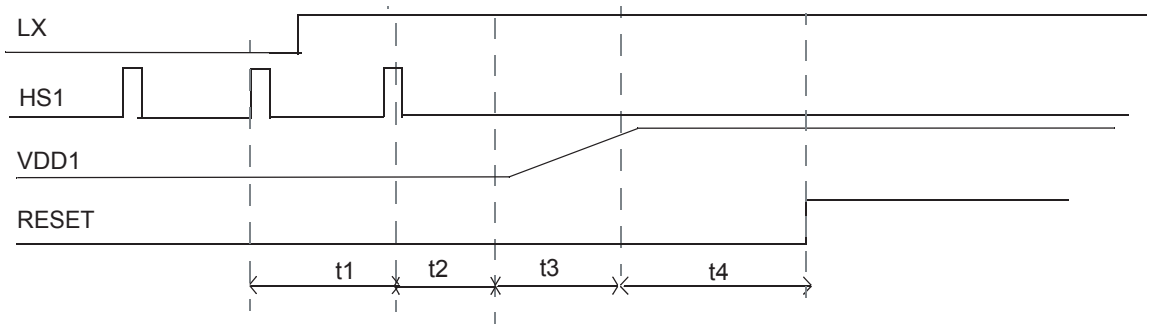


Figure 28.

- T1: Is dependent on the selected cyclic sense timing in the TIM2 register (5 ms to 400 ms). LX is sampled
- 10 µs before the end of cyclic sense on time. If the LX correct wake-up level happens just after the sample
- point, the wake-up will be detected at the next HS1 activation and a complete period is lost.
- T2: It is the same time as LX to VDD1 turn on: typ 100 µs
- T3 & T4: same as page 38
- The total time is 11.5 ms (for a cyclic sense total time of 5 ms) in this example.

WAKE-UP TIMING: STOP MODE

The following paragraphs describe the wake-up events from stop mode, and the sequence of the signals at the SBC level. The wake-up time described is the time from the wake-up event to the SBC $\overline{INT}$ terminal. The wake-up time is the sum of several timings: wake-up signal detection, the $\overline{INT}$ pulse, and a minimum delay between $\overline{INT}$ and SBC ready to operate. At the end of the wake-up time, the SBC is ready to operate, however the MCU might have already been in a restart operation.

LX Wake-Up

Below is the case where the SBC is in stop mode and is awakened by an LX positive edge

- T1(L0 high level to $\overline{INT}$ pulse): typ 100 µs.
- The total time is 133 µs in this case.

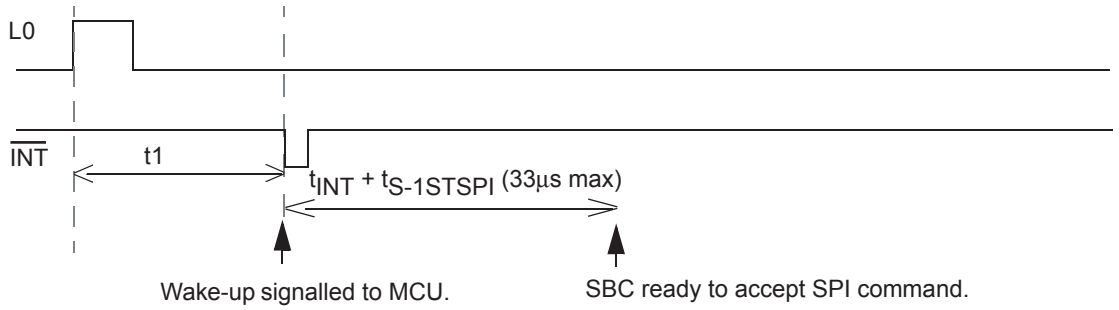


Figure 29. Lx Wake-Up

CAN Wake-Up

The case below describes the signal for CAN wake-up. Refer to page 48 for more details on CAN wake-up signals and the TCAN analysis.

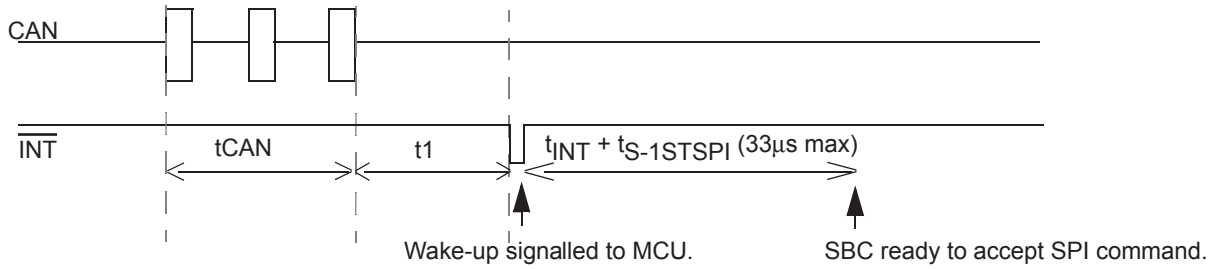


Figure 30. CAN Wake-Up

- TCAN: refer to page 48 for more details.
- T1: Third pulse on CAN to INT pulse: typ 80 µs.
- The total time is 113 µs in this case.

CS Wake-Up

The figure below describes the wake up from a CS signal transition, while the SBC is in stop mode.

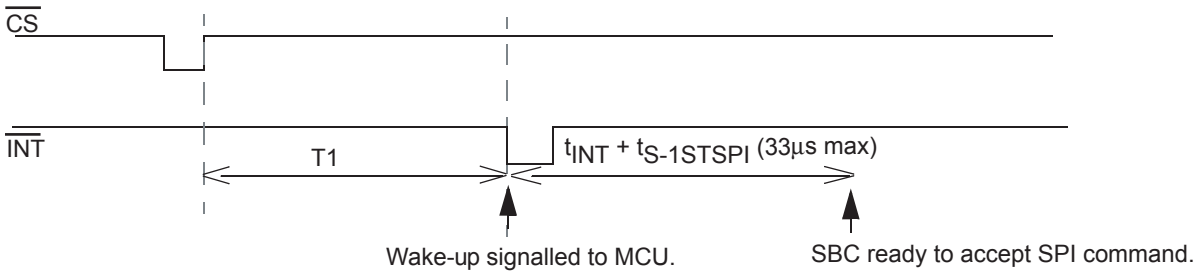


Figure 31. CS Wake-Up

- T1: CS rising edge to INT pulse: typ 60 µs.
- The total time is 133 µs in this case.

Overcurrent Wake-Up

The following figure describes the signal when an overcurrent is detected at V_{DD1}. A V_{DD1} overcurrent condition will lead to a wake-up from stop mode.

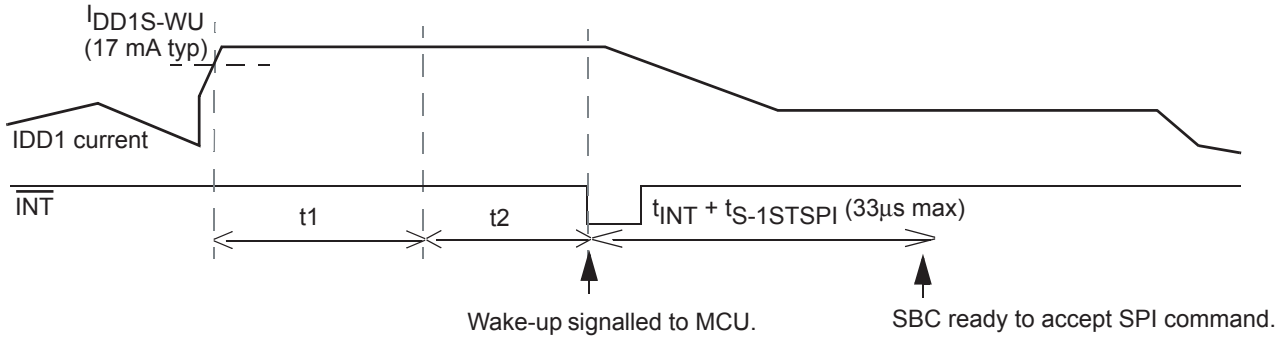


Figure 32. Overcurrent Wake-Up

- T1:V_{DD1} output current deglitcher time:IDD1-DGLT: typ 55 µs
- T2: Over current detected to SBC wake-up ($\overline{INT}$ pulse) = typ 60 µs
- The total time is 148 µs in this case.

LX with Cyclic Sense

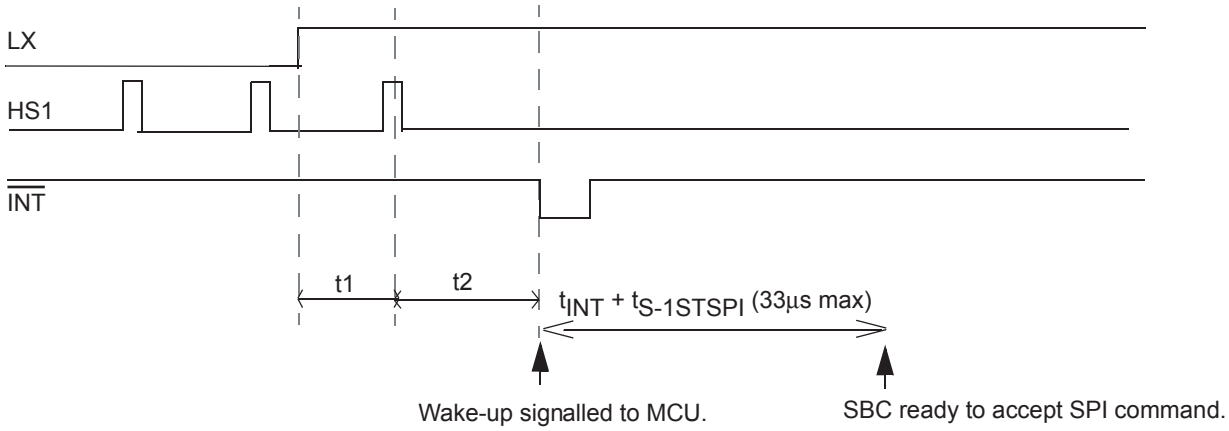


Figure 33.

- T1: Is dependent on the selected cyclic sense timing in the TIM2 register (5 ms to 400 ms). LX is sampled 10 µs before the end of cyclic sense on time. If the LX correct wake-up level happens just after sample point, the wake-up will be detected at the next HS1 activation and a complete period is lost.
- T2: It is the same than Lx to $\overline{INT}$ pulse: typ 100 µs
- The total time is around 5.13 ms (for a cyclic sense total time of 5 ms) in the above example.

MC33989 CAN INTERFACE

This section is a detailed description of the CAN interface of the MC33989.

Block Diagram

Figure 34 is a simplified block diagram of the CAN interface of the MC33989.

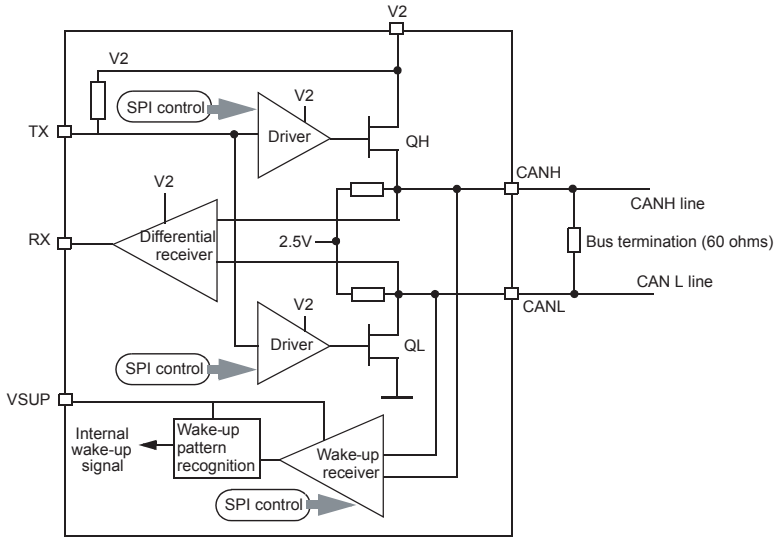


Figure 34. 33989 CAN Interface

CAN Interface Supply

The supply voltage for the CAN driver is the V2 terminal. The CAN interface also has a supply path from the battery line, through the terminal V_{SUP}. This path is used in CAN sleep mode to allow wake-up detection.

During CAN communication (transmission and reception) the CAN interface current is sourced from the V2 terminal. During a CAN low power mode, the current is sourced from the V_{SUP} terminal.

Main Operation Modes Description

The CAN interface of the MC33989 has two main operation modes: Normal mode and sleep mode. The modes are controlled by the SPI command.

In normal mode, used for communication, four different slew rates are available for the user.

In sleep mode, the user has the option to enable or disable the remote CAN wake-up capability.

CAN Driver Operation in Normal Mode

When the CAN interface of the MC33989 is in Normal mode, the driver has two states: recessive or dominant. The driver state is controlled by the TX terminal. The bus state is reported through the RX terminal.

When TX is high, the driver is set in a recessive state, CANH and CANL lines are biased to the voltage set at V2 divided by 2, approx. 2.5 V.

When TX is low, the bus is set into dominant state: the CANL and CANH drivers are active. CANL is pulled to gnd, CANH is pulled high toward 5 V (the voltage at V2).

The RX terminal reports the bus state: the CANH minus the CANL voltage is compared versus an internal threshold (a few hundred mV). If “CANH minus CANL” is below the threshold, the bus is recessive and RX is set high.

If “CANH minus CANL” is above the threshold, the bus is dominant and RX is set low. This is illustrated in the figure below.

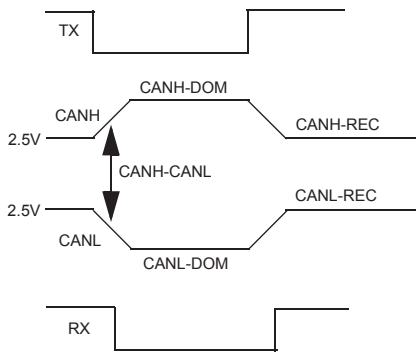


Figure 35. CAN Driver Operation in Normal Mode

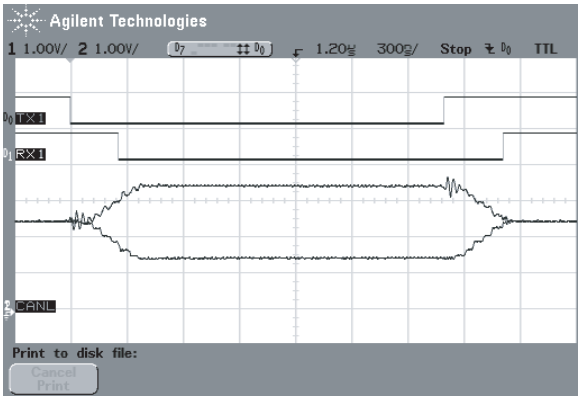
TX and RX Terminals

The TX terminal has an internal pull up to V2. The state of TX depends on the V2 status. RX is a push-pull structure, supplied by V2. When V2 is set at 5V, and CAN is in normal mode, RX reports the bus status. When V2 is off RX is low.

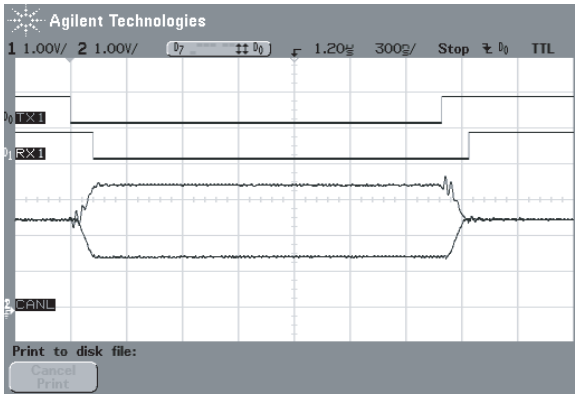
Normal Mode and Slew Rate Selection

The slew rate selection is done via the SPI. Four slew rates are available. The slew rate affects the recessive to dominant and dominant to recessive transitions. This affect is also the delay time from the TX terminal to the bus, and from the bus to RX. The loop time is thus affected by the slew rate selection.

The following figure is an illustration of the slew rate on CANH, CANL, TX and RX.



CAN signal with slew rate 0 selected



CAN signal with slew rate 3 selected

R=60 ohms, CL = CH = 100pF

Figure 36. Normal Mode and Slew Rate Selection

Minimum Baud Rate

As TX permanent dominant is detected after TDOUT (min 200 µs), a minimum Baud rate is required in order to get good behavior: once TX permanent dominant is detected the CAN driver is off.

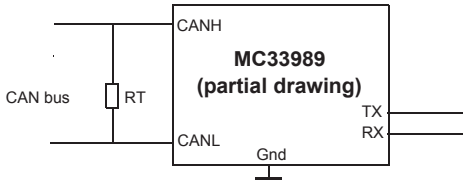
The maximum number of consecutive dominant bits in a frame is 12 (6 bits of active error flag and its echo error flag).

200 µs/12 = 16.7 µs. The minimum Baud rate is 1/6.7 µs = 60 KBaud.

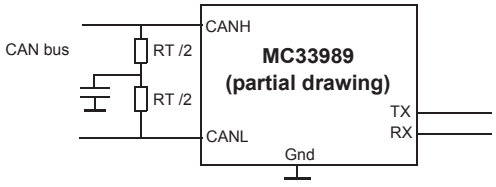
Termination

The MC33989 supports the two main types of bus termination:

- Differential termination resistors between CANH and CANL lines.
- Split termination concept, with mid point of the differential termination connected to gnd through a capacitor.



Differential termination concept



Split termination concept

Figure 37. Bus Termination

CAN Mode versus SBC Modes

The table below indicates the CAN interface modes versus the SBC modes as well as the status of TX, RX and the CAN bus terminals.

Table 34. CAN vs SBC Modes

SBC mode	External ballast for V2	CAN mode	V2 voltage	TX	RX	CANH/CANL (disconnected from other nodes)
Unpowered	YES	Unpowered	0 V	LOW	LOW	Floating to gnd
Reset (with ballast)	YES		0 V	LOW	LOW	Floating to gnd
Normal request (with ballast)	YES		0 V	LOW	LOW	Floating to gnd
Normal	YES	Normal Slew rate 0,1,2,3	5 V	Internal pull up to V2.	Report bus state High if bus recessive, Low if dominant	Bus recessive CANH = CANL = 2.5 V
Normal	YES	Sleep mode	5 V	5 V	5 V	Floating to gnd
Standby with external ballast	YES	Normal or sleep	0 V	LOW	LOW	Floating to gnd
Standby without external ballast, V2 connected to V1	NO	Normal	5 V	Same as normal mode	Same as normal mode	Same as normal mode
Standby without external ballast, V2 connected to V1	NO	Sleep	5 V	5 V	5 V	Floating to gnd
Sleep	—	Sleep	0 V	LOW	LOW	Floating to gnd
Stop	—	Sleep	0 V	LOW	LOW	Floating to gnd

How to Test the MC33989 CAN Interface

The CAN interface can be easily set up and tested. MC33989 can be connected as in the following figure. V2 is connected to V1. The device is supplied with nominal supply (12 V at V_{SUP} input terminal). After power on, reset the device, enter normal request mode, and the CAN interface is set in normal mode, slew rate 0. TX can be driven by a signal generator. RX will report the bus state. The figure below is a simple test schematic.

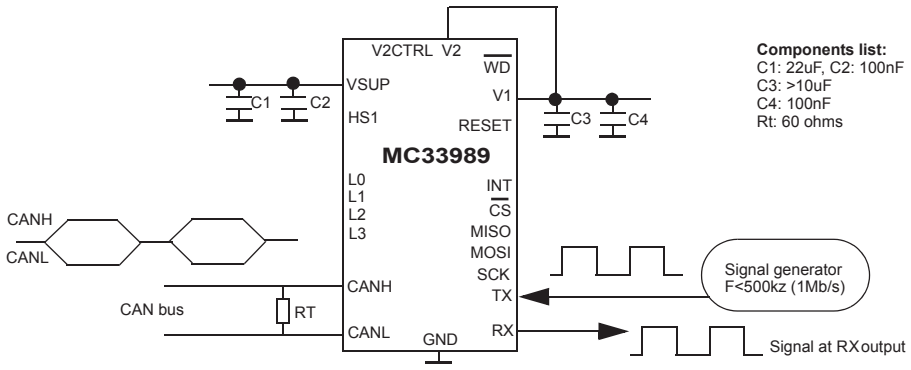


Figure 38. Testing the CAN Interface

CAN LOW POWER MODE AND WAKE UP

Low Power Mode

In low power mode the CAN is internally supplied from the V_{SUP} terminal. The voltage at V2 terminal can be either at 5 V or turned off. The current sourced from V2, when the CAN is in sleep mode, is extremely low. In most case the V2 voltage is off, however the CAN can be set into sleep mode even with 5 V applied on V2.

In low power mode the CANH and CANL driver are disabled, and the receiver is also disabled. CANH and CANL have a typical 50 k ohm impedance to gnd. The wake-up receiver can be activated if wake-up is enable by an SPI command.

When the device is set back into TX RX mode by an SPI command, CANH and CANL are set back into the recessive level. This is illustrated in **Figure 39**.

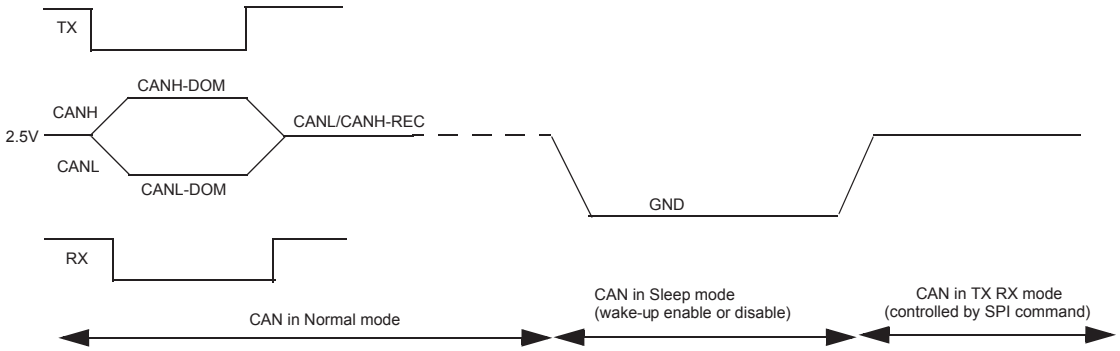


Figure 39. Low Power Mode

Wake-Up

When the CAN interface is in sleep mode with wake up enabled, the CAN bus traffic is detected. The wake-up option has to be enabled prior to setting the CAN in sleep mode. The CAN bus wake-up is a pattern wake-up.

If the CAN is set into sleep mode with “wake-up disabled”, bus traffic will not be detected by the MC33989.

CAN Wake-Up Report: From the SBC in Sleep or Stop Mode

The CAN wake-up reports depend upon the MC33989 low power mode. If the MC33989 is set into sleep mode (V1 and V2 off), the CAN wake-up or any wake-up is reported to the MCU by the V1 turn on, leading to MCU supply turn on and reset release.

If the SBC is in stop mode (V2 of and V1 active), the CAN wake-up or any wake-up is reported by a pulse on the $\overline{\text{INT}}$ output.

CAN Wake-Up Report: From the SBC in Normal or Standby Mode

If the SBC is in normal or standby mode, and the CAN interface is in sleep mode with wake-up enabled, the CAN wake-up will be reported by the bit CANWU in the CAN register.

In case the SBC uses such configuration, the SBC in normal mode and CAN sleep mode with wake up enable, it is recommended to check for the CAN WU bit prior to setting the MC33989 is sleep or stop mode, in case bus traffic has occurred while the CAN interface was in sleep mode.

CAN Wake-Up Report in the SPI Registers

After a CAN wake-up, a flag is set in the CAN register. Bit CAN-WU reports a CAN wake-up event while the SBC was in sleep, stop, normal or standby mode. This bit is set until the CAN is set by the SPI command in normal mode and CAN register read.

Pattern Wake-Up

In order to wake-up the CAN interface, the following criteria must be fulfilled:

- The CAN interface wake-up receiver must receive a series of 3 consecutive valid dominant pulses, each of them has to be longer than 500 ns and shorter than 500 μs.
- The distance between 2 pulses must be lower than 500 μs and the three pulse must occur within a time frame of 1 ms.

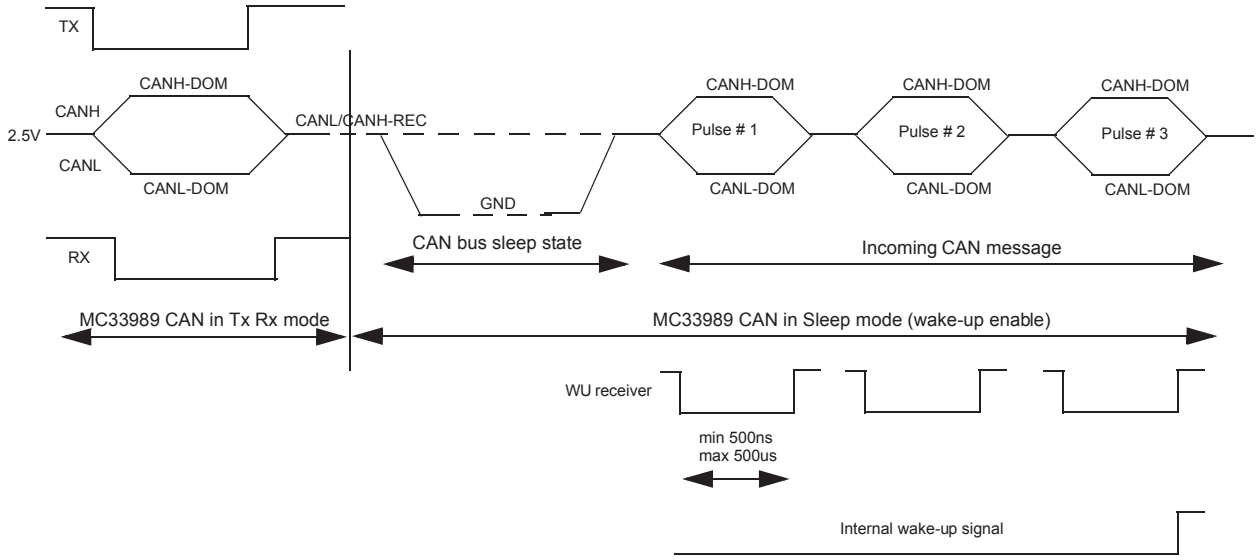
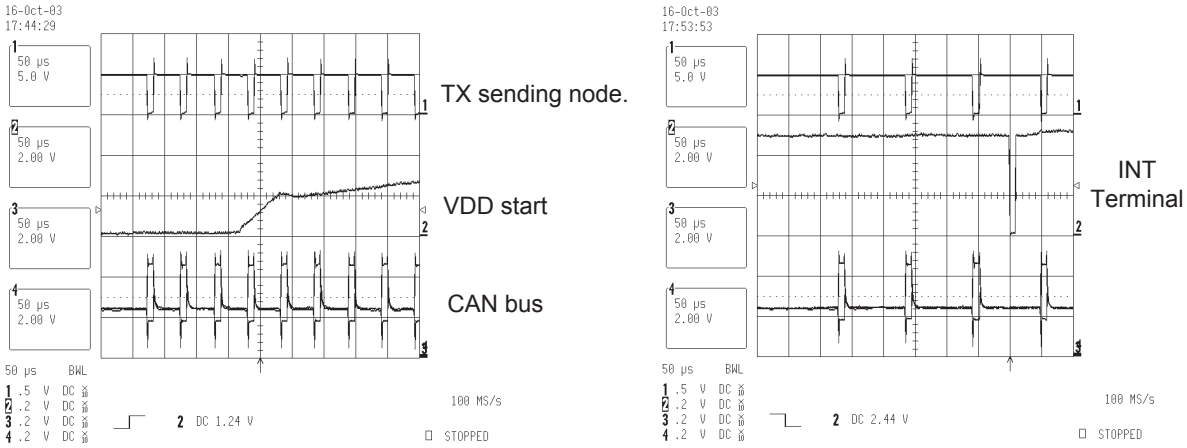


Figure 40. Pattern Wake-Up

The following figure illustrates the SBC key signals when a CAN wake-up occurs in sleep or stop mode.



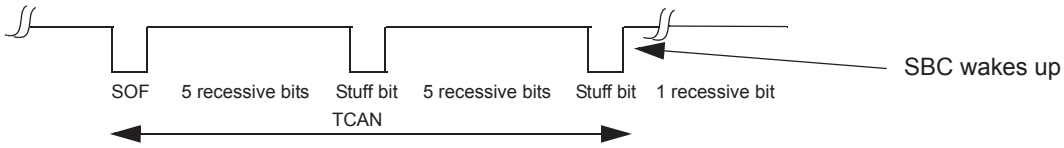
CAN wake-up: SBC in sleep mode. V1 turn on.

CAN wake-up: SBC in stop mode. INT pulse

Figure 41. SBC Key Signals

Analysis: CAN Frame with 11 Bits of Identifier Field at 1

Figure 42 is the calculation for the TCAN time with only “1” in the identifier field.

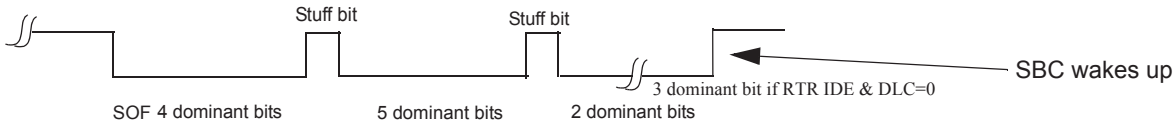


13 bits are needed to wake-up the SBC.
If the minimum baud rate is used (60 KBaud), TCAN = 16.7 µs*13= 217.1 µs
If 250 KBaud is used: TCAN = 4µs *13= 52 µs

Figure 42. CAN Frame with 11 Bits of Identifier Field at 1

Analysis: CAN Frame with 11 Bits of Identifier Field at 0

Figure 43 is the calculation for the TCAN time with only “0” in the identifier field.



17 bits are needed to wake-up the SBC.
If the minimum baud rate is used (60 KBaud), TACN = 16.7 µs*17= 284 µs
If 250 KBaud is used, TCAN = 4µs *17= 68 µs.

Figure 43. CAN Frame with 11 Bits of Identifier Field at 0

FAILURE ON V2 SUPPLY, CAN BUS LINES AND TX TERMINAL

V2LOW

In order to have proper operation of the CAN interface, V2 must be ON. Two case can be considered:

- V2 is connected with an external ballast: in case of a V2 over load condition, the flag V2LOW is set in to the SBC IOR register. This flag is set when V2 is below the 4 V typical. An interrupt can also be triggered upon a V2LOW event. When V2 is low, the CAN interface cannot operate.
- V2 is connected to V1 (no ballast transistor used): V2 will be supplied by the V1 voltage. In case V1 is in an undervoltage condition (ex V1 below the V1 under voltage reset, typ 4.6 V), the device will enter the reset mode. The V2LOW flag will also be set. In this case, the reset terminal is active, and the MCU will not send or receive any CAN messages.

TX Permanent Dominant

A TX permanent dominant condition is detected by the CAN interface and leads to a disable of the CAN driver. The TX permanent dominant is detected if TX stays in dominant (TX low) from more than 360 µs typical. The driver is automatically re-enabled when TX goes to a high level again. When a TX permanent dominant is detected, a bit is set into the SPI register, (bit D2 named TXF in the CAN register). This bit is latched. In order to clear the bit, two conditions are necessary:

- No longer “TX permanent failure” AND
- CAN register read operation.

An interrupt can be enabled.The GFAIL flag in the MCR register will also be set.

CAN Driver Overtemperature:

In case of an overtemperature condition at the CANH or CANL driver, the driver will be automatically disabled and the THERM bit set in the CAN register. If enabled, an interrupt will be signalled. The GFAIL flag is set in the MCR register.

When the CAN is in an overtemperature situation, the device is no longer able to transmit. As soon as the temperature is below the overtemperature level minus hysteresis, the CAN driver is automatically re-enabled.

The THERM bit is latched and two conditions are necessary to clear it:

- No longer “CAN overtemperature situation” AND
- Read operation of the CAN register.

Overcurrent Detection:

The CAN interface can detect and signal over current condition, occurring for instance in case of CANL shorted to VBAT. This is signalled by the bit CUR in the CAN register. An $\overline{\text{INT}}$ can be enabled, and GFAIL bit is set. The CUR bit is latched and two conditions are necessary to clear it:

- No longer “CAN over current situation” AND
- Read operation of the CAN register.

Protection

The MC33989 CAN output is protected for automotive environments.

The CAN driver is protected against overtemperature and overcurrent.

ISO7637 Transient

The CANH and CANL are rated from +40 Vdc to -27 Vdc. This means that the MC33989 CAN output can handle failure situations like the bus directly shorted to the battery line in a load dump situation (+40 V).

Ground disconnection of the module will lead to the CANH and CANL line floating high to the VBAT supply. The rest of the network will not be affected. However the CANH and CANL lines of the ungrounded module will see a negative voltage of the VBAT value, with respect to their gnd level. Such situations can be handled by the CAN interface of the MC33989, but also in cases of a jump start (battery at 27 V) and gnd disconnection.

Fast transient pulses, ISO7637-3. During these pulses, the maximum rating of the CANH and CANL lines of +40 Vdc and -27 Vdc must be respected.

ESD

The CANH and CANL line of the MC33989 are rated at ±4 kV. An external capacitor between CANH and CANL to gnd or a zener diode suppressor can be added to ensure a higher module resistance to ESD.

Current in Case of Bus Short Conditions

In case of short circuit condition on the CAN bus the current in the CAN supply, the CAN line can be different from the nominal case. The **Figure 44** and **Table 35** describe the various cases.

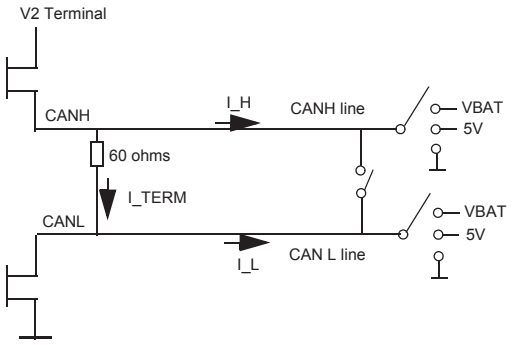


Figure 44. Current in Case of Bus Short Conditions

Table 35. Current in Case of Bus Short Conditions

Condition	I term current	I_H current	I-L current	Comment
	peak current (mA)			
No failure	32	0	0	Normal communication.
CANH line to gnd	0	150	0	No communication. Current flowing from V2 terminal, during CAN driver dominant state. (32)
CANH line to 5 V	55	-55	0	communication OK.
CANH line to +VBAT	150	-150	0	communication OK.
CANL line to gnd	50	0	50	communication OK.
CANL line to 5 V	0	0	-150	no communication (32)
CANL line to VBAT	0	0	-240	no communication (32)
CANH line shorted to CANL line	0	70	-70	no communication (32)

Notes

32. For the failure case which leads to loss of communication and current flow for a very short time period as illustrated in **Figure 45**. So for instance for CANH to gnd, the impact of the peak current on the V2 voltage regulator is very limited. The TX, RX, and CAN signal in the figure are placed in a CANH to CANL short circuit condition.

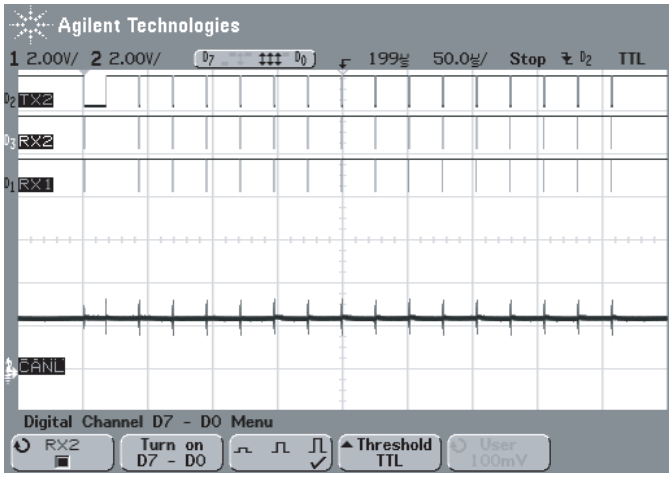
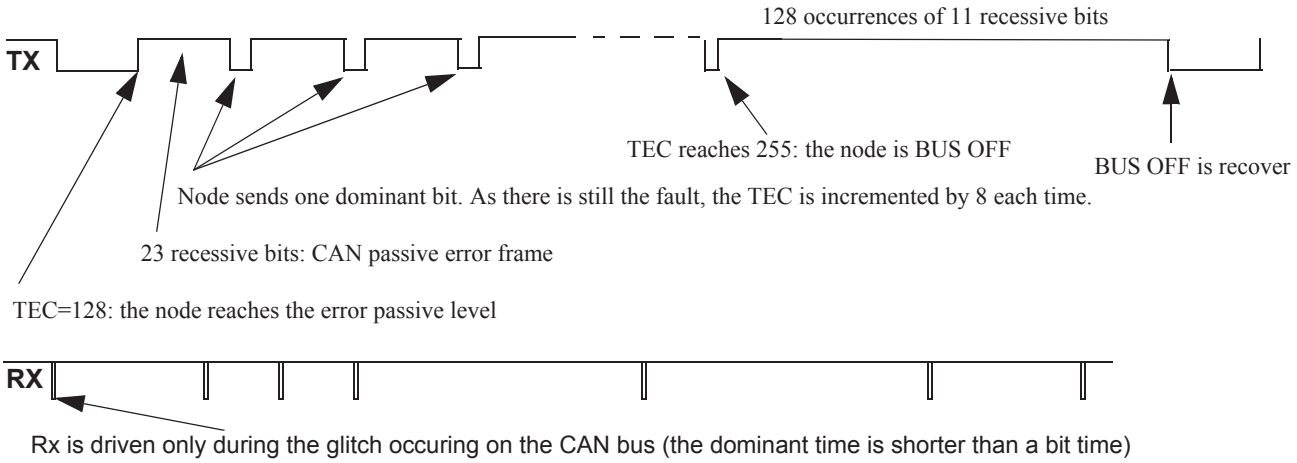


Figure 45. CANH to CANL Short Circuit Condition

The sender node drives TX and the CAN bus, but doesn't receive anything on RX, so the CAN protocol handler inside the MCU increases its TEC «transmit error counter» by 8.The sender node keeps driving TX in dominant until it reaches the error passive level (TEC=128).

When it is in error passive, it sends a passive error frame (23 bits in recessive). Then the sender nodes drive the bus and send only 1 dominant bit, and as nothing is received on RX, the TEC is incremental by 8. After TX is driven 15 times, the TEC reaches 255: then the node is in the BUS OFF state.

When the node is in the BUS OFF state, it needs 128 occurrences of 11 recessive bits (1.408 ms at 1MBauds) in order to recover and be able to transmit again.



The DC current can be calculated as follows:
Idc= (Time in dominant * peak current of the fault) / total error frame time
Idc= (17+15)*peak current / ((23*15)+1408)=32 / 1753*peak current

Example for CANL2Vbat (peak current = - 240 mA): Idc = 32*(-) 240 / 1753=(-)4.38 mA

Figure 46. Node is in Bus Off State

SOFTWARE ASPECTS

Introduction

This section describes the MC33989 operation and the microcontroller SPI software routine that has to be executed in order to control the device. Structure of the Byte: ADR (3 bits) + R/W (1bit) + DATA (4 bits). MSB is sent first. Refer to MC33989 specifications for more details.

How to Enter in Normal Mode After a Power-Up

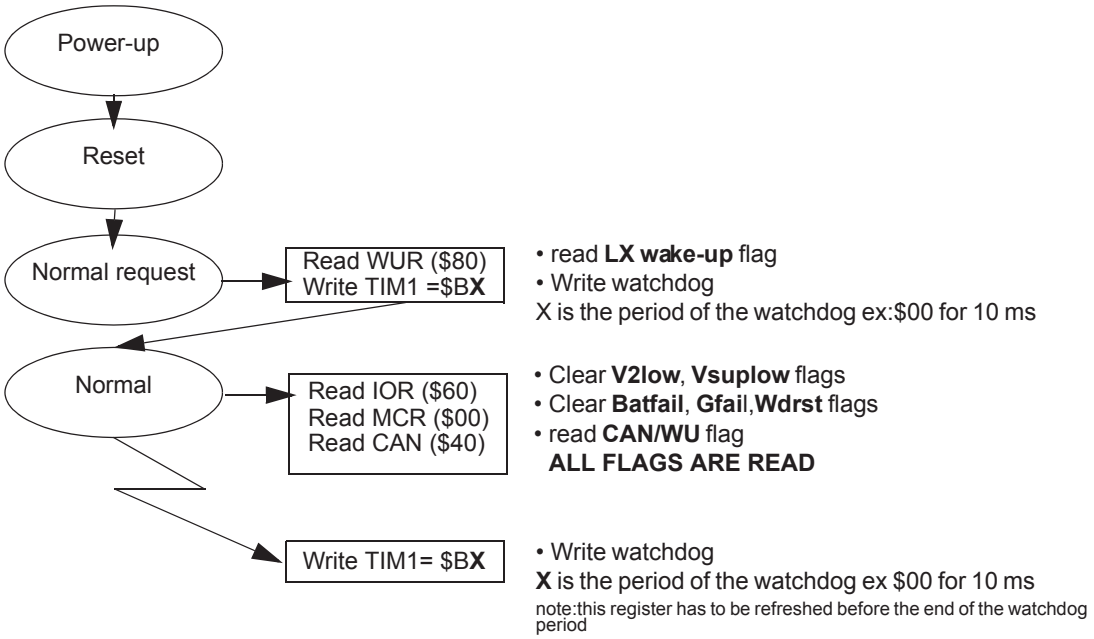


Figure 47. Normal Mode After Power-Up

How to Change CAN Slew Rate

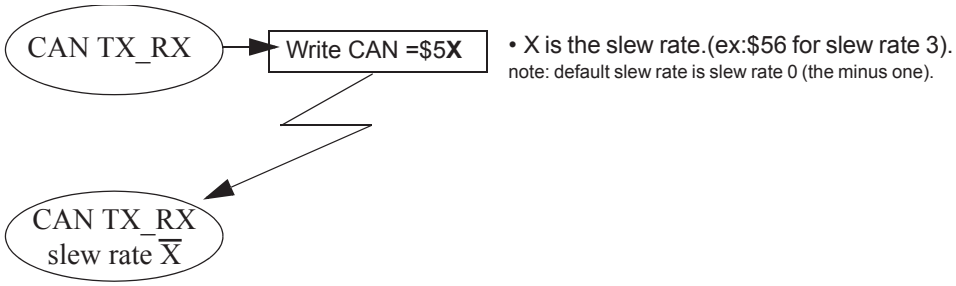


Figure 48. Change CAN Slew Rate

How to Set the CAN Interface in Sleep Mode

How to Control HS1 Output

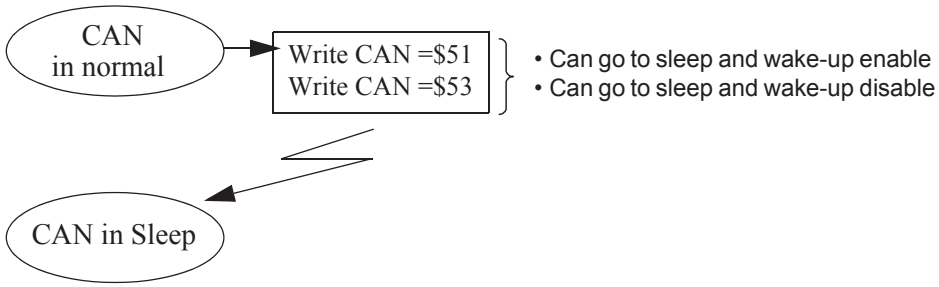


Figure 49. HS1 Output Control

How to Configure Wake-Up Before Going in Low Power Mode

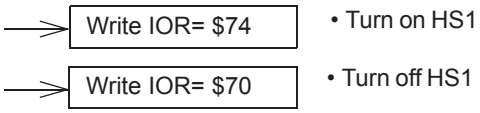


Figure 50. Wake-Up Configure Before Low Power Mode

Enable CAN Wake-Up

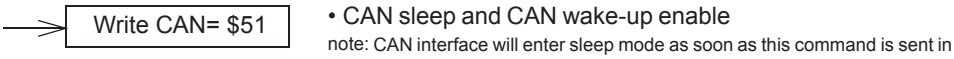


Figure 51. Enable CAN Wake-Up

Enable Wake-Up From LX, No Cyclic Function

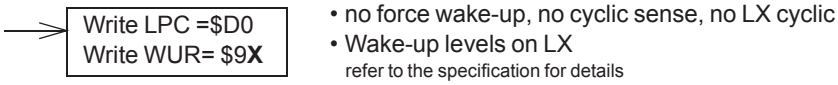


Figure 52. Enable Wake-Up From LX without Cyclic Sense

Enable Wake-Up From LX, with Cyclic Sense Function

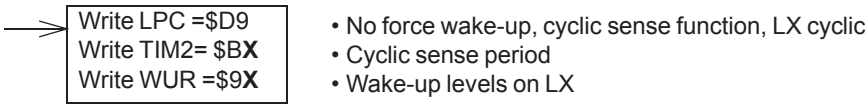


Figure 53. Enable Wake-Up From LX with Cyclic Sense

Force Wake-Up

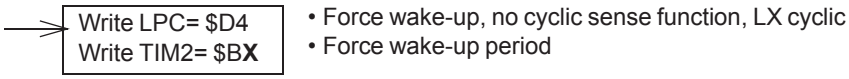


Figure 54. Force Wake-Up

Disable all Wake-Up

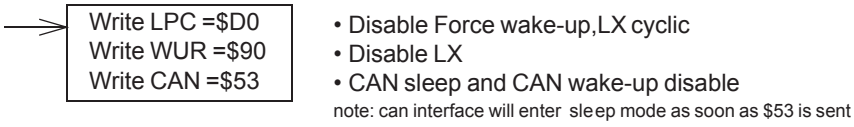


Figure 55. Disable all Wake-Up

How to Enter in Sleep Mode

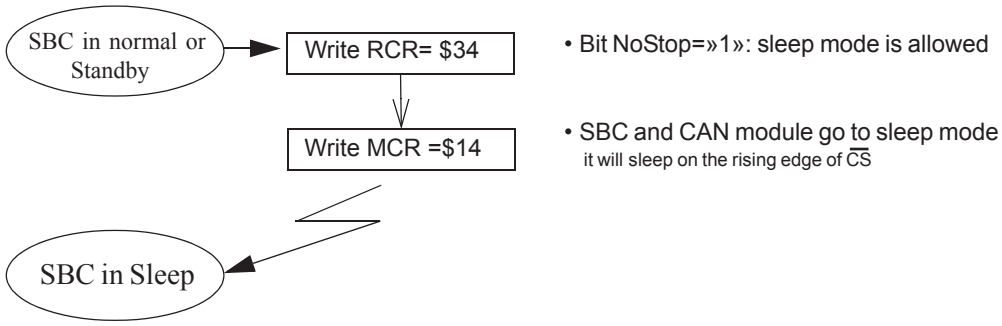


Figure 56. Enter Sleep Mode

How to Enter in Stop Mode with Watchdog

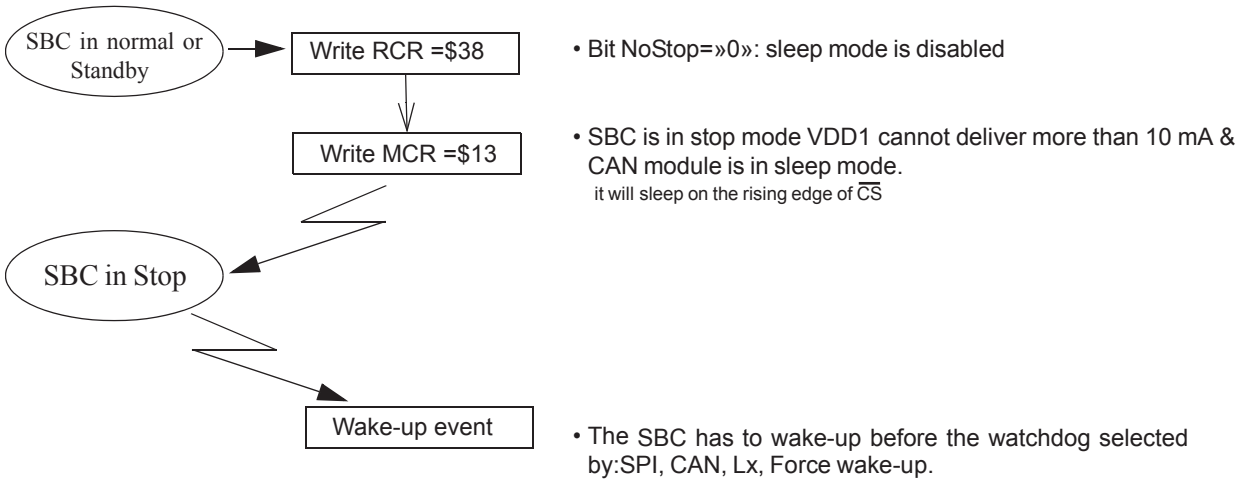


Figure 57. Enter Stop Mode with Watchdog

How to Enter in Stop Mode without Watchdog

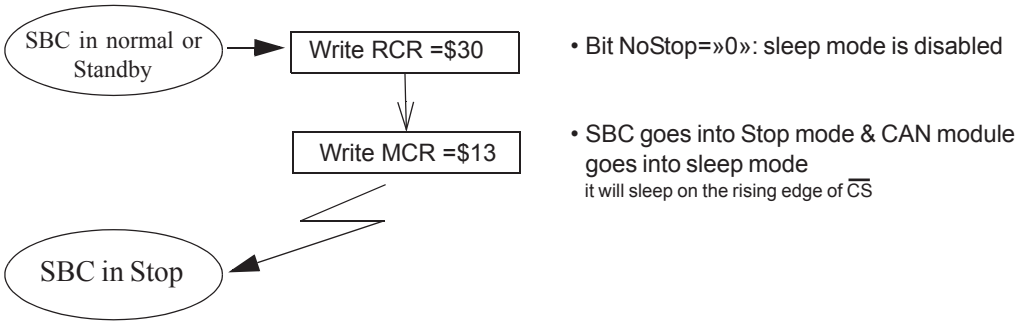


Figure 58. Enter Stop Mode without Watchdog

How to Recognize and Distinguish the Wake-Up Source

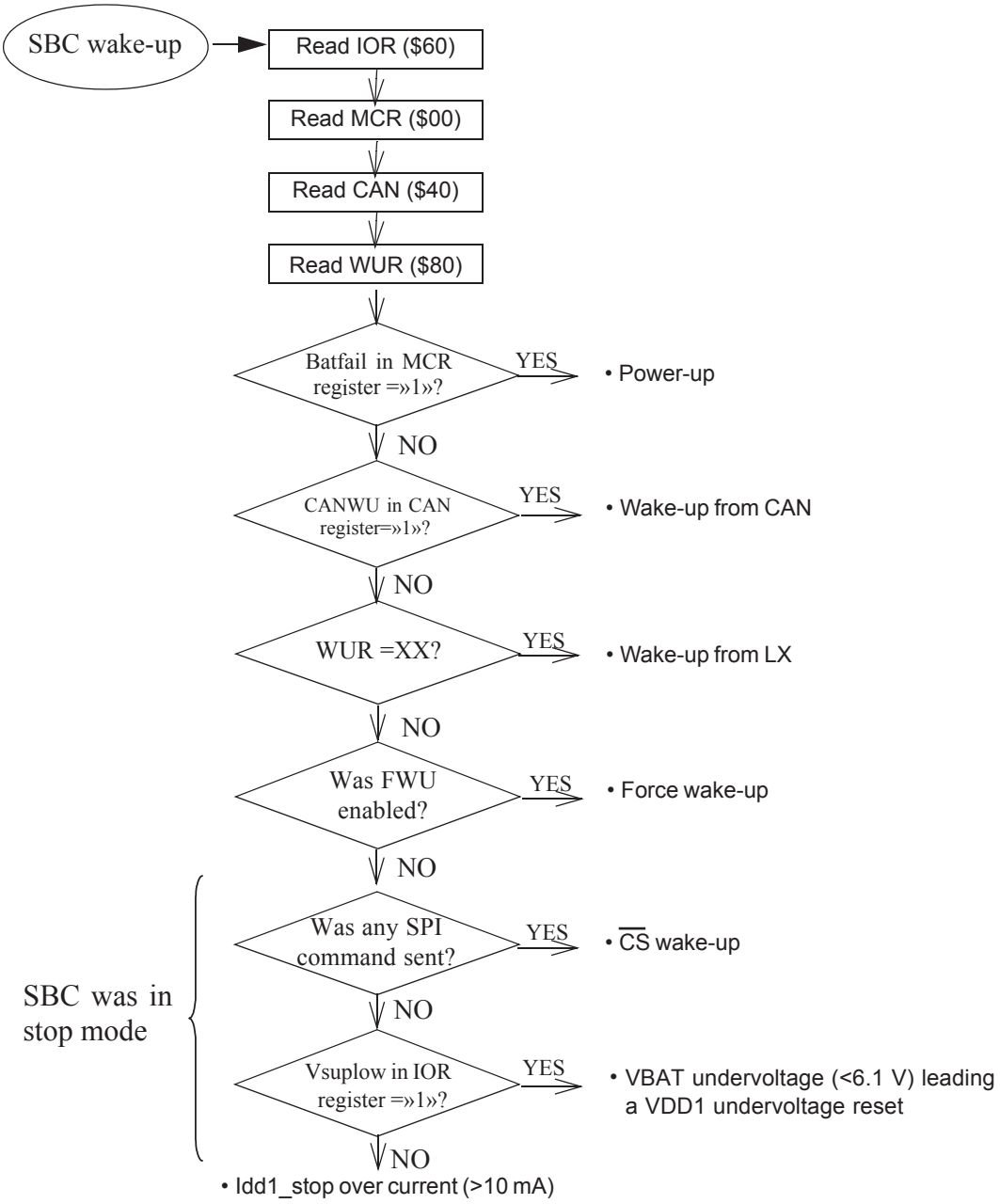


Figure 59. Recognize and Distinguish the Wake-Up Source

How to Use the Interrupt Function

The interruptions are configurable in the INTR register. CAN failure, V2 voltage below 4 V, HS1 overtemperature, V_{SUP} below 6.1 V are interruption configurable.

Recognition and Recovery

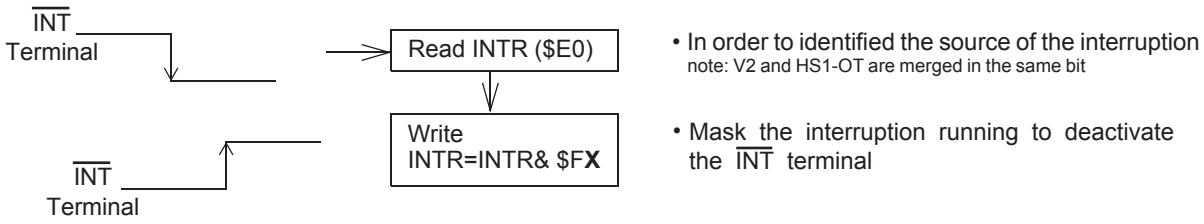


Figure 60. Recognition and Recovery

How to Distinguish Between V2LOW and HS1 Overtemperature

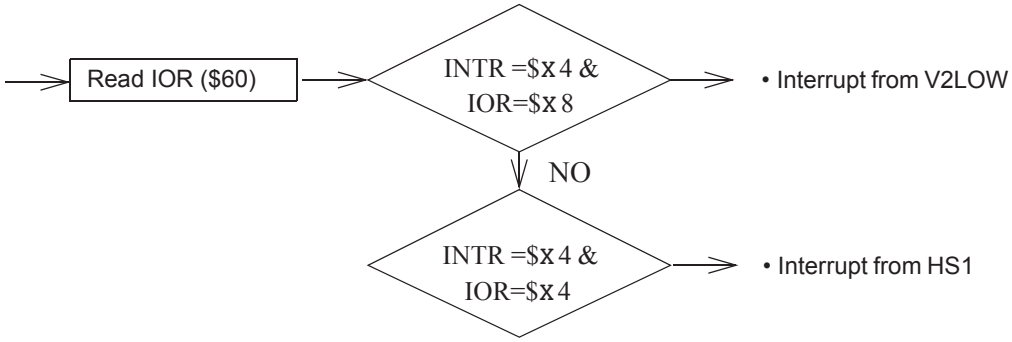
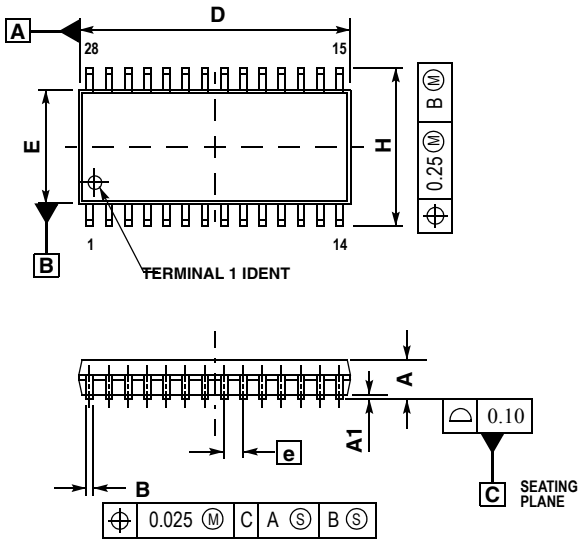


Figure 61. Distinguish Between V2LOW and HS1 Overtemperature

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
4. MAXIMUM MOLD PROTRUSION 0.015 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.13	0.29
B	0.35	0.49
C	0.23	0.32
D	17.80	18.05
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
L	0.41	0.90
θ	0°	8°

DW SUFFIX
28-TERMINAL
98ASB42345B
ISSUE F

ADDITIONAL DOCUMENTATION

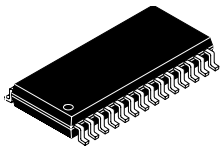
THERMAL ADDENDUM (REV 2.0)

INTRODUCTION

This thermal addendum is provided as a supplement to the MC33989 technical datasheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application, and packaging information is provided in the data sheet.

33989

28-TERMINAL SOICW



DWB SUFFIX
98ASB42345B
28-TERMINAL SOICW

Note For package dimensions, refer to the 33989 device datasheet.

Packaging and Thermal Considerations

The MC33989 is offered in a 28 terminal SOICW, single die package. There is a single heat source (P), a single junction temperature (T_J), and thermal resistance ($R_{\theta JA}$).

$$\{ T_J \} = [R_{\theta JA}] \cdot \{ P \}$$

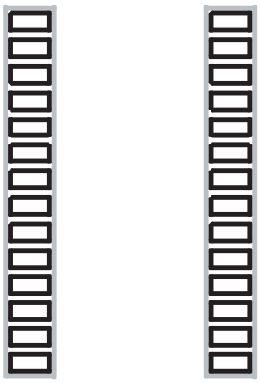
The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below.

Standards

Table 36. Thermal Performance Comparison

Thermal Resistance	[°C/W]
$R_{\theta JA}$ (1) (2)	41
$R_{\theta JB}$ (2) (3)	10
$R_{\theta JA}$ (1) (4)	68
$R_{\theta JC}$ (5)	220

Notes
1. Per JEDEC JESD51-2 at natural convection, still air condition.
2. 2s2p thermal test board per JEDEC JESD51-7.
3. Per JEDEC JESD51-8, with the board temperature on the center trace near the center lead.
4. Single layer thermal test board per JEDEC JESD51-3.
5. Thermal resistance between the die junction and the package top surface; cold plate attached to the package top surface and remaining surfaces insulated.



28 Terminal SOICW
1.27 mm Pitch
18.0 mm x 7.5 mm Body

Figure 62. Surface Mount for SOIC Wide Body non-Exposed Pad

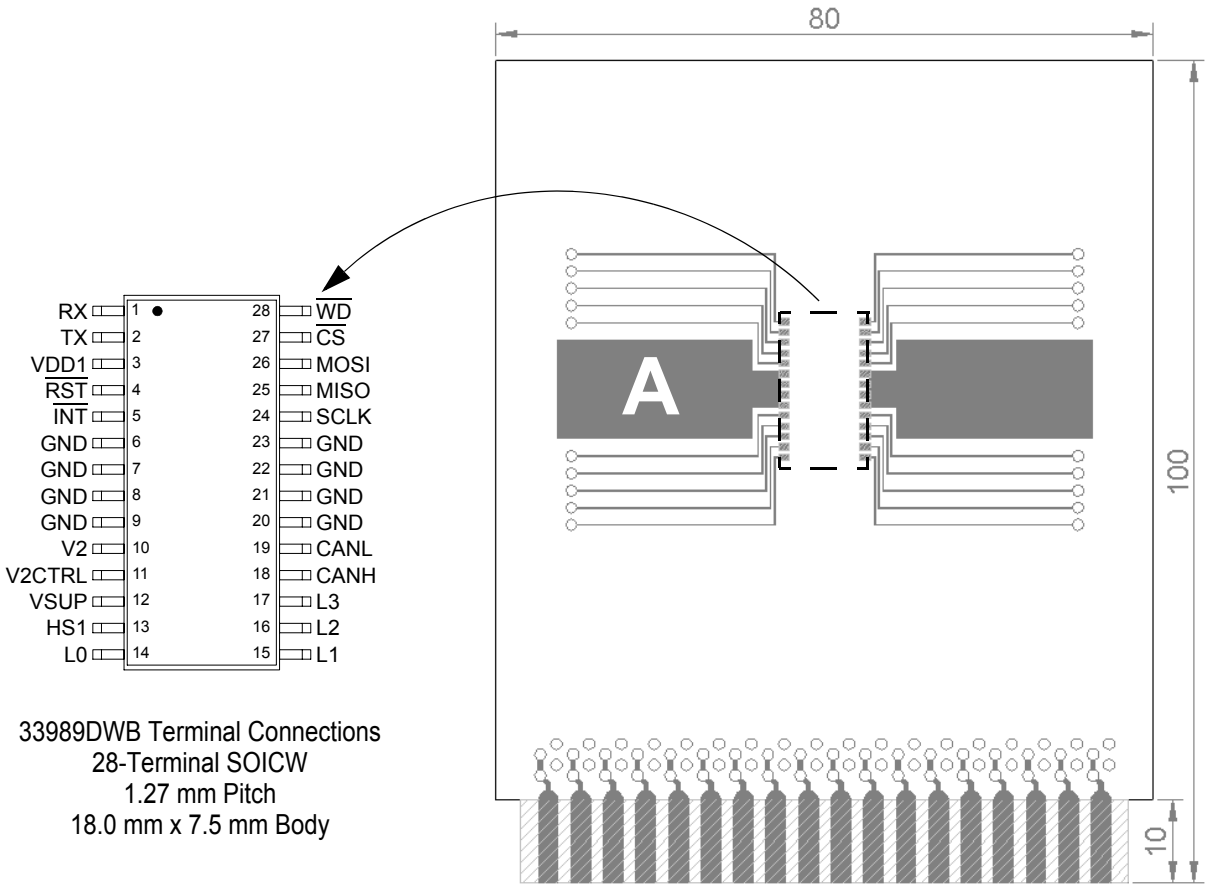


Figure 63. Thermal Test Board

Device on Thermal Test Board

Material:	Single layer printed circuit board FR4, 1.6 mm thickness Cu traces, 0.07 mm thickness
Outline:	80 mm x 100 mm board area, including edge connector for thermal testing
Area **A**:	Cu heat-spreading areas on board surface
Ambient Conditions:	Natural convection, still air

Table 37. Thermal Resistance Performance

Thermal Resistance	Area A (mm^2)	°C/W
$R_{\theta JA}$	0	68
	300	52
	600	47

$R_{\theta JA}$ is the thermal resistance between die junction and ambient air.

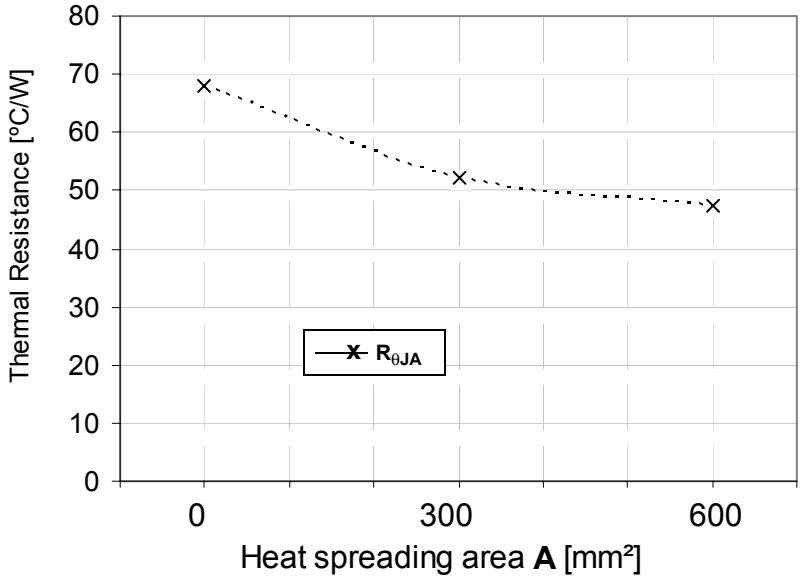


Figure 64. Device on Thermal Test Board $R_{\theta JA}$

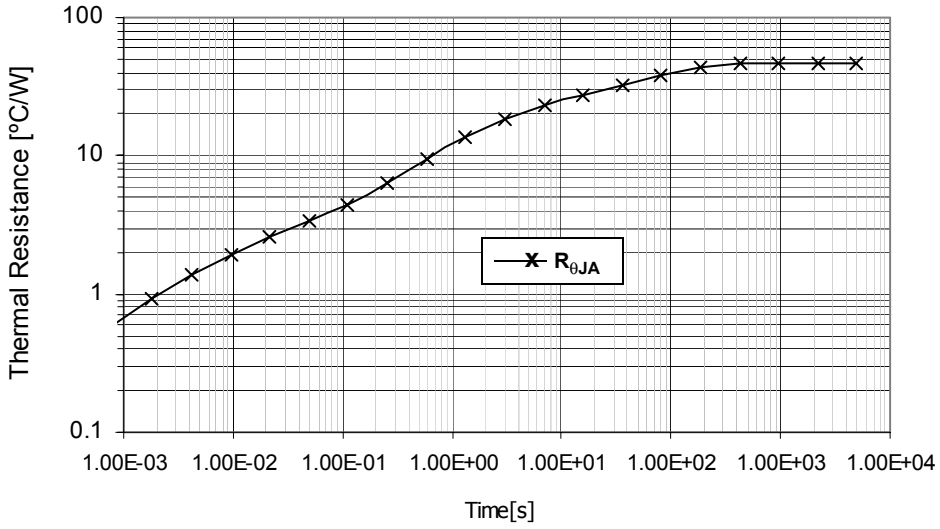


Figure 65. Transient Thermal Resistance $R_{\theta JA}$
1 W Step response, Device on Thermal Test Board Area A = 600 (mm^2)

REVISION HISTORY

Revision	Date	Description of Changes
4.91	7/2002	• Released XC33989: Motorola Format
5.0	8/2005	• Changed document to Freescale format • Added New Orderable Part Number • **Maximum Rating** Table; Added CANH, CANL and ESD ratings • **Static Electrical Characteristics** - Table 3 • POWER INPUT (V_{SUP}): ($I_{SUP(STOP2)}$; Max rating changed from 410 to 210 µA) • POWER OUTPUT(V_{DD1}): V_{DD1OUT} Min rating changed from 4.0 to 4.75 V • Added CAN SUPPLY, CANH and CANL, TX and RX ratings • **Dynamic Electrical Characteristics** - Table 4 • STATE MACHINE TIMING ($\overline{CS}$, SCLK, MOSI, MISO, $\overline{WD}$, $\overline{INT}$): CS_{FWU7} max rating changed from 248 to 128 ms • Added CAN MODULE-SIGNAL EDGE RISE AND FALL TIMES (CANH, CANL) ratings • Revised **Application Section** • Added supplemental Application Notes • Added **Thermal Addendum**
6.0	9/2005	• Cosmetic corrections • CS, INT and WD Terminals were changed to $\overline{CS}$, $\overline{INT}$ and $\overline{WD}$
7.0	11/2005	• Published in error
8.0	11/2005	• **Static Electrical Characteristics** - Table 3, added new parameter “VDDst-cap” and Notes 14 and 16, corrected VDD1 output voltage $V_{DD1OUT2}$ to minimum 4.0 V as previously published in revision 4.91. • **Dynamic Electrical Characteristics** - Table 4, Corrected Max Rating of 248 ms for Cyclic Sense/FWU Timing 7 CS_{FWU7} as previously published in revision 4.91
9.0	1/2006	• **Dynamic Electrical Characteristics** - Table 4,Corrected “Cyclic Sense ON Time” measurement “Unit” from **ms** to **µs**

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