

CY7C130/CY7C131
CY7C140/CY7C141

1K x 8 Dual-Port Static RAM

Features

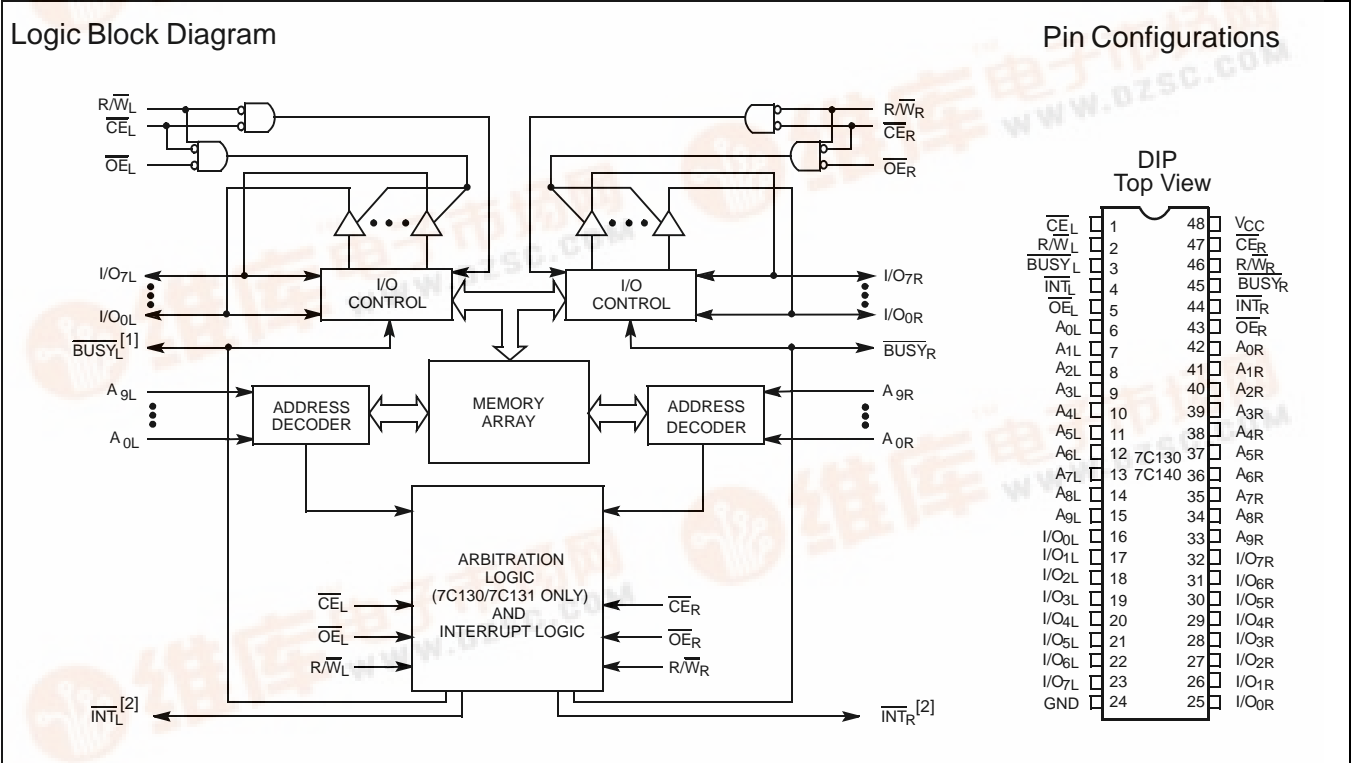
- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- 1K x 8 organization
- 0.65-micron CMOS for optimum speed/power
- High-speed access: 15 ns
- Low operating power: I_{CC} = 110 mA (max.)
- Fully asynchronous operation
- Automatic power-down
- Master CY7C130/CY7C131 easily expands data bus width to 16 or more bits using slave CY7C140/CY7C141
- BUSY output flag on CY7C130/CY7C131; BUSY input on CY7C140/CY7C141
- INT flag for port-to-port communication
- Available in 48-pin DIP (CY7C130/140), 52-pin PLCC, 52-Pin TQFP.
- Pb-Free packages available

Functional Description

The CY7C130/CY7C131/CY7C140 and CY7C141 are high-speed CMOS 1K by 8 dual-port static RAMs. Two ports are provided permitting independent access to any location in memory. The CY7C130/ CY7C131 can be utilized as either a standalone 8-bit dual-port static RAM or as a master dual-port RAM in conjunction with the CY7C140/CY7C141 slave dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data, such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins: chip enable (CE), write enable (R/W), and output enable (OE). Two flags are provided on each port, BUSY and INT. BUSY signals that the port is trying to access the same location currently being accessed by the other port. INT is an interrupt flag indicating that data has been placed in a unique location (3FF for the left port and 3FE for the right port). An automatic power-down feature is controlled independently on each port by the chip enable (CE) pins.

The CY7C130 and CY7C140 are available in 48-pin DIP. The CY7C131 and CY7C141 are available in 52-pin PLCC, 52-pin Pb-free PLCC, 52-pin PQFP and 52-pin Pb-free PQFP.



- Note:
1. CY7C130/CY7C131 (Master): BUSY is open drain output and requires pull-up resistor
CY7C140/CY7C141 (Slave): BUSY is input.
 2. Open drain outputs: pull-up resistor required.



