CY7C1046B

1M x 4 Static RAM

Features

- **High speed**
  - **— t_{AA} = 12 ns**
- **Low active power**
  - **— 935 mW (max.)**
- **Low CMOS standby power (L version)**
  - **— 2.75 mW (max.)**
- **2.0V Data Retention (400 µW at 2.0V retention)**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ features**

Functional Description

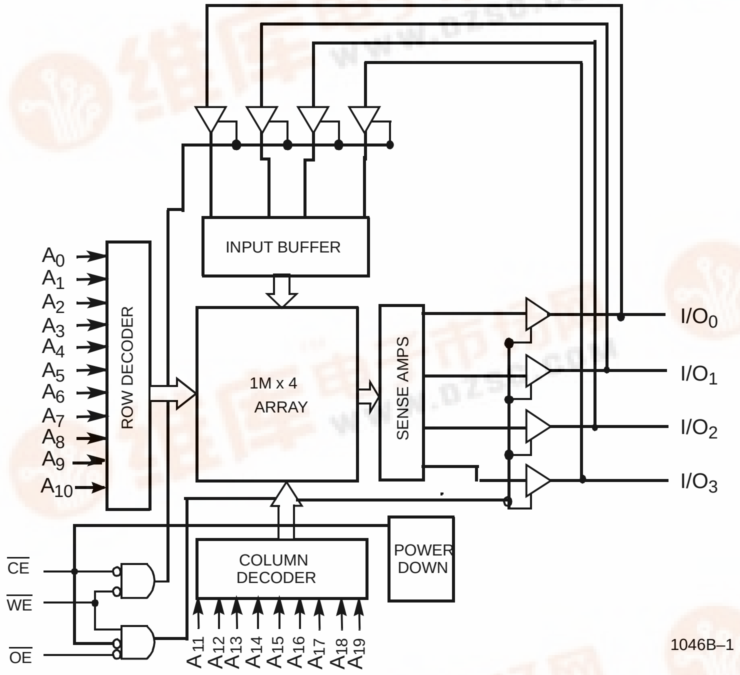
The CY7C1046B is a high-performance CMOS static RAM organized as 1,048,576 words by 4 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{\text{CE}}$), an active LOW Output Enable ($\overline{\text{OE}}$), and three-state drivers. Writing to the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Write Enable ($\overline{\text{WE}}$) inputs LOW. Data on the four I/O pins (I/O_0 through I/O_3) is then written into the location specified on the address pins (A_0 through A_{19}).

Reading from the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Output Enable ($\overline{\text{OE}}$) LOW while forcing Write Enable ($\overline{\text{WE}}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The four input/output pins (I/O_0 through I/O_3) are placed in a high-impedance state when the device is deselected ($\overline{\text{CE}}$ HIGH), the outputs are disabled ($\overline{\text{OE}}$ HIGH), or during a write operation ($\overline{\text{CE}}$ LOW, and $\overline{\text{WE}}$ LOW).

The CY7C1046B is available in a standard 400-mil-wide 32-pin SOJ package with center power and ground (revolutionary) pinout.

Logic Block Diagram



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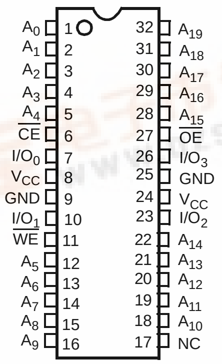
Pin Configuration

SOJ
Top View



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Selection Guide

		7C1046B-12	7C1046B-15	7C1046B-20
Maximum Access Time (ns)		12	15	20
Maximum Operating Current (mA)		170	150	130
Maximum CMOS Standby Current (mA)	Com’l	8	8	8
	L version	0.5	0.5	0.5

Shaded areas contain advance information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....–65°C to +150°C

Ambient Temperature with
Power Applied...–55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[1] .... –0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State[1] ....–0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ....–0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage .... >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current.. >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	4.5V–5.5V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C1046B-12		7C1046B-15		7C1046B-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]		–0.3	0.8	–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$	–1	+1	–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND $\leq V_{OUT} \leq V_{CC}$, Output Disabled	–1	+1	–1	+1	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., $f = f_{MAX} = 1/t_{RC}$		170		150		130	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$		20		20		20	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$, or $V_{IN} \leq 0.3V$, f = 0 Com'l		8		8		8	mA
		L version		0.5		0.5		0.5	

Shaded areas contain advance information.

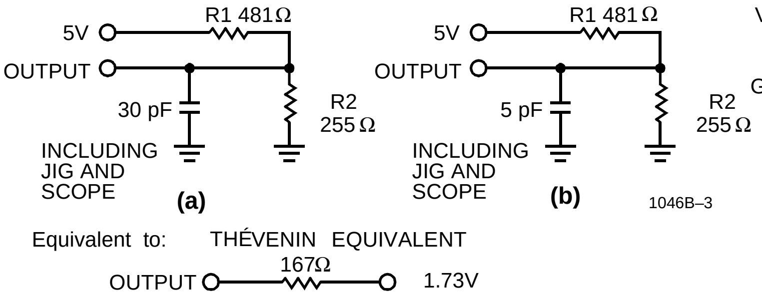
Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	6	pF
C_{OUT}	I/O Capacitance		6	pF

Note:

1. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
2. T_A is the "Instant On" case temperature.
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



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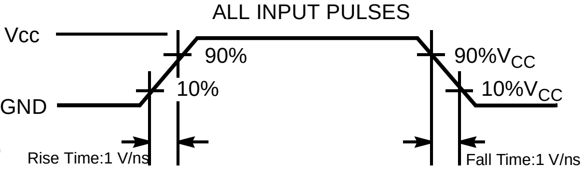

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Switching Characteristics[4] Over the Operating Range

Parameter	Description	7C1046B-12		7C1046B-15		7C1046B-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{power}	V_{CC}(typical) to the first access[5]	1		1		1		µs
t_{RC}	Read Cycle Time	12		15		20		ns
t_{AA}	Address to Data Valid		12		15		20	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{\text{CE}}$ LOW to Data Valid		12		15		20	ns
t_{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		6		7		8	ns
t_{LZOE}	$\overline{\text{OE}}$ LOW to Low Z[7]	0		0		0		ns
t_{HZOE}	$\overline{\text{OE}}$ HIGH to High Z[6, 7]		6		7		8	ns
t_{LZCE}	$\overline{\text{CE}}$ LOW to Low Z[7]	3		3		3		ns
t_{HZCE}	$\overline{\text{CE}}$ HIGH to High Z[6, 7]		6		7		8	ns
t_{PU}	$\overline{\text{CE}}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{\text{CE}}$ HIGH to Power-Down		12		15		20	ns
WRITE CYCLE[8, 9]								
t_{WC}	Write Cycle Time	12		15		20		ns
t_{SCE}	$\overline{\text{CE}}$ LOW to Write End	8		10		15		ns
t_{AW}	Address Set-Up to Write End	8		10		15		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{\text{WE}}$ Pulse Width	8		10		12		ns
t_{SD}	Data Set-Up to Write End	6		8		10		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z[7]	3		3		3		ns
t_{HZWE}	$\overline{\text{WE}}$ LOW to High Z[6, 7]		6		7		8	ns

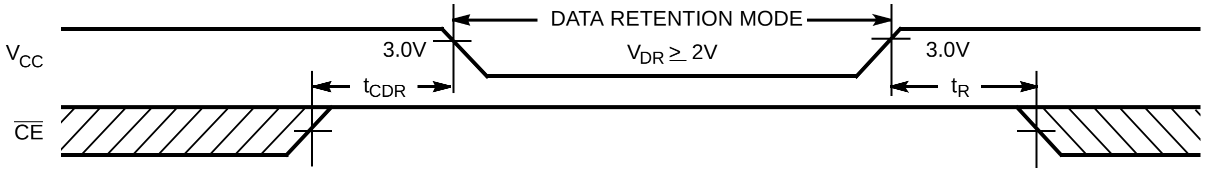
Notes:

4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. This part has a voltage regulator which steps down the voltage from 5V to 3.3V internally. t_{power} time has to be provided initially before a read/write operation is started.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW, and $\overline{\text{WE}}$ LOW. $\overline{\text{CE}}$ and $\overline{\text{WE}}$ must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
9. The minimum write cycle time for Write Cycle no. 3 ($\overline{\text{WE}}$ controlled, $\overline{\text{OE}}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Data Retention Characteristics Over the Operating Range

Parameter	Description		Conditions[10]	Min.	Max	Unit
V_{DR}	V_{CC} for Data Retention			2.0		V
I_{CCDR}	Data Retention Current	Com'l	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		200	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time			0		ns
t_R	Operation Recovery Time			200		µs

Data Retention Waveform



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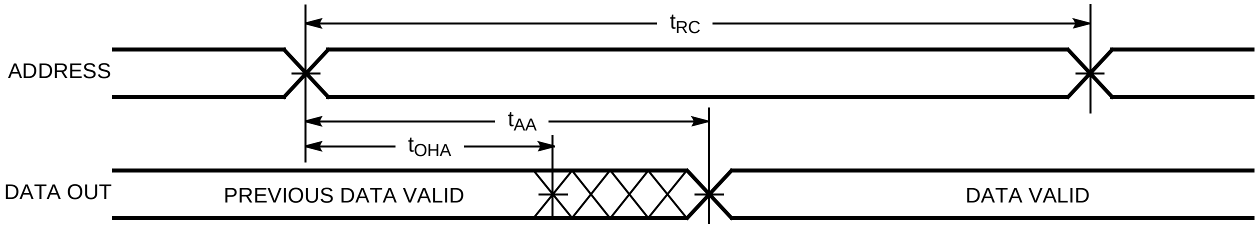
Switching Waveforms

Read Cycle No. 1[11, 12]



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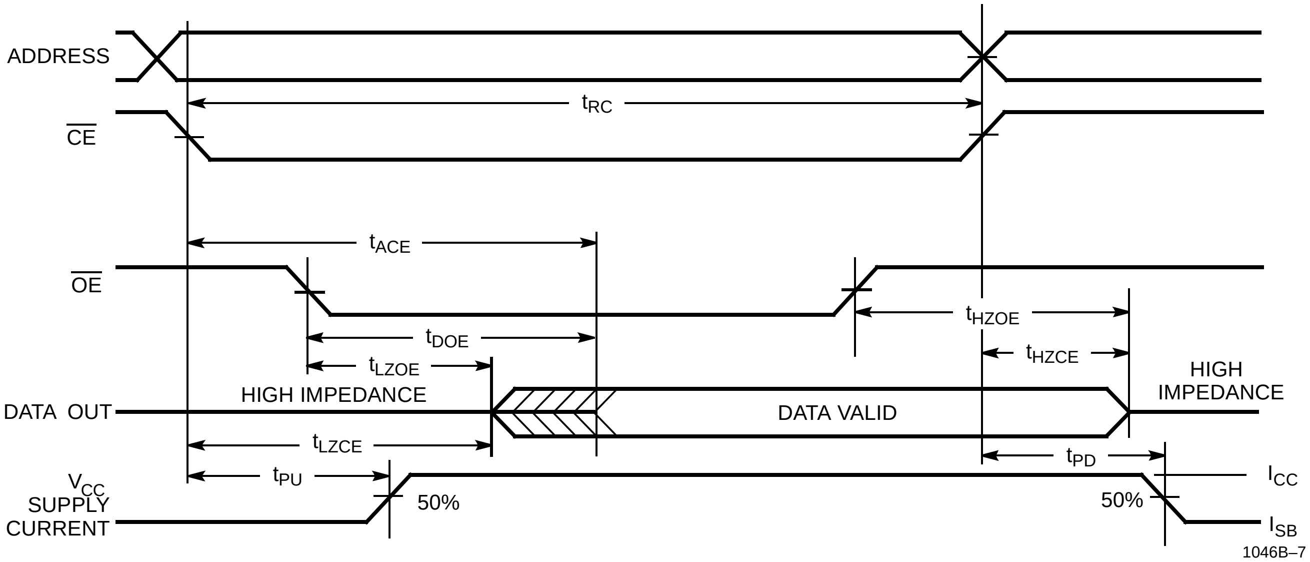
Read Cycle No. 2 ($\overline{OE}$ Controlled)[12, 13]



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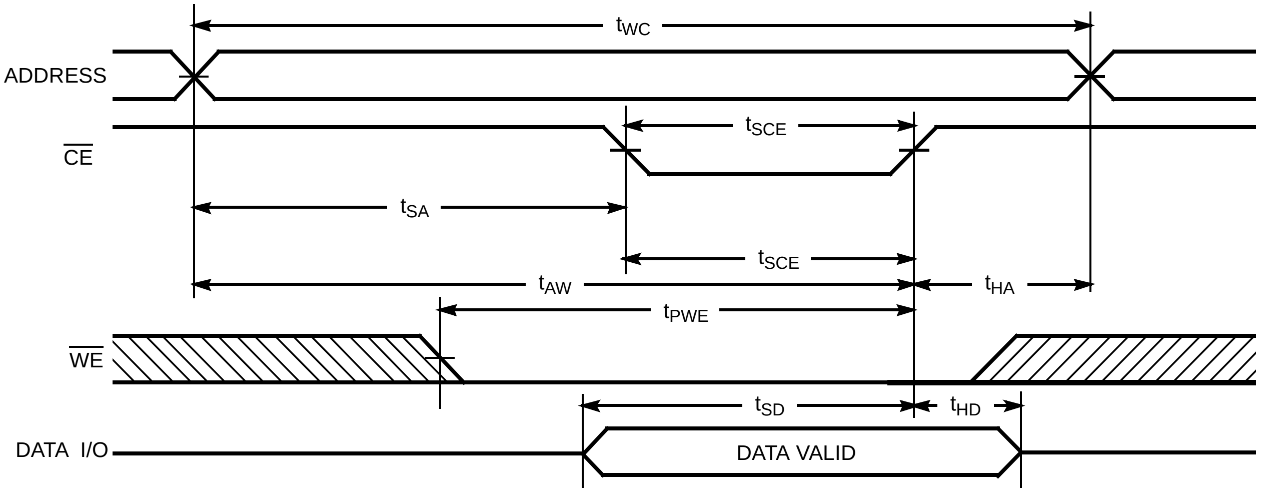
Notes:

10. No input may exceed V_{CC} + 0.5V.
11. Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled)[14, 15]



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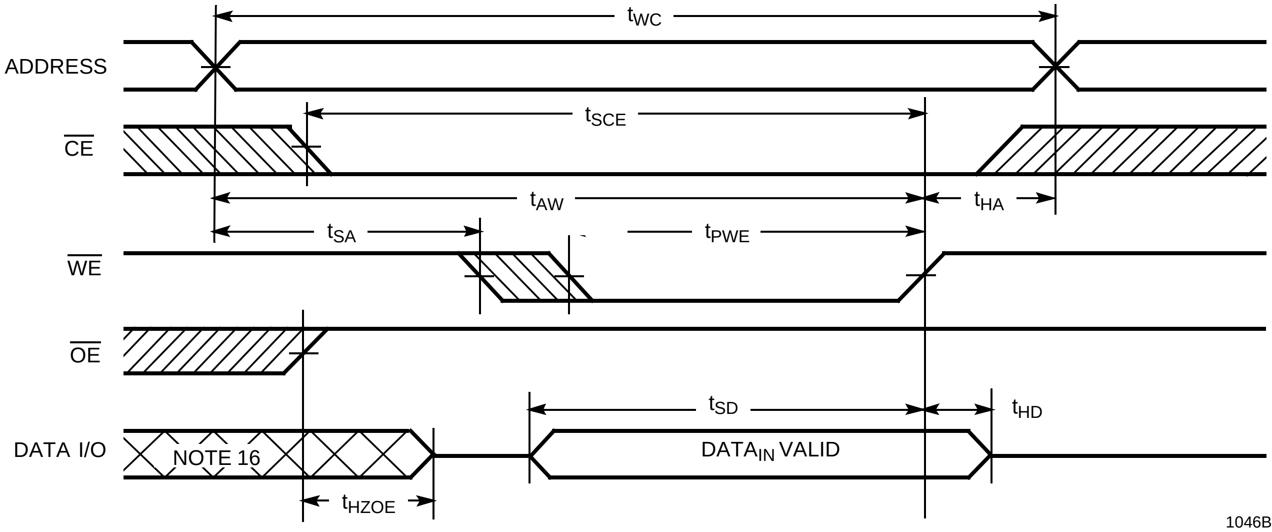
Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[14, 15]



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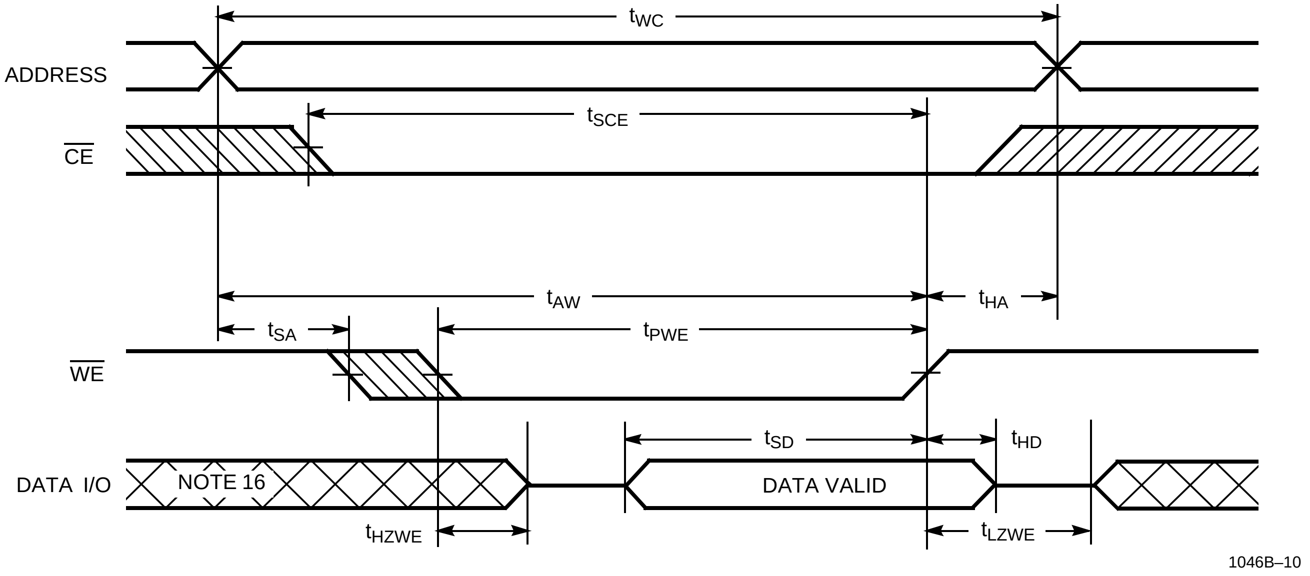
Notes:

14. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
16. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)[15]



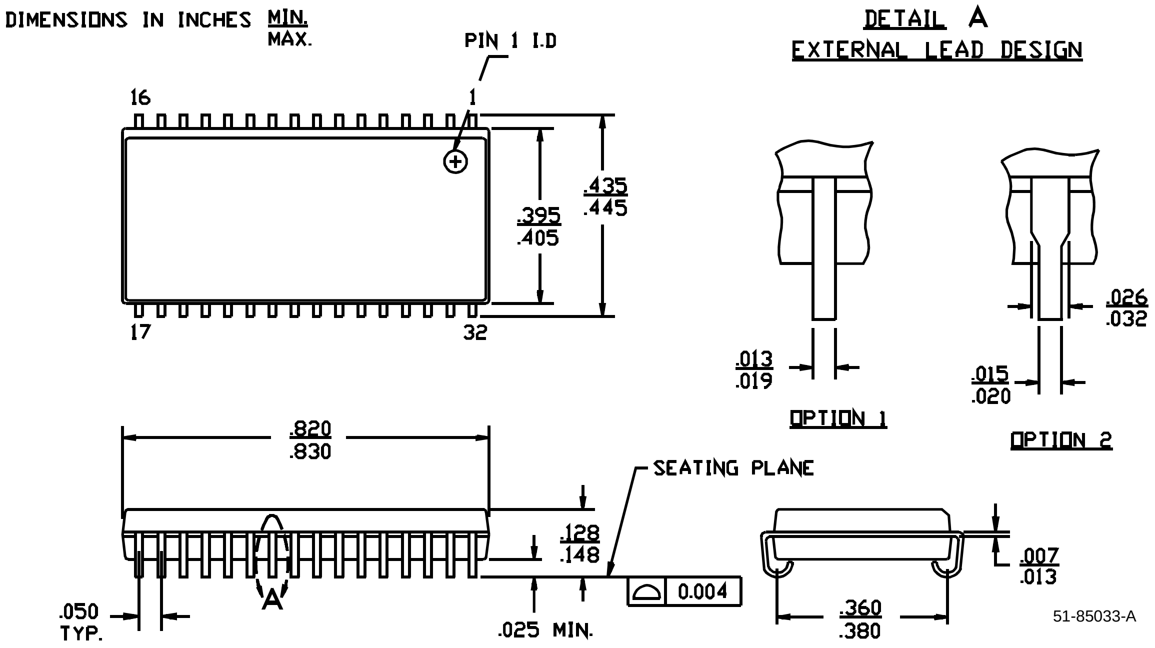
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1046B-12VC	V33	32-Lead (400-Mil) Molded SOJ	Commercial
15	CY7C1046B-15VC	V33	32-Lead (400-Mil) Molded SOJ	
20	CY7C1046B-20VC	V33	32-Lead (400-Mil) Molded SOJ	
12	CY7C1046BL-12VC	V33	32-Lead (400-Mil) Molded SOJ	
15	CY7C1046BL-15VC	V33	32-Lead (400-Mil) Molded SOJ	
20	CY7C1046BL-20VC	V33	32-Lead (400-Mil) Molded SOJ	

Shaded areas contain advance information.

Package Diagram

32-Lead (400-Mil) Molded SOJ V33



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REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	109888	09/22/01	SZV	Change from Spec number: 38-00948 to 38-05144