



CYPRESS

CY7C1024AV33

128K x 24 Static RAM

Features

- High speed
— $t_{AA} = 10 \text{ ns}$
- CMOS for optimum speed/power
- Center power/ground pinout
- Automatic power-down when deselected
- Easy memory expansion with CE1, CE2, CE3 and OE options

Functional Description^[1]

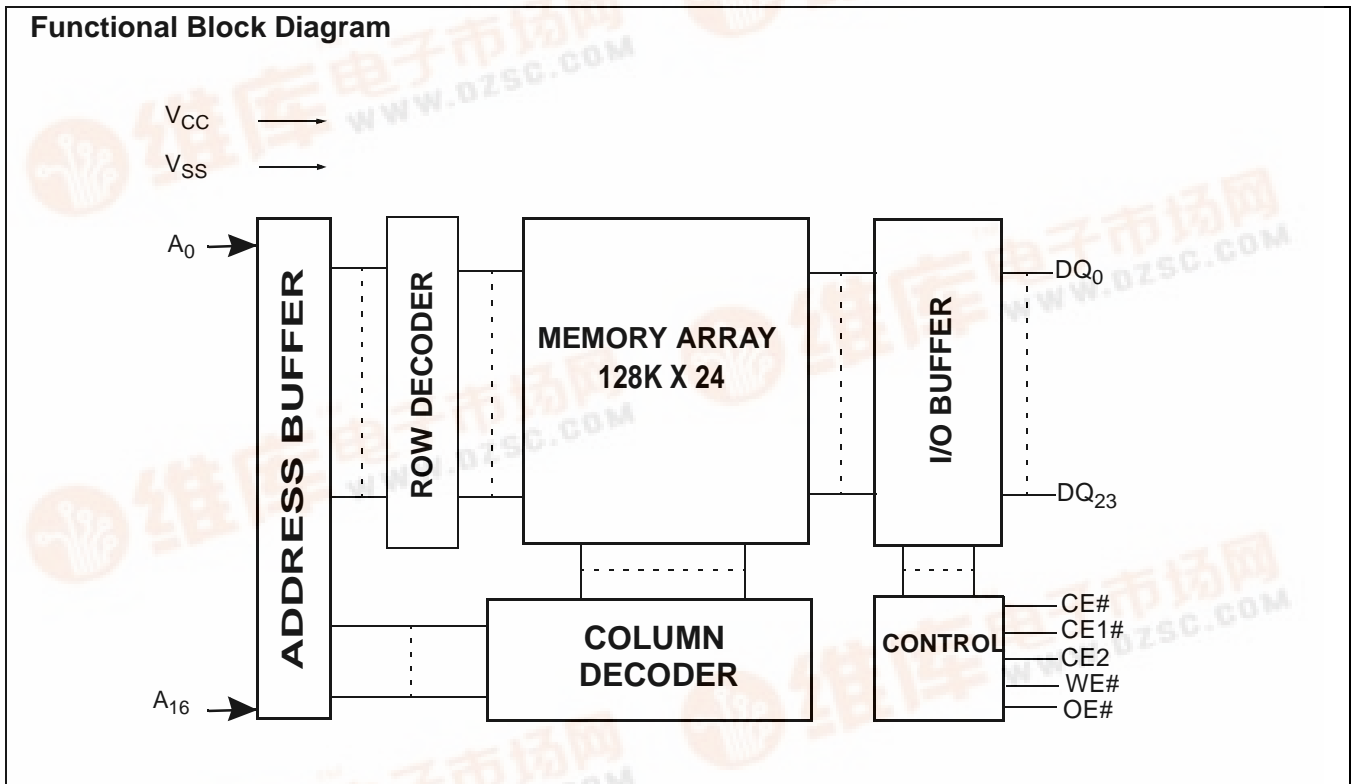
The CY7C1024AV33 is a high-performance CMOS static RAM organized as 131,072 words by 24 bits. Easy memory expansion is provided by an active LOW $\overline{CE1}$, $\overline{CE3}$, active HIGH CE2, an active LOW Output Enable (\overline{OE}), and three-state drivers. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$) active and Write Enable (\overline{WE}) inputs LOW. Data on the 24 I/O pins (I/O_0 through I/O_{23}) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$) active and Output Enable (\overline{OE}) LOW while forcing Write Enable (\overline{WE}) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The 24 input/output pins (I/O_0 through I/O_{23}) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), or during a write operation ($\overline{CE1}$, $\overline{CE3}$ LOW, $\overline{CE2}$ HIGH, and \overline{WE} LOW).

The CY7C1024AV33 is available in a standard 119-ball BGA package and a 100-pin TQFP package.



Selection Guide

	7C1024AV33-10	7C1024AV33-12	7C1024AV33-15
Maximum Access Time (ns)	10	12	15
Maximum Operating Current (mA)	275	250	225
Maximum Standby Current (mA)	15	15	15

Note:

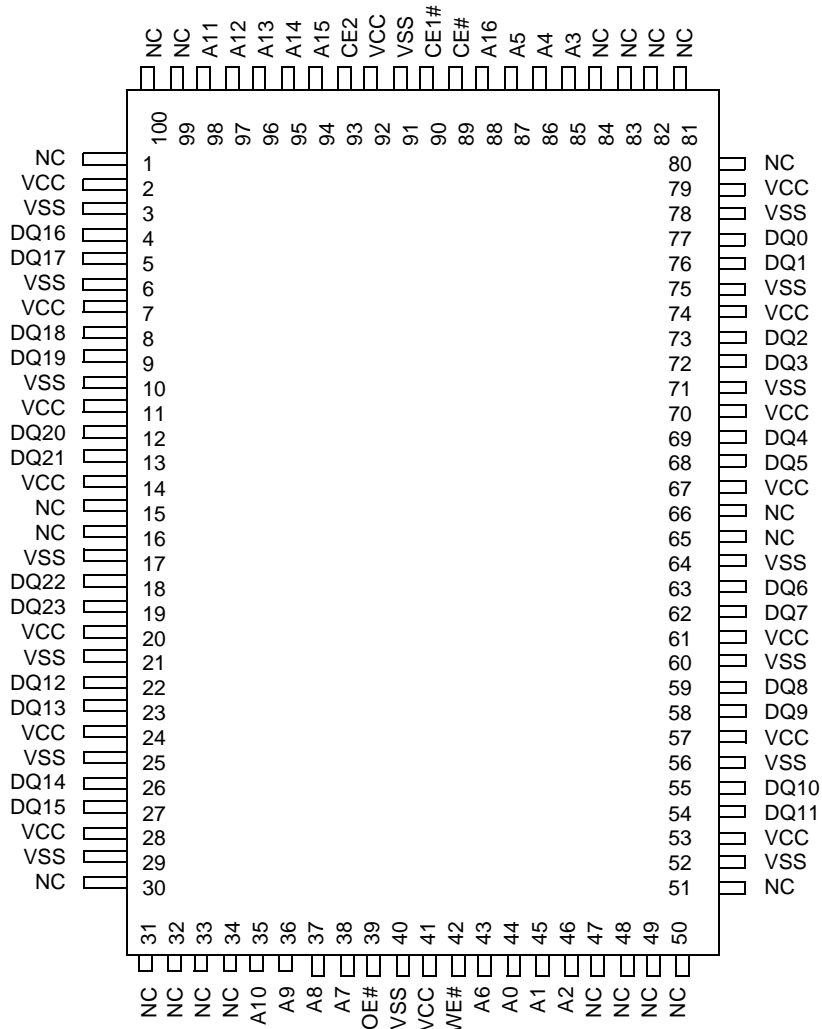
1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.



Pin Configurations
**119 BGA
Top View**

	1	2	3	4	5	6	7
A	NC	A	A	A	A	A	NC
B	NC	A	A	$\overline{\text{CE1}}$	A	A	NC
C	DQ	NC	CE2	NC	$\overline{\text{CE3}}$	NC	DQ
D	DQ	V _{CC}	V _{SS}	V _{SS}	V _{SS}	V _{CC}	DQ
E	DQ	V _{SS}	V _{CC}	V _{SS}	V _{CC}	V _{SS}	DQ
F	DQ	V _{CC}	V _{SS}	V _{SS}	V _{SS}	V _{CC}	DQ
G	DQ	V _{SS}	V _{CC}	V _{SS}	V _{CC}	V _{SS}	DQ
H	DQ	V _{CC}	V _{SS}	V _{SS}	V _{SS}	V _{CC}	DQ
J	NC	V _{SS}	V _{CC}	V _{SS}	V _{CC}	V _{SS}	NC
K	DQ	V _{CC}	V _{SS}	V _{SS}	V _{SS}	V _{CC}	DQ
L	DQ	V _{SS}	V _{CC}	V _{SS}	V _{CC}	V _{SS}	DQ
M	DQ	V _{CC}	V _{SS}	V _{SS}	V _{SS}	V _{CC}	DQ
N	DQ	V _{SS}	V _{CC}	V _{SS}	V _{CC}	V _{SS}	DQ
P	DQ	V _{CC}	V _{SS}	V _{SS}	V _{SS}	V _{CC}	DQ
R	DQ	NC	NC	NC	NC	NC	DQ
T	NC	A	A	$\overline{\text{WE}}$	A	A	NC
U	NC	A	A	$\overline{\text{OE}}$	A	A	NC

Pin Configurations (continued)

**100-pin TQFP
Top View**

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied..... -55°C to +125°C

Supply Voltage on V_{CC} to Relative GND^[2].... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State^[2] -0.5V to V_{CC} + 0.5V

DC Input Voltage^[2]..... -0.5V to V_{CC} + 0.5V

Note:

2. Minimum Voltage is = -2.0V for pulse durations of less than 20 ns.

Current into Outputs (LOW) 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

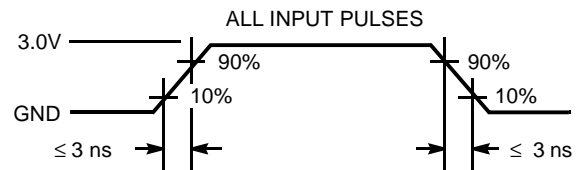
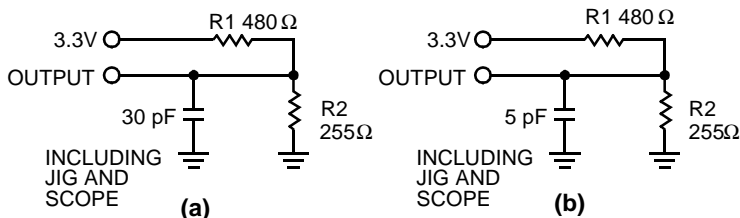
Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	3.3V ±10%
Industrial	-40°C to +85°C	3.3V ±10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions ^[3]	1024AV33-10		1024AV33-12		1024AV33-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage ^[2]		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I _{Ix}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-3	+3	-3	+3	-3	+3	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	-5	+5	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}		275		250		225	mA
I _{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V _{CC} , $\overline{CE} \geq V_{IH}$ V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		60		60		60	mA
I _{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V _{CC} , CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0		15		15		15	mA

Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 3.3V	10	pF
C _{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms


Equivalent to: THÉVENIN EQUIVALENT

167 Ω

OUTPUT — 1.73V

Notes:

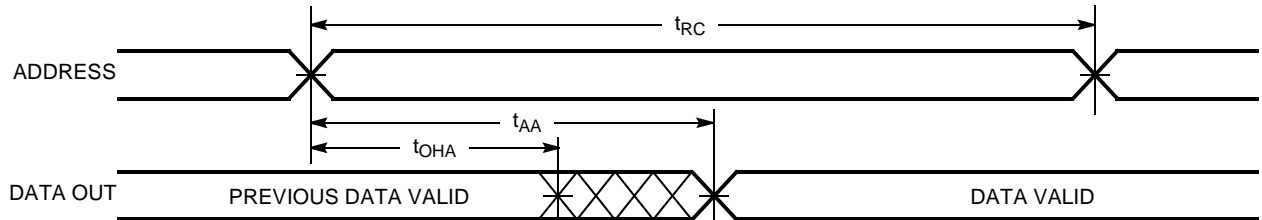
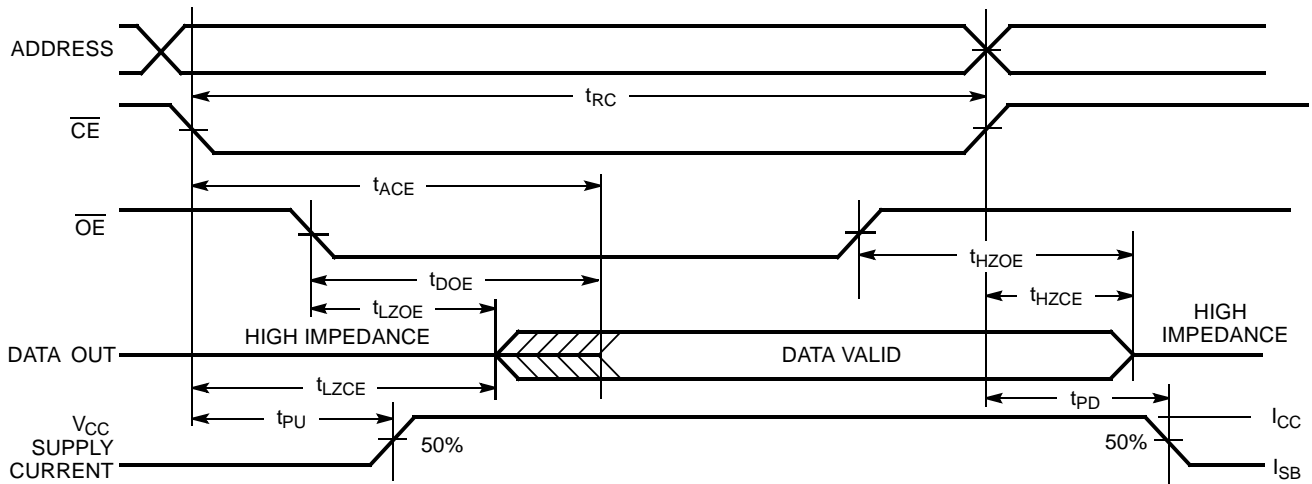
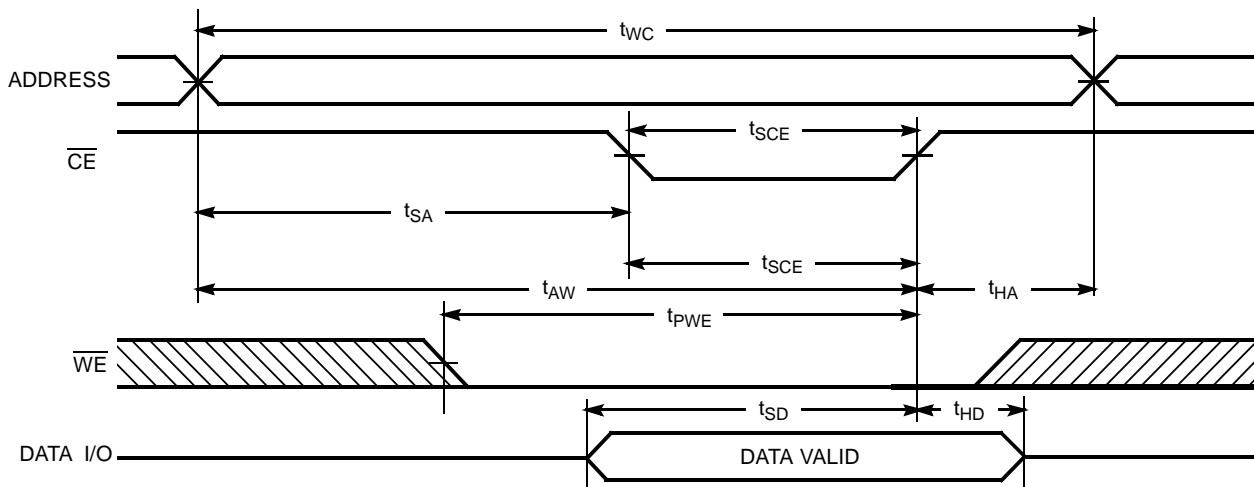
- CE is a combination of $\overline{CE1}$, CE2, and $\overline{CE3}$
- Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics^[5] Over the Operating Range

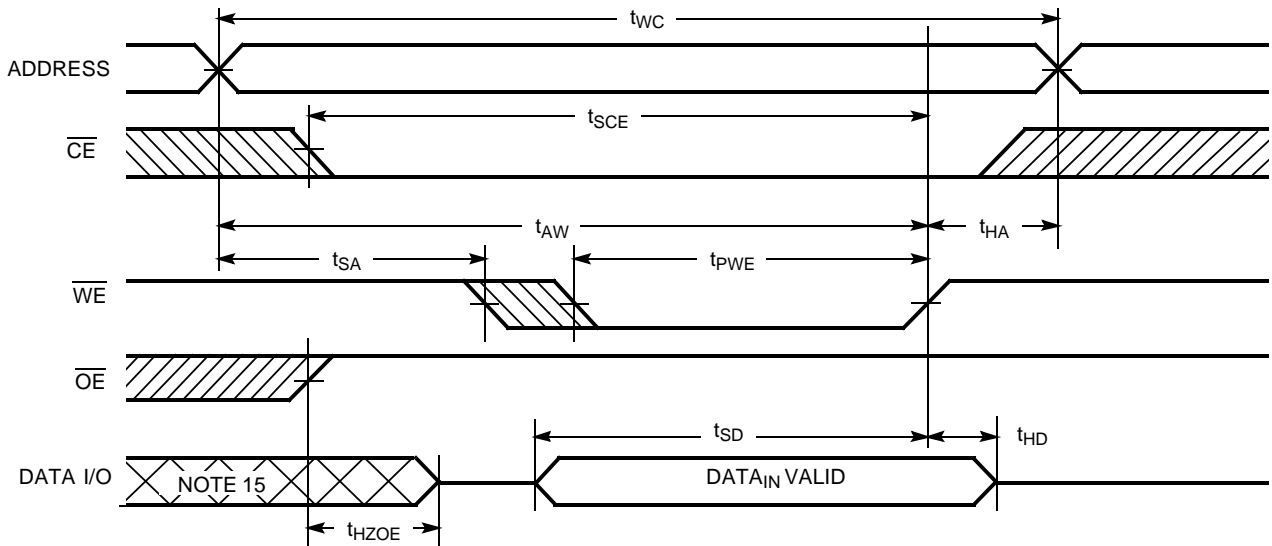
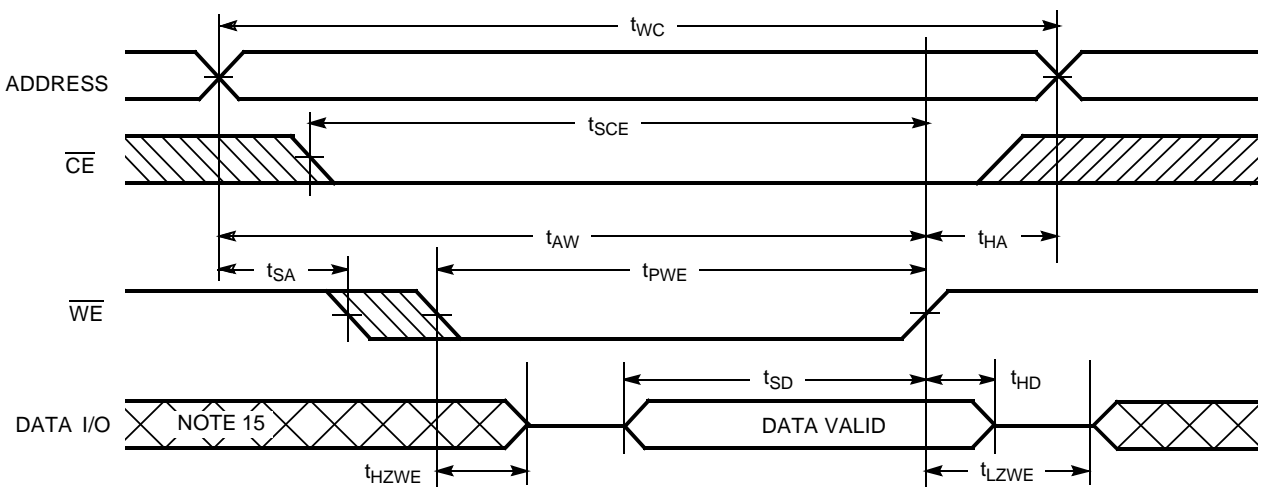
Parameter	Description ^[3]	7C1024AV33-10		7C1024AV33-12		7C1024AV33-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	10		12		15		ns
t _{AA}	Address to Data Valid		10		12		15	ns
t _{OHA}	Data Hold from Address Change	3		3		3		ns
t _{ACE}	\overline{CE} active to Data Valid		10		12		15	ns
t _{DOE}	\overline{OE} LOW to Data Valid		5		6		7	ns
t _{LZOE}	\overline{OE} LOW to Low Z	0		0		0		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[6, 7]		5		6		6	ns
t _{LZCE}	\overline{CE} active to Low Z ^[7]	3		3		3		ns
t _{HZCE}	\overline{CE} inactive to High Z ^[6, 7]		5		6		6	ns
t _{PU}	\overline{CE} active to Power-Up	0		0		0		ns
t _{PD}	\overline{CE} inactive to Power-Down		10		12		15	ns
WRITE CYCLE^[8, 9]								
t _{WC}	Write Cycle Time	10		12		15		ns
t _{SCE}	\overline{CE} active to Write End	8		9		9		ns
t _{AW}	Address Set-Up to Write End	7		8		8		ns
t _{HA}	Address Hold from Write End	0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		ns
t _{PWE}	\overline{WE} Pulse Width	7		8		8		ns
t _{SD}	Data Set-Up to Write End	5		6		6		ns
t _{HD}	Data Hold from Write End	0		0		0		ns
t _{LZWE}	\overline{WE} HIGH to Low Z ^[7]	3		3		3		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[6, 7]		5		6		6	ns

Notes:

5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
9. The minimum write cycle time for Write Cycle no. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms
Read Cycle No. 1^[10, 11]

Read Cycle No. 2 (OE Controlled)^[3, 11, 12]

Write Cycle No. 1 (CE Controlled)^[3, 13, 14]

Notes:

10. Device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.
11. \overline{WE} is HIGH for read cycle.
12. Address valid prior to or coincident with \overline{CE} transition LOW.
13. Data I/O is high impedance if $\overline{OE} = V_{IL}$.
14. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)
Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} HIGH During Write)^[13, 14]

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[3, 14]

Note:

15. During this period the I/Os are in the output state and input signals should not be applied.

Truth Table

CE1	CE2	CE3	OE	WE	I/O ₀ -I/O ₂₃	Mode	Power
H	X	X	X	X	High Z	Power-Down	Standby (I _{SB})
X	L	X	X	X	High Z	Power-Down	Standby (I _{SB})
X	X	H	X	X	High Z	Power-Down	Standby (I _{SB})
L	H	L	L	H	Data Out	Read	Active (I _{CC})
L	H	L	X	L	Data In	Write	Active (I _{CC})
L	H	L	H	H	High Z	Selected, Outputs Disabled	Active (I _{CC})

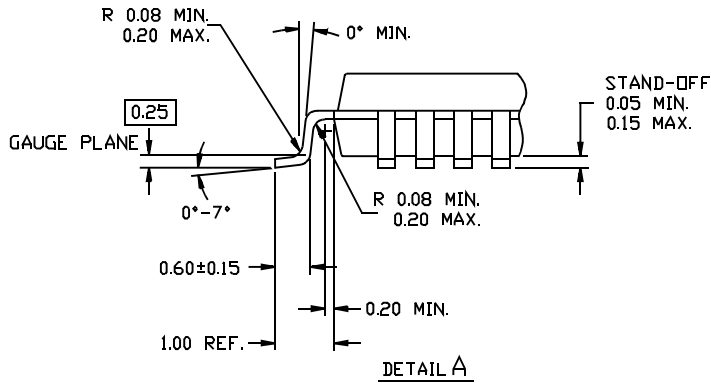
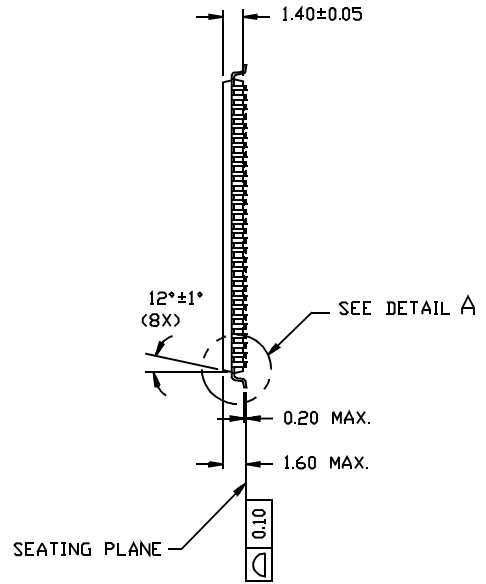
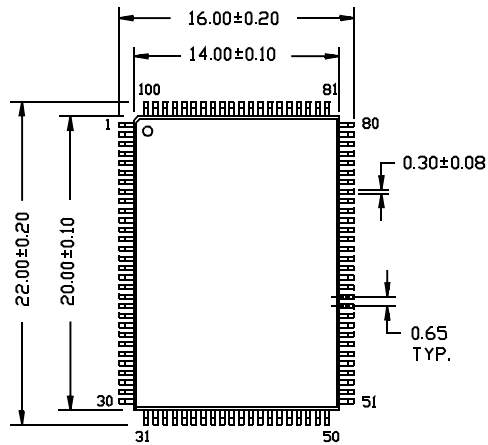
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1024AV33-10AC	A101	100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm)	Commercial
	CY7C1024AV33-10BGC	BG119	119-Ball PBGA	
12	CY7C1024AV33-12AC	A101	100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm)	Industrial
	CY7C1024AV33-12BGC	BG119	119-Ball PBGA	
	CY7C1024AV33-12BGI	BG119	119-Ball PBGA	
15	CY7C1024AV33-15AC	A101	100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm)	Commercial
	CY7C1024AV33-15BGC	BG119	119-Ball PBGA	
	CY7C1024AV33-15BGI	BG119	119-Ball PBGA	Industrial

Package Diagrams

100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101

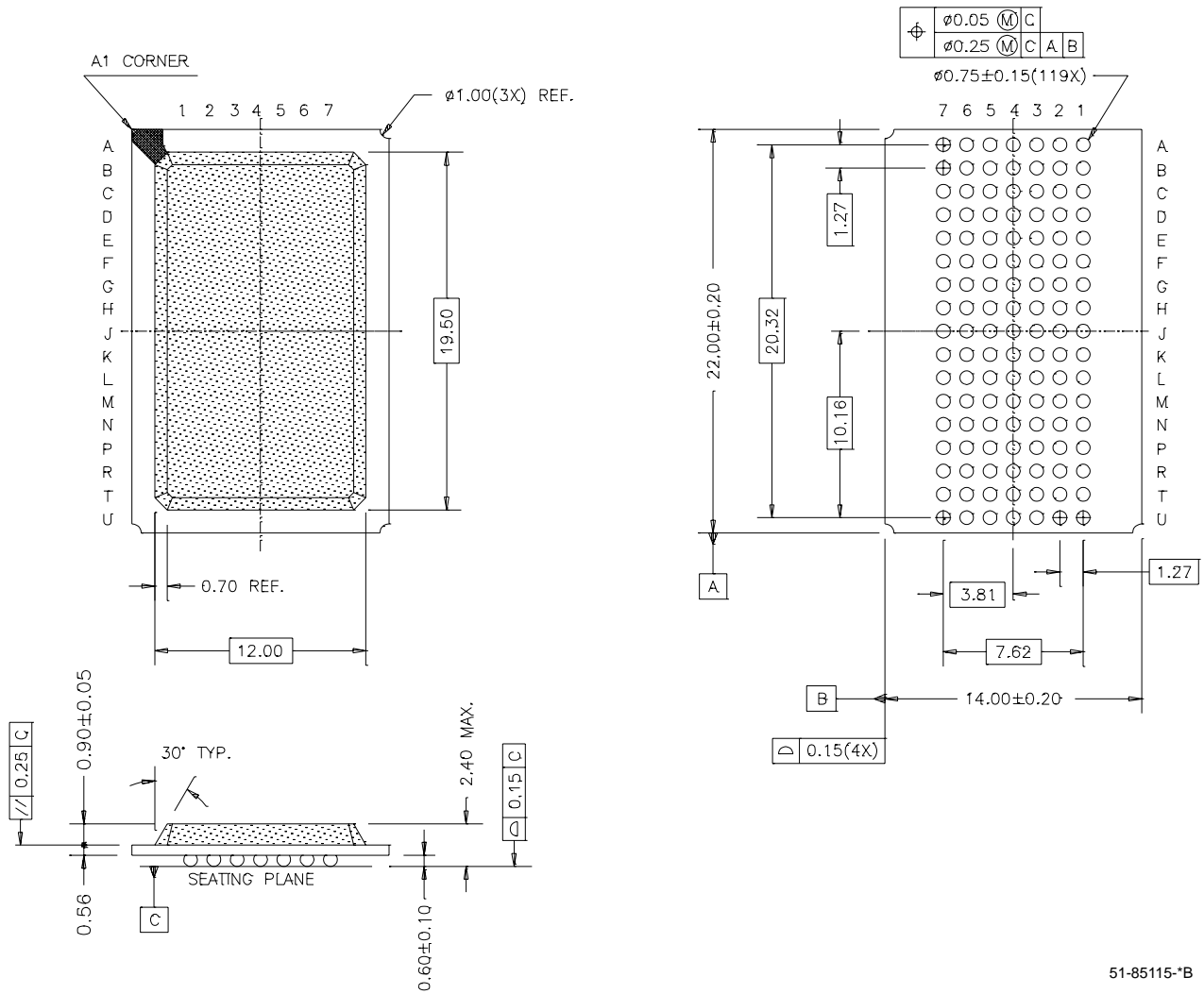
DIMENSIONS ARE IN MILLIMETERS.



51-85050-A

Package Diagrams (continued)

119-Lead PBGA (14 x 22 x 2.4 mm) BG119



51-85115-*B

All product and company names mentioned in this document may be the trademarks of their respective holders.



Document History Page

Document Title: CY7C1024AV33 128K x 24 Static RAM				
Document Number: 38-05149				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	109893	09/22/01	SZV	Change from Spec number: 38-00983 to 38-05149
*A	116473	09/16/02	CEA	Add applications foot note to data sheet, page 1.
*B	121472	11/14/02	DSG	Update package diagram 51-85115 (BG119) to rev. *B



中发网 WWW.ZFA.CN

全球最大的PDF中文下载站



中发网
www.zfa.cn

PDF 资料下载尽在中发网