



## CY7C1021CV33

# 1-Mbit (64K x 16) Static RAM

### Features

- **Temperature Ranges**
  - Commercial: 0°C to 70°C
  - Industrial: -40°C to 85°C
  - Automotive: -40°C to 125°C
- **Pin- and function-compatible with CY7C1021BV33**
- **High speed**
  - $t_{AA} = 8 \text{ ns}$  (Commercial & Industrial)
  - $t_{AA} = 12 \text{ ns}$  (Automotive)
- **CMOS for optimum speed/power**
- **Low active power: 360 mW (max.)**
- **Automatic power-down when deselected**
- **Independent control of upper and lower bits**
- **Available in 44-pin TSOP II, 400-mil SOJ, 48-ball FBGA**
- **Also available in Lead-Free 44-pin TSOP II, 400-mil SOJ packages**

### Functional Description<sup>[1]</sup>

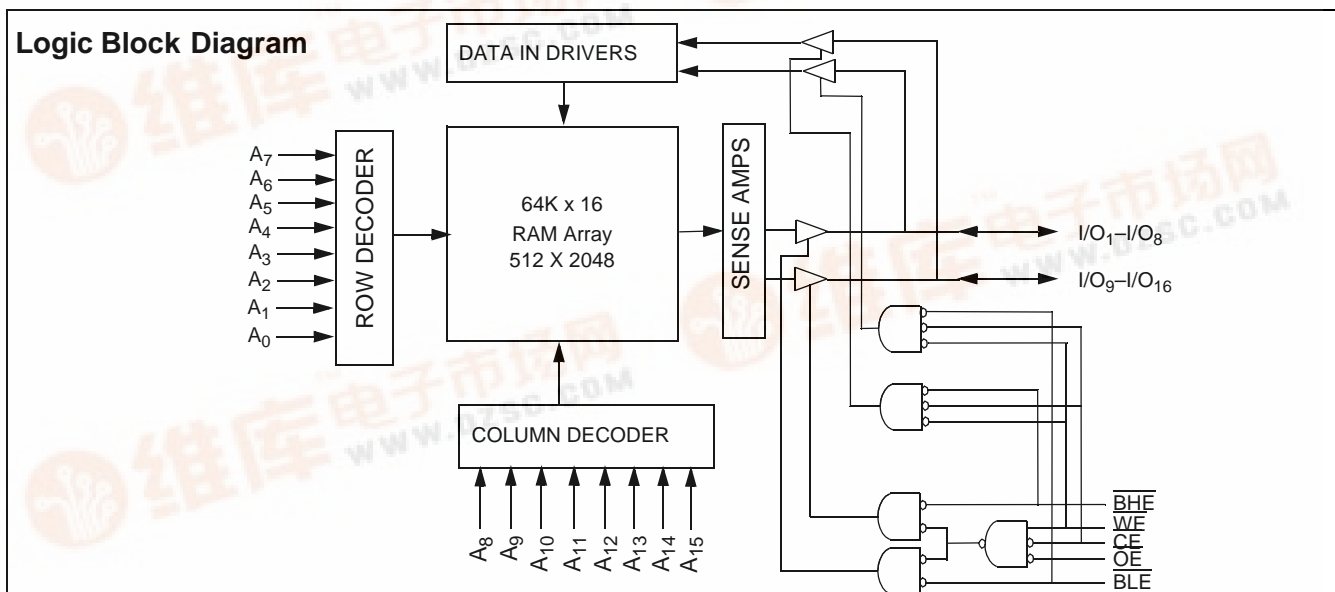
The CY7C1021CV33 is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_1$  through  $I/O_8$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{15}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins ( $I/O_9$  through  $I/O_{16}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{15}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_1$  to  $I/O_8$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on  $I/O_9$  to  $I/O_{16}$ . See the truth table at the end of this data sheet for a complete description of Read and Write modes.

The input/output pins ( $I/O_1$  through  $I/O_{16}$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a Write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CY7C1021CV33 is available in standard 44-pin TSOP Type II, 400-mil-wide SOJ packages, as well as a 48-ball FBGA.



**Note:**

1. For best-practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.





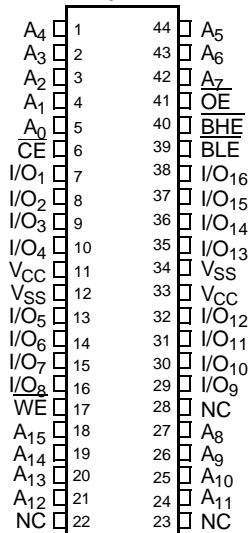
Selection Guide

	CY7C1021CV33-8	CY7C1021CV33-10	CY7C1021CV33-12	CY7C1021CV33-15	Unit
Maximum Access Time	8	10	12	15	ns
Maximum Operating Current	95	90	85	80	mA
	Automotive	-	-	90	-
Maximum CMOS Standby Current	5	5	5	5	mA
	Automotive	-	-	10	-

Pin Configurations

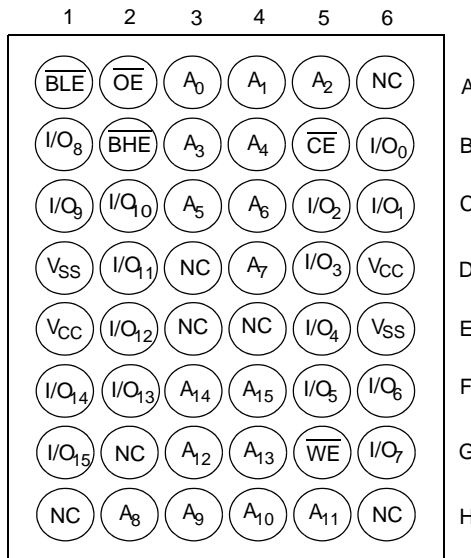
SOJ / TSOP II

Top View



48-ball FBGA

(Top View)



**Pin Definitions**

Pin Name	SOJ, TSOP Pin Number	BGA Pin Number	I/O Type	Description
A <sub>0</sub> -A <sub>15</sub>	1-5, 18-21, 24-27, 42-44	A3, A4, A5, B3, B4, C3, C4, D4, H2, H3, H4, H5, G3, G4, F3, F4	Input	<b>Address Inputs used to select one of the address locations.</b>
I/O <sub>0</sub> -I/O <sub>15</sub> <sup>[2]</sup>	7-10, 13-16, 29-32, 35-38	B6, C6, C5, D5, E5, F5, F6, G6, B1, C1, C2, D2, E2, F2, F1, G1	Input/Output	<b>Bidirectional Data I/O lines.</b> Used as input or output lines depending on operation.
NC	22, 23, 28	A6, D3, E3, E4, G2, H1, H6	No Connect	<b>No Connects.</b> Not connected to the die.
$\overline{\text{WE}}$	17	G5	Input/Control	<b>Write Enable Input, active LOW.</b> When selected LOW, a Write is conducted. When deselected HIGH, a Read is conducted.
$\overline{\text{CE}}$	6	B5	Input/Control	<b>Chip Enable Input, active LOW.</b> When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{\text{BHE}}, \overline{\text{BLE}}$	39, 40	A1, B2	Input/Control	<b>Byte Write Select Inputs, active LOW.</b> $\overline{\text{BLE}}$ controls I/O <sub>8</sub> -I/O <sub>1</sub> , $\overline{\text{BHE}}$ controls I/O <sub>16</sub> -I/O <sub>9</sub> .
$\overline{\text{OE}}$	41	A2	Input/Control	<b>Output Enable, active LOW.</b> Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins.
V <sub>SS</sub>	12,34	D1, E6	Ground	<b>Ground for the device.</b> Should be connected to ground of the system.
V <sub>CC</sub>	11,33	D6, E1	Power Supply	<b>Power Supply inputs to the device.</b>

**Note:**

2. I/O<sub>1</sub>-I/O<sub>16</sub> for SOJ/TSOP and I/O<sub>0</sub>-I/O<sub>15</sub> for BGA packages.



**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature ..... -65°C to +150°C
- Ambient Temperature with Power Applied..... -55°C to +125°C
- Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[3]</sup> .... -0.5V to +4.6V
- DC Voltage Applied to Outputs in High-Z State<sup>[3]</sup>..... -0.5V to V<sub>CC</sub>+0.5V
- DC Input Voltage<sup>[3]</sup>..... -0.5V to V<sub>CC</sub>+0.5V
- Current into Outputs (LOW) ..... 20 mA

- Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)
- Latch-up Current..... >200 mA

**Operating Range**

Range	Ambient Temperature (T <sub>A</sub> )	V <sub>CC</sub>
Commercial	0°C to +70°C	3.3V ± 10%
Industrial	-40°C to +85°C	3.3V ± 10%
Automotive	-40°C to +125°C	3.3V ± 10%

**Electrical Characteristics Over the Operating Range**

Parameter	Description	Test Conditions	1021CV33-8		1021CV33-10		1021CV33-12		1021CV33-15		Unit		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.			
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		2.4		2.4		V		
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4		0.4	V		
V <sub>IH</sub>	Input HIGH Voltage		2.0	V <sub>CC</sub> + 0.3	2.0	V <sub>CC</sub> + 0.3	2.0	V <sub>CC</sub> + 0.3	2.0	V <sub>CC</sub> + 0.3	V		
V <sub>IL</sub>	Input LOW Voltage <sup>[3]</sup>		-0.3	0.8	-0.3	0.8	-0.3	0.8	-0.3	0.8	V		
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	Com'l / Ind'l		-1	+1	-1	+1	-1	+1	-1	+1	μA
			Automotive						-12	+12			μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	Com'l / Ind'l		-1	+1	-1	+1	-1	+1	-1	+1	μA
			Automotive		-	-	-	-	-12	+12	-	-	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[4]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-300		-300		-300		-300	mA		
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	Com'l / Ind'l			95		90		85		80	mA
			Automotive			-		-		90		-	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current — TTL Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>IH</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	Com'l / Ind'l			15		15		15		15	mA
			Automotive			-		-		20		-	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current — CMOS Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0	Com'l / Ind'l			5		5		5		5	mA
			Automotive			-		-		10		-	mA

**Notes:**

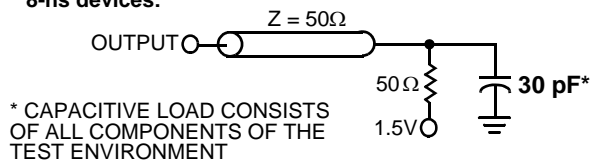
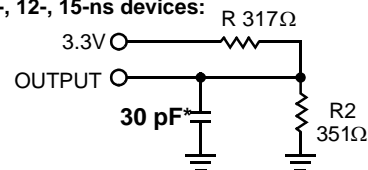
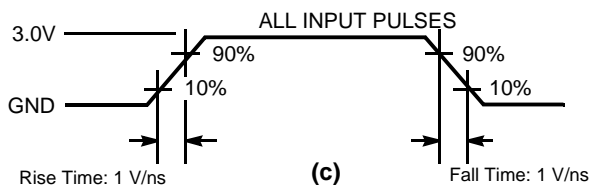
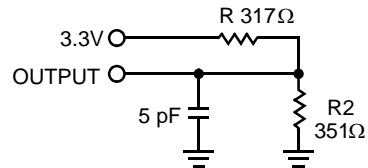
- 3. V<sub>IL</sub> (min.) = -2.0V and V<sub>IH</sub> (max) = V<sub>CC</sub> + 0.5V for pulse durations of less than 20 ns.
- 4. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

**Thermal Resistance<sup>[5]</sup>**

Parameter	Description	Test Conditions	48-ball FBGA	44-lead SOJ	44-lead TSOP-II	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	95.32	65.06	76.92	°C/W
$\Theta_{JC}$	Thermal Resistance (Junction to Case)		10.68	34.21	15.86	°C/W

**Capacitance<sup>[5]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 3.3\text{V}$	8	pF
$C_{OUT}$	Output Capacitance		8	pF

**AC Test Loads and Waveforms<sup>[6]</sup>**
**8-ns devices:**

**(a)**
**10-, 12-, 15-ns devices:**

**(b)**

**(c)**
**High-Z characteristics:**

**(d)**
**Note:**

- Tested initially and after any design or process changes that may affect these parameters.
- AC characteristics (except High-Z) for all 8-ns parts are tested using the load conditions shown in Figure (a). All other speeds are tested using the Thevenin load shown in Figure (b). High-Z characteristics are tested for all speeds using the test load shown in Figure (d).

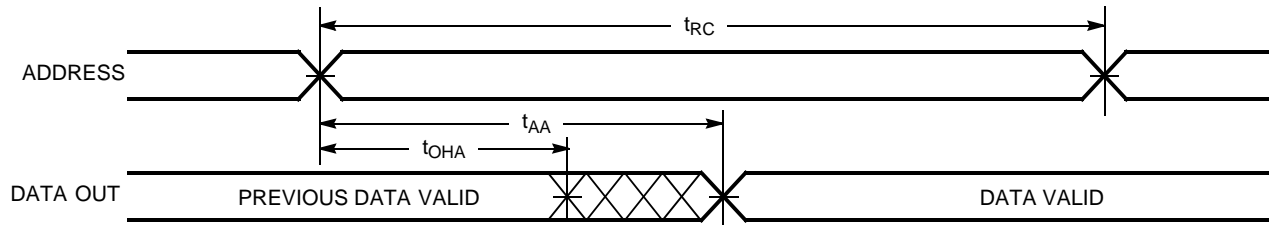
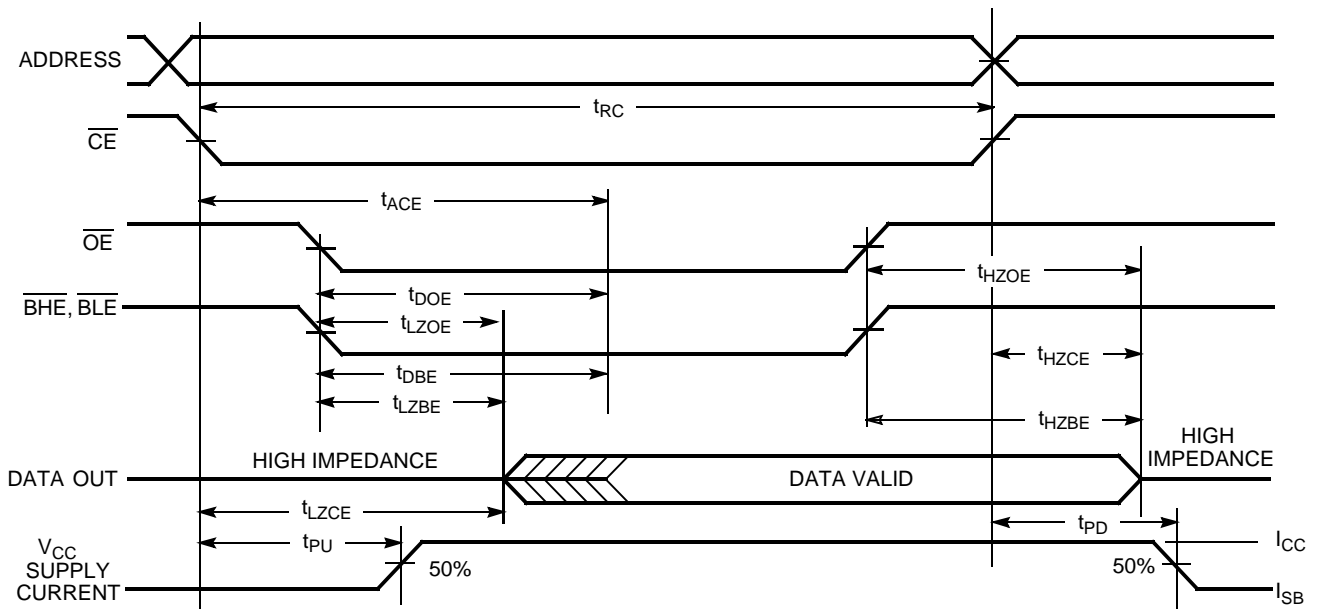


Switching Characteristics Over the Operating Range<sup>[7]</sup>

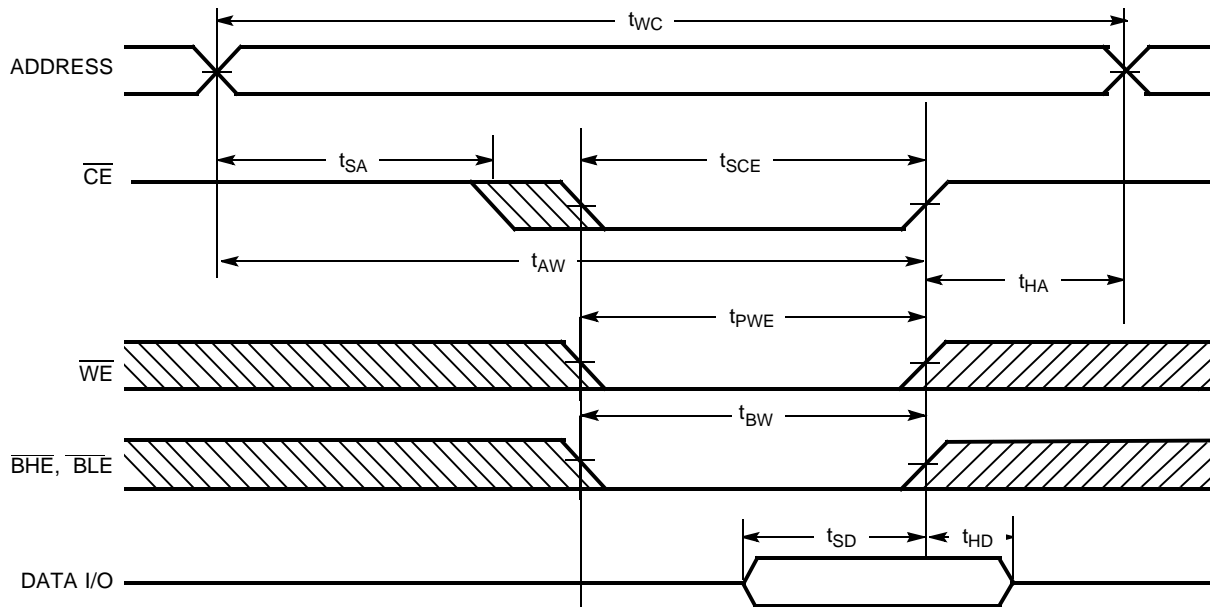
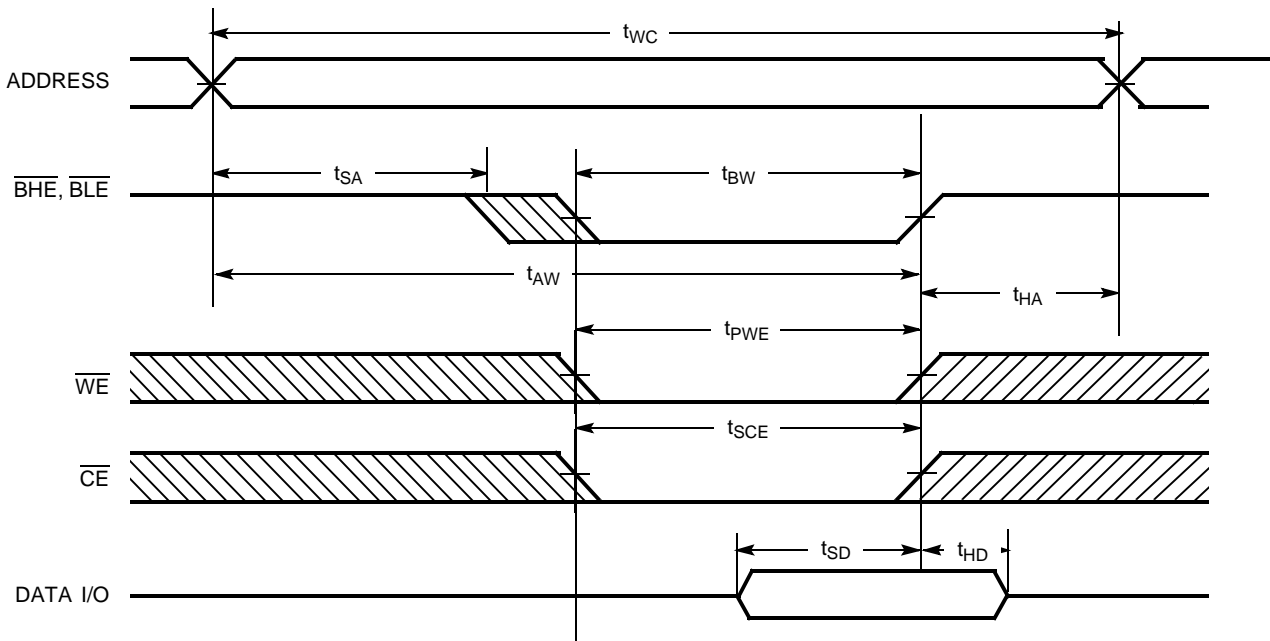
Parameter	Description	1021CV33-8		1021CV33-10		1021CV33-12		1021CV33-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>										
t <sub>RC</sub>	Read Cycle Time	8		10		12		15		ns
t <sub>AA</sub>	Address to Data Valid		8		10		12		15	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		3		3		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		8		10		12		15	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		5		5		6		7	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low-Z <sup>[8]</sup>	0		0		0		0		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High-Z <sup>[8, 9]</sup>		4		5		6		7	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low-Z <sup>[8]</sup>	3		3		3		3		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High-Z <sup>[8, 9]</sup>		4		5		6		7	ns
t <sub>PU</sub> <sup>[10]</sup>	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t <sub>PD</sub> <sup>[10]</sup>	$\overline{CE}$ HIGH to Power-Down		8		10		12		15	ns
t <sub>DBE</sub>	Byte Enable to Data Valid		5		5		6		7	ns
t <sub>LZBE</sub>	Byte Enable to Low-Z	0		0		0		0		ns
t <sub>HZBE</sub>	Byte Disable to High-Z		4		5		6		7	ns
<b>Write Cycle<sup>[11]</sup></b>										
t <sub>WC</sub>	Write Cycle Time	8		10		12		15		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	7		8		9		10		ns
t <sub>AW</sub>	Address Set-up to Write End	7		8		9		10		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		0		ns
t <sub>SA</sub>	Address Set-up to Write Start	0		0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	6		7		8		10		ns
t <sub>SD</sub>	Data Set-up to Write End	5		5		6		8		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		0		ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low-Z <sup>[8]</sup>	3		3		3		3		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High-Z <sup>[8, 9]</sup>		4		5		6		7	ns
t <sub>BW</sub>	Byte Enable to End of Write	6		7		8		9		ns

Notes:

7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
8. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
9. t<sub>HZOE</sub>, t<sub>HZBE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
10. This parameter is guaranteed by design and is not tested.
11. The internal Write time of the memory is defined by the overlap of  $\overline{CE}$  LOW,  $\overline{WE}$  LOW and  $\overline{BHE/BLE}$  LOW.  $\overline{CE}$ ,  $\overline{WE}$  and  $\overline{BHE/BLE}$  must be LOW to initiate a Write, and the transition of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.

**Switching Waveforms**
**Read Cycle No. 1**<sup>[12, 13]</sup>

**Read Cycle No. 2 (OE Controlled)**<sup>[13, 14]</sup>

**Notes:**

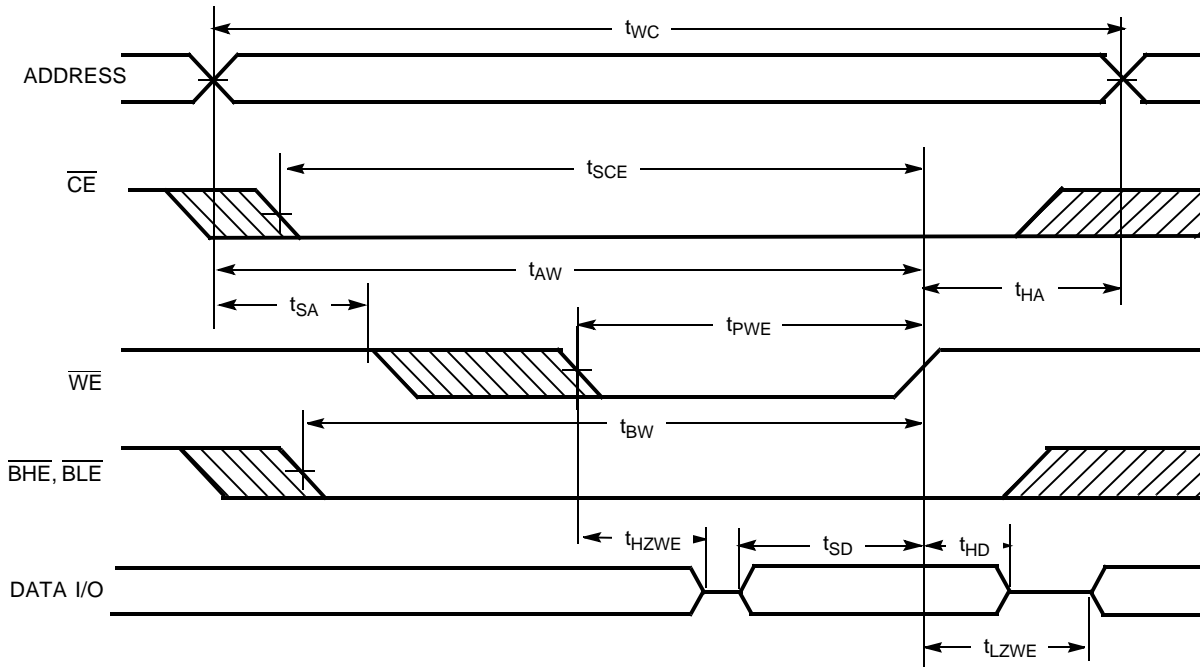
- 12. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and/or  $\overline{BLE}$  =  $V_{IL}$ .
- 13.  $\overline{WE}$  is HIGH for Read cycle.
- 14. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)<sup>[15, 16]</sup>**

**Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)**

**Notes:**

15. Data I/O is high impedance if  $\overline{\text{OE}}$  or  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{\text{IH}}$ .
16. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.



**Switching Waveforms** (continued)

**Write Cycle No. 3 (WE Controlled, LOW)**

**Truth Table**

CE	OE	WE	BLE	BHE	I/O <sub>1</sub> -I/O <sub>8</sub>	I/O <sub>9</sub> -I/O <sub>16</sub>	Mode	Power
H	X	X	X	X	High-Z	High-Z	Power-down	Standby (I <sub>SB</sub> )
L	L	H	L	L	Data Out	Data Out	Read – All bits	Active (I <sub>CC</sub> )
			L	H	Data Out	High-Z	Read – Lower bits only	Active (I <sub>CC</sub> )
			H	L	High-Z	Data Out	Read – Upper bits only	Active (I <sub>CC</sub> )
L	X	L	L	L	Data In	Data In	Write – All bits	Active (I <sub>CC</sub> )
			L	H	Data In	High-Z	Write – Lower bits only	Active (I <sub>CC</sub> )
			H	L	High-Z	Data In	Write – Upper bits only	Active (I <sub>CC</sub> )
L	H	H	X	X	High-Z	High-Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )
L	X	X	H	H	High-Z	High-Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range	
8	CY7C1021CV33-8VC	V34	44-lead (400-Mil) Molded SOJ	Commercial	
	CY7C1021CV33-8ZC	Z44	44-lead TSOP Type II		
	CY7C1021CV33-8BAC	BA48A	48-ball FBGA		
10	CY7C1021CV33-10VC	V34	44-lead (400-Mil) Molded SOJ	Commercial	
	CY7C1021CV33-10VI	V34	44-lead (400-Mil) Molded SOJ	Industrial	
	CY7C1021CV33-10ZC	Z44	44-lead TSOP Type II		Commercial
			44-lead TSOP Type II		Industrial
	CY7C1021CV33-10BAC	BA48A	48-ball FBGA		Commercial
	CY7C1021CV33-10BAI		48-ball FBGA		Industrial



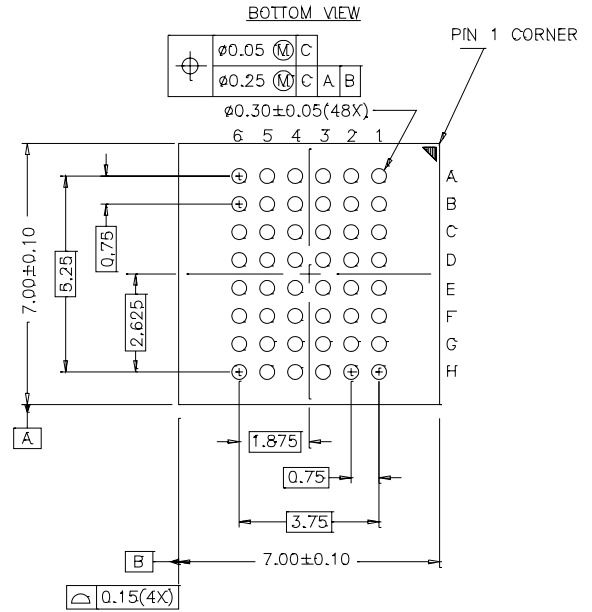
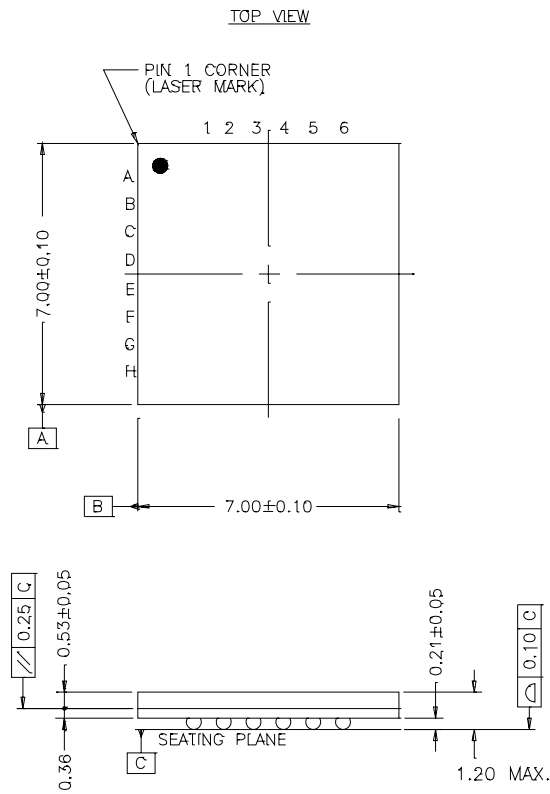
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1021CV33-12VC	V34	44-pin (400-Mil) Molded SOJ	Commercial
	CY7C1021CV33-12VI			Industrial
	CY7C1021CV33-12VE			Automotive
	CY7C1021CV33-12ZC	Z44	44-pin TSOP Type II	Commercial
	CY7C1021CV33-12ZI			Industrial
	CY7C1021CV33-12ZSE			Automotive
	CY7C1021CV33-12BAC	BA48A	48-ball FBGA	Commercial
	CY7C1021CV33-12BAI			Industrial
	CY7C1021CV33-12BAE			Automotive
15	CY7C1021CV33-15VC	V34	44-pin (400-Mil) Molded SOJ	Commercial
	CY7C1021CV33-15VI			Industrial
	CY7C1021CV33-15ZC	Z44	44-pin TSOP Type II	Commercial
	CY7C1021CV33-15ZI			Industrial
	CY7C1021CV33-15BAC	BA48A	48-ball FBGA	Commercial
	CY7C1021CV33-15BAI			Industrial
8	CY7C1021CV33-8VXC	V34	44-lead (400-Mil) Molded SOJ (Pb-Free)	Commercial
	CY7C1021CV33-8ZXC	Z44	44-lead TSOP Type II (Pb-Free)	Commercial
	CY7C1021CV33-8BAXC	BA48A	48-ball FBGA (Pb-Free)	Commercial
10	CY7C1021CV33-10VXC	V34	44-lead (400-Mil) Molded SOJ (Pb-Free)	Commercial
	CY7C1021CV33-10VXI	V34	44-lead (400-Mil) Molded SOJ (Pb-Free)	Industrial
	CY7C1021CV33-10ZXC	Z44	44-lead TSOP Type II (Pb-Free)	Commercial
	CY7C1021CV33-10ZXI	Z44	44-lead TSOP Type II (Pb-Free)	Industrial
	CY7C1021CV33-10BAXC	BA48A	48-ball FBGA (Pb-Free)	Commercial
	CY7C1021CV33-10BAXI			Industrial
12	CY7C1021CV33-12VXC	V34	44-pin (400-Mil) Molded SOJ (Pb-Free)	Commercial
	CY7C1021CV33-12VXI	V34	44-pin (400-Mil) Molded SOJ (Pb-Free)	Industrial
	CY7C1021CV33-12VXE	V34	44-pin (400-Mil) Molded SOJ (Pb-Free)	Automotive
	CY7C1021CV33-12ZXC	Z44	44-lead TSOP Type II (Pb-Free)	Commercial
	CY7C1021CV33-12ZXI	Z44	44-lead TSOP Type II (Pb-Free)	Industrial
	CY7C1021CV33-12ZSXE	Z44	44-pin TSOP Type II (Pb-Free)	Automotive
	CY7C1021CV33-12BAXC	BA48A	48-ball FBGA (Pb-Free)	Commercial
	CY7C1021CV33-12BAXI	BA48A	48-ball FBGA (Pb-Free)	Industrial
	CY7C1021CV33-12BAXE	BA48A	48-ball FBGA (Pb-Free)	Automotive
15	CY7C1021CV33-15VXC	V34	44-pin (400-Mil) Molded SOJ (Pb-Free)	Commercial
	CY7C1021CV33-15VXI	V34	44-pin (400-Mil) Molded SOJ (Pb-Free)	Industrial
	CY7C1021CV33-15ZXC	Z44	44-lead TSOP Type II (Pb-Free)	Commercial
	CY7C1021CV33-15ZXI	Z44	44-lead TSOP Type II (Pb-Free)	Industrial
	CY7C1021CV33-15BAXC	BA48A	48-ball FBGA (Pb-Free)	Commercial
	CY7C1021CV33-15BAXI			Industrial

Shaded areas contain advance information. Please contact your local Cypress sales representative for availability of these parts.

Package Diagrams

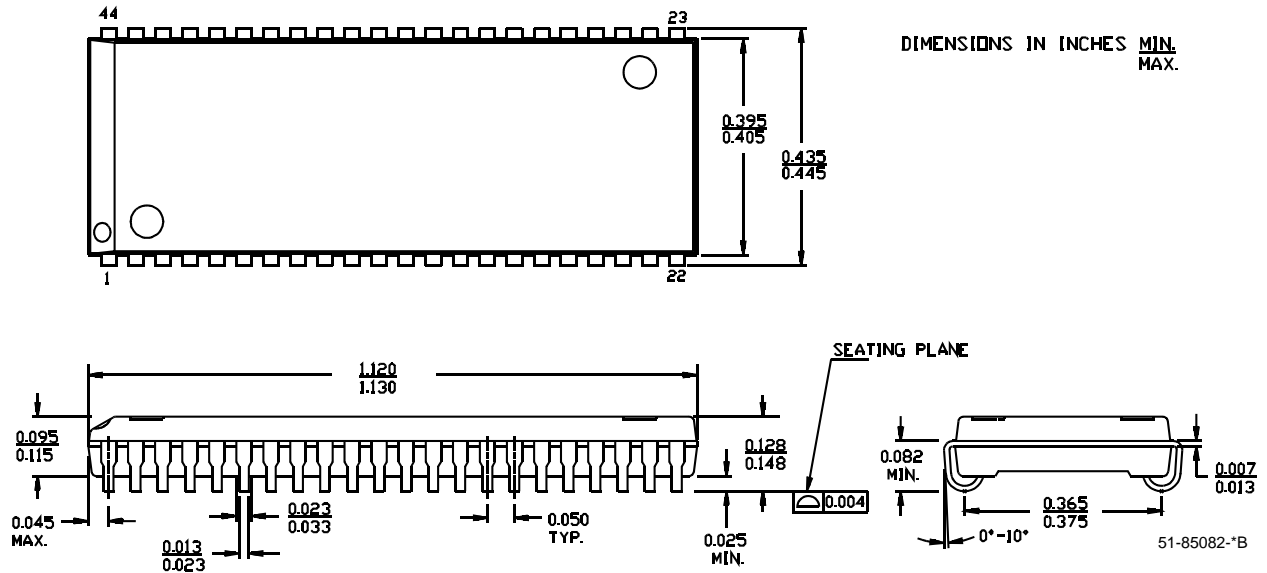
48-Ball (7.00 mm x 7.00 mm x 1.2 mm) FBGA BA48A



51-85096-\*E

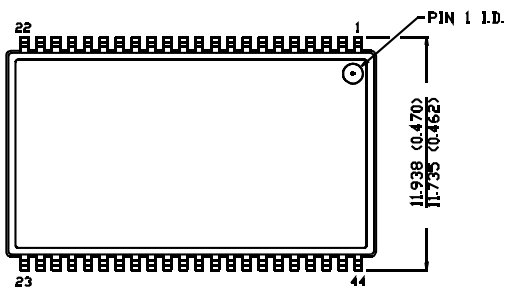
Package Diagrams (continued)

44-Lead (400-Mil) Molded SOJ V34

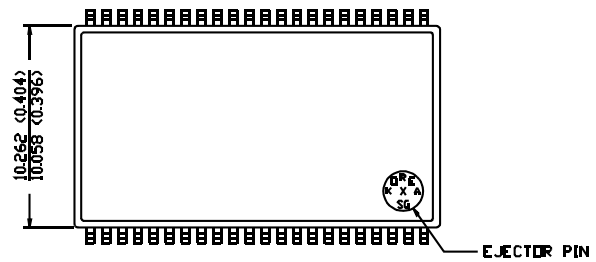


44-pin TSOP II Z44

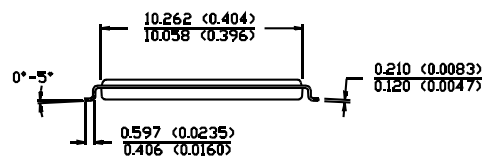
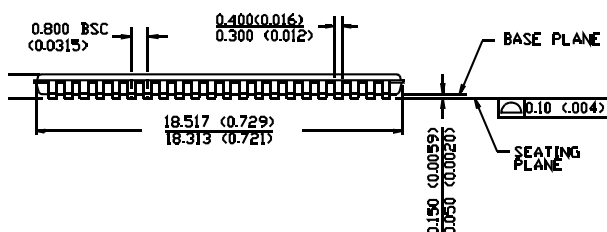
DIMENSION IN MM (INCH)  
MAX  
MIN.



TOP VIEW



BOTTOM VIEW



51-85087-A

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Document History Page

<b>Document Title: CY7C1021CV33 1-Mbit (64K x 16) Static RAM</b>				
<b>Document Number: 38-05132</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	109472	12/06/01	HGK	New Data Sheet
*A	115044	05/08/02	HGK	Ram7 version C4K x 16 Async. Remove "Preliminary"
*B	115808	06/25/02	HGK	I <sub>SB1</sub> and I <sub>CC</sub> values changed
*C	120413	10/31/02	DFP	Updated BGA pin E4 to NC.
*D	238454	See ECN	RKF	1) Added Automotive Specs to Datasheet 2) Added Pb-Free devices in the Ordering information
*E	334398	See ECN	SYT	Added Pb-Free on page# 9 and 10



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