25AA040A/25LC040A

4K SPI™ Bus Serial EEPROM

Device Selection Table

Part Number	Vcc Range	Page Size	Temp. Ranges	Packages
25AA040A	1.8-5.5V	16 Bytes	I	P, MS, SN, ST
25LC040A	2.5-5.5V	16 Bytes	I, E	P, MS, SN, ST

Features

- Max. clock 10 MHz
- Low-power CMOS technology
  - Max Write Current: 5 mA at 5.5V, 10MHz
  - Read Current: 5 mA at 5.5V, 10MHz
  - Standby Current 5 µA at 5.5V
- 512 x 8-bit organization
- Write Page mode (up to 16 bytes)
- Sequential Read
- Self-timed ERASE and WRITE cycles (5 ms max.)
- Block write protection
  - Protect none, 1/4, 1/2 or all of array
- Built-in write protection
  - Power-on/off data protection circuitry
  - Write enable latch
  - Write-protect pin
- High reliability
  - Endurance: 1,000,000 erase/write cycles
  - Data retention: > 200 years
  - ESD protection: > 4000V
- Temperature ranges supported;
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C
- Standard and Pb-free packages available

Pin Function Table

Name	Function
$\overline{CS}$	Chip Select Input
SO	Serial Data Output
$\overline{WP}$	Write-Protect
VSS	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{HOLD}$	Hold Input
VCC	Supply Voltage

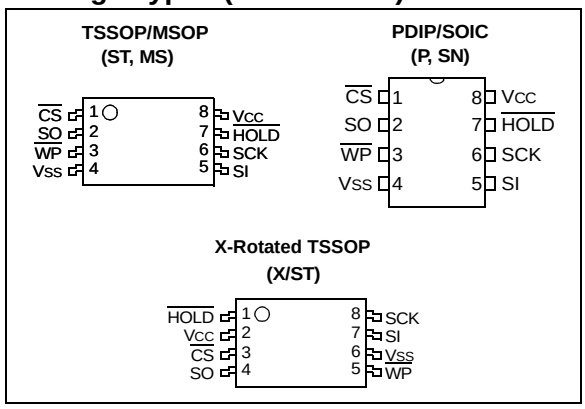
Description

The Microchip Technology Inc. 25XX040A* is a 4k-bit Serial Electrically Erasable Programmable Read-Only Memory (EEPROM). The memory is accessed via a simple Serial Peripheral Interface™ (SPI™) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a Chip Select ($\overline{CS}$) input.

Communication to the device can be paused via the hold pin ($\overline{HOLD}$). While the device is paused, transitions on its inputs will be ignored, with the exception of Chip Select, allowing the host to service higher priority interrupts.

The 25XX040A is available in standard packages including 8-lead PDIP and SOIC, and advanced packages including 8-lead MSOP, 8-lead TSSOP and rotated TSSOP. Pb-free (Pure Matte Sn) finish is also available.

Package Types (not to scale)



SPI is a registered trademark of Motorola Corporation.

*25XX040A is used in this document as a generic part number for the 25AA040A and the 25LC040A.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V

Storage temperature .....-65°C to 150°C

Ambient temperature under bias.....-40°C to 125°C

ESD protection on all pins.....4 kV

† NOTICE**:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Industrial (I): TA = -40°C to +85°C VCC = 1.8V to 5.5V Automotive (E): TA = -40°C to +125°C VCC = 2.5V to 5.5V			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
D001	VIH1	High-level input voltage	0.7 VCC	VCC+1	V	
D002	VIL1	Low-level input voltage	-0.3	0.3 VCC	V	VCC ≥ 2.7V **(Note 1)**
D003	VIL2		-0.3	0.2 VCC	V	VCC < 2.7V **(Note 1)**
D004	VOL	Low-level output voltage	—	0.4	V	IOL = 2.1 mA
D005	VOL		—	0.2	V	IOL = 1.0 mA, VCC < 2.5V
D006	VOH	High-level output voltage	VCC -0.5	—	V	IOH = -400 µA
D007	ILI	Input leakage current	—	±1	µA	$\overline{CS}$ = VCC, VIN = VSS TO VCC
D008	ILO	Output leakage current	—	±1	µA	$\overline{CS}$ = VCC, VOUT = VSS TO VCC
D009	CINT	Internal Capacitance (all inputs and outputs)	—	7	pF	TA = 25°C, CLK = 1.0 MHz, VCC = 5.0V **(Note 1)**
D010	ICC Read	Operating Current	—	5	mA	VCC = 5.5V; FCLK = 10.0 MHz; SO = Open
			—	2.5	mA	VCC = 2.5V; FCLK = 5.0 MHz; SO = Open
D011	ICC Write		—	5	mA	VCC = 5.5V
			—	3	mA	VCC = 2.5V
D012	ICCS	Standby Current	—	5	µA	$\overline{CS}$ = VCC = 5.5V, Inputs tied to VCC or VSS, TA = +125°C
			—	1	µA	$\overline{CS}$ = VCC = 2.5V, Inputs tied to VCC or VSS, TA = +85°C

Note 1: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Industrial (I): TA = -40°C to +85°C VCC = 1.8V to 5.5V Automotive (E): TA = -40°C to +125°C VCC = 2.5V to 5.5V			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
1	FCLK	Clock Frequency	— — —	10 5 3	MHz MHz MHz	4.5V ≤ Vcc < 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
2	TCSS	$\overline{CS}$ Setup Time	50 100 150	— — —	ns ns ns	4.5V ≤ Vcc < 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
3	TCSH	$\overline{CS}$ Hold Time	100 200 250	— — —	ns ns ns	4.5V ≤ Vcc < 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
4	TCSD	$\overline{CS}$ Disable Time	50	—	ns	—
5	TSU	Data Setup Time	10 20 30	— — —	ns ns ns	4.5V ≤ Vcc < 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
6	THD	Data Hold Time	20 40 50	— — —	ns ns ns	4.5V ≤ Vcc < 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
7	TR	CLK Rise Time	—	2	µs	**(Note 1)**
8	TF	CLK Fall Time	—	2	µs	**(Note 1)**
9	THI	Clock High Time	50 100 150	— — —	ns ns ns	4.5V ≤ Vcc < 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
10	TLO	Clock Low Time	50 100 150	— — —	ns ns ns	4.5V ≤ Vcc < 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
11	TCLD	Clock Delay Time	50	—	ns	—
12	TCLE	Clock Enable Time	50	—	ns	—
13	TV	Output Valid from Clock Low	— — —	50 100 160	ns ns ns	4.5V ≤ Vcc < 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
14	THO	Output Hold Time	0	—	ns	**(Note 1)**
15	TDIS	Output Disable Time	— — —	40 80 160	ns ns ns	4.5V ≤ Vcc < 5.5V **(Note 1)** 2.5V ≤ Vcc < 4.5V **(Note 1)** 1.8V ≤ Vcc < 2.5V **(Note 1)**
16	THS	$\overline{HOLD}$ Setup Time	20 40 80	— — —	ns ns ns	4.5V ≤ Vcc < 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from our web site: www.microchip.com.

3: TWC begins on the rising edge of $\overline{CS}$ after a valid write sequence and ends when the internal write cycle is complete.

TABLE 1-2: AC CHARACTERISTICS (CONTINUED)

AC CHARACTERISTICS			Industrial (I): TA = -40°C to +85°C VCC = 1.8V to 5.5V Automotive (E): TA = -40°C to +125°C VCC = 2.5V to 5.5V			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
17	THH	$\overline{HOLD}$ Hold Time	20 40 80	— — —	ns ns ns	4.5V ≤ Vcc < 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
18	THZ	$\overline{HOLD}$ Low to Output High-Z	30 60 160	— — —	ns ns ns	4.5V ≤ Vcc < 5.5V **(Note 1)** 2.5V ≤ Vcc < 4.5V **(Note 1)** 1.8V ≤ Vcc < 2.5V **(Note 1)**
19	THV	$\overline{HOLD}$ High to Output Valid	30 60 160	— — —	ns ns ns	4.5V ≤ Vcc < 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
20	TWC	Internal Write Cycle Time	—	5	ms	**(NOTE 3)**
21	—	Endurance	1M	—	E/W Cycles	**(NOTE 2)**

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from our web site: www.microchip.com.

3: TWC begins on the rising edge of $\overline{CS}$ after a valid write sequence and ends when the internal write cycle is complete.

TABLE 1-3: AC TEST CONDITIONS

AC Waveform:	
VLO = 0.2V	—
VHI = VCC - 0.2V	**(Note 1)**
VHI = 4.0V	**(Note 2)**
CL = 100pF	—
Timing Measurement Reference Level	
Input	0.5 VCC
Output	0.5 VCC

Note 1: For VCC ≤ 4.0V

2: For VCC ≥ 4.0V

FIGURE 1-1: HOLD TIMING

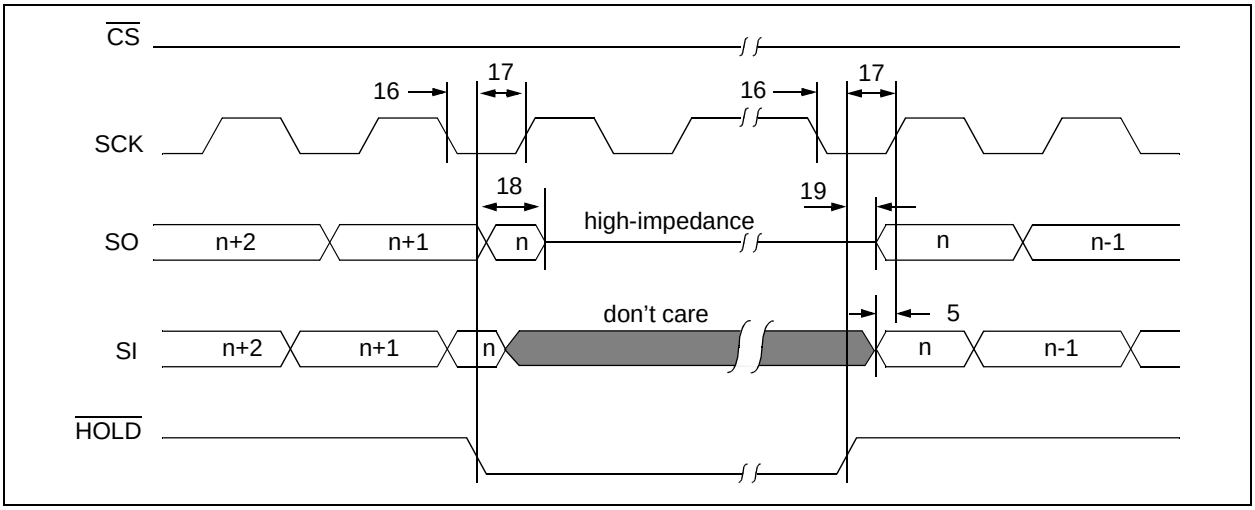


FIGURE 1-2: SERIAL INPUT TIMING

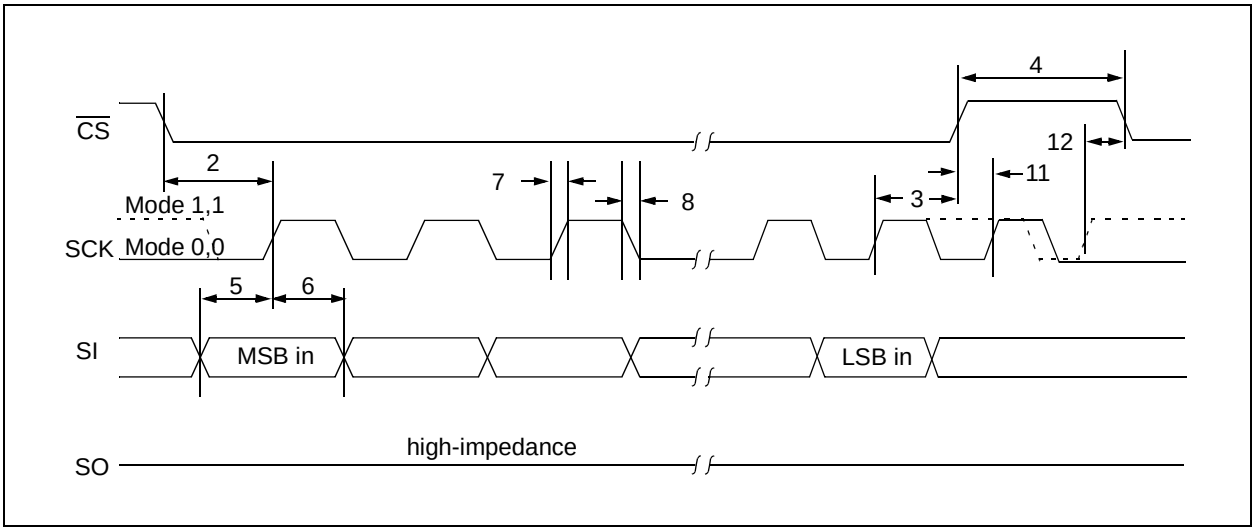
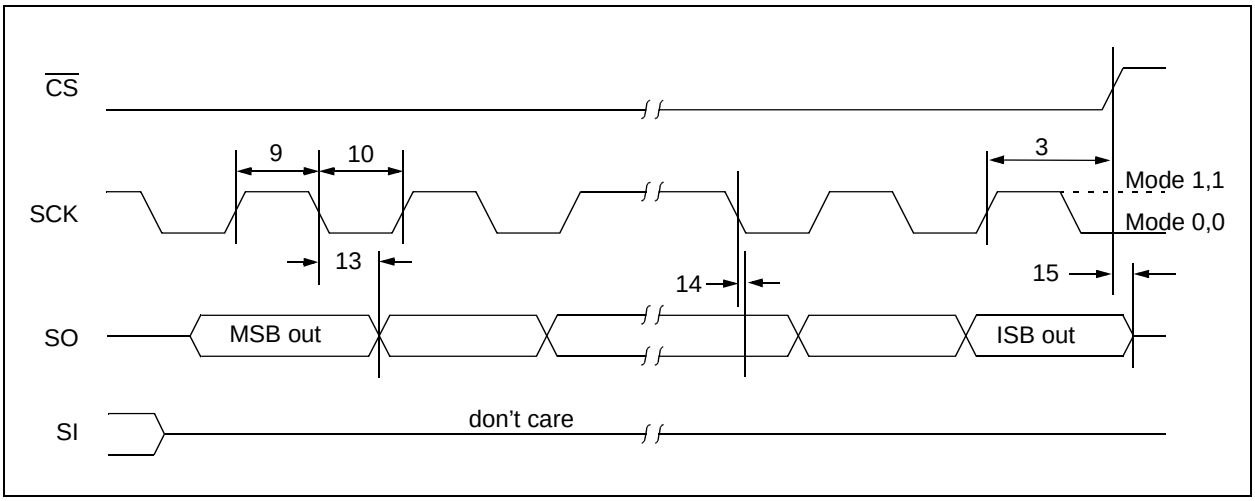


FIGURE 1-3: SERIAL OUTPUT TIMING



2.0 FUNCTIONAL DESCRIPTION

2.1 Principles of Operation

The 25XX040A is a 512-byte Serial EEPROM designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PICmicro® microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly in firmware to match the SPI protocol.

The 25XX040A contains an 8-bit instruction register. The device is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The $\overline{CS}$ pin must be low and the $\overline{HOLD}$ pin must be high for the entire operation.

Table 2-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses and data are transferred MSb first, LSb last.

Data (SI) is sampled on the first rising edge of SCK after $\overline{CS}$ goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input and place the 25XX040A in 'HOLD' mode. After releasing the $\overline{HOLD}$ pin, operation will resume from the point when the $\overline{HOLD}$ was asserted.

2.2 Read Sequence

The device is selected by pulling $\overline{CS}$ low. The 8-bit read instruction is transmitted to the 25XX040A followed by a 9-bit address. The MSb (A8) is sent to the slave during the instruction sequence. See Figure 2-1 for more details.

After the correct read instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. Data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses to the slave. The internal address pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (1FFh), the address counter rolls over to address 000h allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the $\overline{CS}$ pin (Figure 2-1).

2.3 Write Sequence

Prior to any attempt to write data to the 25XX040A, the write enable latch must be set by issuing the WREN instruction (Figure 2-4). This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the 25XX040A. After all eight bits of the instruction are transmitted, $\overline{CS}$ must be driven high to set the write enable latch.

If the write operation is initiated immediately after the WREN instruction without $\overline{CS}$ driven high, data will not be written to the array since the write enable latch was not properly set.

After setting the write enable latch, the user may proceed by driving $\overline{CS}$ low, issuing a write instruction, followed by the remainder of the address, and then the data to be written. Keep in mind that the Most Significant address bit (A8) is included in the instruction byte for the 25XX040A. Up to 16 bytes of data can be sent to the device before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page. Additionally, a page address begins with XXXX 0000 and ends with XXXX 1111. If the internal address counter reaches XXXX 1111 and clock signals continue to be applied to the chip, the address counter will roll back to the first address of the page and over-write any data that previously existed in those locations.

Note:	Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and, end at addresses that are integer multiples of page size - 1. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

For the data to be actually written to the array, the $\overline{CS}$ must be brought high after the Least Significant bit (D0) of the n^{th} data byte has been clocked in. If $\overline{CS}$ is driven high at any other time, the write operation will not be completed. Refer to Figure 2-2 and Figure 2-3 for more detailed illustrations on the byte write sequence and the page write sequence respectively. While the write is in progress, the Status Register may be read to check the status of the WPEN, WIP, WEL, BP1 and BP0 bits (Figure 2-6). Attempting to read a memory array location will not be possible during a write cycle. Polling the WIP bit in the Status Register is recommended in order to determine if a write cycle is in progress. When the write cycle is completed, the write enable latch is reset.

BLOCK DIAGRAM

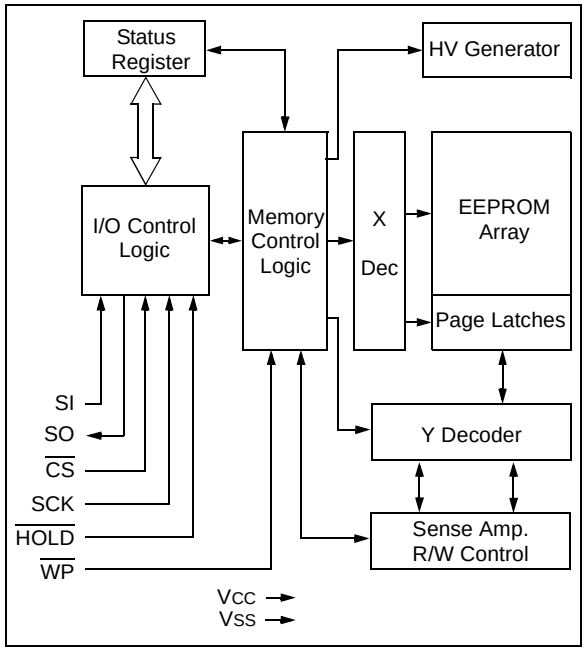


TABLE 2-1: INSTRUCTION SET

Instruction Name	Instruction Format	Description
READ	0000 $A_8$011	Read data from memory array beginning at selected address
WRITE	0000 $A_8$010	Write data to memory array beginning at selected address
WRDI	0000 x100	Reset the write enable latch (disable write operations)
WREN	0000 x110	Set the write enable latch (enable write operations)
RDSR	0000 x101	Read Status Register
WRSR	0000 x001	Write Status Register

Note: A_8 is the 9th address bit, which is used to address the entire 512 byte array.

x = Don't care.

FIGURE 2-1: READ SEQUENCE

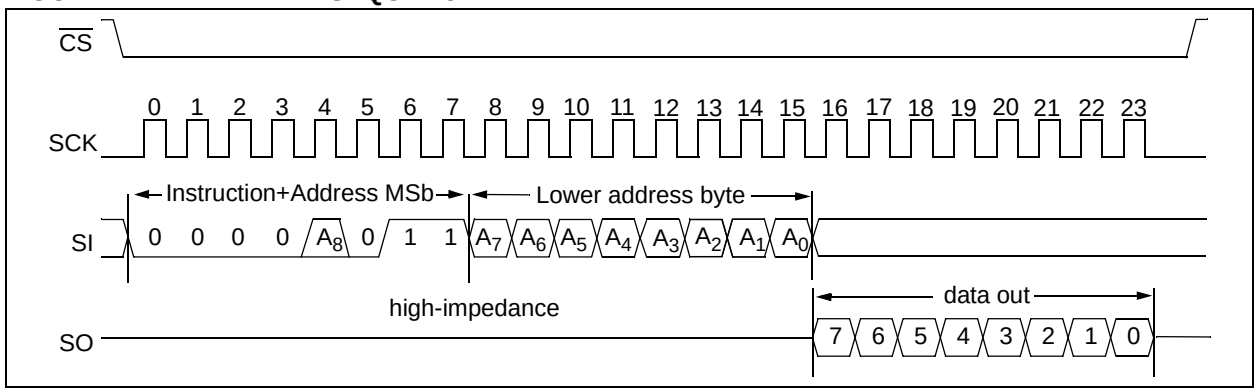


FIGURE 2-2: BYTE WRITE SEQUENCE

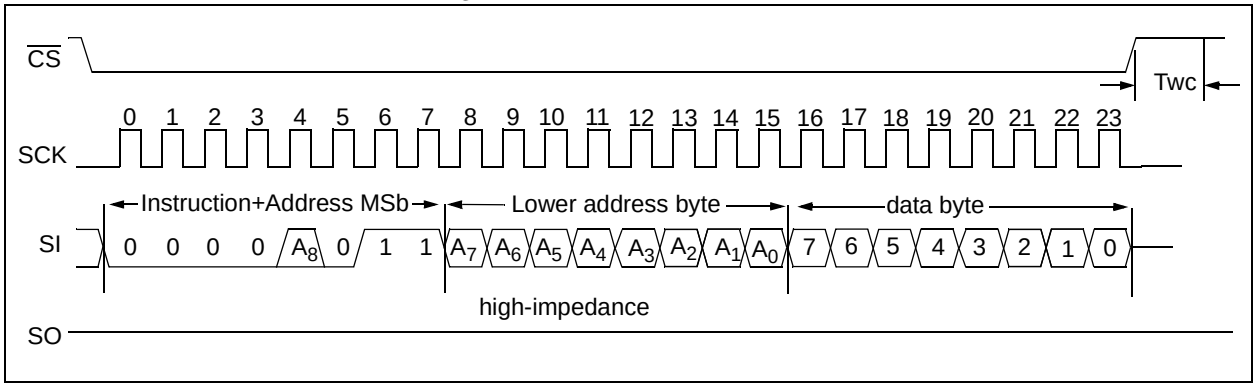
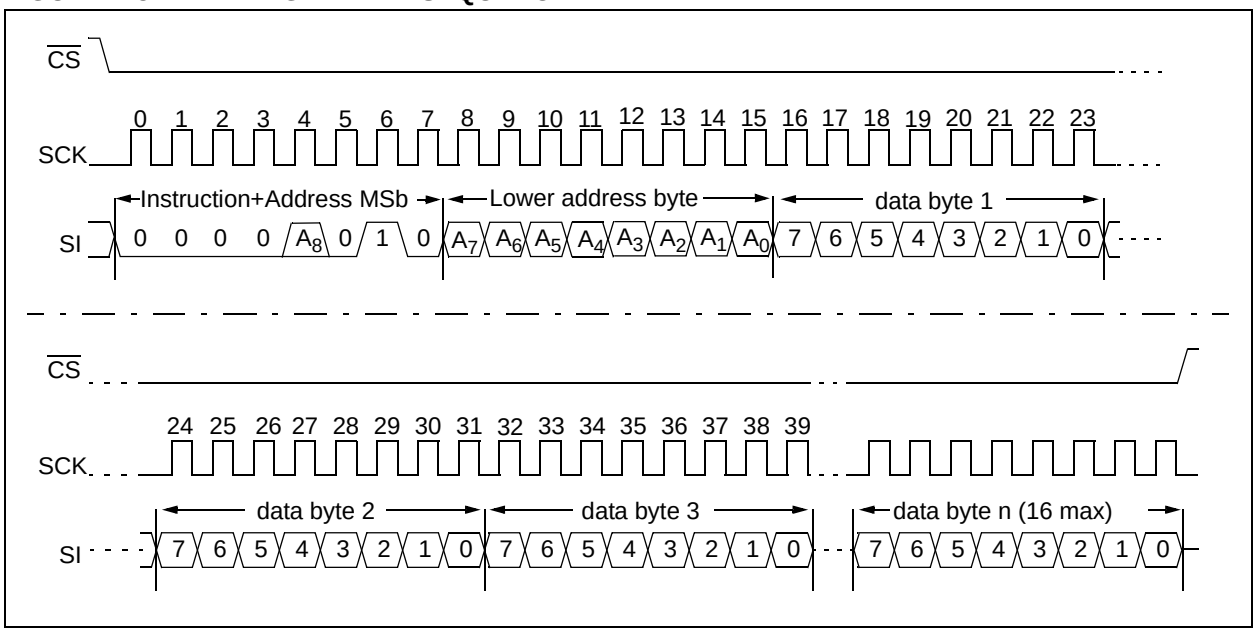


FIGURE 2-3: PAGE WRITE SEQUENCE



2.4 Write Enable (WREN) and Write Disable (WRDI)

The 25XX040A contains a write enable latch. See Table 2-4 for the Write-Protect Functionality Matrix. This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch, and the WRDI will reset the latch.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed

FIGURE 2-4: WRITE ENABLE SEQUENCE (WREN)

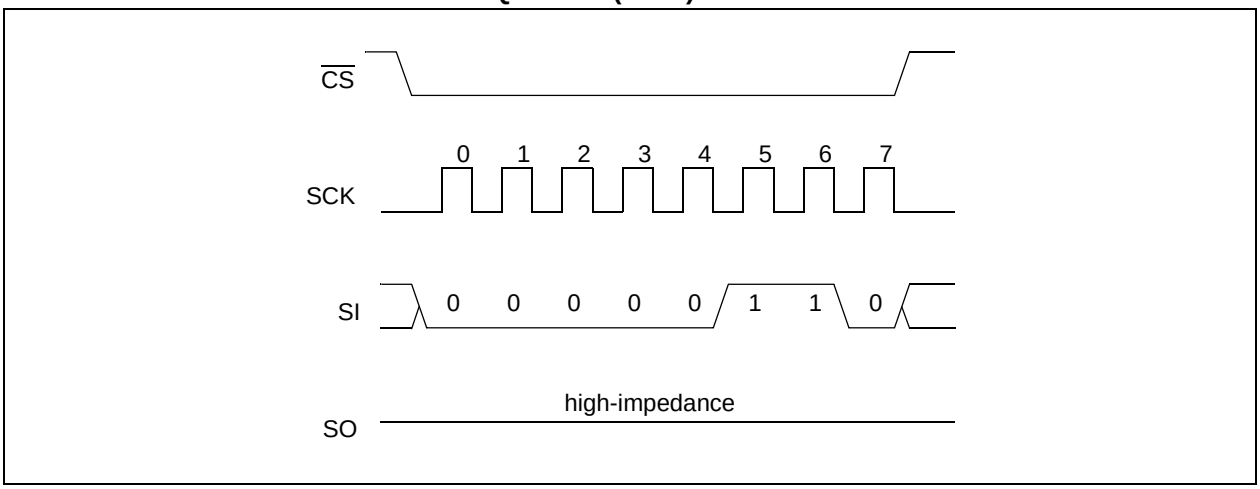
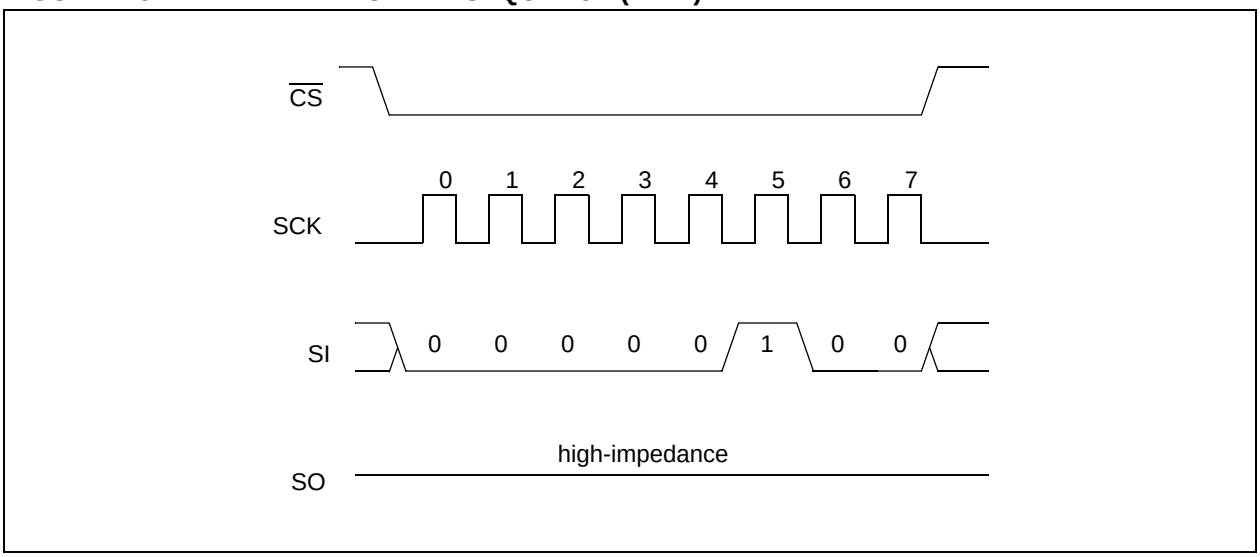


FIGURE 2-5: WRITE DISABLE SEQUENCE (WRDI)



2.5 Read Status Register Instruction (RDSR)

The Read Status Register instruction (RDSR) provides access to the Status Register. See Figure 2-6 for the RDSR timing sequence. The Status Register may be read at any time, even during a write cycle. The Status Register is formatted as follows:

TABLE 2-2: STATUS REGISTER

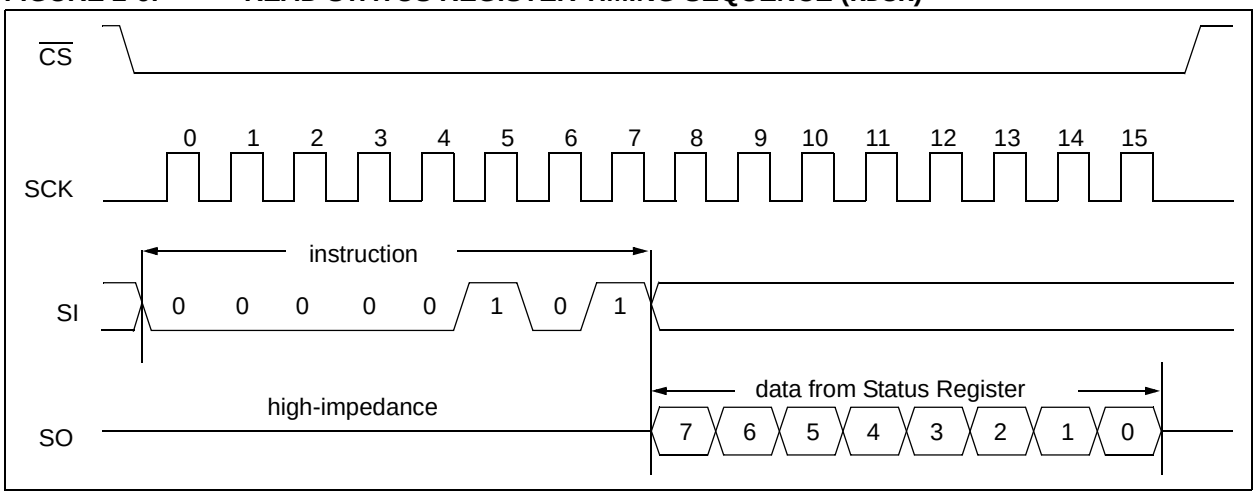
7	6	5	4	3	2	1	0
–	–	–	–	W/R	W/R	R	R
X	X	X	X	BP1	BP0	WEL	WIP
W/R = writable/readable. R = read-only.							

The **Write-In-Process (WIP)** bit indicates whether the 25XX040A is busy with a write operation. When set to a '1', a write is in progress, when set to a '0', no write is in progress. This bit is read-only.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch and is read-only. When set to a '1', the latch allows writes to the array, when set to a '0', the latch prohibits writes to the array. The state of this bit can always be updated via the WREN or WRDI commands regardless of the state of write protection on the Status Register. These commands are shown in Figure 2-4 and Figure 2-5.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write-protected. These bits are set by the user issuing the WRSR instruction, which is shown in Figure 2-7. These bits are nonvolatile and are described in more detail in Table 2-3.

FIGURE 2-6: READ STATUS REGISTER TIMING SEQUENCE (RDSR)



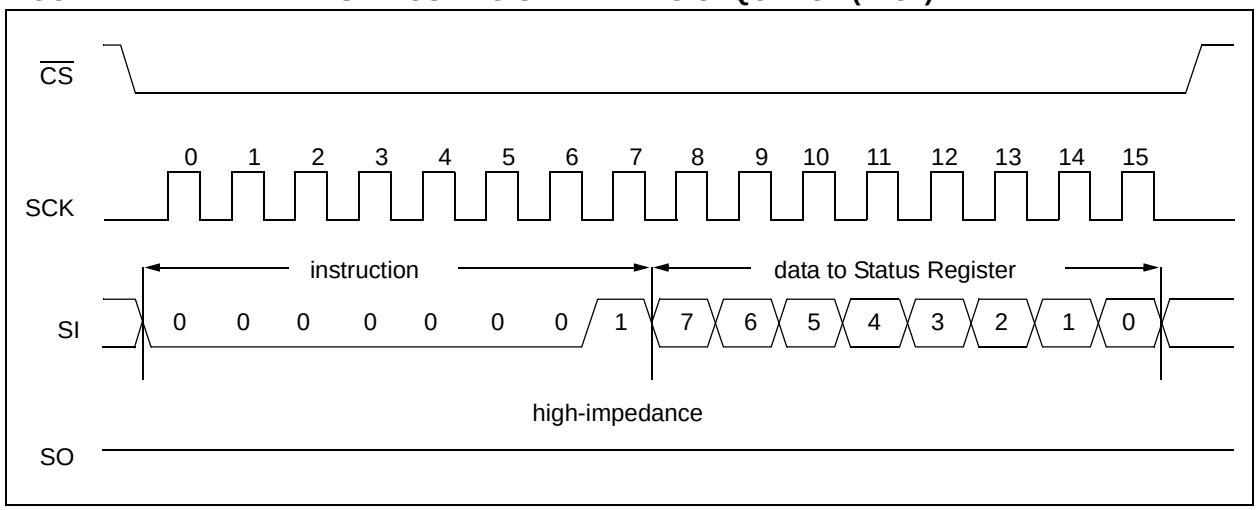
2.6 Write Status Register Instruction (WRSR)

The Write Status Register instruction (WRSR) allows the user to write to the nonvolatile bits in the Status Register as shown in Table 2-2. See Figure 2-7 for the WRSR timing sequence. Four levels of protection for the array are selectable by writing to the appropriate bits in the Status Register. The user has the ability to write-protect none, one, two or all four of the segments of the array as shown in Table 2-3.

TABLE 2-3: ARRAY PROTECTION

BP1	BP0	Array Addresses Write-Protected
0	0	none
0	1	upper 1/4 (180h - 1FFh)
1	0	upper 1/2 (100h - 1FFh)
1	1	all (000h - 1FFh)

FIGURE 2-7: WRITE STATUS REGISTER TIMING SEQUENCE (WRSR)



Note: An internal write cycle (TWC) is initiated on the rising edge of $\overline{CS}$ after a valid write Status Register sequence.

2.7 Data Protection

The following protection has been implemented to prevent inadvertent writes to the array:

- The write enable latch is reset on power-up
- A write enable instruction must be issued to set the write enable latch
- After a byte write, page write or Status Register write, the write enable latch is reset
- $\overline{CS}$ must be set high after the proper number of clock cycles to start an internal write cycle
- Access to the array during an internal write cycle is ignored and programming is continued

2.8 Power-On State

The 25XX040A powers on in the following state:

- The device is in low-power Standby mode ($\overline{CS}$ = 1)
- The write enable latch is reset
- SO is in high-impedance state
- A high-to-low-level transition on $\overline{CS}$ is required to enter active state

TABLE 2-4: WRITE-PROTECT FUNCTIONALITY MATRIX

$\overline{WP}$ (pin 3)	WEL (SR bit 1)	Protected Blocks	Unprotected Blocks	Status Register
0 (low)	x	Protected	Protected	Protected
1 (high)	0	Protected	Protected	Protected
1 (high)	1	Protected	Writable	Writable

x = don't care

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Name	Pin Number	Rotated TSSOP	Function
$\overline{CS}$	1	3	Chip Select Input
SO	2	4	Serial Data Output
$\overline{WP}$	3	5	Write-Protect Pin
VSS	4	6	Ground
SI	5	7	Serial Data Input
SCK	6	8	Serial Clock Input
$\overline{HOLD}$	7	1	Hold Input
VCC	8	2	Supply Voltage

3.1 Chip Select ($\overline{CS}$)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{CS}$ input signal. If $\overline{CS}$ is brought high during a program cycle, the device will go into Standby mode as soon as the programming cycle is complete. When the device is deselected, SO goes to the high-impedance state, allowing multiple parts to share the same SPI bus. A low-to-high transition on $\overline{CS}$ after a valid write sequence initiates an internal write cycle. After power-up, a low level on $\overline{CS}$ is required prior to any sequence being initiated.

3.2 Serial Output (SO)

The SO pin is used to transfer data out of the 25XX040A. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

3.3 Write-Protect ($\overline{WP}$)

The $\overline{WP}$ pin is a hardware write-protect input pin. When it is low, all writes to the array or Status Registers are disabled, but any other operations function normally. When $\overline{WP}$ is high, all functions, including nonvolatile writes, operate normally. At any time, when $\overline{WP}$ is low, the write enable reset latch will be reset and programming will be inhibited. However, if a write cycle is already in progress, $\overline{WP}$ going low will not change or disable the write cycle. See Table 2-4 for the Write-Protect Functionality Matrix.

3.4 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the serial clock.

3.5 Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the 25XX040A. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

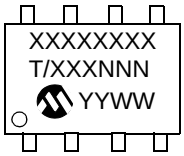
3.6 Hold ($\overline{HOLD}$)

The $\overline{HOLD}$ pin is used to suspend transmission to the 25XX040A while in the middle of a serial sequence without having to retransmit the entire sequence again. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the $\overline{HOLD}$ pin may be pulled low to pause further serial communication without resetting the serial sequence. The $\overline{HOLD}$ pin must be brought low while SCK is low, otherwise the HOLD function will not be invoked until the next SCK high-to-low transition. The 25XX040A must remain selected during this sequence. The SI, SCK and SO pins are in a high-impedance state during the time the device is paused and transitions on these pins will be ignored. To resume serial communication, $\overline{HOLD}$ must be brought high while the SCK pin is low, otherwise serial communication will not resume. Lowering the HOLD line at any time will tri-state the SO line.

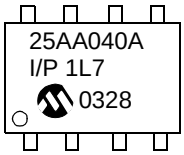
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

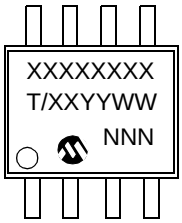
8-Lead PDIP



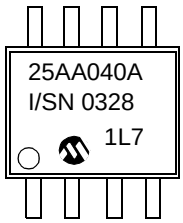
Example:



8-Lead SOIC

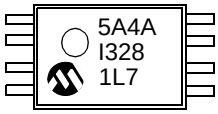


Example:



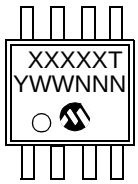
8-Lead TSSOP

Example:

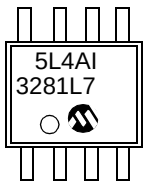


TSSOP 1st Line Marking Codes		
Device	std mark	Pb-free mark
25AA040A	5A4A	NA4A
25AA040X	5A4X	NA4X
25LC040A	5L4A	NL4A
25LC040X	5L4X	NL4X

8-Lead MSOP (150 mil)



Example:



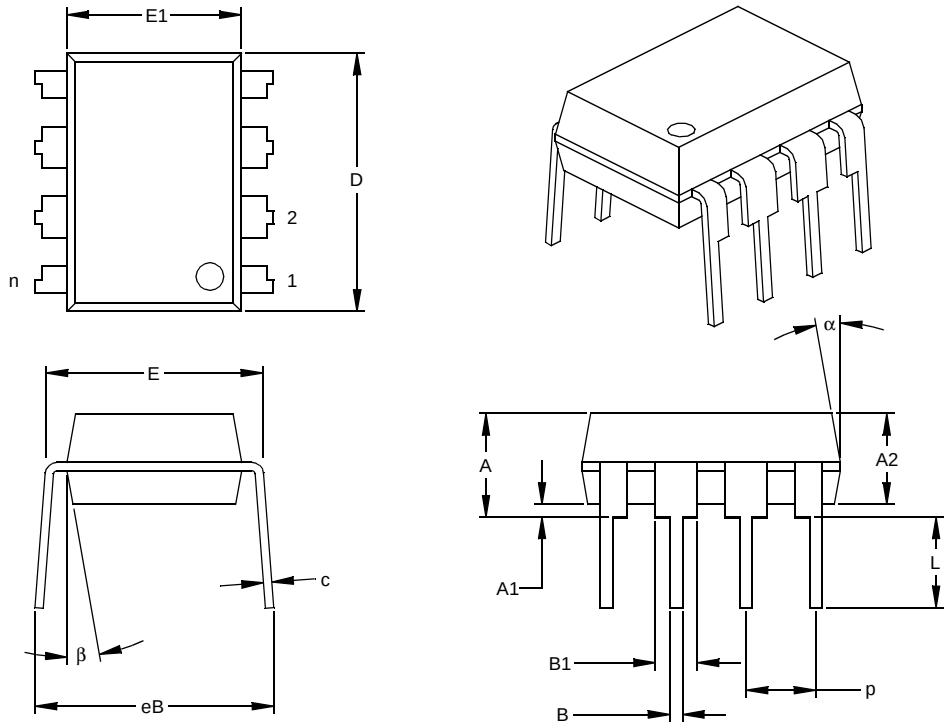
MSOP 1st Line Marking Codes		
Device	std mark	Pb-free mark
25AA040A	5A4A	G5A4A
25LC040A	5L4A	G5L4A

Legend:	XX...X	Part number
	T	Temperature (I, E)
	Blank	Commercial
	YY	Year code (last 2 digits of calendar year) except TSSOP
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

***** Standard EEPROM device marking consists of Microchip part number, year code, week code, and traceability code. For device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

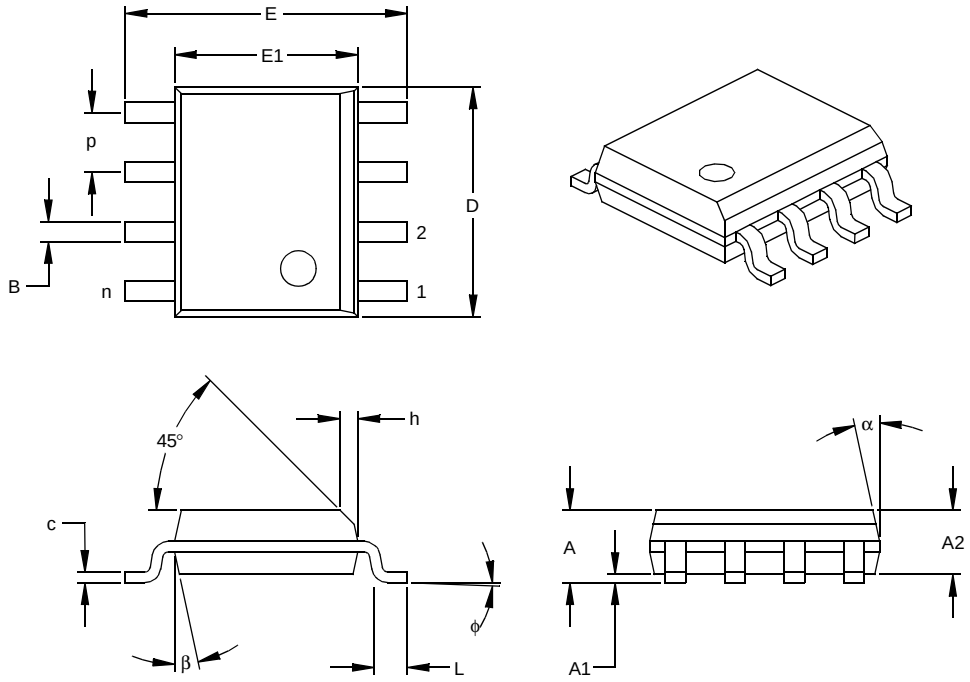


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)

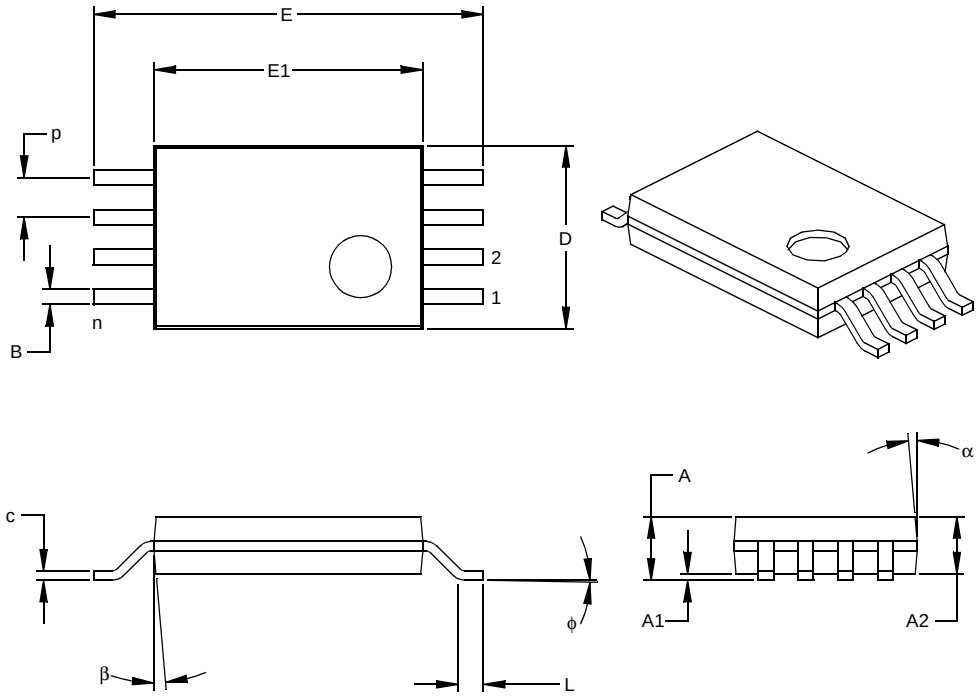


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)

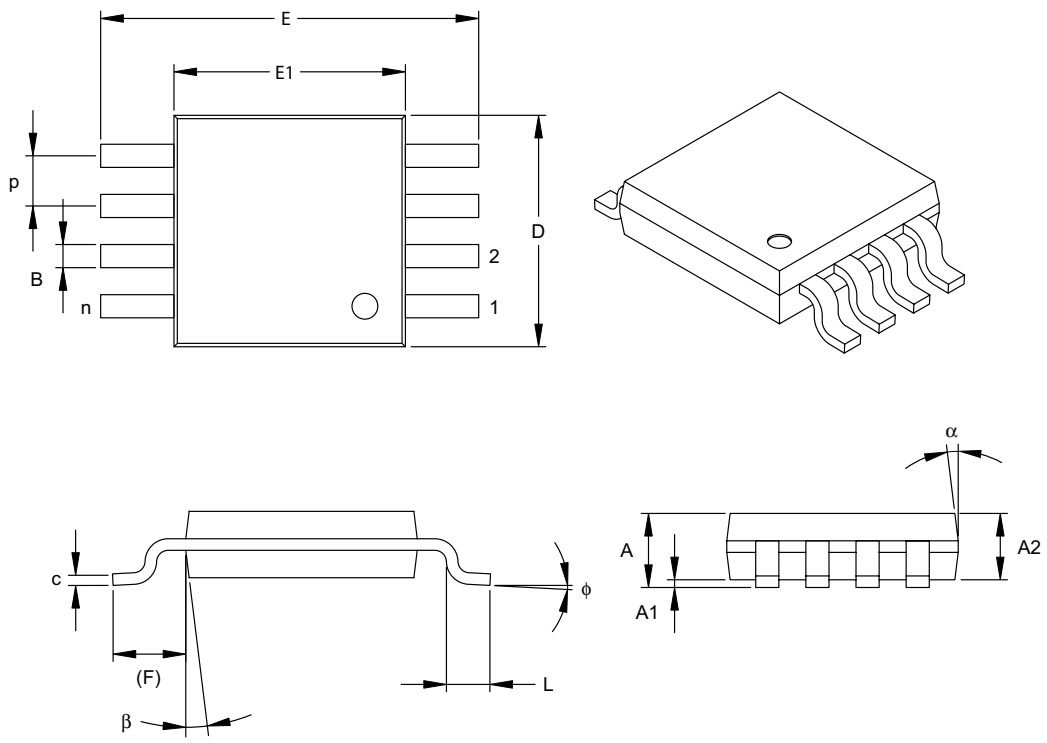


Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	ϕ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-086

8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E		.193 TYP.			4.90 BSC	
Molded Package Width	E1		.118 BSC			3.00 BSC	
Overall Length	D		.118 BSC			3.00 BSC	
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F		.037 REF			0.95 REF	
Foot Angle	φ	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	α	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°	5°	-	15°

*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-187

Drawing No. C04-111

APPENDIX A: REVISION HISTORY

Revision B

Corrections to Section 1.0, Electrical Characteristics.

NOTES:

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www.microchip.com

The file transfer site is available by using an FTP service to connect to:

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The web site and file transfer site provide a variety of services. Users may download files for the latest Development Tools, Data Sheets, Application Notes, User's Guides, Articles and Sample Programs. A variety of Microchip specific business information is also available, including listings of Microchip sales offices, distributors and factory representatives. Other data available for consideration is:

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4. What additions to the document do you think would enhance the structure and subject?

5. What deletions from the document could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	—	X	/XX	X
Device	Tape & Reel		Temperature	Package	Lead Finish

Device	25AA040A		4k-bit, 1.8V, 16 Byte Page, SPI Serial EEPROM
	25LC040A		4k-bit, 2.5V, 16 Byte Page, SPI Serial EEPROM
	25AA040AX		4k-bit, 1.8V, 16 Byte Page, SPI Serial EEPROM, in alternate pinout (ST only)
	25LC040AX		4k-bit, 2.5V, 16 Byte Page, SPI EEPROM, in alternate pinout (ST only)
Tape & Reel	Blank	=	Standard packaging
	T	=	Tape & Reel
Temperature Range	I	=	-40°C to+85°C
	E	=	-40°C to+125°C
Package	MS	=	Plastic MSOP (Micro Small Outline), 8-lead
	P	=	Plastic DIP (300 mil body), 8-lead
	SN	=	Plastic SOIC (150 mil body), 8-lead
	ST	=	TSSOP, 8-lead
Lead Finish	Blank	=	Standard 63% / 37% Sn/Pb
	G	=	Matte Tin (Pure Sn)

Examples:

a) 25AA040A-I/MS = 4k-bit, 16-byte page, 1.8V Serial EEPROM, Industrial temp., MSOP package

b) 25AA040A-I/STG = 4k-bit, 16-byte page, 1.8V Serial EEPROM, Industrial temp., TSSOP package, Pb-free

c) 25AA040AT-I/SN = 4k-bit, 16-byte page, 1.8V Serial EEPROM, Industrial temp., Tape & Reel, SOIC package

d) 25LC040A-I/MSG = 4k-bit, 16-byte page, 2.5V Serial EEPROM, Industrial temp., MSOP package, Pb-free

e) 25LC040AT-I/SN = 4k-bit, 16-byte page, 2.5V Serial EEPROM, Industrial temp., Tape & Reel, SOIC package

f) 25LC040AT-I/ST = 4k-bit, 16-byte page, 2.5V Serial EEPROM, Industrial temp., Tape & Reel, TSSOP package

g) 25LC040AT-E/SN = 4k-bit, 16-byte page, 2.5V Serial EEPROM, Extended temp., Tape & Reel, SOIC package

h) 25LC040AT-I/SNG = 4k-bit, 16-byte page, 2.5V Serial EEPROM, Tape & Reel, Industrial temp., SOIC package, Pb-free

i) 25LC040AX-E/ST = 4k-bit, 16-byte page, 2.5V Serial EEPROM, Extended temp., rotated pinout, TSSOP package

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Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

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- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

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