



**CY62136V MoBL®**

## 2-Mbit (128K x 16) Static RAM

### Features

- **Temperature Ranges**
  - Commercial: 0°C to 70°C
  - Industrial: -40°C to 85°C
  - Automotive: -40°C to 125°C
- **High speed: 55 ns and 70 ns**
- **70-ns speed bin offered in both Industrial and Automotive grades**
- **Wide voltage range: 2.7V–3.6V**
- **Ultra-low active, standby power**
- **Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Package available in a standard 44-pin TSOP Type II (forward pinout) package**
- **Also available in Lead-free package**

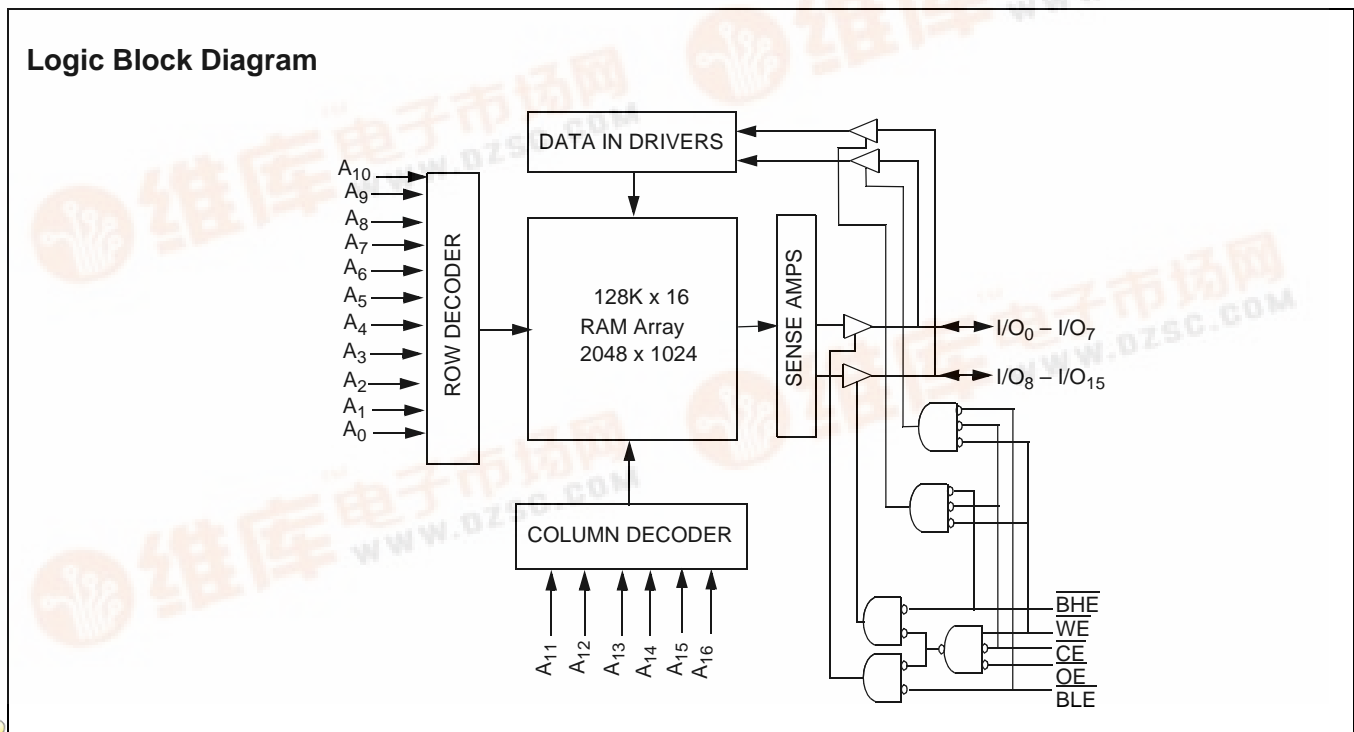
### Functional Description<sup>[1]</sup>

The CY62136V is a high-performance CMOS static RAM organized as 128K words by 16 bits. This device features

advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ( $\overline{CE}$  HIGH). The input/output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state when: deselected ( $\overline{CE}$  HIGH), outputs are disabled ( $\overline{OE}$  HIGH), BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation ( $\overline{CE}$  LOW, and WE LOW).

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>).

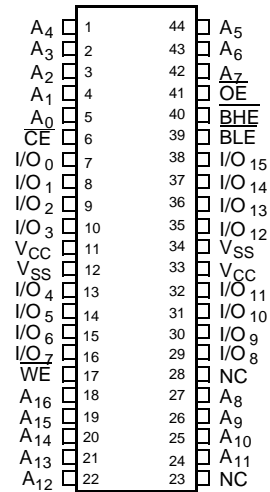
Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O<sub>8</sub> to I/O<sub>15</sub>. See the Truth Table at the back of this data sheet for a complete description of read and write modes.



Note: For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

**Product Portfolio**

Product	V <sub>CC</sub> Range (V)			Speed	Grades	Power Dissipation (Industrial)			
	Min	Typ. <sup>[2]</sup>	Max			Operating, I <sub>CC</sub> (mA)		Standby, I <sub>SB2</sub> (μA)	
						Typ. <sup>[2]</sup>	Maximum	Typ. <sup>[2]</sup>	Maximum
CY62136VLL	2.7	3.0	3.6	55	Industrial	7	20	1	15
					Industrial	7	15	1	15
				Automotive	7	20	1	20	
CY62136VSL				55	Industrial	7	20	1	5
				70	Industrial	7	15	1	5

**Pin Configurations<sup>[3]</sup>**
**TSOP II (Forward)  
Top View**

**Notes:**

2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub> Typ, T<sub>A</sub> = 25°C.
3. NC pins are not connected on the die



**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature ..... -65°C to +150°C
- Ambient Temperature with Power Applied ..... -55°C to +125°C
- Supply Voltage to Ground Potential ..... -0.5V to +4.6V
- DC Voltage Applied to Outputs in High-Z State<sup>[4]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V
- DC Input Voltage<sup>[4]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

- Output Current into Outputs (LOW) ..... 20 mA
- Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)
- Latch-up Current ..... > 200 mA

**Operating Range**

Range	Ambient Temperature [T <sub>A</sub> ] <sup>[6]</sup>	V <sub>CC</sub>
Industrial	-40°C to +85°C	2.7V to 3.6V
Automotive	-40°C to +125°C	

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	CY62136V-55			CY62136V-70			Unit	
			Min.	Typ. <sup>[2]</sup>	Max.	Min.	Typ. <sup>[2]</sup>	Max.		
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1.0 mA, V <sub>CC</sub> = 2.7V	2.4			2.4			V	
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA, V <sub>CC</sub> = 2.7V			0.4			0.4	V	
V <sub>IH</sub>	Input HIGH Voltage	V <sub>CC</sub> = 3.6V	2.2		V <sub>CC</sub> +0.5V	2.2		V <sub>CC</sub> +0.5V	V	
V <sub>IL</sub>	Input LOW Voltage	V <sub>CC</sub> = 2.7V	-0.5		0.8	-0.5		0.8	V	
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	Industrial	-1	+1	-1		+1	μA	
			Automotive			-10		+10	μA	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	Industrial	-1	+1	-1		+1	μA	
			Automotive			-10		+10	μA	
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub> , V <sub>CC</sub> = 3.6V, I <sub>OUT</sub> = 0 mA, CMOS Levels, f = 1 MHz,	Industrial		7	20		7	15	mA
			Automotive					7	20	mA
					1	2		1	2	mA
I <sub>SB1</sub>	Automatic CE Power-down Current— CMOS Inputs	CE ≥ V <sub>CC</sub> -0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> -0.3V or V <sub>IN</sub> ≤ 0.3V, f = f <sub>MAX</sub>			100			100	μA	
I <sub>SB2</sub>	Automatic CE Power-down Current— CMOS Inputs	CE ≥ V <sub>CC</sub> -0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> -0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0, V <sub>CC</sub> = 3.6V	Industrial (LL)		1	15		1	15	μA
			Industrial (SL)		1	5		1	5	μA
			Automotive					1	20	μA

**Thermal Resistance**

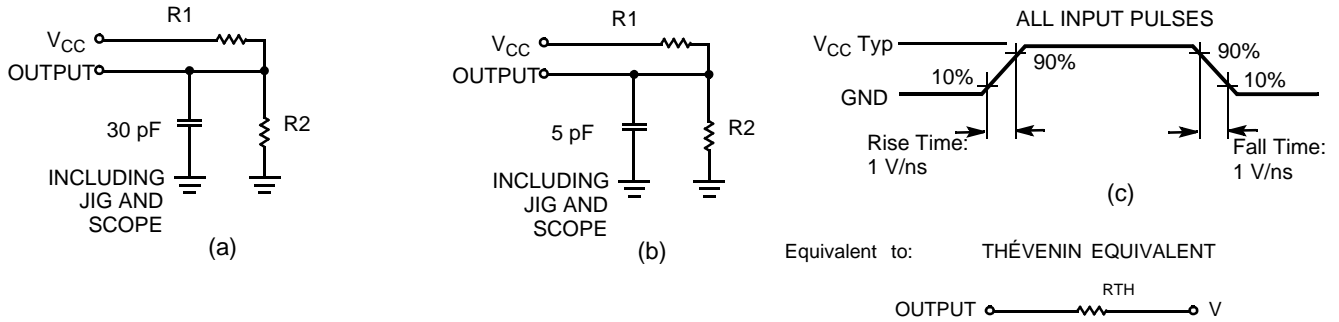
Parameter	Description	Test Conditions	TSOPII	Unit
Θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient) <sup>[5]</sup>	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	60	°C/W
Θ <sub>JC</sub>	Thermal Resistance (Junction to Case) <sup>[5]</sup>		22	°C/W

**Capacitance<sup>[5]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC</sub> (typ)	6	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

**Notes:**

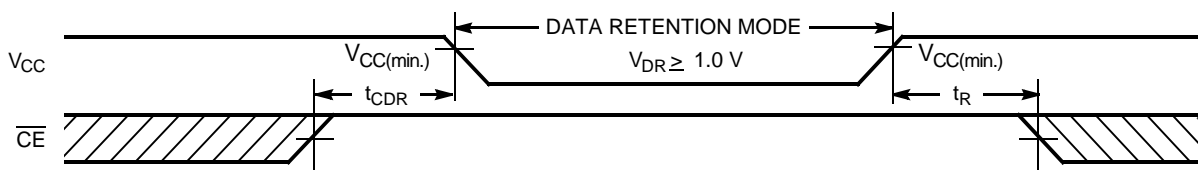
- 4. V<sub>IL</sub>(min) = -2.0V for pulse durations less than 20 ns.
- 5. Tested initially and after any design or process changes that may affect these parameters.
- 6. T<sub>A</sub> is the "Instant-On" case temperature.

**AC Test Loads and Waveforms**


Parameters	3.0V	Unit
R1	1105	Ohms
R2	1550	Ohms
$R_{TH}$	645	Ohms
$V_{TH}$	1.75	Volts

**Data Retention Characteristics (Over the Operating Range)**

Parameter	Description	Conditions <sup>[8]</sup>	Min.	Typ. <sup>[2]</sup>	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		1.0		3.6	V
$I_{CCDR}$	Data Retention Current	$V_{CC} = 1.0V, \overline{CE} \geq V_{CC} - 0.3V,$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V,$ No input may exceed $V_{CC} + 0.3V$		0.5	7.5	$\mu A$
		LL				
		SL			5	
$t_{CDR}^{[5]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[7]}$	Operation Recovery Time		70			ns

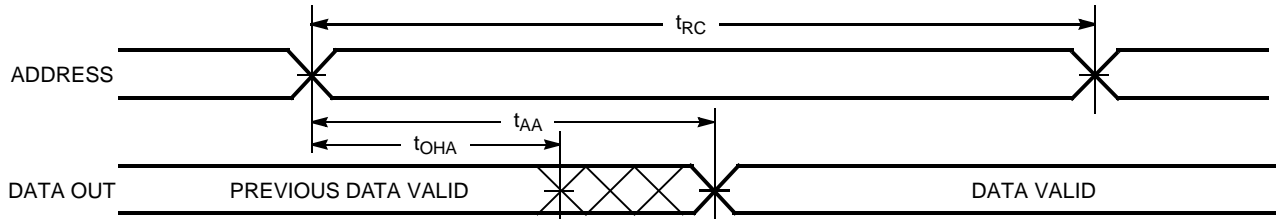
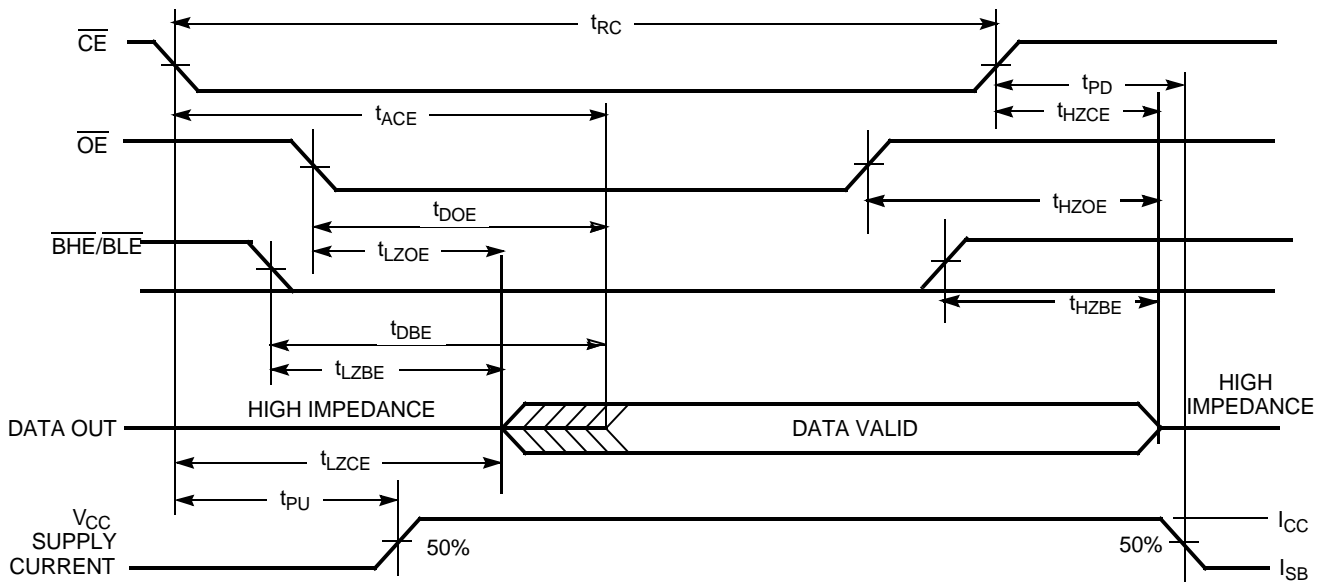
**Data Retention Waveform**


**Switching Characteristics** Over the Operating Range <sup>[8]</sup>

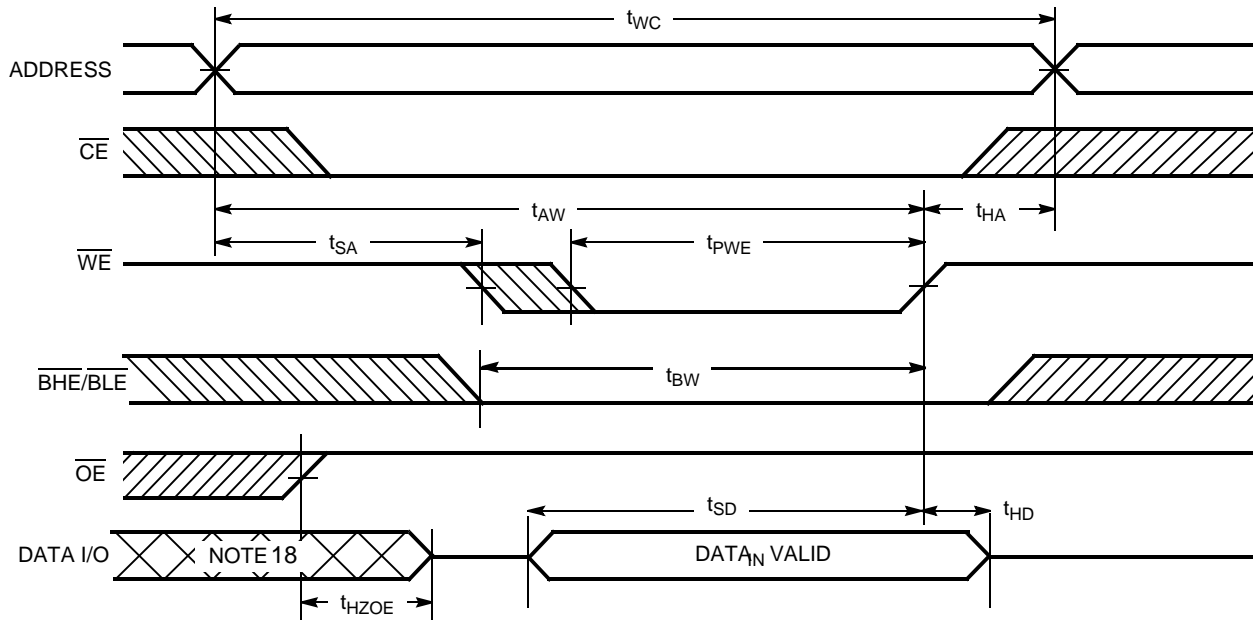
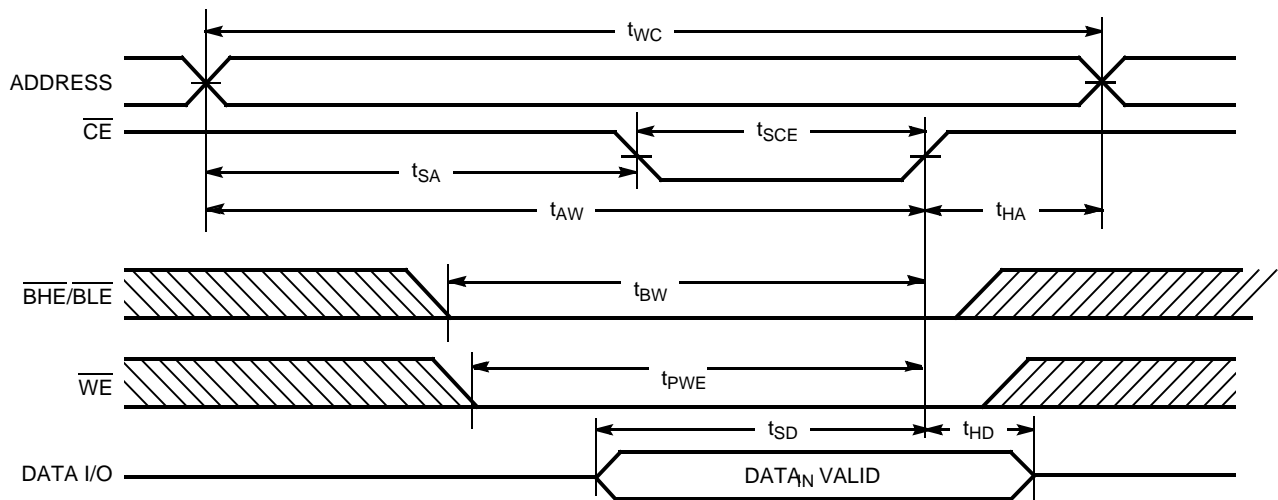
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
<b>Read Cycle</b>						
t <sub>RC</sub>	Read Cycle Time	55		70		ns
t <sub>AA</sub>	Address to Data Valid		55		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		10		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		55		70	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		25		35	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low-Z <sup>[9]</sup>	5		5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High-Z <sup>[9, 10]</sup>		25		25	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low-Z <sup>[9]</sup>	10		10		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High-Z <sup>[9, 10]</sup>		25		25	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-up	0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-down		55		70	ns
t <sub>DBE</sub>	$\overline{BLE}$ / $\overline{BHE}$ LOW to Data Valid		25		35	ns
t <sub>LZBE</sub>	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low-Z <sup>[9, 10]</sup>	5		5		ns
t <sub>HZBE</sub>	$\overline{BLE}$ / $\overline{BHE}$ HIGH to High-Z <sup>[11]</sup>		25		25	ns
<b>Write Cycle<sup>[11, 12]</sup></b>						
t <sub>WC</sub>	Write Cycle Time	55		70		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	45		60		ns
t <sub>AW</sub>	Address Set-up to Write End	45		60		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Set-up to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	40		50		ns
t <sub>BW</sub>	$\overline{BLE}$ / $\overline{BHE}$ LOW to Write End	50		60		ns
t <sub>SD</sub>	Data Set-up to Write End	25		30		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High-Z <sup>[9, 10]</sup>		20		25	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low-Z <sup>[9]</sup>	5		10		ns

**Notes:**

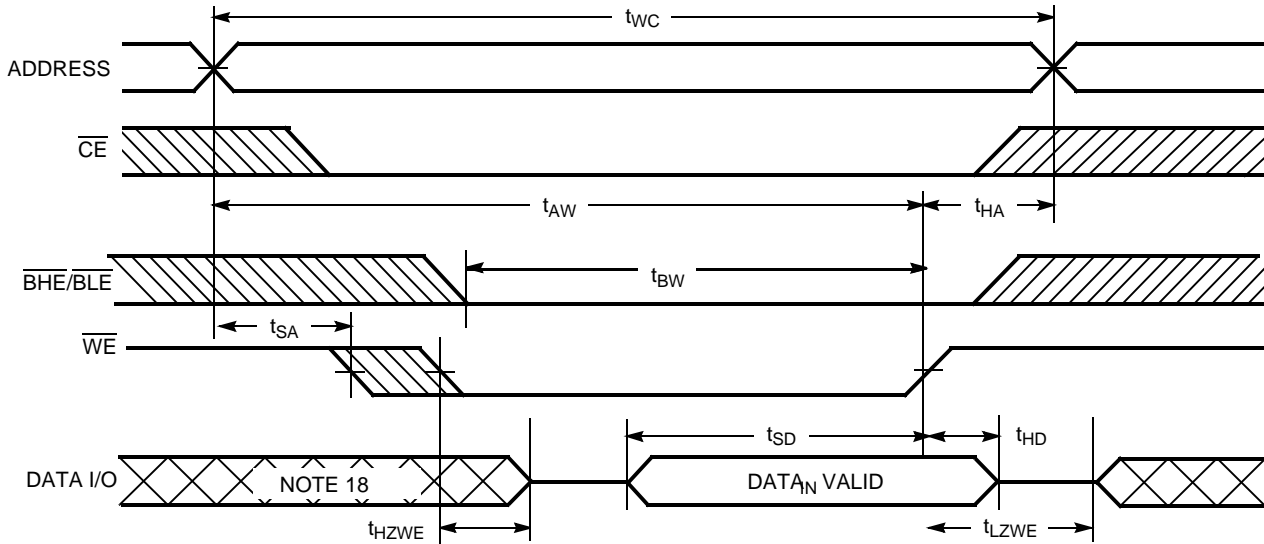
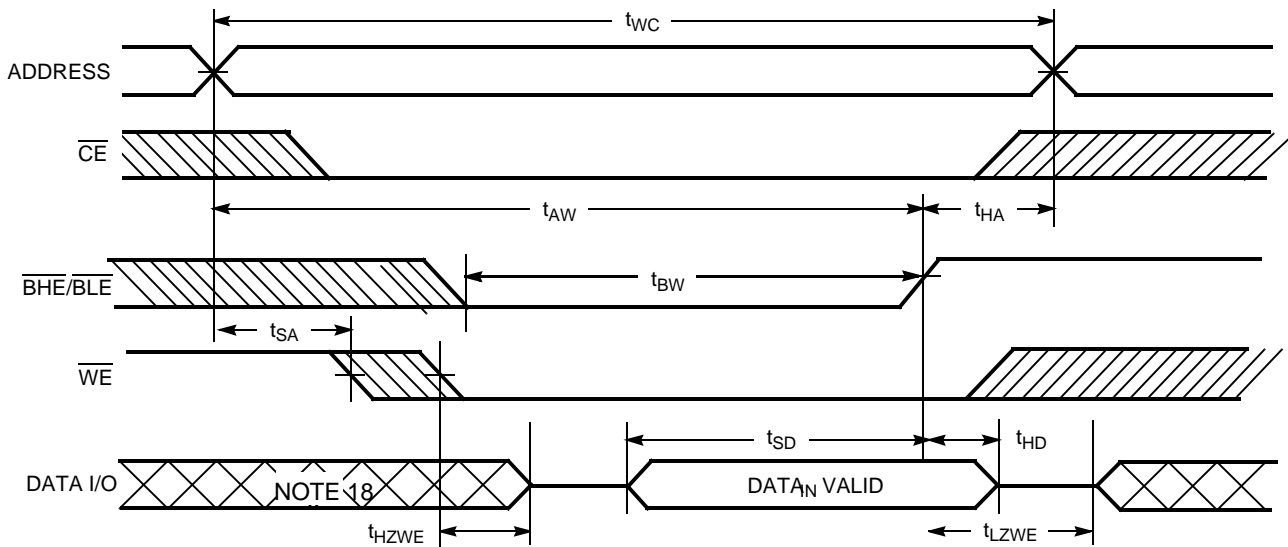
7. Full device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min)</sub> ≥ 100 ms or stable at V<sub>CC(min)</sub> ≥ 100 ms.
8. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to V<sub>CC</sub> typ., and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
9. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
10. t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
11. The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
12. The minimum write cycle time for write cycle 3 (WE controlled, OE LOW) is the sum of t<sub>HZWE</sub> and t<sub>SD</sub>.

**Switching Waveforms**
**Read Cycle No. 1<sup>[13, 14]</sup>**

**Read Cycle No. 2<sup>[14, 15]</sup>**

**Notes:**

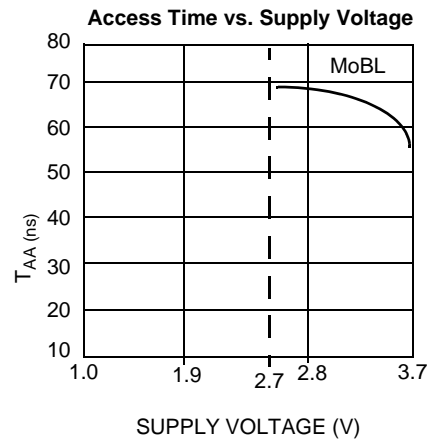
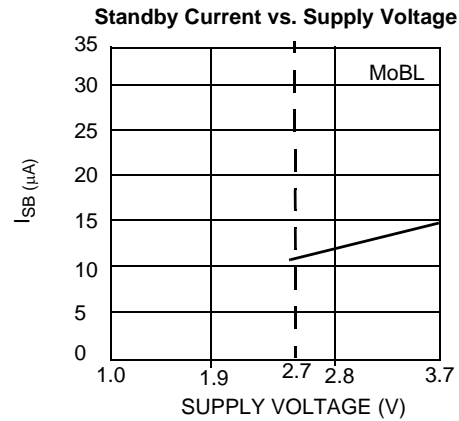
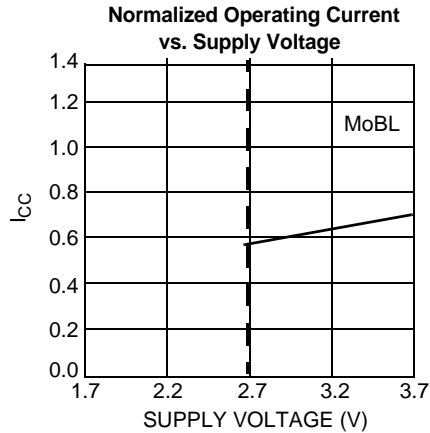
- 13. Device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .
- 14.  $\overline{WE}$  is HIGH for read cycle.
- 15. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[11, 16, 17]</sup>**

**Write Cycle No. 2 ( $\overline{CE}$  Controlled)<sup>[11, 16, 17]</sup>**

**Notes:**

16. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
17. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.
18. During this period, the I/Os are in output state and input signals should not be applied.

**Switching Waveforms (continued)**
**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[12, 17]</sup>**

**Write Cycle No. 4 ( $\overline{BHE}/\overline{BLE}$  Controlled,  $\overline{OE}$  LOW)<sup>[18]</sup>**




**Typical DC and AC Characteristics**

**Truth Table**

CE	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/Power-down	Standby ( $I_{SB}$ )
L	H	L	L	L	Data Out (I/O <sub>0</sub> -I/O <sub>15</sub> )	Read	Active ( $I_{CC}$ )
L	H	L	H	L	Data Out (I/O <sub>0</sub> -I/O <sub>7</sub> ); I/O <sub>8</sub> -I/O <sub>15</sub> in High-Z	Read	Active ( $I_{CC}$ )
L	H	L	L	H	Data Out (I/O <sub>8</sub> -I/O <sub>15</sub> ); I/O <sub>0</sub> -I/O <sub>7</sub> in High-Z	Read	Active ( $I_{CC}$ )
L	H	L	H	H	High-Z	Deselect/Output Disabled	Active ( $I_{CC}$ )
L	H	H	L	L	High-Z	Deselect/Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	High-Z	Deselect/Output Disabled	Active ( $I_{CC}$ )
L	H	H	L	H	High-Z	Deselect/Output Disabled	Active ( $I_{CC}$ )
L	L	X	L	L	Data In (I/O <sub>0</sub> -I/O <sub>15</sub> )	Write	Active ( $I_{CC}$ )
L	L	X	H	L	Data In (I/O <sub>0</sub> -I/O <sub>7</sub> ); I/O <sub>8</sub> -I/O <sub>15</sub> in High-Z	Write	Active ( $I_{CC}$ )
L	L	X	L	H	Data In (I/O <sub>8</sub> -I/O <sub>15</sub> ); I/O <sub>0</sub> -I/O <sub>7</sub> in High-Z	Write	Active ( $I_{CC}$ )

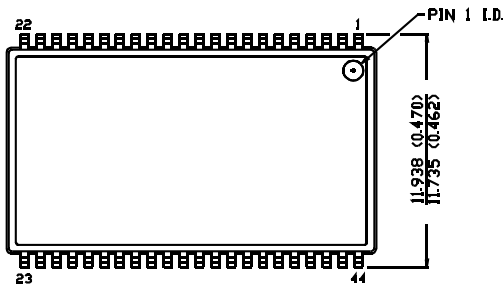
**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62136VLL-55ZI	Z44	44-pin TSOP II	Industrial
	CY62136VSL-55ZI	Z44	44-pin TSOP II	Industrial
	CY62136VLL-55ZXI	Z44	44-pin TSOP II (Pb-Free)	Industrial
70	CY62136VLL-70ZI	Z44	44-pin TSOP II	Industrial
	CY62136VLL-70ZXI	Z44	44-pin TSOP II (Pb-Free)	Industrial
	CY62136VLL-70ZSE	Z44	44-pin TSOP II	Automotive
	CY62136VLL-70ZSXE	Z44	44-pin TSOP II (Pb-Free)	Automotive
	CY62136VSL-70ZI	Z44	44-pin TSOP II	Industrial

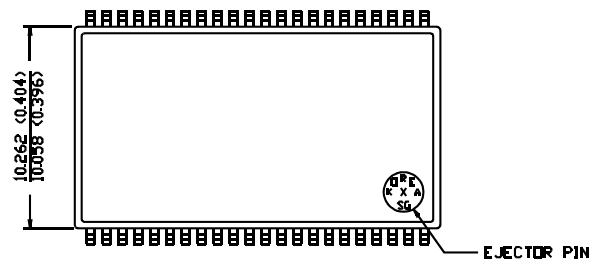
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**Package Diagrams**
**44-pin TSOP II Z44**

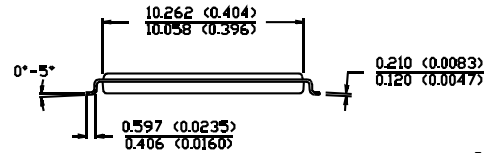
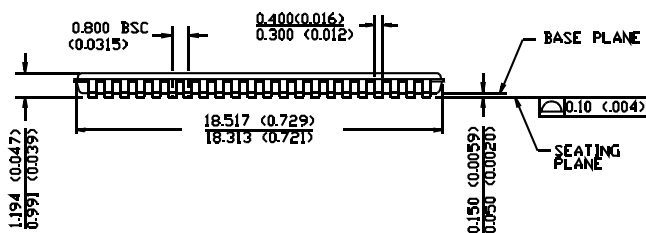
DIMENSION IN MM (INCH)  
MAX  
MIN



**TOP VIEW**



**BOTTOM VIEW**



51-85087-A

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Document History Page

Document Title: CY62136V MoBL® 2-Mbit (128K x 16) Static RAM				
Document Number: 38-05087				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	107347	05/25/01	SZV	Changed from Spec #: 38-00728 to 38-05087
*A	116509	09/04/02	GBI	Added footnote 1 Added SL power bin Deleted fBGA package; replacement fBGA package available in CY62136CV30
*B	269729	See ECN	SYT	Added Automotive Information for 70-ns Speed Bin. Added Footnotes # 3 and # 6. Corrected Typo in Electrical Characteristics for I <sub>CC</sub> (Max)-55 ns from 15 to 20 mA. Added SL row for I <sub>SB2</sub> in the Electrical Characteristics table. Changed Package Name from Z44 to ZS44. Replaced 'Z' with 'ZS' in the Ordering Code.
*C	344595	See ECN	SYT	Added Lead-Free Package on page# 9 Changed Package Name from ZS44 to Z44 for the 44 TSOP II Package Replaced 'ZS' with 'Z' in the Ordering Code for Industrial



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