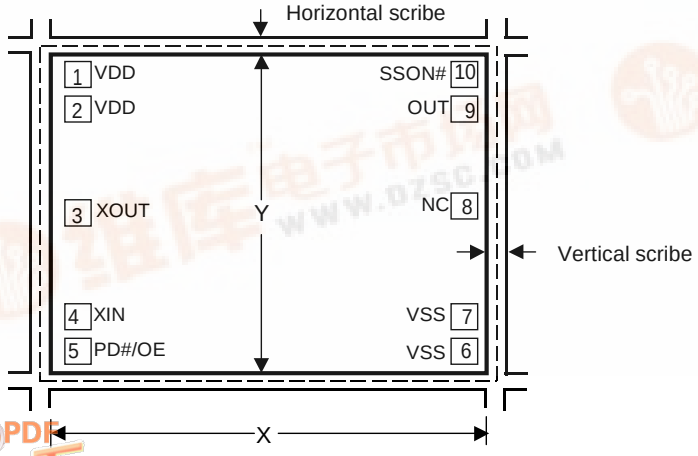
CYPRESS

CY5057

High-Frequency Flash Programmable PLL Die with Spread Spectrum

Features	Benefits
• **Flash-programmable die for in-package programming of crystal oscillators**	Enables quick turnaround of custom oscillators, and lowers inventory costs through stocking blank parts. In addition, the part can be programmed up to 100 times, which reduces programming errors and provides an easy upgrade path for existing designs
• **High-resolution phase-locked loop (PLL) with 10-bit multiplier and seven-bit divider**	Enables synthesis of highly accurate and stable output clock frequencies with zero or low PPM
• **Flash-programmable capacitor tuning array**	Enables fine-tuning of output clock frequency by adjusting C_{Load} of the crystal
• **Simple two-pin programming interface (excluding V_{DD} and V_{SS} pins)**	Allows the device to go into standard four- or six-pin packages.
• **On-chip oscillator used with external 25.1-MHz fundamental tuned crystal**	Lowers cost of oscillator, as PLL can be programmed to a high frequency using a low-frequency, low-cost crystal
• **Flash-programmable spread spectrum with spread percentages between ±0.25% and ±2.00%**	Provides various spread percentage
• **Spread Spectrum On/Off function**	Provides ability to enable or disable Spread Spectrum with an external pin
• **Operating frequency 5–170 MHz at 3.3V ± 10%**	Services most PC, networking, and consumer applications
• **Seven-bit linear post divider with divide options from divide-by-2 to divide-by-127**	Provides flexibility in output configurations and testing
• **Programmable PD# or OE pin**	Enables low-power operation or output enable function
• **Programmable asynchronous or synchronous OE and PD# modes**	Provides flexibility for system applications, through selectable instantaneous or synchronous change in outputs
• **Low jitter output < 200 ps (pk-pk) at 3.3V ± 10%**	Suitable for most PC, consumer, and networking applications
• **Controlled rise and fall times and output slew rate**	Has lower EMI than oscillators
• **Software Configuration Support**	Easy-to-use software support for design entry

Die Pad Description



Note:

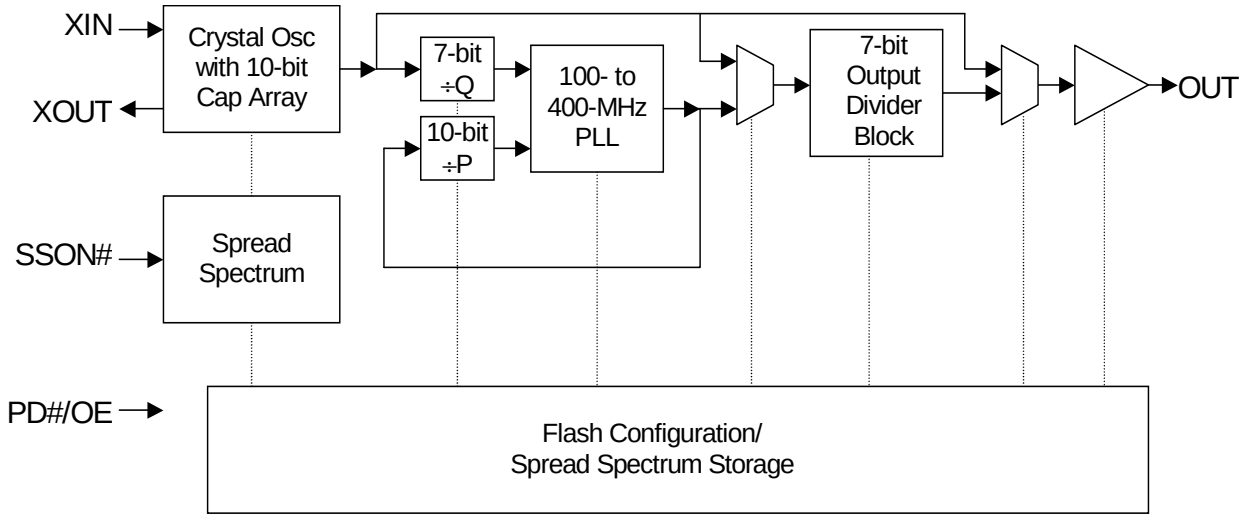
Active Die Size: X = 75.0 mils / 1907 µm
Y = 56.2 mils / 1428 µm

Scribe: X (horizontal)= 2.8 mils / 71 µm
Y (vertical)= 3.4 mils / 86.2 µm

Bond pad opening: 85 µm x 85 µm

Pad pitch: 125 µm x 125 µm
(Pad center to pad center)

Wafer thickness: 11 mils TYPICAL



Die Pad Summary Pad coordinates are referenced from the center of the die (X = 0, Y = 0).

Name	Die Pad	Description	X coordinate	Y coordinate
V_{DD}	1,2	Power supply	–843.612	597.849, 427.266
V_{SS}	6,7	Ground	883.743, 887.355	–563.304, –369.957
XIN	4	Crystal gate pin	–843.612	–1.806
XOUT	3	Crystal drain pin	–843.612	236.565
PD#/OE	5	Flash-programmable to function as power down or output enable in normal operating mode. Weak pull-up is default enabled.	–843.612	–424.662
V_{PP}		Super voltage while going into programming mode.		
SDA		Data pin while going into and while in programming mode.		
SSON#	10	Active low spread spectrum control. Asserting LOW turns the internal modulation waveform on. Strong pulldown is default enabled. Pulldown is disabled in powerdown mode.	834.183	589.848
SCL		Clock pin in programming mode. Should be double bonded to the OUT pad for pinouts not using the SSON# function. There is an internal pull-down resistor on this pad.		
OUT	9	Clock output. There is an internal pull-down resistor on this pad. Strong pulldown is default enabled. Default output is from the reference.	834.183	462.840
NC	8	No connect pin. (Do not connect this pad)	834.183	335.832

Functional Description

The CY5057 is a flash-programmable, high-accuracy, PLL-based die designed for the crystal oscillator market. It also contains spread spectrum circuitry that can be enabled or disabled with an external pin. The die is integrated with a low-cost 25.1-MHz fundamental tuned crystal in a four- or six-pin through-hole or surface mount package. The oscillator devices can be stocked as blank parts and custom frequencies can be programmed in-package at the last stage before shipping. This enables fast-turn manufacturing of custom and standard crystal oscillators without the need for dedicated, expensive crystals.

The CY5057 contains an on-chip oscillator and unique oscillator tuning circuit for fine-tuning the output frequency. The crystal C_{load} can be selectively adjusted by programming a set of flash memory bits. This feature can be used to compensate for crystal variations or to obtain a more accurate synthesized frequency.

The CY5057 uses a simple two-pin programming interface excluding the V_{SS} and V_{DD} pins. Clock outputs can be generated from 5 MHz to 170 MHz at 3.3V ± 10% operating voltage. The entire Flash configuration can be reprogrammed multiple times, allowing programmed inventory to be altered or reused.

The CY5057 PLL die has been designed for very high resolution. It has a 10-bit feedback counter multiplier and a seven-bit reference counter divider. This enables the synthesis of highly accurate and stable output clock frequencies with zero or low PPM error. The output of the PLL or the oscillator can be further modified by a seven-bit linear post divider with a total of 126 divider options (2 to 127).

The CY5057 also contains flexible power management controls. These parts include both power-down mode (PD# = 0) and output enable mode (OE = 1). The power-down and output enable modes have an additional setting to determine timing (asynchronous or synchronous) with respect to the output signal.

Controlled rise and fall times, unique output driver circuits, and innovative circuit layout techniques enable the CY5057 to have low jitter and accurate outputs making it suitable for most PC, networking and consumer applications.

The CY5057 also has an additional spread spectrum feature that can be disabled or enabled with an external pin. Please refer to Spread Spectrum section for details.

Flash Configuration and Spread Spectrum Storage Block

The following table summarizes the features which are configurable by flash memory bits. Please refer to the “CY5057 Programming Specification” for programming details. The specification can be obtained from your Cypress factory representative.

Flash Programmable Features	
Adjust Frequency	Feedback counter value (P)
	Reference counter value (Q)
	Output divider selection
	Oscillator tuning (load capacitance values)
Oscillator direct output	
Power management mode (OE or PD#)	
Power management timing (synchronous or asynchronous)	
Spread Spectrum	

PLL Output Frequency

The CY5057 contains a high-resolution PLL with a 10-bit multiplier and a seven-bit divider.The output frequency of the PLL is determined by the following formula:

$$F_{PLL} = \frac{2 \bullet (P_{BL} + 4) + Po}{(Q_L + 2)} \bullet F_{REF}$$

where Q_L is the loaded or programmed reference counter value (Q counter), P_{BL} is the loaded or programmed feedback counter value (P counter), and Po is the P offset bit (can only be 0 or 1). In Spread Spectrum mode, the time-averaged P value is used to calculate the average frequency.

Power Management Features

The CY5057 contains Flash-programmable PD# (active LOW) and OE (active HIGH) functions. If power-down mode is selected (PD# = 0), the oscillator and PLL are placed in a low supply current standby mode and the output is tri-stated and weakly pulled low. The oscillator and PLL circuits must re-lock when the part leaves Powerdown Mode. If output enable mode is selected (OE = 0), the output is tri-stated and weakly pulled low. In this mode the oscillator and PLL circuits continue to operate, allowing a rapid return to normal operation when the output is enabled.

In addition, the PD# and OE modes can be programmed to occur synchronously or asynchronously with respect to the output signal. When the asynchronous setting is used, the powerdown or output disable occurs immediately (allowing for logic delays) irrespective of position in the clock cycle. However, when the synchronous setting is used, the part waits for a falling edge at the output before powerdown or output enable signal initiated, thus preventing output glitches. In either asynchronous or synchronous setting, the output is always enabled synchronously by waiting for the next falling edge of the output.

Spread Spectrum

The CY5057 contains spread spectrum with flash programmable spread percentage and modulation frequency. Center spread non-linear “Hershey kiss” modulation can be obtained. Spread percentage can be programmed to values between ±0.250% and ±2.00%, in 0.25% intervals. Only one spread profile (for one specific percentage spread and for one output frequency) can be programmed into the device at a time

The CY5057 has a spread spectrum On/Off function. The spread spectrum can be enabled or disabled by users through an external pin. Timing of this feature is shown in “switching waveform” section.

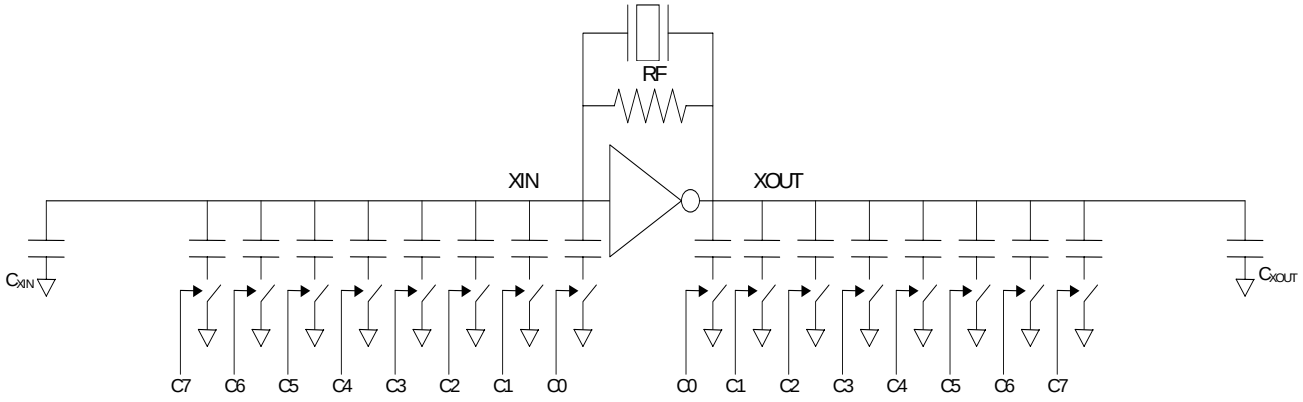


Figure 1. Crystal Oscillator Tuning Circuit

Crystal Oscillator Tuning Cap Values[1]

Bit	Capacitance per Bit (pF)
C_7	24.32
C_6	12.16
C_5	6.08
C_4	3.04
C_3	1.52
C_2	0.76
C_1	0.38
C_0	0.19

Note:
1. C_{XIN}, C_{XOUT}, and parasitic capacitance due to fixture and package should be included when calculating the total capacitance.

Absolute Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage .....–0.5 to +7.0V

Input Voltage ..... –0.5V to V_{DD} + 0.5

Storage Temperature (Non-condensing).....–55°C to +125°C

Junction Temperature ..... –40°C to +125°C

Data Retention @ Tj = 125°C.....> 10 years

Maximum Programming Cycles.....100

Static Discharge Voltage..... ≥ 2000V (per MIL-STD-883, Method 3015)

Operating Conditions

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage (3.3V)	3.0	3.6	V
T_{AJ}[2]	Operating Temperature, Junction	–40	100	°C
C_{LC}	Max. Capacitive Load on the output (CMOS levels spec) V_{DD} = 3.0V–3.6V, output frequency = 5–170 MHz		15	pF
X_{REF}	Reference Frequency with spread spectrum disabled. Fundamental tuned crystals only.	25.1	25.1	MHz
C_{in}	Input Capacitance (except crystal pins)		7	pF
C_{XIN}	Crystal input capacitance (all internal caps off)	10	14	pF
C_{Xout}	Crystal output capacitance (all internal caps off)	10	14	pF
T_{PU}	Power-up time for all V_{DD}'s to reach minimum specified voltage (power ramps must be monotonic)	0.05	500	ms

DC Electrical Characteristics, Tj = –40 to 100°C

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input Low Voltage PD#/OE and SSON# pins	CMOS levels, 30% of V_{DD} V_{DD} = 3.0V–3.6V		0.3	V_{DD}
V_{IH}	Input High Voltage PD#/OE and SSON# pins	CMOS levels, 70% of V_{DD} V_{DD} = 3.0V–3.6V	0.7		V_{DD}
V_{OL}	Output Low Voltage, OUT pin	V_{DD} = 3.0V–3.6V, I_{OL} = 8 mA		0.4	V
V_{OH}	Output High Voltage, CMOS levels	V_{DD} = 3.0V–3.6V, I_{OH} = –8 mA	V_{DD} – 0.4		V
I_{ILPDOE}	Input Low Current, PD#/OE pin	V_{IN} = V_{SS} (Internal pull-up = 3MΩ typical)		10	µA
I_{IHPDOE}	Input High Current, PD#/OE pin	V_{IN} = V_{DD} (Internal pull-up = 100kΩ typical)		10	µA
I_{ILSR}	Input Low Current, SSON# pin	V_{IN} = V_{SS} (Internal pull-down = 100kΩ typical)		10	µA
I_{IHSR}	Input High Current, SSON# pin	V_{IN} = V_{DD} (Internal pull-down = 100kΩ typical)		50	µA
I_{DD}	Supply Current	No Load, V_{DD} = 3.0V–3.6V, Fout = 170 MHz		50	mA
I_{OZ}	Output Leakage Current, OUT pin	V_{DD} = 3.0V–3.6V, Output disabled with OE		50	µA
I_{PD}	Standby Current	V_{DD} = 3.0V–3.6V, Device powered down with PD#		50	µA
R_{UP}	Pull-up Resistor on PD#/OE pin	V_{DD} = 3.0 to 3.6V, measured at V_{IN} =V_{SS} V_{DD} = 3.0V–3.6V, measured at V_{IN} = 0.7V_{DD}	1 80	6 150	MΩ kΩ
R_{DN}	Pull-down Resistor on SSON# and OUT Pins	V_{DD} = 3.0V–3.6V, measured at V_{IN} = 0.5V_{DD}	80	150	kΩ
Rf	Crystal Feedback Resistor	V_{DD} = 3.0V–3.6V, measured at X_{IN} = 0.	100		kΩ

Note:

2. In Cypress standard TSSOP packages with external crystal.

AC Electrical Characteristics[2] Tj = –40 to 100°C

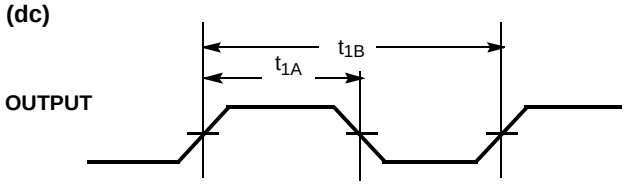
Parameter	Description	Test Conditions	Min.	Max.	Unit
F_{out}	Output Frequency	V_{DD} = 3.0 to 3.6V, C_L = 15 pF	5	170	MHz
tr	OUT Rise Time	V_{DD} = 3.0V–3.6V, 20% to 80% V_{DD}, C_L = 15 pF		2.7	ns
tf	OUT Fall Time	V_{DD} = 3.0V–3.6V, 80% to 20% V_{DD}, C_L = 15 pF		2.7	ns
DC	OUT Duty Cycle	Divider output, Measured at $V_{DD}/2$ Crystal direct output, Measured at $V_{DD}/2$	45 40	55 60	% %
t_{J1}	Peak to Peak Period Jitter	$F_{out} \geq$133 MHz, $V_{DD}/2$, SS off 25 MHz $\leq F_{out}<$ 133 MHz, $V_{DD}/2$, SS off $F_{out}<$ 25MHz, $V_{DD}/2$, SS off		200 400 1% of $1/F_{out}$	ps ps s
t_{J2}	Cycle to Cycle Jitter	F_{out} >133 MHz, $V_{DD}/2$, SS on 25MHz $\leq F_{out}<$ 133 MHz, $V_{DD}/2$, SS on $F_{out}<$ 25 MHz, $V_{DD}/2$, SS on		200 400 1% of $1/F_{out}$	ps ps s
F_{MOD}	Modulation Frequency		30	33	kHz
DL	Crystal Drive Level	Measured at 25.1 MHz, with 20Ω R, cap setting = hex16, DL = 10		540	µW
–R	Negative Resistance	Measured at 25.1 MHz		–140	Ω

Timing Parameters[2]

Parameter	Description	Min.	Max.	Unit
T_{SSON1}	Time from steady state spread to steady state non-spread		600	µs
T_{SSON2}	Time from steady state non-spread to steady state spread		100	µs
T_{SSON3}	Minimum SSON# pulse width (positive or negative)	250		µs
T_{MOD}	Spread Spectrum Modulation period	30	33.33	µs
$T_{STP,SYNC}$	Time from falling edge on PD# to stopped outputs, synchronous mode, T = $1/F_{out}$		1.5T + 350	ns
$T_{STP,ASYNC}$	Time from falling edge on PD# to stopped outputs, asynchronous mode		350	ns
$T_{PU,SYNC}$	Time from rising edge on PD# to outputs at valid frequency, synchronous mode		3	ms
$T_{PU,ASYNC}$	Time from rising edge on PD# to outputs at valid frequency, asynchronous mode		3	ms
$T_{PXZ,SYNC}$	Time from falling edge on OE to high-impedance outputs, synchronous mode, T = $1/F_{out}$		1.5T+350	ns
$T_{PXZ,ASYNC}$	Time from falling edge on OE to high-impedance outputs, asynchronous mode		350	ns
$T_{PZX,SYNC}$	Time from rising edge on OE to running outputs, synchronous mode, T=$1/F_{out}$		1.5T + 350	ns
$T_{PZX,ASYNC}$	Time from rising edge on OE to running outputs, asynchronous mode		350	ns
T_{LOCK}	PLL lock time		10	ms

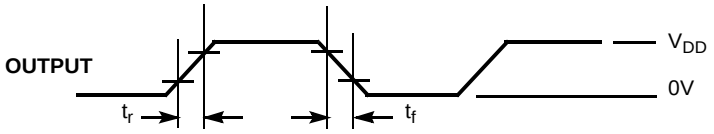
Switching Waveforms

Duty Cycle Timing (dc)



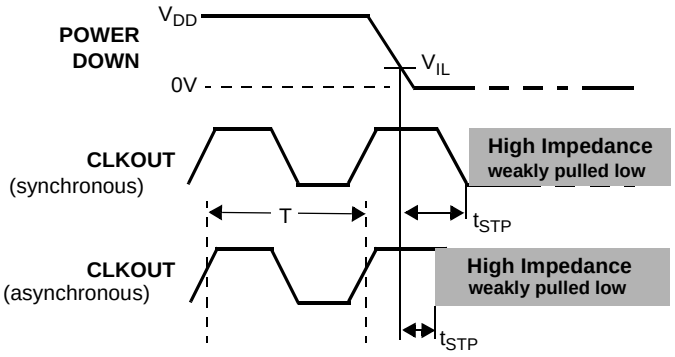
$$\text{Duty} = \frac{t_{1A}}{t_{1B}} \times [100\%]$$

Output Rise/Fall Time

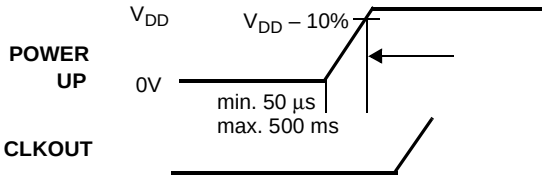


Switching Waveforms (continued)

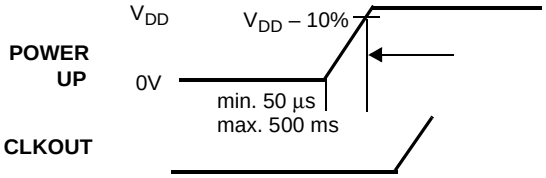
Power-down Timing (synchronous and asynchronous modes)



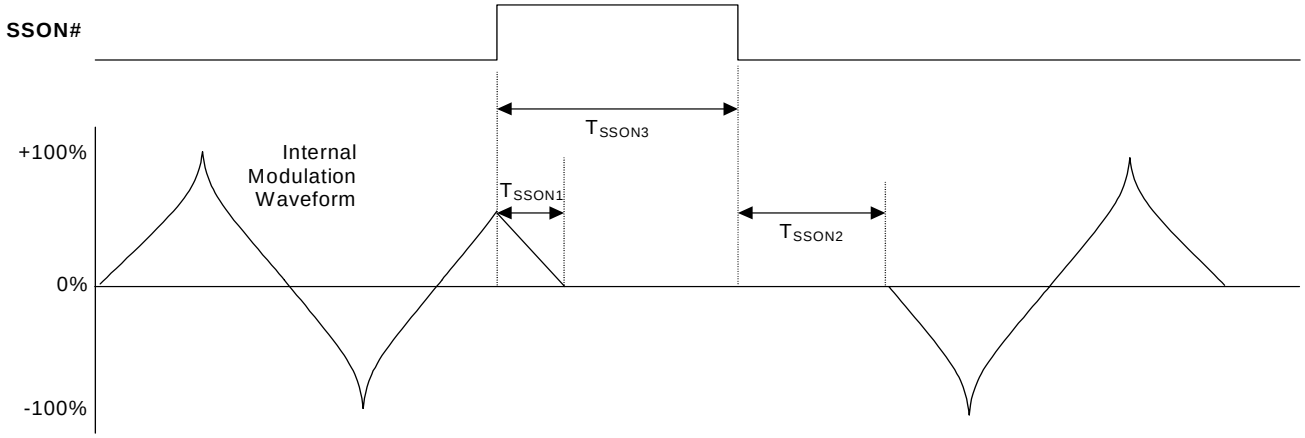
Power-up Timing



Power-up Timing



Spread Spectrum On/OFF Timing



Ordering Information

Ordering Code	Type	Operating Range
CY5057-11WAF	Wafer (background to 11 mils)	–40°C to 100°C

Document History Page

Document Title: CY5057 High-Frequency Flash Programmable PLL Die with Spread Spectrum Document Number: 38-07363				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	112486	05/01/02	CKN	New Data Sheet
*A	121373	12/10/02	CKN	Added scribe lines to Die Pad Description Added wafer thickness to Die Pad Description Added X and Y coordinates to Die Pad Description Removed list of discrete frequencies and discrete spread percentages Removed references to discrete frequencies and profile tables Replaced with description of software for full programmability Operating frequency changed to 5 MHz–170 MHz Removed C0 and C1 from crystal oscillator tuning circuit; renumbered other capacitors Changed maximum junction temperature to 125°C Changed PDOE internal pull-up value to 1–6 Mohm when $V_{IN} = V_{SS}$ Changed IILPDOE to 10 µA Changed Rf spec to 100 kohm, at condition $X_{IN} = 0$ Change DL spec to 540 µW, at condition cap setting = hex16, DL=10 Added power up timing diagram separate from power down timing diagram Removed die information table
*B	127414	07/01/03	RGL	Added –11 and other details to Ordering Information Added t_{PU} details to Operating Conditions Changed Max T_{SSON1} value to 600 in Timing Parameters table Changed Parameter T_{PU} under Timing Parameters to T_{LOCK} with the description “PLL lock time” Altered Min and Max values in Power-up Timing figure