FastEdge™ Series
CY2PP318

1:8 Differential Clock/Data Fanout Buffer

Features

- Eight ECL/PECL differential outputs
- Two ECL/PECL differential inputs
- Hot-swappable/-insertable
- 34 ps typical output-to-output skew
- 50 ps typical part-to-part skew
- 500 ps typical propagation delay
- 0.13 ps typical RMS phase jitter
- 7.6 ps typical peak period jitter
- 1.5 GHz Operation (2.2 GHz max. toggle frequency)
- PECL mode supply range: V_{CC} = 2.5V± 5% to 3.3V±5% with V_{EE} = 0V
- ECL mode supply range: V_{EE} = –2.5V± 5% to –3.3V±5% with V_{CC} = 0V
- Industrial temperature range: –40°C to 85°C
- 28-pin PLCC package
- Temperature compensation like 100K ECL

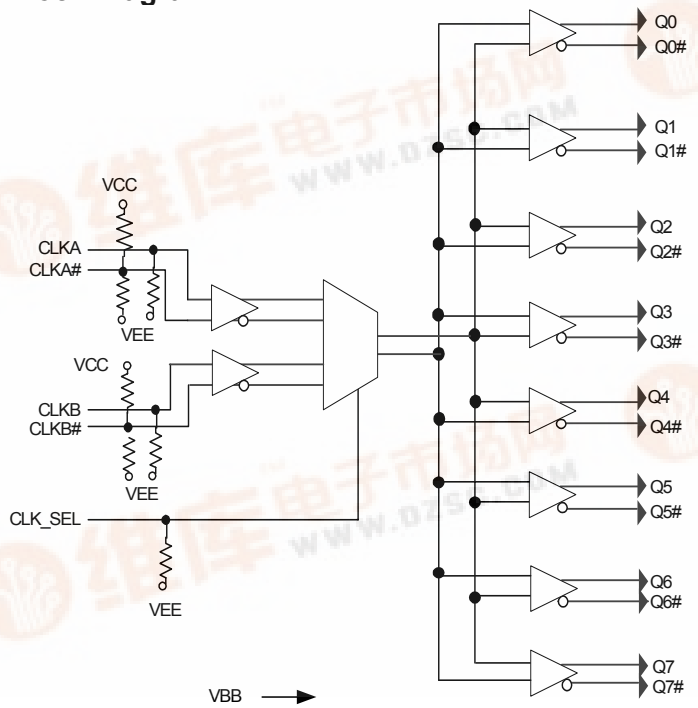
Functional Description

The CY2PP318 is a low-skew, low propagation delay 1-to-8 differential fanout buffer targeted to meet the requirements of high-performance clock and data distribution applications. The device is implemented on SiGe technology and has a fully differential internal architecture that is optimized to achieve low signal skews at operating frequencies of up to 1.5 GHz.

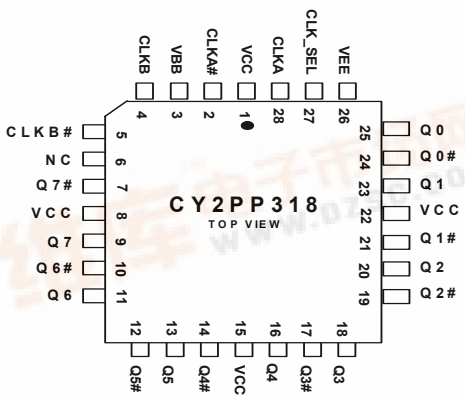
The device features two differential input paths that are multiplexed internally. This mux is controlled by the CLK_SEL pin. The CY2PP318 may function not only as a differential clock buffer but also as a signal-level translator and fanout on ECL/PECL signal to eight ECL/PECL differential loads. An external bias pin, VBB, is provided for this purpose. In such an application, the VBB pin should be connected to either one of the CLKA# or CLKB# inputs and bypassed to ground via a 0.01-µF capacitor.

Since the CY2PP318 introduces negligible jitter to the timing budget, it is the ideal choice for distributing high frequency, high precision clocks across back-planes and boards in communication systems. Furthermore, advanced circuit design schemes, such as internal temperature compensation, ensure that the CY2PP318 delivers consistent performance over various platforms.

Block Diagram



Pin Configuration



Pin Definitions[1, 2, 3]

Pin	Name	I/O	Type	Description
3	VBB	O	Bias	**Reference Voltage Output**
26	VEE	–PWR	Power	**Negative Supply**
1, 8, 15, 22	VCC	+PWR	Power	**Positive Supply**
28	CLKA	I, PD	ECL/PECL	**ECL/PECL Differential Input Clocks**
2	CLKA#	I, PD/PU	ECL/PECL	**ECL/PECL Differential Input Clocks**
4	CLKB	I, PD	ECL/PECL	**ECL/PECL Differential Input Clocks**
5	CLKB#	I, PD/PU	ECL/PECL	**ECL/PECL Differential Input Clocks**
27	CLK_SEL	I, PD	ECL/PECL	**ECL/PECL Input Clock Select**
6	NC			**No Connect**
25,23,20,18,16,13,11,9	Q(0:7)	O	ECL/PECL	**ECL/PECL Differential Output Clocks**
24,21,19,17,14,12,10,7	Q(0;7)#	O	ECL/PECL	**ECL/PECL Differential Output Clocks**

Table 1.

Control	Operation
CLK_SEL	
0	CLKA, CLKA# input pair is active (Default condition with no connection to pin) CLKA can be driven with ECL- or PECL-compatible signals with respective power configurations
1	CLKB, CLKB# input pair is active. CLKB can be driven with ECL- or PECL-compatible signals with respective power configurations

Governing Agencies

The following agencies provide specifications that apply to the CY2PP318. The agency name and relevant specification is listed below in *Table 2*.

Table 2.

Agency Name	Specification
JEDEC	JESD 020B (MSL) JESD 51 (Theta JA) JESD 8–2 (ECL) JESD 65–B (skew,jitter)
Mil-Spec	883E Method 1012.1 (Thermal Theta JC)

Notes:
1. In the I/O column, the following notation is used: I for Input, O for Output, PD for Pull-Down, PU for Pull-Up, and PWR for Power.
2. In ECL mode (negative power supply mode), V_{EE} is either –3.3V or –2.5V and V_{CC} is connected to GND (0V). In PECL mode (positive power supply mode), V_{EE} is connected to GND (0V) and V_{CC} is either +3.3V or +2.5V. In both modes, the input and output levels are referenced to the most positive supply (V_{CC}) and are between V_{CC} and V_{EE}.
3. V_{BB} is available for use for single-ended bias mode for |3.3V| supplies (not |2.5V|).

Absolute Maximum Ratings

Parameter	Description	Condition	Min.	Max.	Unit
V_{CC}	Positive Supply Voltage	Non-Functional	–0.3	4.6	V
V_{EE}	Negative Supply Voltage	Non-Functional	-4.6	0.3	V
T_S	Temperature, Storage	Non-Functional	–65	+150	°C
T_J	Temperature, Junction	Non-Functional		150	°C
ESD_h	ESD Protection	Human Body Model	2000		V
M_{SL}	Moisture Sensitivity Level		3		N.A.
Gate Count	Total Number of Used Gates	Assembled Die	28		gates

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

Operating Conditions

Parameter	Description	Condition	Min.	Max.	Unit
I_{BB}	Output Reference Current	Relative to V_{BB}		|200|	uA
LU_I	Latch Up Immunity	Functional, typical	100		mA
T_A	Temperature, Operating Ambient	Functional	–40	+85	°C
$Ø_{Jc}$	Dissipation, Junction to Case	Functional	39[4]		°C/W
$Ø_{Ja}$	Dissipation, Junction to Ambient	Functional	60[4]		°C/W
I_{EE}	Maximum Quiescent Supply Current	V_{EE} pin		100[5]	mA
C_{IN}	Input Pin Capacitance			3	pF
L_{IN}	Pin Inductance			1	nH
V_{IN}	Input Voltage	Relative to V_{CC}[6]	–0.3	V_{CC} + 0.3	V
V_{TT}	Output Termination Voltage	Relative to V_{CC}[6]	V_{CC} – 2		V
V_{OUT}	Output Voltage	Relative to V_{CC}[6]	–0.3	V_{CC} + 0.3	V
I_{IN}	Input Current[7]	$V_{IN} = V_{IL}$, or $V_{IN} = V_{IH}$		I150I	uA

PECL DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
V_{CC}	Operating Voltage	2.5V ± 5%, V_{EE} = 0.0V 3.3V ± 5%, V_{EE} = 0.0V	2.375 3.135	2.625 3.465	V V
V_{CMR}	Differential Cross Point Voltage[8]	Differential operation	1.2	V_{CC}	V
V_{OH}	Output High Voltage	I_{OH} = –30 mA[9]	V_{CC} – 1.25	V_{CC} – 0.7	V
V_{OL}	Output Low Voltage V_{CC} = 3.3V ± 5% V_{CC} = 2.5V ± 5%	I_{OL} = –5 mA[9]	 V_{CC} – 1.995 V_{CC} –1.995	 V_{CC} – 1.5 V_{CC} – 1.3	 V V
V_{IH}	Input Voltage, High	Single-ended operation	V_{CC} – 1.165	V_{CC} – 0.880[10]	V
V_{IL}	Input Voltage, Low	Single-ended operation	V_{CC} – 1.945[10]	V_{CC} – 1.625	V
V_{BB}[3]	Output Reference Voltage	Relative to V_{CC}[6]	V_{CC} – 1.620	V_{CC} – 1.220	V

Notes:
4. Theta JA EIA JEDEC 51 test board conditions (typical value); Theta JC 883E Method 1012.1
5. Power Calculation: V_{CC} * I_{EE} +0.5 (I_{OH} + I_{OL}) (V_{OH} – V_{OL}) (number of differential outputs used); I_{EE} does not include current going off chip.
6. where V_{CC} is 3.3V±5% or 2.5V±5%.
7. Inputs have internal pull-up/pull-down or biasing resistors which affect the input current.
8. Refer to *Figure 1*.
9. Equivalent to a termination of 50Ω to VTT. I_{OHMIN}= (V_{OHMIN} – V_{TT})/50; I_{OHMAX} = (V_{OHMAX} – V_{TT})/50; I_{OLMIN} = (V_{OLMIN} – V_{TT})/50; I_{OLMAX} = (V_{OLMAX} – V_{TT})/50.
10. V_{IL} will operate down to V_{EE}; V_{IH} will operate up to V_{CC}.

ECL DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
V_{EE}	Negative Power Supply	–2.5V ± 5%, V_{CC} = 0.0V –3.3V ± 5%, V_{CC} = 0.0V	–2.625 –3.465	–2.375 –3.135	V
V_{CMR}	Differential cross point voltage[8]	Differential operation	V_{EE} + 1.2	0V	V
V_{OH}	Output High Voltage	I_{OH} = –30 mA[9]	–1.25	–0.7	V
V_{OL}	Output Low Voltage V_{EE} = –3.3V ± 5% V_{EE} = –2.5V ± 5%	I_{OL} = –5 mA[9]	 –1.995 –1.995	 –1.5 –1.3	V
V_{IH}	Input Voltage, High	Single-ended operation	–1.165	–0.880[10]	V
V_{IL}	Input Voltage, Low	Single-ended operation	–1.945[10]	–1.625	V
V_{BB}[3]	Output Reference Voltage		–1.620	–1.220	V

AC Electrical Specifications

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
V_{PP}	Differential Input Voltage[8]	Differential operation	0.1		1.3	V
F_{CLK}	Input Frequency	50% duty cycle Standard load			1.5	GHz
T_{PD}	Propagation Delay CLKA or CLKB to Output pair	<660 MHz[11]	400	500	680	ps
V_O	Output Voltage (peak-to-peak; see *Figure 2*)	<1 GHz	0.375	–	–	V
V_{CMRO}	Output Common Voltage Range		–	–		V
$tsk_{(O)}$	Output-to-output Skew	<660 MHz[11], See *Figure 3*	–	–	50	ps
$tsk_{(PP)}$	Part-to-Part Output Skew[11]		–	50	150	ps
$t_{jit(per)}$	Output Period Jitter (peak)[12]	156.25 MHz[11]	–	7.6	15	ps
$t_{jit(pn)}$	Output RMS Phase Jitter[11, 12] (see *Figure 6*)	156.25 MHz, broadband, 3.3V	–	0.156	–	ps
		156.25 MHz, Filtered, 3.3V	–	0.134	–	ps
		312.5 MHz, broadband, 3.3V	–	0.275	–	ps
		312.5 MHz, Filtered, 3.3V	–	0.266	–	ps
$tsk_{(P)}$	Output Pulse Skew[13]	660 MHz[11], See *Figure 3*	–	–	35	ps
T_R,T_F	Output Rise/Fall Time (see *Figure 2*)	660 MHz 50% duty cycle Differential 20% to 80%	0.08	–	0.3	ns

Notes:
11. 50% duty cycle; standard load; differential operation.
12. For further information regarding jitter, please refer to the application note “Understanding data sheet jitter specifications for Cypress timing products”.
13. Output pulse skew is the absolute difference of the propagation delay times: $| t_{PLH} - t_{PHL} |$.

Timing Definitions

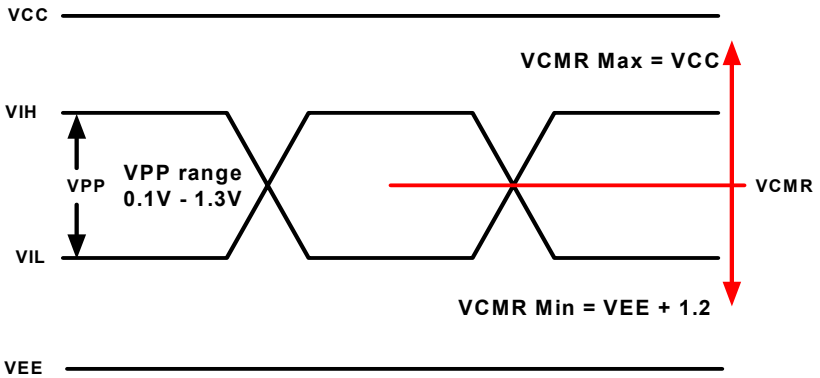


Figure 1. PECL/ECL Input Waveform Definitions

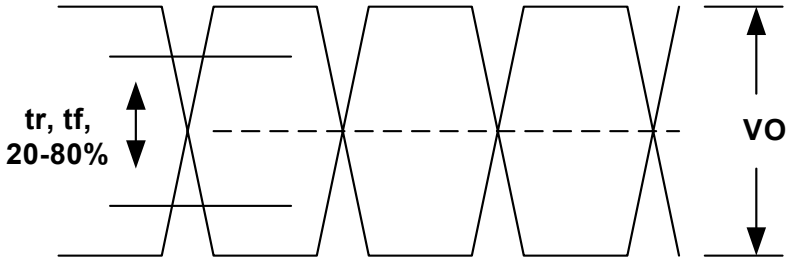


Figure 2. ECL/LVPECL Output

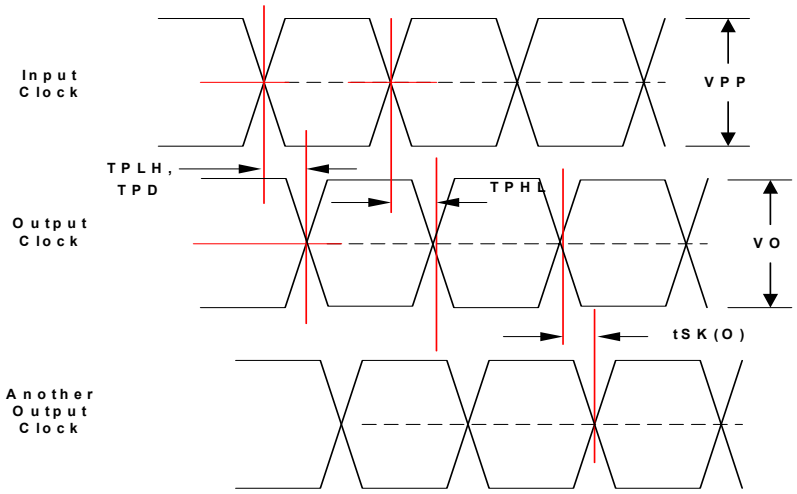


Figure 3. Propagation Delay (T_{PD}), output pulse skew ($|t_{PLH}-t_{PHL}|$), and output-to-output skew ($t_{SK(O)}$) for both CLKA or CLKB to Output Pair, PECL/ECL to PECL/ECL

Test Configuration

Standard test load using a differential pulse generator and differential measurement instrument.

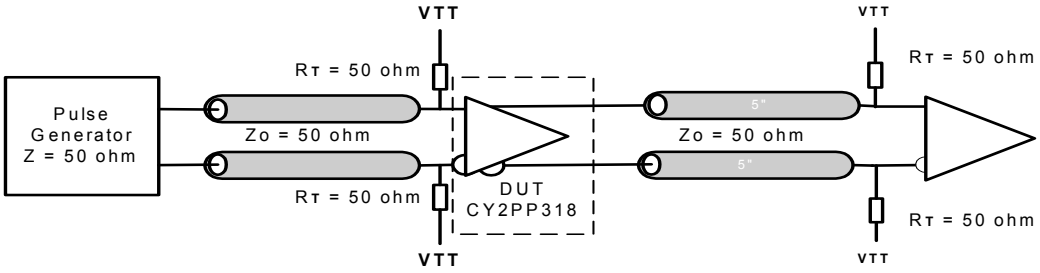


Figure 4. CY2PP318 AC Test Reference

Supplemental Parametric Information

RMS Phase Jitter: **0.134 ps typical @ 156.25 MHz, 10 GbE Filter (1.875 MHz – 20 MHz)**
0.156 ps typical @ 156.25 MHz, Broadband (Raw Data from 10 Hz – 20 MHz)

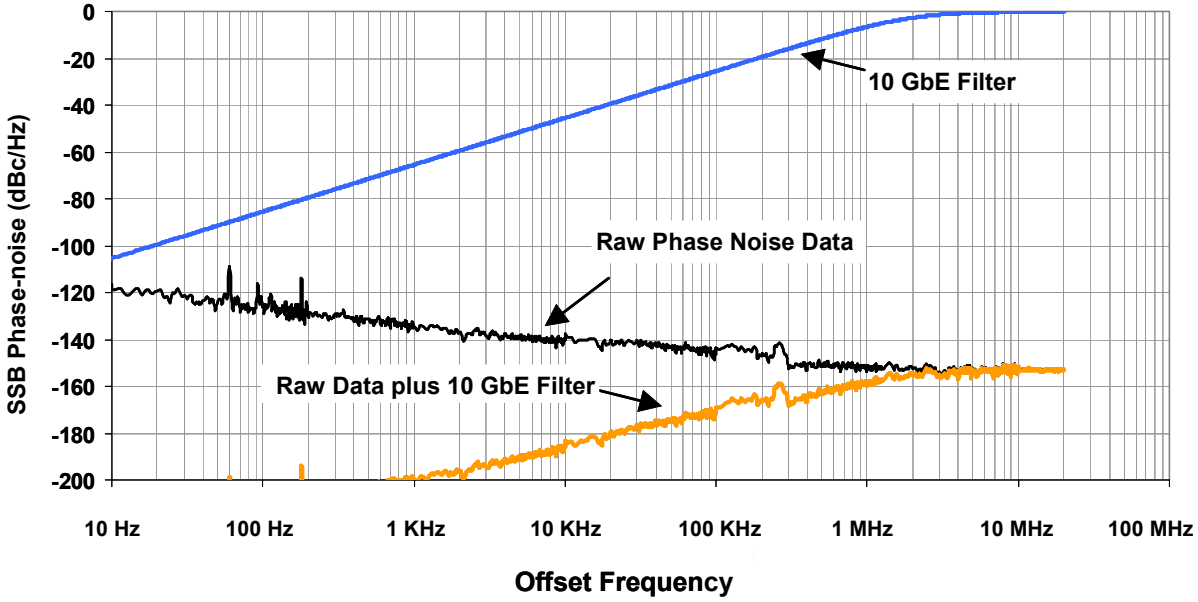


Figure 5. Typical Phase-noise Characteristics at 156.25 MHz, 3.3V, Room Temperature

Applications Information

Termination Examples

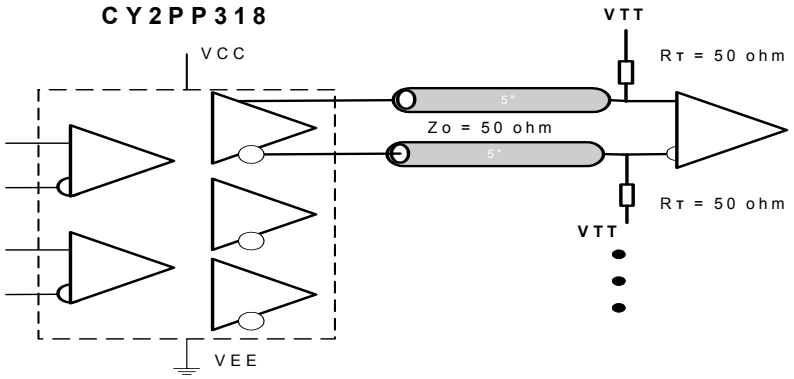


Figure 6. Standard LVPECL – PECL Output Termination

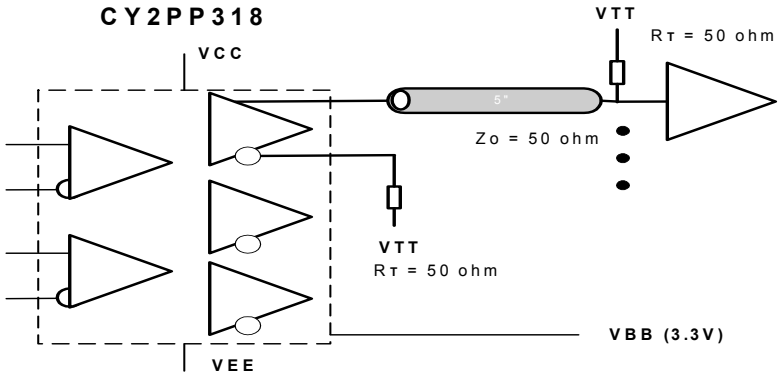


Figure 7. Driving a PECL/ECL Single-ended Input

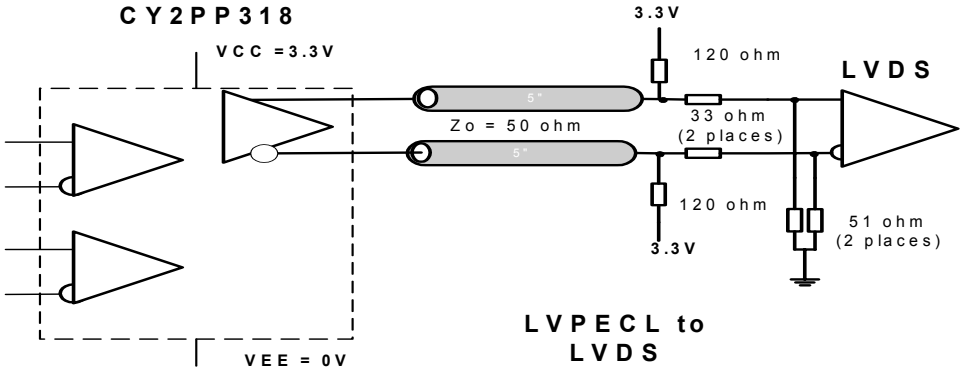


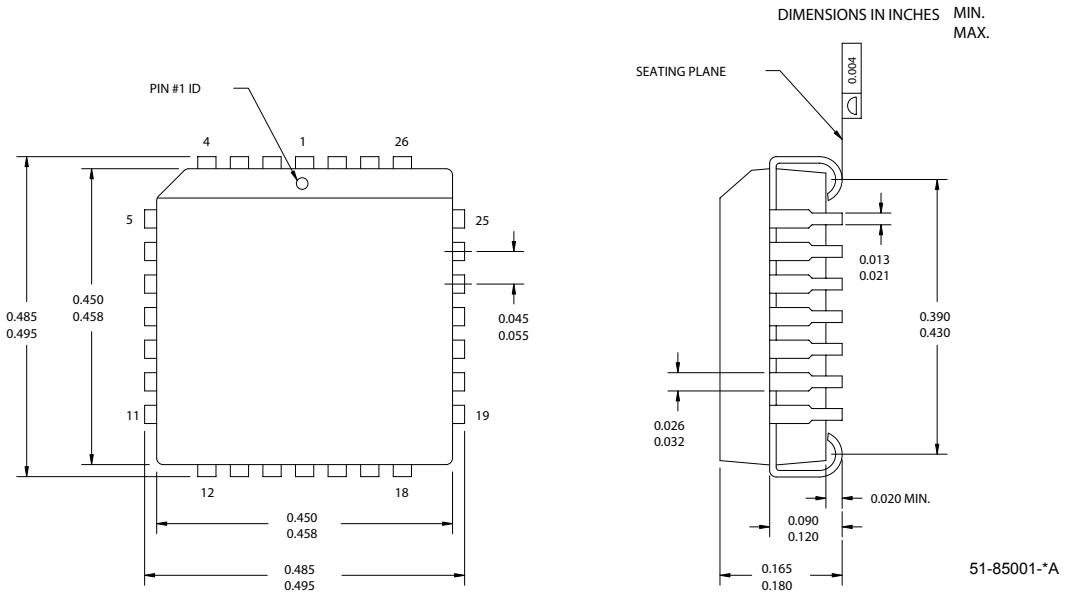
Figure 8. Low-voltage Positive Emitter-coupled Logic (LVPECL) to a Low-voltage Differential Signaling (LVDS) Interface

Ordering Information

Part Number	Package Type	Product Flow
CY2PP318JI	28-pin PLCC	Industrial, –40° to 85°C
CY2PP318JIT	28-pin PLCC – Tape and Reel	Industrial, –40° to 85°C

Package Drawing and Dimensions

28-Lead Plastic Leaded Chip Carrier J64



Document History Page

Document Title: CY2PP318 FastEdge™ Series 1:8 Differential Clock/Data Fanout Buffer Document Number: 38-07501				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	122041	02/13/03	RGL	New Data Sheet
*A	125923	06/11/03	RGL	Shifted the pin location Changed the title (ComLink to FastEdge) Corrected Specs that does not match EROS/IROS
*B	204240	See ECN	RGL	Change pin 1 from VCC to VCCO
*C	222602	See ECN	RGL	Changed the ECL and PECL mode ranges in the features section Specified tsk max value to 150ps Replaced I_{CC} calculation with power calculation in the footnote. Reformatted datasheet Revised jitter spec as period jitter (rms) Max operating frequency 1.5 GHz
*D	229352	See ECN	RGL	Added JEDEC Spec for MSL
*E	247624	See ECN	RGL/GGK	Changed V_{OH} and V_{OL} to match with the Char Data
*F	381820	See ECN	RGL/GGK	Updated Jitter Specs, Added typical information
*G	392938	See ECN	RGL	Added jitter to Features section