FastEdge™ Series
CY2PP3115

1:15 Differential Clock/Data Fanout Buffer

Features

- Fifteen ECL/PECL differential outputs grouped in four banks
- Two ECL/PECL differential inputs
- Selectable divide by two outputs
- Hot-swappable/-insertable
- 41 ps typical output-to-output skew
- 86 ps typical part-to-part skew
- 900 ps typical propagation delay
- 0.2 ps typical RMS phase jitter
- 9 ps typical peak period jitter
- 1.5 GHz operation
- PECL mode supply range: V_{CC} = 2.5V± 5% to 3.3V±5% with V_{EE} = 0V
- ECL mode supply range: V_{EE} = –2.5V± 5% to –3.3V±5% with V_{CC} = 0V
- Industrial temperature range: –40°C to 85°C
- 52-pin 1.4mm TQFP package
- Pin compatible with MC100ES6222

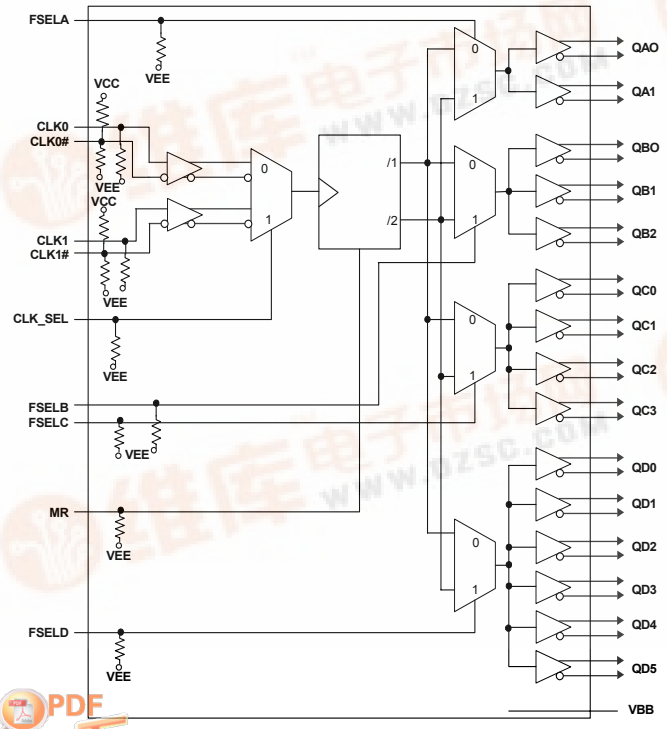
Functional Description

The CY2PP3115 is a low-skew, low propagation delay 1-to-15 differential fanout buffer targeted to meet the requirements of high-performance clock and data distribution applications. The device is implemented on SiGe technology and has a fully differential internal architecture that is optimized to achieve low signal skews at operating frequencies of up to 1.5 GHz.

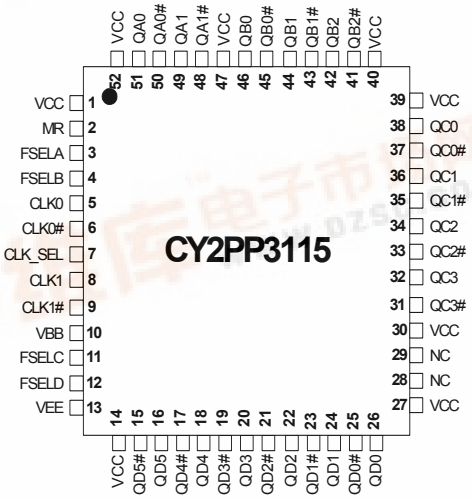
The device features two differential input paths that are multiplexed internally. This mux is controlled by the CLK_SEL pin. The CY2PP3115 may function not only as a differential clock buffer but also as a signal-level translator and fanout on ECL/PECL single-ended signal to 15 ECL/PECL differential loads. An external bias pin, VBB, is provided for this purpose. In such an application, the VBB pin should be connected to either one of the CLKA# or CLKB# inputs and bypassed to ground via a 0.01-µF capacitor.

Since the CY2PP3115 introduces negligible jitter to the timing budget, it is the ideal choice for distributing high frequency, high precision clocks across back-planes and boards in communication systems. Furthermore, advanced circuit design schemes, such as internal temperature compensation, ensure that the CY2PP3115 delivers consistent performance over various platforms.

Block Diagram



Pin Configuration



Pin Definitions[1, 2, 3]

Pin No.	Name	I/O	Type	Description
1,14,27,30,39,40,47,52	VCC	+PWR	POWER	Power Supply, positive connection
2	MR	I,PD	ECL/PECL	Reset
3,4,11,12	FSEL(A,B,C,D)	I,PD	ECL/PECL	Output Divider Selects
5,8	CLK(0:1)	I,PD	ECL/PECL	Differential Clock Inputs – TRUE
6,9	CLK(0:1)#	I,PD/PU	ECL/PECL	Differential Clock Inputs – COMPLEMENT
10	VBB	O	Bias	Reference Voltage Output
13	VEE	–PWR	POWER	Power Supply, Negative Connection
28,29	NC			No Connect. Pad Only
7	CLK_SEL	I,PD	ECL/PECL	Clock Input Select
26,24,22,20,18,16	QD(0:5)	O	ECL/PECL	Bank D True Output
25,23,21,19,17,15	QD(0:5)#	O	ECL/PECL	Bank D Complement Output
38,36,34,32	QC(0:3)	O	ECL/PECL	Bank C True Output
37,35,33,31	QC(0:3)#	O	ECL/PECL	Bank C Complement Output
46,44,42	QB(0:2)	O	ECL/PECL	Bank B True Output
45,43,41	QB(0:2)#	O	ECL/PECL	Bank B Complement Output
51,49	QA(0:1)	O	ECL/PECL	Bank A True Output
50,48	QA(0:1)#	O	ECL/PECL	Bank A Complement Output

Table 1. Function Table

Control Pin	0	1
FSELA (Asynchronous)	÷1	÷2
FSELB (Asynchronous)	÷1	÷2
FSELC (Asynchronous)	÷1	÷2
FSELD (Asynchronous)	÷1	÷2
CLK_SEL (Asynchronous)	CLK0	CLK1
MR (Asynchronous)	Active	Reset (QX = L and QX# = H)

Governing Agencies

The following agencies provide specifications that apply to the CY2PP3115. The agency name and relevant specification is listed below in *Table 2*.

Table 2.

Agency Name	Specification
JEDEC	JESD 51 (Theta JA) JESD 8–2 (ECL) JESD 65–B (skew,jitter)
Mil-Spec	883E Method 1012.1 (Thermal Theta JC)

Notes:
1. In the I/O column, the following notation is used: I for Input, O for Output, PD for Pull-Down, PU for Pull-Up, and PWR for Power.
2. In ECL mode (negative power supply mode), V_{EE} is either –3.3V or –2.5V and V_{CC} is connected to GND (0V). In PECL mode (positive power supply mode), V_{EE} is connected to GND (0V) and V_{CC} is either +3.3V or +2.5V. In both modes, the input and output levels are referenced to the most positive supply (V_{CC}) and are between V_{CC} and V_{EE}.
3. V_{BB} is available for use for single-ended bias mode when V_{CC} is +3.3V.

Absolute Maximum Ratings

Parameter	Description	Condition	Min.	Max.	Unit
V_{CC}	Positive Supply Voltage	Non-Functional	–0.3	4.6	V
V_{EE}	Negative Supply Voltage	Non-Functional	–4.6	0.3	V
T_S	Temperature, Storage	Non-Functional	–65	+150	°C
T_J	Temperature, Junction	Non-Functional		150	°C
ESD_h	ESD Protection	Human Body Model	2000		V
M_{SL}	Moisture Sensitivity Level		3		N.A.
Gate Count	Total Number of Used Gates	Assembled Die	50		gates

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

Operating Conditions

Parameter	Description	Condition	Min.	Max.	Unit
I_{BB}	Output Reference Current	Relative to V_{BB}		|200|	µA
LU_I	Latch Up Immunity	Functional, typical	100		mA
T_A	Temperature, Operating Ambient	Functional	–40	+85	°C
$Ø_{Jc}$	Dissipation, Junction to Case	Functional	22[4]		°C/W
$Ø_{Ja}$	Dissipation, Junction to Ambient	Functional	54[4]		°C/W
I_{EE}	Maximum Quiescent Supply Current	V_{EE} pin		200[5]	mA
C_{IN}	Input pin capacitance			3	pF
L_{IN}	Pin Inductance			1	nH
V_{IN}	Input Voltage	Relative to V_{CC}[6]	–0.3	V_{CC} + 0.3	V
V_{BB}[3]	Output Reference Voltage	Relative to V_{CC}[6]	V_{CC} – 1.620	V_{CC} – 1.220	V
V_{TT}	Output Termination Voltage	Relative to V_{CC}[6]	V_{CC} – 2		V
V_{OUT}	Output Voltage	Relative to V_{CC}[6]	–0.3	V_{CC} + 0.3	V
I_{IN}	Input Current[7]	$V_{IN} = V_{IL}$, or $V_{IN} = V_{IH}$		I150I	µA

PECL DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
V_{CC}	Operating Voltage	2.5V ± 5%, V_{EE} = 0.0V 3.3V ± 5%, V_{EE} = 0.0V	2.375 3.135	2.625 3.465	V V
V_{CMR}	Differential Cross Point Voltage[8]	Differential operation	1.2	V_{CC}	V
V_{OH}	Output High Voltage	I_{OH} = –30 mA[9]	V_{CC} – 1.25	V_{CC} – 0.7	V
V_{OL}	Output Low Voltage V_{CC} = 3.3V ± 5% V_{CC} = 2.5V ± 5%	I_{OL} = –5 mA[9]	 V_{CC} – 1.995 V_{CC} –1.995	 V_{CC} – 1.5 V_{CC} – 1.3	 V V
V_{IH}	Input Voltage, High	Single-ended operation	V_{CC} – 1.165	V_{CC} – 0.880[10]	V
V_{IL}	Input Voltage, Low	Single-ended operation	V_{CC} – 1.945[10]	V_{CC} – 1.625	V

Notes:
4. Theta JA EIA JEDEC 51 test board conditions (typical value); Theta JC 883E Method 1012.1
5. Power Calculation: $V_{CC} * I_{EE} + 0.5 (I_{OH} + I_{OL}) (V_{OH} – V_{OL})$ (number of differential outputs used); I_{EE} does not include current going off chip.
6. where V_{CC} is 3.3V±5% or 2.5V±5%
7. Inputs have internal pull-up/pull-down or biasing resistors which affect the input current.
8. Refer to *Figure 1*.
9. Equivalent to a termination of 50Ω to VTT. $I_{OHMIN} = (V_{OHMIN} – V_{TT})/50$; $I_{OHMAX} = (V_{OHMAX} – V_{TT})/50$; $I_{OLMIN} = (V_{OLMIN} – V_{TT})/50$; $I_{OLMAX} = (V_{OLMAX} – V_{TT})/50$;
10. V_{IL} will operate down to V_{EE}; V_{IH} will operate up to V_{CC}.

ECL DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
V_{EE}	Negative Power Supply	–2.5V ± 5%, V_{CC} = 0.0V –3.3V ± 5%, V_{CC} = 0.0V	–2.625 –3.465	–2.375 –3.135	V
V_{CMR}	Differential cross point voltage[8]	Differential operation	V_{EE} + 1.2	0V	V
V_{OH}	Output High Voltage	I_{OH} = –30 mA[9]	–1.25	–0.7	V
V_{OL}	Output Low Voltage V_{EE} = –3.3V ± 5% V_{EE} = –2.5V ± 5%	I_{OL} = –5 mA[9]	 –1.995 –1.995	 –1.5 –1.3	V
V_{IH}	Input Voltage, High	Single-ended operation	–1.165	–0.880[10]	V
V_{IL}	Input Voltage, Low	Single-ended operation	–1.945[10]	–1.625	V

AC Electrical Specifications

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
V_{PP}	Differential Input Voltage[8]	Differential operation	0.1	–	1.3	V
F_{CLK}	Input Frequency	50% duty cycle standard load		–	1.5	GHz
T_{PD}	Propagation Delay CLKA or CLKB to Output pair	< 1 GHz[11]	–	900	1200	ps
Vo	Output Voltage (peak-to-peak; see *Figure 2*)	< 1 GHz	0.375	–	–	V
V_{CMRO}	Output Common Voltage Range (typical)		–	V_{CC} – 1.425	–	V
$tsk_{(0)}$	Output-to-output Skew	<660 MHz[11], see *Figure 3*	–	41	60	ps
$tsk_{(PP)}$	Part-to-Part Output Skew[11]		–	86	150	ps
$t_{jit(per)}$	Output Period Jitter (peak)[12]	156.25 MHz[11]	–	9	20	ps
$t_{jit(pn)}$	Output RMS Phase Jitter[12] (see *Figure 5*)	156.25 MHz, broadband, 3.3V	–	0.285	–	ps
		156.25 MHz, Filtered, 3.3V	–	0.254	–	ps
		312.5 MHz, broadband, 3.3V	–	0.198	–	ps
		312.5 MHz, Filtered, 3.3V	–	0.184	–	ps
$tsk_{(P)}$	Output Pulse Skew[13]	660 MHz[11], see *Figure 3*	–	–	75	ps
T_R,T_F	Output Rise/Fall Time (see *Figure 2*)[11]		0.08	–	0.3	ns

Timing Definitions

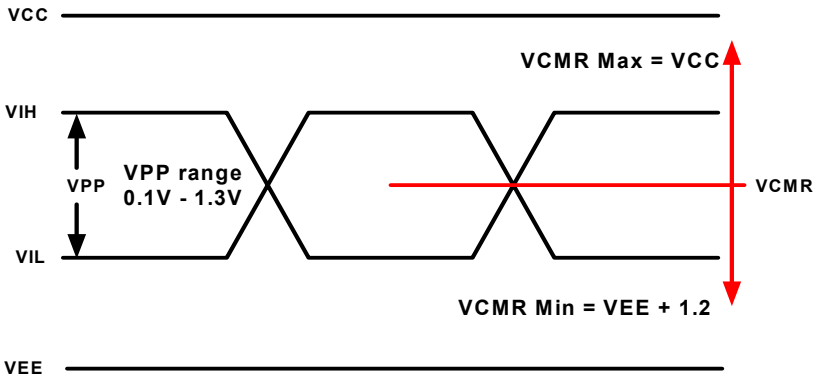


Figure 1. PECL/ECL Input Waveform Definitions

Notes:
11. 50% duty cycle; standard load; differential operation
12. For further information regarding jitter, please refer to the application note “Understanding data sheet jitter specifications for Cypress timing products”.
13. Output pulse skew is the absolute difference of the propagation delay times: $| t_{PLH} – t_{PHL} |$.

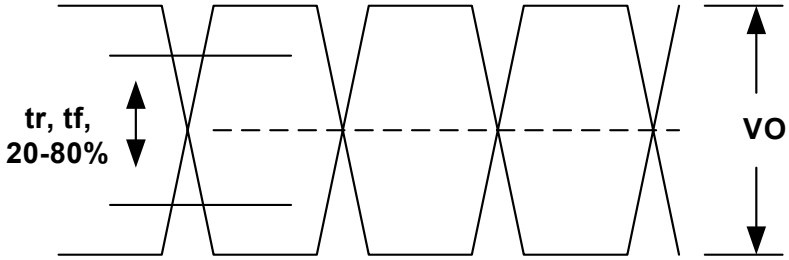


Figure 2. ECL/LVPECL Output

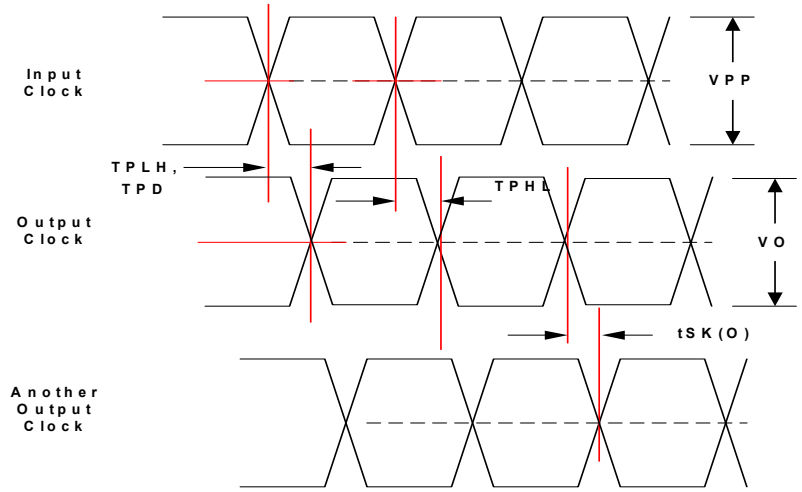


Figure 3. Propagation Delay (T_{PD}), Output Pulse Skew ($|t_{PLH}-t_{PHL}|$), and Output-to-Output Skew ($t_{SK(O)}$) for both CLKA or CLKB to Output Pair, PECL/ECL to PECL/ECL

Test Configuration

Standard test load using a differential pulse generator and differential measurement instrument.

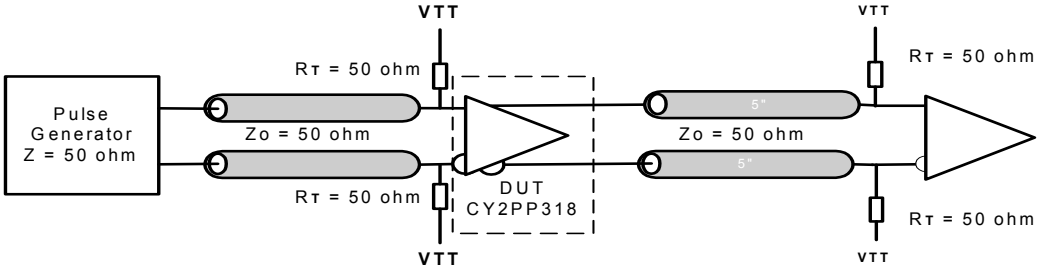


Figure 4. CY2PP3115 AC Test Reference

Supplemental Parametric Information

RMS Phase Jitter: 0.254 ps typical @ 156.25 MHz, 10 GbE Filter (1.875 MHz – 20 MHz)
0.285 ps typical @ 156.25 MHz, Broadband (Raw Data from 10 Hz – 20 MHz)

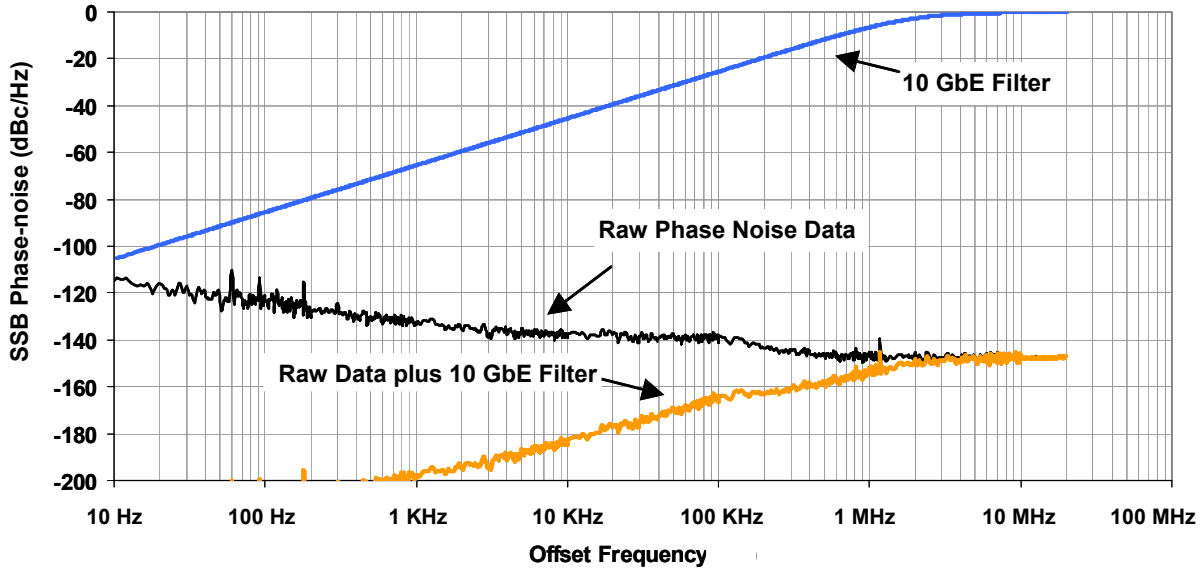


Figure 5. Typical Phase-noise Characteristics at 156.25 MHz, 3.3V, Room Temperature

Applications Information

Termination Examples

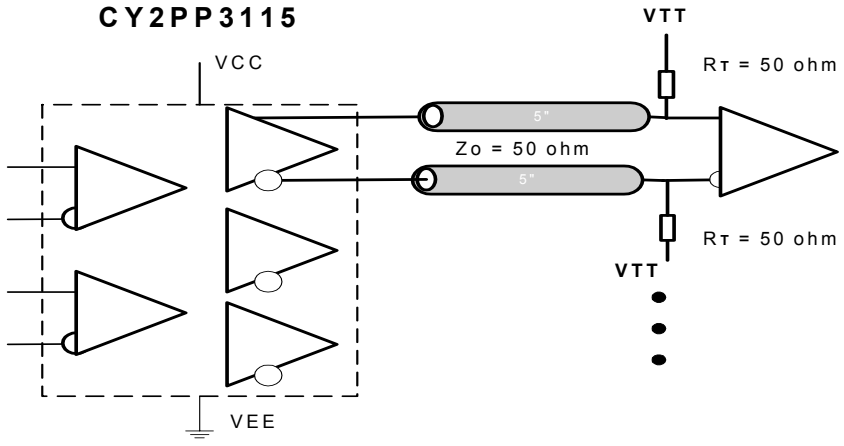


Figure 6. Standard LVPECL – PECL Output Termination

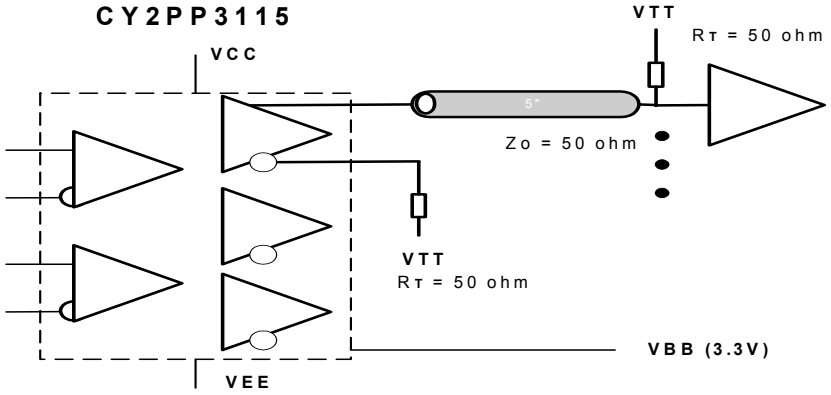


Figure 7. Driving a PECL/ECL Single-ended Input

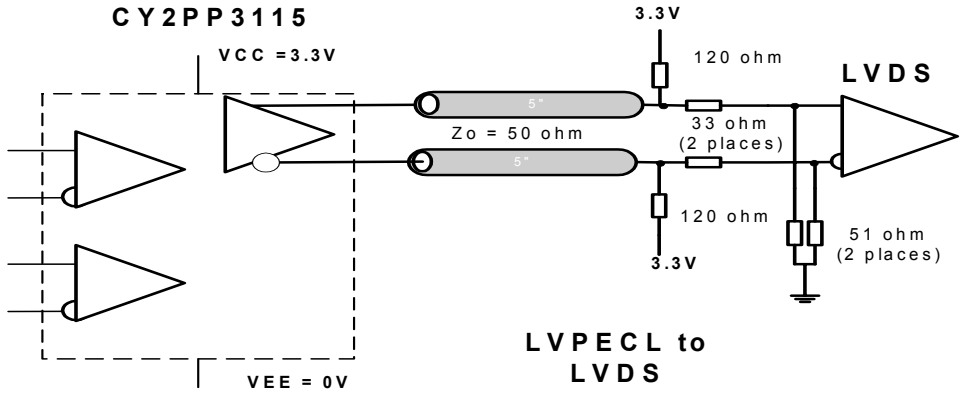
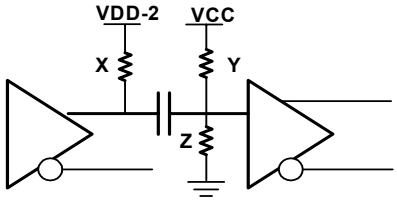


Figure 8. Low-voltage Positive Emitter-coupled Logic (LVPECL) to a Low-voltage Differential Signaling (LVDS) Interface



One output is shown for clarity

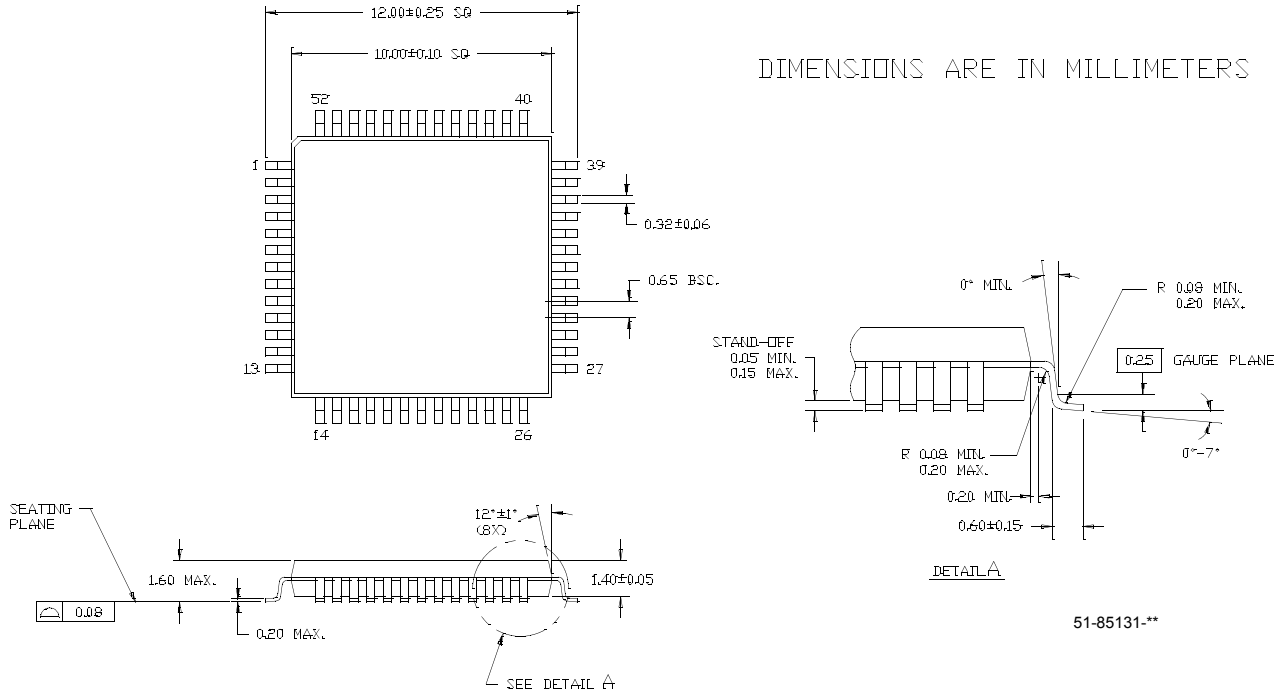
Figure 9. Termination for LVPECL to HTSL Interface for V_{CC} = 2.5V would use X = 50 Ohms, Y = 2300 Ohms, and Z = 1000 Ohms. See application note titled, "PECL Translation, SAW Oscillators, and Specs" for other signaling standards and supplies.

Ordering Information

Part Number	Package Type	Product Flow
CY2PP3115AI	52-Pin TQFP	Industrial, –40° to 85°C
CY2PP3115AIT	52-Pin TQFP – Tape and Reel	Industrial, –40° to 85°C
Lead-free		
CY2PP3115AXI	52-Pin TQFP	Industrial, –40° to 85°C
CY2PP3115AXIT	52-Pin TQFP – Tape and Reel	Industrial, –40° to 85°C

Package Drawing and Dimensions

52-Lead Thin Plastic Quad Flat Pack (10x10x1.4 mm) A52



Document History Page

Document Title: CY2PP3115 FastEdge™ Series 1:15 Differential Clock/Data Fanout Buffer Document Number: 38-07502				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	122042	02/12/03	RGL	New Data Sheet
*A	131090	11/21/03	RGL	Supplied numbers for all specs with TBD after characterization
*B	235909	See ECN	RGL	Updated AC Specs to agree with char report
*C	247619	See ECN	RGL/GGK	Changed V_{OH} and V_{OL} to match the Char Data
*D	380381	See ECN	RGL	Updated Jitter specs Changed single-ended inputs to ECL/PECL Added Lead-free devices
*E	393409	See ECN	RGL	Corrected the jitter specs