FastEdge™ Series
CY2DP3120

1:20 Differential Clock/Data Fanout Buffer

Features

- Twenty ECL/PECL differential outputs
- One ECL/PECL compatible differential or single-ended clock inputs
- One HSTL compatible differential or single-ended clock inputs
- Hot-swappable/-insertable
- 50 ps output-to-output skew
- 150 ps device-to-device skew
- 500 ps propagation delay (typical)
- 1.4 ps RMS period jitter (max.)
- 1.5 GHz Operation (2.7 GHz max. toggle frequency)
- PECL mode supply range: V_{CC} = 2.5V± 5% to 3.3V±5% with V_{EE} = 0V
- ECL mode supply range: V_{EE} = –2.5V± 5% to –3.3V±5% with V_{CC} = 0V
- Industrial temperature range: –40°C to 85°C
- 52-pin 1.4-mm TQFP package
- Temperature compensation like 100K ECL
- Pin compatible with MC100ES6221

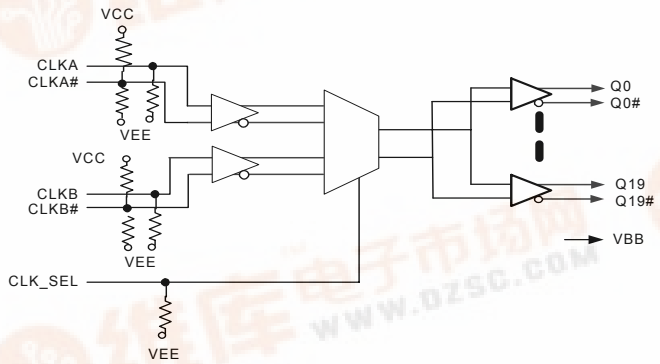
Functional Description

The CY2DP3120 is a low-skew, low propagation delay 1-to-20 differential fanout buffer targeted to meet the requirements of high-performance clock and data distribution applications. The device is implemented on SiGe technology and has a fully differential internal architecture that is optimized to achieve low signal skews at operating frequencies of up to 1.5 GHz.

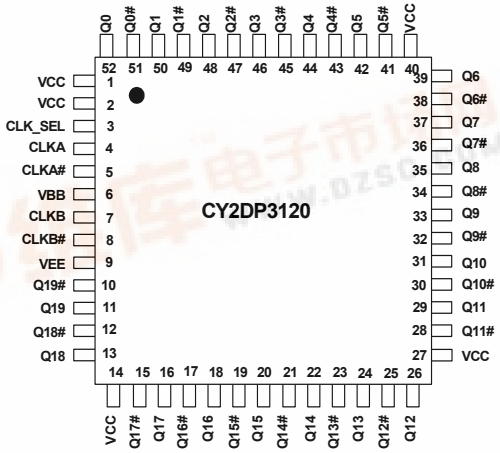
The device features two differential input paths that are multiplexed internally. This mux is controlled by the CLK_SEL pin. The CY2DP3120 may function not only as a differential clock buffer but also as a signal-level translator and fanout on ECL/PECL signal to twenty ECL/PECL differential loads. An external bias pin, VBB, is provided for this purpose. In such an application, the VBB pin should be connected to either one of the CLKA# or CLKB# inputs and bypassed to ground via a 0.01-µF capacitor. Traditionally, in ECL, it is used to provide the reference level to a receiving single-ended input that might have a different self-bias point.

Since the CY2DP3120 introduces negligible jitter to the timing budget, it is the ideal choice for distributing high frequency, high precision clocks across back-planes and boards in communication systems. Furthermore, advanced circuit design schemes, such as internal temperature compensation, ensure that the CY2DP3120 delivers consistent performance over various platforms.

Block Diagram



Pin Configuration



Pin Definitions[1, 2, 3]

Pin	Name	I/O	Type	Description
3	CLK_SEL	I,PD	ECL/PECL/HSTL	**Input clock select**
4	CLKA,	I,PD	ECL/PECL	**Differential input clocks**
6	VBB[3]	O	Bias	**Reference voltage output**
5	CLKA#	I,PD/PU	ECL/PECL	**Differential input clocks**
7	CLKB,	I,PD	HSTL	**Alternate differential input clocks**
8	CLKB#	I,PD/PU	HSTL	**Alternate differential input clocks**
9	VEE[2]	-PWR	Power	**Negative supply**
1,2,14,27,40	VCC	+PWR	Power	**Positive Supply**
52,50,48,46,44,42,39,37, 35,33,31,29,26,24,22,20, 18,16,13,11	Q(0:19)	O	ECL/PECL	**True output**
51,49,47,45,43,41,38,36, 34,32,30,28,25,23,21,19, 17,15,12,10	Q#(0:19)	O	ECL/PECL	**Complement output**

Table 1.

Control	Operation
CLK_SEL	
0	CLKA, CLKA# input pair is active (Default condition with no connection to pin) CLKA can be driven with ECL- or PECL-compatible signals with respective power configurations
1	CLKB, CLKB# input pair is active. CLKB can be driven with HSTL-compatible signals with respective power configurations

Governing Agencies

The following agencies provide specifications that apply to the CY2DP3120. The agency name and relevant specification is listed below in *Table 2*.

Table 2.

Agency Name	Specification
JEDEC	JESD 020B (MSL) JESD 51 (Theta JA) JESD 8–2 (ECL) JESD 65–B (skew,jitter)
Mil-Spec	883E Method 1012.1 (Thermal Theta JC)

Notes:
1. In the I/O column, the following notation is used: I for Input, O for Output, PD for Pull-Down, PU for Pull-Up, and PWR for Power
2. In ECL mode (negative power supply mode), V_{EE} is either –3.3V or –2.5V and V_{CC} is connected to GND (0V). In PECL mode (positive power supply mode), V_{EE} is connected to GND (0V) and V_{CC} is either +3.3V or +2.5V. In both modes, the input and output levels are referenced to the most positive supply (V_{CC}) and are between V_{CC} and V_{EE}.
3. V_{BB} is available for use for single-ended bias mode for |3.3V| supplies (not |2.5V|).

Absolute Maximum Ratings

Parameter	Description	Condition	Min.	Max.	Unit
V_{CC}	Positive Supply Voltage	Non-Functional	–0.3	4.6	V
V_{EE}	Negative Supply Voltage	Non-Functional	-4.6	0.3	V
T_S	Temperature, Storage	Non-Functional	–65	+150	°C
T_J	Temperature, Junction	Non-Functional		150	°C
ESD_h	ESD Protection	Human Body Model	2000		V
M_{SL}	Moisture Sensitivity Level		3		N.A.
Gate Count	Total Number of Used Gates	Assembled Die	50		gates

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

Operating Conditions

Parameter	Description	Condition	Min.	Max.	Unit
I_{BB}	Output Reference Current	Relative to V_{BB}		|200|	uA
LU_I	Latch Up Immunity	Functional, typical	100		mA
T_A	Temperature, Operating Ambient	Functional	–40	+85	°C
$Ø_{Jc}$	Dissipation, Junction to Case	Functional	22[4]		°C/W
$Ø_{Ja}$	Dissipation, Junction to Ambient	Functional	60[4]		°C/W
I_{EE}	Maximum Quiescent Supply Current	V_{EE} pin		250[5]	mA
C_{IN}	Input pin capacitance			3	pF
L_{IN}	Pin Inductance			1	nH
V_{IN}	Input Voltage	Relative to V_{CC}[6]	–0.3	V_{CC} + 0.3	V
V_{TT}	Output Termination Voltage	Relative to V_{CC}[6]	V_{CC} – 2		V
V_{OUT}	Output Voltage	Relative to V_{CC}[6]	–0.3	V_{CC} + 0.3	V
I_{IN}	Input Current (ECL,PECL and HSTL)[7]	$V_{IN} = V_{IL}$, or $V_{IN} = V_{IH}$		I150I	uA

PECL/HSTL DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
V_{CC}	Operating Voltage	2.5V ± 5%, V_{EE} = 0.0V 3.3V ± 5%, V_{EE} = 0.0V	2.375 3.135	2.625 3.465	V V
V_{CMR}	PECL Input Differential Crosspoint Voltage[8]	Differential operation	1.2	V_{CC}	V
V_X	HSTL Input Differential Crosspoint Voltage[9]	Standard Load Differential Operation	0.68	0.9	V
V_{OH}	Output High Voltage	I_{OH} = –30 mA[10]	V_{CC} – 1.25	V_{CC} – 0.7	V
V_{OL}	Output Low Voltage V_{CC} = 3.3V ± 5% V_{CC} = 2.5V ± 5%	I_{OL} = –5 mA[10]	 V_{CC} – 1.995 V_{CC} –1.995	 V_{CC} – 1.5 V_{CC} – 1.3	 V V
V_{IH}	Input Voltage, High	Single-ended operation	V_{CC} – 1.165	V_{CC} – 0.880 [11]	V
V_{IL}	Input Voltage, Low	Single-ended operation	V_{CC} – 1.945 [11]	V_{CC} – 1.625	V
V_{BB}[3]	Output Reference Voltage	Relative to V_{CC}[6]	V_{CC} – 1.620	V_{CC} – 1.220	V

Notes:
4. Theta JA EIA JEDEC 51 test board conditions (typical value); Theta JC 883E Method 1012.1
5. Power Calculation: V_{CC} * I_{EE} +0.5 (I_{OH} + I_{OL}) (V_{OH} – V_{OL}) (number of differential outputs used); I_{EE} does not include current going off chip.
6. where V_{CC} is 3.3V±5% or 2.5V±5%
7. Inputs have internal pull-up/pull-down or biasing resistors which affect the input current.
8. Refer to Figure 1
9. V_X(AC) is the crosspoint of the differential HSTL input signal. Normal AC operation is obtained when the crosspoint is within the V_X(AC) range and the input swing lies within the V_{DIF}(AC) specification. Violation of V_X(AC) or V_{DIF}(AC) impacts the device propagation delay, device and part-to-part skew. Refer to Fig. 2.
10. Equivalent to a termination of 50Ω to VTT. I_{OHMIN}=(V_{OHMIN}-V_{TT})/50; I_{OHMAX}=(V_{OHMAX}-V_{TT})/50; I_{OLMIN}=(V_{OLMIN}-V_{TT})/50; I_{OLMAX}=(V_{OLMAX}-V_{TT})/50;
11. V_{IL} will operate down to V_{EE}; V_{IH} will operate up to V_{CC}

ECL DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
V_{EE}	Negative Power Supply	–2.5V ± 5%, V_{CC} = 0.0V –3.3V ± 5%, V_{CC} = 0.0V	–2.625 –3.465	–2.375 –3.135	V
V_{CMR}	ECL Input Differential cross point voltage[8]	Differential operation	V_{EE} + 1.2	0V	V
V_{OH}	Output High Voltage	I_{OH} = –30 mA[10]	–1.25	–0.7	V
V_{OL}	Output Low Voltage V_{EE} = –3.3V ± 5% V_{EE} = –2.5V ± 5%	I_{OL} = –5 mA[10]	 –1.995 –1.995	 –1.5 –1.3	V
V_{IH}	Input Voltage, High	Single-ended operation	–1.165	–0.880 [11]	V
V_{IL}	Input Voltage, Low	Single-ended operation	–1.945 [11]	–1.625	V
V_{BB}[3]	Output Reference Voltage		– 1.620	– 1.220	V

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
V_{PP}	ECL/PECL Differential Input Voltage[8]	Differential operation	0.1	1.3	V
F_{CLK}	Input Frequency	50% duty cycle Standard load		1.5	GHz
T_{PD}	Propagation Delay CLKA or CLKB to Output pair	660 MHz [13]	400	750	ps
V_{DIF}	HSTL Differential Input Voltage[12]	Duty Cycle Standard Load Differential Operation	0.4	1.9	V
Vo	Output Voltage (peak-to-peak; see *Figure 3*)	< 1 GHz	0.375	–	V
V_{CMRO}	Output Common Voltage Range (typical)		V_{CC} – 1.425		V
$tsk_{(0)}$	Output-to-output Skew	660 MHz [13], See Figure 3	–	50	ps
$tsk_{(PP)}$	Part-to-Part Output Skew	660 MHz [13]	–	150	ps
T_{PER}	Output Period Jitter (rms)[14]	660 MHz [13]	–	1.4	ps
$tsk_{(P)}$	Output Pulse Skew[]	660 MHz [13], See Figure 3	–	50	ps
T_R,T_F	Output Rise/Fall Time (see *Figure 3*)	660 MHz 50% duty cycle Differential 20% to 80%	0.08	0.3	ns

Notes:

12. V_{DIF} (AC) is the minimum differential HSTL input voltage swing required to maintain AC characteristics including tkpd and device-to-device skew
13. 50% duty cycle; standard load; differential operation
14. For 3.3V supplies. Jitter measured differentially using an Agilent 8133A Pulse Generator with an 8500A LeCroy Wavemaster Oscilloscope using at least 10,000 data points

Output pulse skew is the absolute difference of the propagation delay times: $| t_{PLH} – t_{PHL} |$.

Timing Definitions

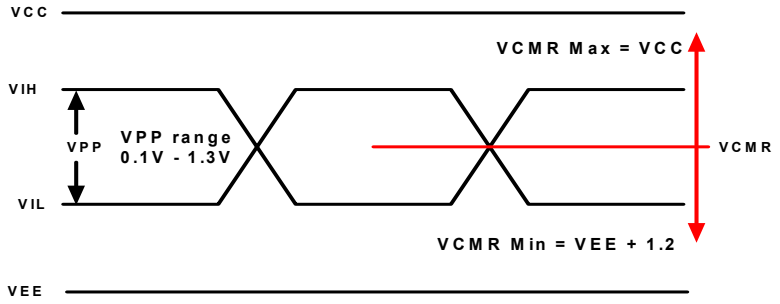


Figure 1. PECL/ECL Input Waveform Definitions

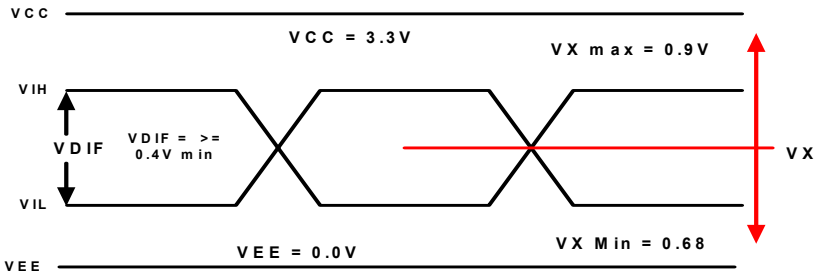


Figure 2. HSTL Differential Input Waveform Definitions

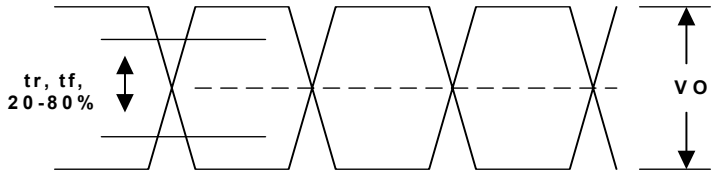


Figure 3. ECL/LVPECL Output

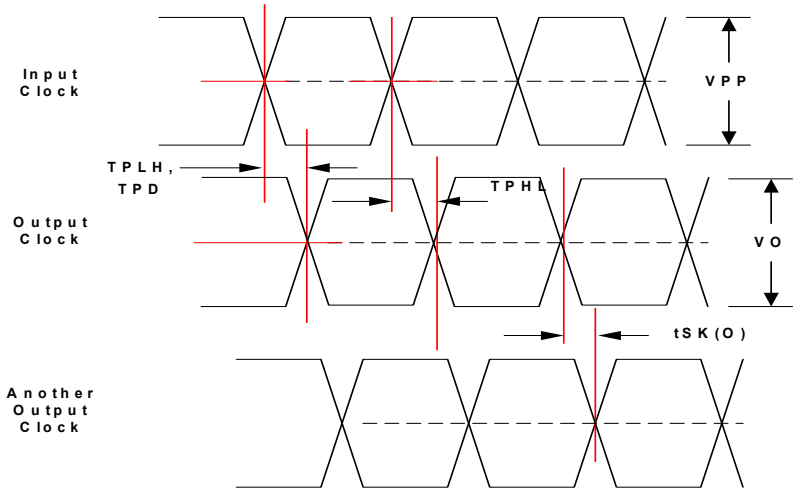


Figure 4. Propagation Delay (T_{PD}), output pulse skew ($|t_{PLH}-t_{PHL}|$), and output-to-output skew ($t_{SK(O)}$) for both CLKA or CLKB to Output Pair, PECL/ECL to PECL/ECL

Test Configuration

Standard test load using a differential pulse generator and differential measurement instrument.

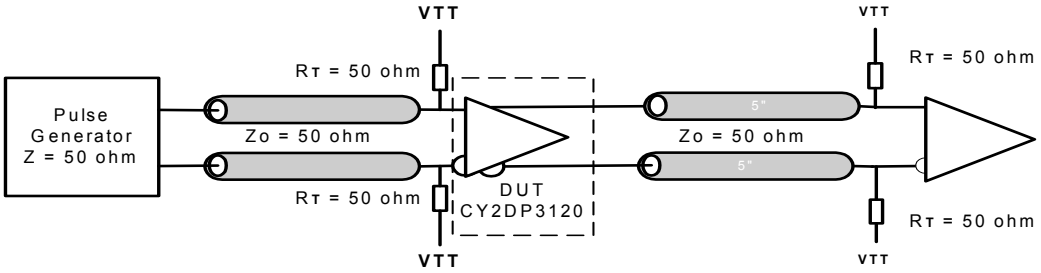


Figure 5. CY2DP3120 AC Test Reference

Applications Information

Termination Examples

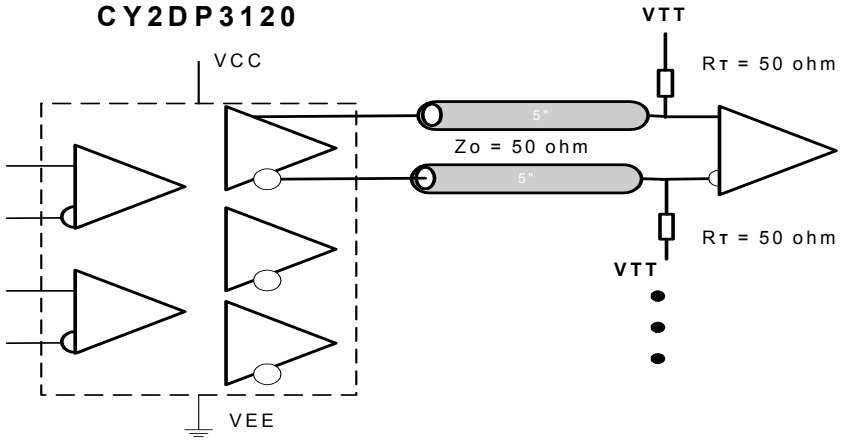


Figure 6. Standard LVPECL – PECL Output Termination

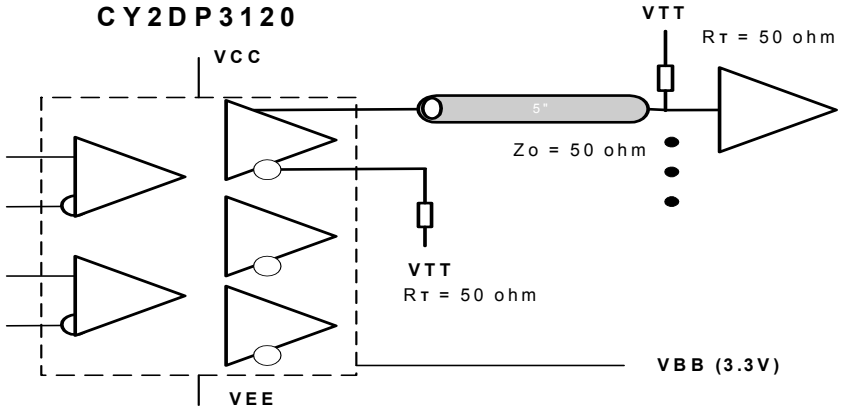


Figure 7. Driving a PECL/ECL Single-ended Input

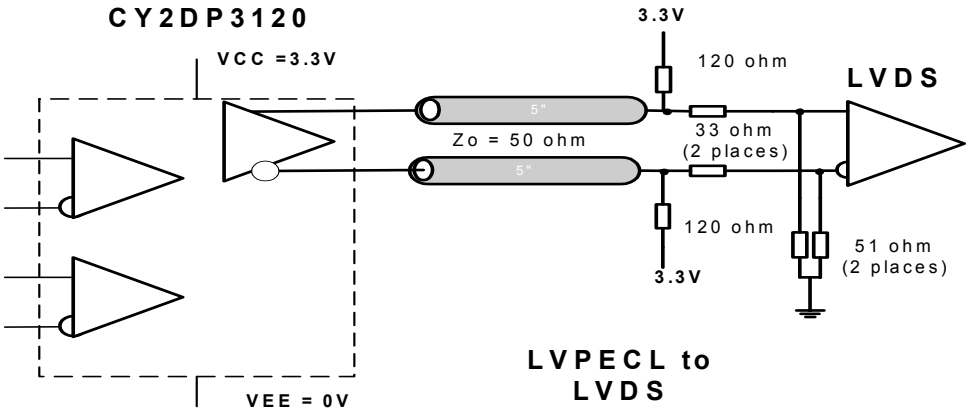
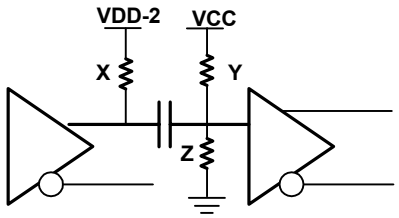


Figure 8. Low-voltage Positive Emitter-coupled Logic (LVPECL) to a Low-voltage Differential Signaling (LVDS) Interface



One output is shown for clarity

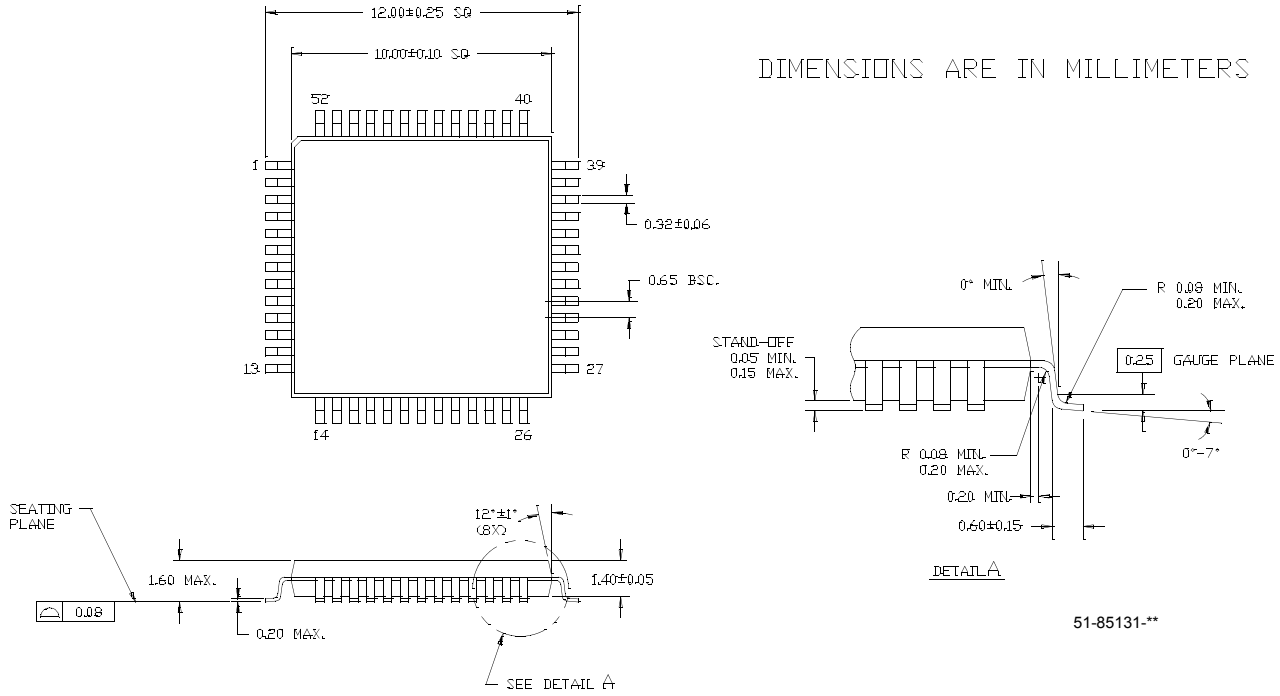
Figure 9. Termination for LVPECL to HTSL interface for VCC=2.5V would use X=50 Ohms, Y=2300 Ohms, and Z=1000 Ohms. See application note titled, "PECL Translation, SAW Oscillators, and Specs" for other signalling standards and supplies.

Ordering Information

Part Number	Package Type	Product Flow
CY2DP3120AI	52-pin TQFP	Industrial, –40° to 85°C
CY2DP3120AIT	52-pin TQFP – Tape and Reel	Industrial, –40° to 85°C
CY2DP3120AXI	52-pin TQFP - Lead Free	Industrial, –40° to 85°C
CY2DP3120AXIT	52-pin TQFP – Tape and Reel - Lead Free	Industrial, –40° to 85°C

Package Diagram

52-lead Thin Plastic Quad Flat Pack (10 × 10 × 1.4 mm) A52



Document History Page

Document Title: CY2DP3120 FastEdge™ Series 1:20 Differential Clock/Data Fanout Buffer Document Number: 38-07514				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	122438	12/05/02	RGL	New data sheet
*A	125457	04/17/03	RGL	Corrected typo Q14 to Q4 in pin 44 in the pin configuration diagram Changed pin #s 1,14,27 and 40 from VCC to VCCO Changed title to FastEdge™ Series 1:20 Differential Clock/Data Fanout Buffer
*B	229391	See ECN	RGL	Supplied data to all TBD's to match the device
*C	247606	See ECN	RGL/GGK	Changed V_{OH} and V_{OL} to match the Char Data