CY29943

2.5V or 3.3V 200-MHz 1:18 Clock Distribution Buffer

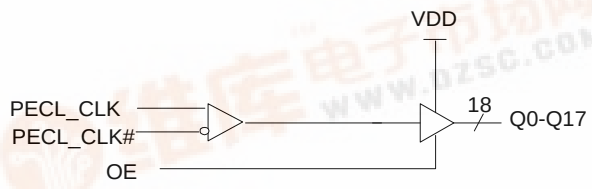
Features

- **200-MHz clock support**
- **2.5V or 3.3V operation**
- **LVPECL clock input**
- **LVCMOS-/LVTTL-compatible inputs**
- **18 clock outputs: drive up to 36 clock lines**
- **200 ps max. output-to-output skew**
- **Output Enable control**
- **Pin compatible with MPC942P**
- **Available in Industrial and Commercial**
- **32-pin LQFP package**

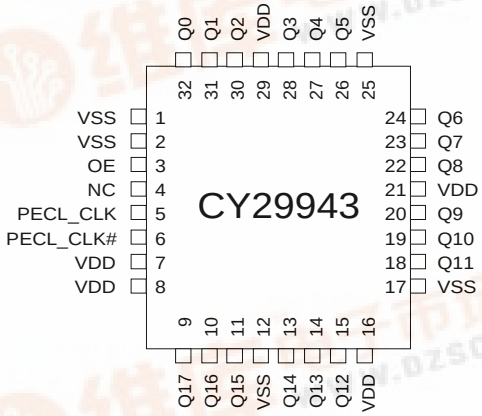
Description

The CY29943 is a low-voltage 200-MHz clock distribution buffer with an LVPECL-compatible input clock. All other control inputs are LVCMOS-/LVTTL-compatible. The eighteen outputs are 2.5V or 3.3V LVCMOS- or LVTTL-compatible and can drive 50Ω series or parallel terminated transmission lines. For series terminated transmission line, each output can drive one or two traces giving the device an effective fanout of 1:36. Low output-to-output skews make the CY29943 an ideal clock distribution buffer for nested clock trees in the most demanding of synchronous systems.

Block Diagram



Pin Configuration



Pin Description[1]

Pin	Name	PWR	I/O	Description
5	PECL_CLK		I, PU	**PECL Input Clock**
6	PECL_CLK#		I, PD	**PECL Input Clock**
3	OE		I, PU	**Output Enable**. When HIGH, all the outputs are enabled. When set LOW, the outputs are at high impedance.
9, 10, 11, 13, 14, 15, 18, 19, 20, 22, 23, 24, 26, 27, 28, 30, 31, 32	Q(17:0)	VDD	O	**Clock Outputs**
7, 8, 16, 21, 29	VDD			**3.3V or 2.5V Power Supply**
1, 2, 12, 17, 25	VSS			**Common Ground**
4	NC			**No Connection**

Note:
1. PD = internal pull-down, PU = internal pull-up.

Maximum Ratings[2]

Maximum Input Voltage Relative to V_{SS}: ..... V_{SS} – 0.3V
Maximum Input Voltage Relative to V_{DD}: ..... V_{DD} + 0.3V
Storage Temperature: ..... –65°C to + 150°C
Operating Temperature: ..... –40°C to +85°C
Maximum ESD protection ..... 2 kV
Maximum Power Supply: 5.5V
Maximum Input Current: ..... ±20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters (V_{DD} = 3.3V ±5% or 2.5V ±5%, V_{DDC} = 3.3V ±5% or 2.5V ±5%, over the specified temperature range)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage		V_{SS}		0.8	V
V_{IH}	Input High Voltage		2.0		V_{DD}	V
I_{IL}	Input Low Current[3]				–200	µA
I_{IH}	Input High Current[3]				200	µA
V_{PP}	Peak-to-Peak Input Voltage		500		1000	mV
VCMR	Common Mode Range[4] PECL_CLK	V_{DD} = 3.3V	V_{DD} – 1.4		V_{DD} – 0.6	V
		V_{DD} = 2.5V	V_{DD} – 1.0		V_{DD} – 0.6	
V_{OL}	Output Low Voltage[5]	I_{OL} = 20 mA			0.5	V
V_{OH}	Output High Voltage[5]	I_{OH} = –20 mA, V_{DD} = 3.3V	2.4			V
		I_{OH} = –16 mA, V_{DD} = 2.5V	2.0			
I_{DDQ}	Quiescent Supply Current			5	7	mA
I_{DD}	Dynamic Supply Current	V_{DD} = 3.3V, Outputs @ 150 MHz, CL = 15 pF		285		mA
		V_{DD} = 3.3V, Outputs @ 200 MHz, CL = 15 pF		335		
		V_{DD} = 2.5V, Outputs @ 150 MHz, CL = 15 pF		200		
		V_{DD} = 2.5V, Outputs @ 200 MHz, CL = 15 pF		240		
Z_{out}	Output Impedance	V_{DD} = 3.3V	8	12	16	Ω
		V_{DD} = 2.5V	10	15	20	
C_{in}	Input Capacitance			4		pF

Notes:
2. **Multiple Supplies:** The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
3. Inputs have pull-up/pull-down resistors that effect input current.
4. The V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the "High" input is within the V_{CMR} range and the input lies within the VPP specification.
5. Driving series or parallel terminated 50Ω (or 50Ω to $V_{DD}/2$) transmission lines.

AC Parameters[6] (V_{DD} = 3.3V ±5% or 2.5V ±5%, V_{DDC} = 3.3V ±5% or 2.5V ±5%, over the specified temperature range)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Fmax	Input Frequency				200	MHz
Tpd	PECL_CLK to Q Delay[7, 8]	V_{DD} = 3.3V	2.0	3.5	4.0	ns
		V_{DD} = 2.5V	2.6	4.0	5.2	
FoutDC	Output Duty Cycle[7, 8, 9]		40		60	%
Tskew	Output-to-Output Skew[7, 8]				200	ps
Tskew(pp)	Part-to-Part Skew[10]	V_{DD} = 3.3V			1.7	ns
		V_{DD} = 2.5V			2.2	
Tskew(pp)	Part-to-Part Skew[11]				1.0	ns
Tr/Tf	Output Clocks Rise/Fall Time[7, 8]	0.8V to 2.0V, V_{DD} = 3.3V	0.2		1.1	ns
		0.5V to 1.8V, V_{DD} = 2.5V				

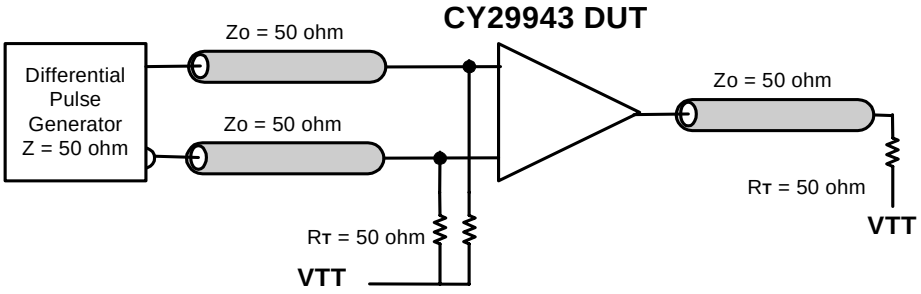


Figure 1. PECL_CLK CY29943 Test Reference for V_{CC} = 3.3V and V_{CC} = 2.5V

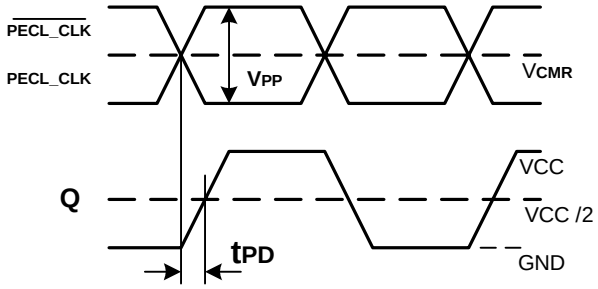


Figure 2. Propagation Delay (TPD) Test Reference

Notes:
6. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
7. Outputs driving 50Ω transmission lines.
8. Outputs loaded with 15 pF each.
9. See *Figure 1*.
10. Across temperature and voltage ranges, includes output skew.
11. For a specific temperature and voltage, includes output skew.

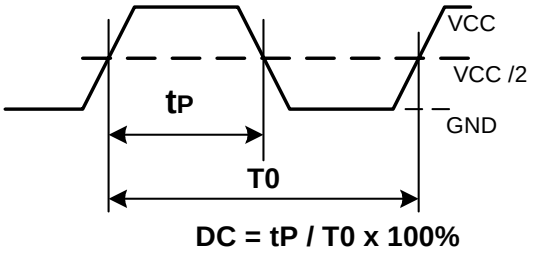


Figure 3. Output Duty Cycle (FoutDC)

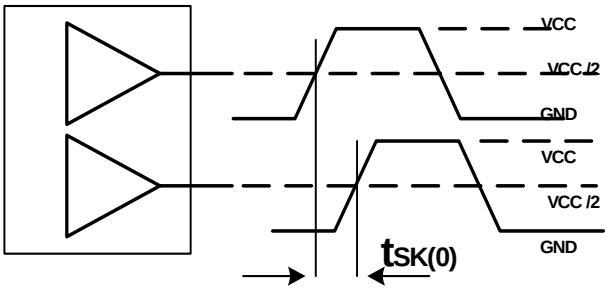


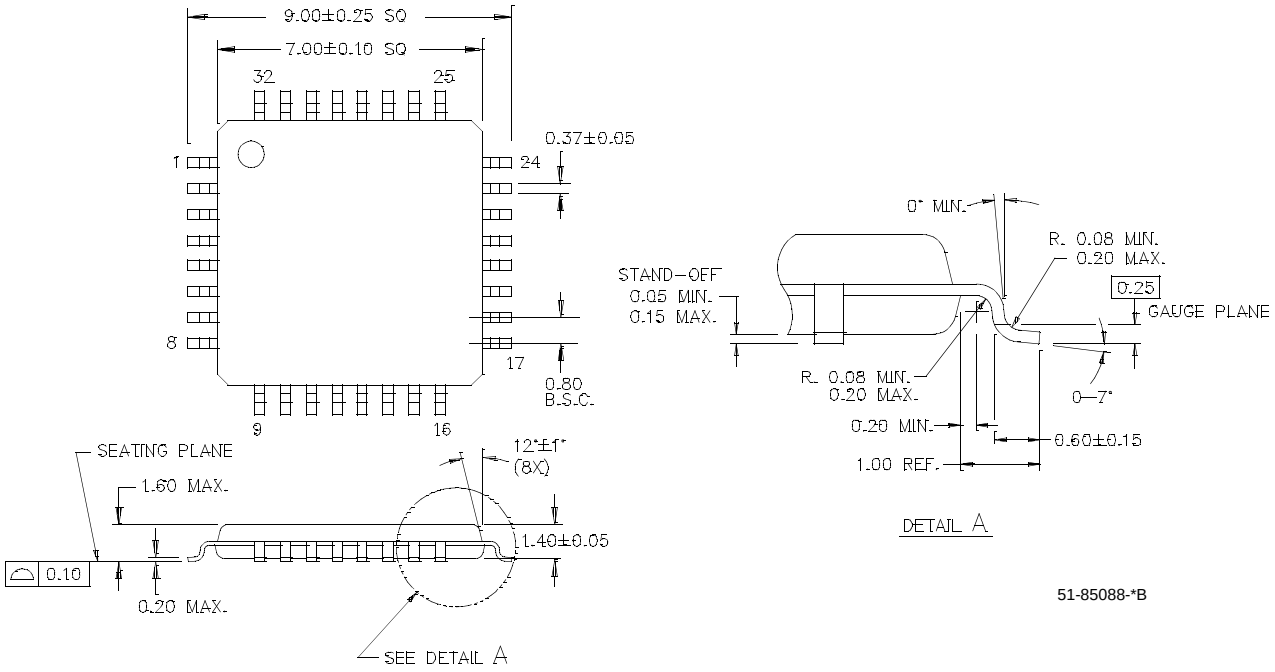
Figure 4. Output-to-Output Skew tsk(0)

Ordering Information

Part Number	Package Type	Production Flow
CY29943AI	32-pin LQFP	Industrial, –40°C to +85°C
CY29943AIT	32-pin LQFP–Tape and Reel	Industrial, –40°C to +85°C
CY29943AC	32-pin LQFP	Commercial, 0°C to +70°C
CY29943ACT	32-pin LQFP–Tape and Reel	Commercial, 0°C to +70°C

Package Drawing and Dimensions

32-Lead Thin Plastic Quad Flatpack 7 x 7 x 1.4 mm A32.14



Document History Page

Document Title: CY29943 2.5V or 3.3V 200-MHz 1:18 Clock Distribution Buffer Document Number: 38-07285				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111096	02/07/02	BRK	New data sheet
*A	116779	08/14/02	HWT	Add Commercial Temperature range in the ordering Information
*B	118744	09/18/02	HWT	Update output duty cycle on page 4
*C	122877	12/21/02	RBI	Add power up requirements to maximum rating information.