CYPRESS

CY2305C
CY2309C

Low-cost 3.3V Zero Delay Buffer

Features

- **10-MHz to 100-/133-MHz operating range, compatible with CPU and PCI bus frequencies**
- **Zero input-output propagation delay**
- **Multiple low-skew outputs**
  - **— One input drives five outputs (CY2305C)**
  - **— One input drives nine outputs, grouped as 4 + 4 + 1 (CY2309C)**
- **75ps typical cycle-cycle jitter (15pF, 66MHz), compatible with Pentium®-based systems**
- **Test Mode to bypass phase-locked loop (PLL) (CY2309C) only [see "Select Input Decoding" on page 2])**
- **Available in space-saving 16-pin 150-mil SOIC or 4.4-mm TSSOP packages (CY2309C), and 8-pin, 150-mil SOIC package (CY2305C)**
- **3.3V operation**
- **Industrial temperature available**

Functional Description

The CY2305C and CY2309C are die replacement parts for CY2305 and CY2309.

The CY2309C is a low-cost 3.3V zero delay buffer designed to distribute high-speed clocks and is available in a 16-pin SOIC or TSSOP package. The CY2305C is an 8-pin version of the CY2309C. It accepts one reference input, and drives out five low-skew clocks. The -1H versions of each device operate at up to 100-/133-MHz frequencies, and have higher drive than the -1 devices. All parts have on-chip PLLs which lock to an input clock on the REF pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad.

The CY2309C has two banks of four outputs each, which can be controlled by the Select inputs as shown in the "Select Input Decoding" table on page 2. If all output clocks are not required, BankB can be three-stated. The select inputs also allow the input clock to be directly applied to the outputs for chip and system testing purposes.

The CY2305C and CY2309C PLLs enter a power-down mode when there are no rising edges on the REF input. In this state, the outputs are three-stated and the PLL is turned off, resulting in less than 12.0 μA of current draw for commercial temperature devices and 25.0 μA for industrial temperature parts. The CY2309C PLL shuts down in one additional case as shown in the table below.

In the special case when S2:S1 is 1:0, the PLL is bypassed and REF is output from DC to the maximum allowable frequency. The part behaves like a non-zero delay buffer in this mode, and the outputs are not tri-stated.

The CY2305C/CY2309C is available in two/three different configurations, as shown in the Ordering Information Table. The CY2305C-1/CY2309C-1 is the base part. The CY2305-1H/ CY2309-1H is the high-drive version of the -1, and its rise and fall times are much faster than the -1s.

These parts are not intended for 5V input-tolerant applications.

Block Diagram   **Pin Configuration**
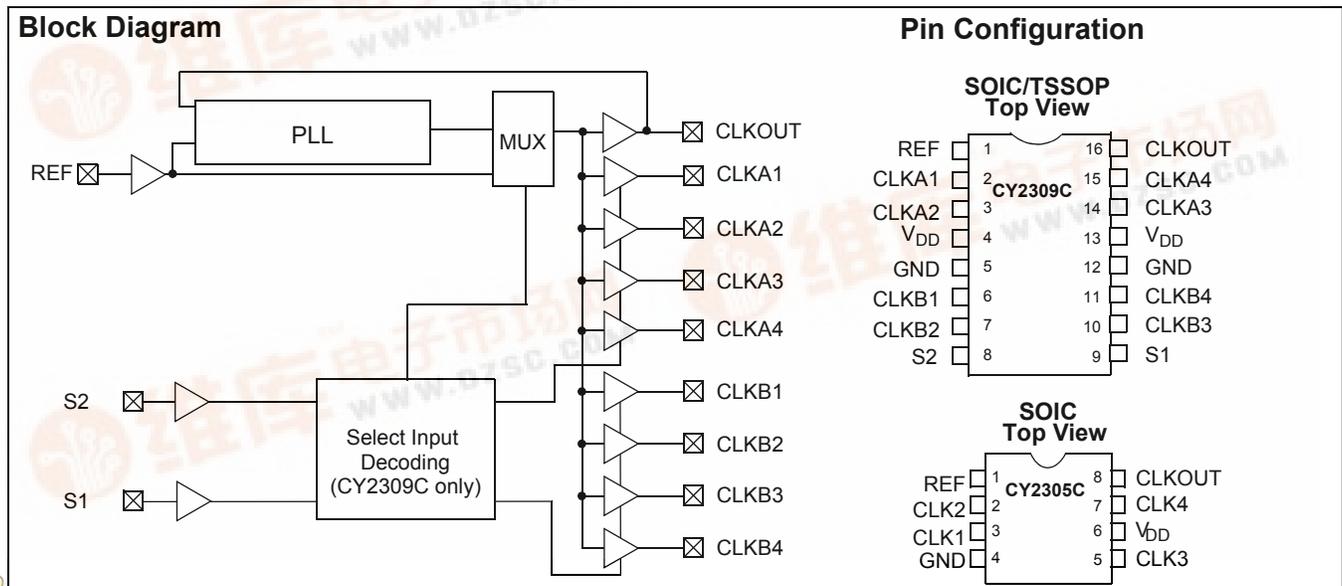
Pin Description for CY2309C

Pin	Signal	Description
1	REF[1]	Input reference frequency, 5V-tolerant input
2	CLKA1[2]	Buffered clock output, Bank A
3	CLKA2[2]	Buffered clock output, Bank A
4	V_{DD}	3.3V supply
5	GND	Ground
6	CLKB1[2]	Buffered clock output, Bank B
7	CLKB2[2]	Buffered clock output, Bank B
8	S2[3]	Select input, bit 2
9	S1[3]	Select input, bit 1
10	CLKB3[2]	Buffered clock output, Bank B
11	CLKB4[2]	Buffered clock output, Bank B
12	GND	Ground
13	V_{DD}	3.3V supply
14	CLKA3[2]	Buffered clock output, Bank A
15	CLKA4[2]	Buffered clock output, Bank A
16	CLKOUT[2]	Buffered output, internal feedback on this pin

Pin Description for CY2305C

Pin	Signal	Description
1	REF[1]	Input reference frequency, 5V-tolerant input
2	CLK2[2]	Buffered clock output
3	CLK1[2]	Buffered clock output
4	GND	Ground
5	CLK3[2]	Buffered clock output
6	V_{DD}	3.3V supply
7	CLK4[2]	Buffered clock output
8	CLKOUT[2]	Buffered clock output, internal feedback on this pin

Select Input Decoding for CY2309C

S2	S1	CLOCK A1–A4	CLOCK B1–B4	CLKOUT[4]	Output Source	PLL Shutdown
0	0	Three-state	Three-state	Driven	PLL	N
0	1	Driven	Three-state	Driven	PLL	N
1	0	Driven	Driven	Driven	Reference	Y
1	1	Driven	Driven	Driven	PLL	N

Zero Delay and Skew Control

All outputs should be uniformly loaded to achieve Zero Delay between the input and output. Since the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input-output delay. This is shown in the above graph.

For applications requiring zero input-output delay, all outputs, including CLKOUT, must be equally loaded. Even if CLKOUT is not used, it must have a capacitive load, equal to that on other outputs, for obtaining zero input-output delay.

For zero output-output skew, be sure to load all outputs equally. For further information refer to the application note entitled "CY2305 and CY2309 as PCI and SDRAM Buffers."

Notes:
1. Weak pull-down.
2. Weak pull-down on all outputs.
3. Weak pull-ups on these inputs.
4. This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and output.

Absolute Maximum Conditions

Supply Voltage to Ground Potential .... –0.5V to +4.6V

DC Input Voltage (Except REF) ....–0.5V to V_{DD} + 0.5V

DC Input Voltage REF..................................... –0.5V to 4.6V

Storage Temperature .... –65°C to +150°C

Junction Temperature.. 150°C

Static Discharge Voltage
(per MIL-STD-883, Method 3015) .... > 2,000V

Operating Conditions for CY2305CSXC-XX and CY2309CSXC-XX Commercial Temp. Devices

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	0	70	°C
C_L	Load Capacitance, below 100 MHz		30	pF
C_L	Load Capacitance, from 100 MHz to 133 MHz		10	pF
C_{IN}	Input Capacitance		7	pF
t_{PU}	Power-up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics for CY2305CSXC-XX and CY2309CSXC-XX Commercial Temp. Devices

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage[5]		–	0.8	V
V_{IH}	Input HIGH Voltage[5]		2.0	–	V
I_{IL}	Input LOW Current	V_{IN} = 0V	–	50.0	μA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}	–	100.0	μA
V_{OL}	Output LOW Voltage[6]	I_{OL} = 8 mA (–1) I_{OH} = 12 mA (–1H)	–	0.4	V
V_{OH}	Output HIGH Voltage[6]	I_{OH} = –8 mA (–1) I_{OL} = –12 mA (–1H)	2.4	–	V
I_{DD} (PD mode)	Power Down Supply Current	REF = 0 MHz	–	12.0	μA
I_{DD}	Supply Current	Unloaded outputs at 66.67 MHz, SEL inputs at V_{DD}	–	32.0	mA

Switching Characteristics for CY2305CSXC-1and CY2309CSC-1 Commercial Temp. Devices[7]

Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
t1	Output Frequency	30-pF load 10-pF load	10 10	–	100 133.33	MHz MHz
	Duty Cycle[6] = $t_2 \div t_1$	Measured at 1.4V, F_{out} = 66.67 MHz	40.0	50.0	60.0	%
t3	Rise Time[6]	Measured between 0.8V and 2.0V	–	–	2.50	ns
t_4	Fall Time[6]	Measured between 0.8V and 2.0V	–	–	2.50	ns
t_5	Output to Output Skew[6]	All outputs equally loaded	–	–	250	ps
t_{6A}	Delay, REF Rising Edge to CLKOUT Rising Edge[6]	Measured at V_{DD}/2	–	0	±350	ps
t_{6B}	Delay, REF Rising Edge to CLKOUT Rising Edge[6]	Measured at V_{DD}/2. Measured in PLL Bypass Mode, CY2309 device only.	1	5	8.7	ns
t_7	Device to Device Skew[6]	Measured at V_{DD}/2 on the CLKOUT pins of devices	–	0	700	ps
t_J	Cycle to Cycle Jitter[6]	Measured at 66.67 MHz, loaded outputs	–	75	200	ps
t_{LOCK}	PLL Lock Time[6]	Stable power supply, valid clock presented on REF pin	–	–	1.0	ms

Notes:
5. REF input has a threshold voltage of V_{DD}/2.
6. Parameter is guaranteed by design and characterization. Not 100% tested in production.
7. All parameters specified with loaded outputs.

Switching Characteristics for CY2305CSXC-1H and CY2309CSXC-1H Commercial Temp. Devices[7]

Parameter	Name	Description	Min.	Typ.	Max.	Unit
t1	Output Frequency	30-pF load 10-pF load	10 10	– 	100 133.33	MHz MHz
	Duty Cycle[6] = $t_2 \div t_1$	Measured at 1.4V, F_{out} = 66.67 MHz	40.0	50.0	60.0	%
	Duty Cycle[6] = $t_2 \div t_1$	Measured at 1.4V, F_{out} < 50.0 MHz	45.0	50.0	55.0	%
t3	Rise Time[6]	Measured between 0.8V and 2.0V	–	–	1.50	ns
t_4	Fall Time[6]	Measured between 0.8V and 2.0V	–	–	1.50	ns
t_5	Output to Output Skew[6]	All outputs equally loaded	–	–	250	ps
t_{6A}	Delay, REF Rising Edge to CLKOUT Rising Edge[6]	Measured at V_{DD}/2	–	0	±350	ps
t_{6B}	Delay, REF Rising Edge to CLKOUT Rising Edge[6]	Measured at V_{DD}/2. Measured in PLL Bypass Mode, CY2309 device only.	1	5	8.7	ns
t_7	Device to Device Skew[6]	Measured at V_{DD}/2 on the CLKOUT pins of devices	–	0	700	ps
t_8	Output Slew Rate[6]	Measured between 0.8V and 2.0V using Test Circuit #2	1	–	–	V/ns
t_J	Cycle to Cycle Jitter[6]	Measured at 66.67 MHz, loaded outputs	–	–	200	ps
t_{LOCK}	PLL Lock Time[6]	Stable power supply, valid clock presented on REF pin	–	–	1.0	ms

Operating Conditions for CY2305CSXI-XX and CY2309CSXI-XX Industrial Temp. Devices

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	–40	85	°C
C_L	Load Capacitance, below 100 MHz	–	30	pF
C_L	Load Capacitance, from 100 MHz to 133 MHz	–	10	pF
C_{IN}	Input Capacitance	–	7	pF

Electrical Characteristics for CY2305CSXI-XX and CY2309CSXI-XX Industrial Temp. Devices

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage[5]		—	0.8	V
V_{IH}	Input HIGH Voltage[5]		2.0	–	V
I_{IL}	Input LOW Current	V_{IN} = 0V	–	50.0	μA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}	–	100.0	μA
V_{OL}	Output LOW Voltage[6]	I_{OL} = 8 mA (–1) I_{OH} =12 mA (–1H)	–	0.4	V
V_{OH}	Output HIGH Voltage[6]	I_{OH} = –8 mA (–1) I_{OL} = –12 mA (–1H)	2.4	–	V
I_{DD} (PD mode)	Power-down Supply Current	REF = 0 MHz	–	25.0	μA
I_{DD}	Supply Current	Unloaded outputs at 66.67 MHz, SEL inputs at V_{DD}	–	35.0	mA

Switching Characteristics for CY2305CSXI-1 and CY2309CSXI-1 Industrial Temp. Devices [7]

| Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
t1	Output Frequency	30-pF load 10-pF load	10 10		100 133.33	MHz MHz
	Duty Cycle[6] = $t_2 \div t_1$	Measured at 1.4V, F_{out} = 66.67 MHz	40.0	50.0	60.0	%
t3	Rise Time[6]	Measured between 0.8V and 2.0V	–	–	2.50	ns
t4	Fall Time[6]	Measured between 0.8V and 2.0V	–	–	2.50	ns
t5	Output to Output Skew[6]	All outputs equally loaded	–	–	250	ps
t6A	Delay, REF Rising Edge to CLKOUT Rising Edge[6]	Measured at $V_{DD}/2$	–	0	±350	ps
t6B	Delay, REF Rising Edge to CLKOUT Rising Edge[6]	Measured at $V_{DD}/2$. Measured in PLL Bypass Mode, CY2309 device only.	1	5	8.7	ns
t7	Device to Device Skew[6]	Measured at $V_{DD}/2$ on the CLKOUT pins of devices	–	0	700	ps
tJ	Cycle to Cycle Jitter[6]	Measured at 66.67 MHz, loaded outputs	–	75	200	ps
tLOCK	PLL Lock Time[6]	Stable power supply, valid clock presented on REF pin	–	–	1.0	ms

Switching Characteristics for CY2305CSXI-1H and CY2309CSXI-1H Industrial Temp. Devices[7]

| Parameter	Name	Description	Min.	Typ.	Max.	Unit
t_1	Output Frequency	30-pF load 10-pF load	10 10	– 	100 133.33	MHz MHz
	Duty Cycle[6] = $t_2 \div t_1$	Measured at 1.4V, F_{out} = 66.67 MHz	40.0	50.0	60.0	%
	Duty Cycle[6] = $t_2 \div t_1$	Measured at 1.4V, F_{out} < 50.0 MHz	45.0	50.0	55.0	%
t_3	Rise Time[6]	Measured between 0.8V and 2.0V	–	–	1.50	ns
t_4	Fall Time[6]	Measured between 0.8V and 2.0V	–	–	1.50	ns
t_5	Output to Output Skew[6]	All outputs equally loaded	–	–	250	ps
t_{6A}	Delay, REF Rising Edge to CLKOUT Rising Edge[6]	Measured at $V_{DD}/2$	–	0	±350	ps
t_{6B}	Delay, REF Rising Edge to CLKOUT Rising Edge[6]	Measured at $V_{DD}/2$. Measured in PLL Bypass Mode, CY2309 device only.	1	5	8.7	ns
t_7	Device to Device Skew[6]	Measured at $V_{DD}/2$ on the CLKOUT pins of devices	–	0	700	ps
t_8	Output Slew Rate[6]	Measured between 0.8V and 2.0V using Test Circuit #2	1	–		V/ns
t_J	Cycle to Cycle Jitter[6]	Measured at 66.67 MHz, loaded outputs	–	–	200	ps
t_{LOCK}	PLL Lock Time[6]	Stable power supply, valid clock presented on REF pin	–	–	1.0	ms

Switching Waveforms

Duty Cycle Timing
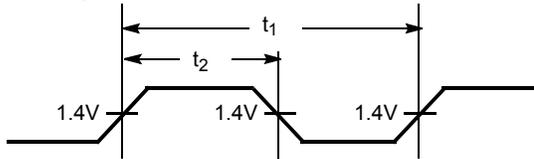
All Outputs Rise/Fall Time
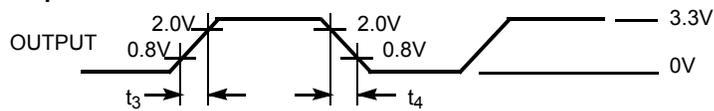
Output-Output Skew
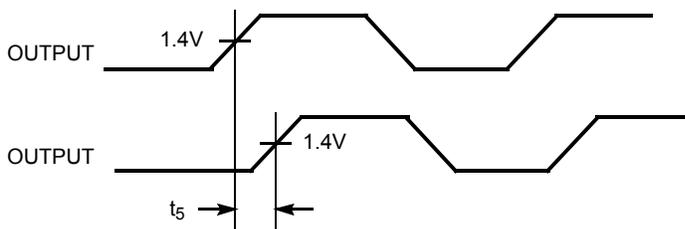
Input-Output Propagation Delay
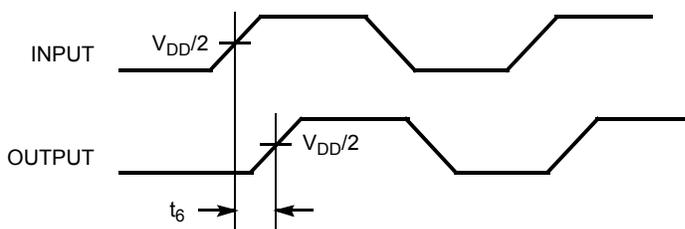
Device-Device Skew

## Test Circuits
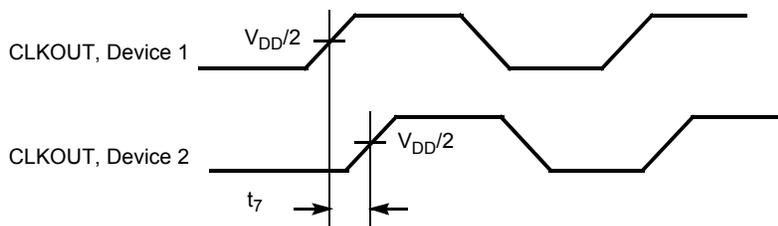
Test Circuit # 1

Test Circuit # 2
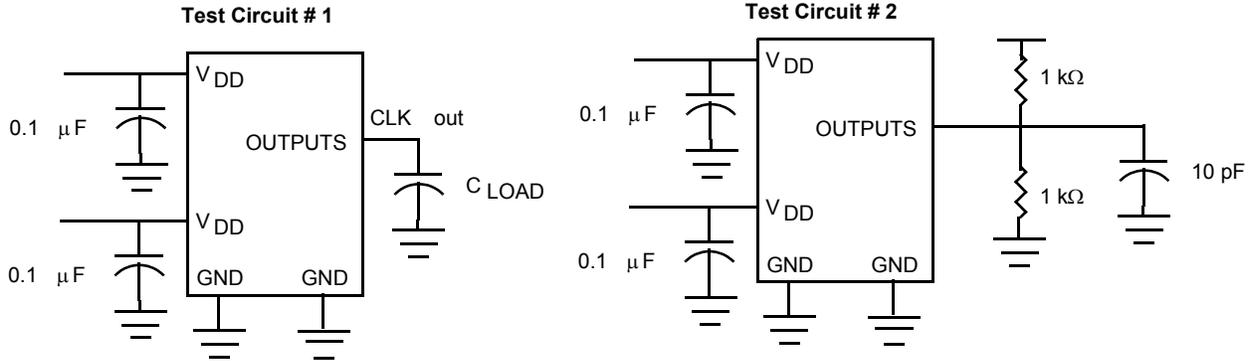
For parameter t_8 (output slew rate) on -1H devices

Ordering Information

Ordering Code	Package Type	Operating Range
Lead-free - CY2305C		
CY2305CSXC-1	8-pin 150-mil SOIC	Commercial
CY2305CSXC-1T	8-pin 150-mil SOIC – Tape and Reel	Commercial
CY2305CSXC-1H	8-pin 150-mil SOIC	Commercial
CY2305CSXC-1HT	8-pin 150-mil SOIC – Tape and Reel	Commercial
CY2305CSXI-1	8-pin 150-mil SOIC	Industrial
CY2305CSXI-1T	8-pin 150-mil SOIC – Tape and Reel	Industrial
CY2305CSXI-1H	8-pin 150-mil SOIC	Industrial
CY2305CSXI-1HT	8-pin 150-mil SOIC – Tape and Reel	Industrial
Lead-free - CY2309C		
CY2309CSXC-1	16-pin 150-mil SOIC	Commercial
CY2309CSXC-1T	16-pin 150-mil SOIC – Tape and Reel	Commercial
CY2309CSXC-1H	16-pin 150-mil SOIC	Commercial
CY2309CSXC-1HT	16-pin 150-mil SOIC – Tape and Reel	Commercial
CY2309CSXI-1	16-pin 150-mil SOIC	Industrial
CY2309CSXI-1T	16-pin 150-mil SOIC – Tape and Reel	Industrial
CY2309CSXI-1H	16-pin 150-mil SOIC	Industrial
CY2309CSXI-1HT	16-pin 150-mil SOIC – Tape and Reel	Industrial
CY2309CZXC-1	16-pin 4.4-mm TSSOP	Commercial
CY2309CZXC-1T	16-pin 4.4-mm TSSOP – Tape and Reel	Commercial
CY2309CZXC-1H	16-pin 4.4-mm TSSOP	Commercial
CY2309CZXC-1HT	16-pin 4.4-mm TSSOP – Tape and Reel	Commercial
CY2309CZXI-1	16-pin 4.4-mm TSSOP	Industrial
CY2309CZXI-1T	16-pin 4.4-mm TSSOP – Tape and Reel	Industrial
CY2309CZXI-1H	16-pin 4.4-mm TSSOP	Industrial
CY2309CZXI-1HT	16-pin 4.4-mm TSSOP – Tape and Reel	Industrial

Package Drawing and Dimensions

8-lead (150-Mil) SOIC S8

PIN 1 ID

4   1

0.150[3.810]
0.157[3.987]

0.230[5.842]
0.244[6.197]

5   8
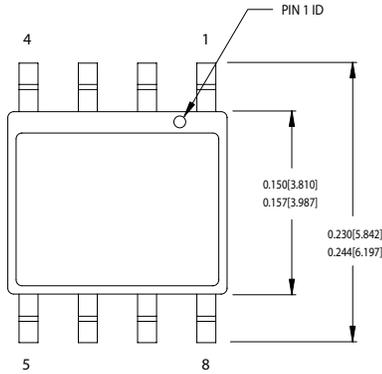
1. DIMENSIONS IN INCHES[MM] MIN.
   MAX.

2. PIN 1 ID IS OPTIONAL,
   ROUND ON SINGLE LEADFRAME
   RECTANGULAR ON MATRIX LEADFRAME

3. REFERENCE JEDEC MS-012

4. PACKAGE WEIGHT 0.07gms

PART #
S08.15 STANDARD PKG.
SZ08.15 LEAD FREE PKG.

0.189[4.800]
0.196[4.978]

SEATING PLANE

0.010[0.254]
0.016[0.406]   X 45°

0.061[1.549]
0.068[1.727]

0.004[0.102]

0.050[1.270]
BSC

0.004[0.102]
0.0098[0.249]

0°~8°

0.016[0.406]
0.035[0.889]

0.0075[0.190]
0.0098[0.249]

0.0138[0.350]
0.0192[0.487]
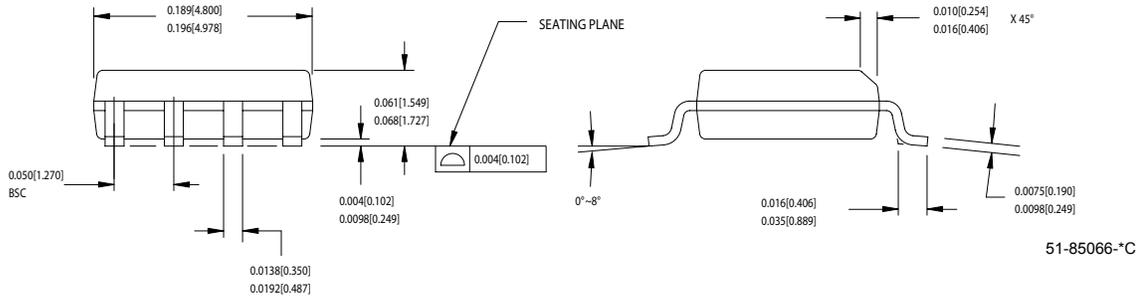
51-85066-*C

16-Lead (150-Mil) SOIC S16

PIN 1 ID

8   1

0.150[3.810]
0.157[3.987]

0.230[5.842]
0.244[6.197]

9   16
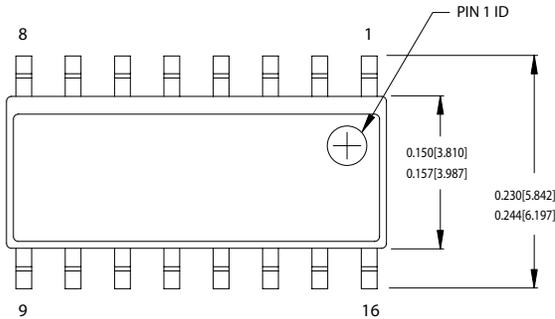
DIMENSIONS IN INCHES[MM] MIN.
   MAX.

REFERENCE JEDEC MS-012

PACKAGE WEIGHT 0.15gms

PART #
S16.15 STANDARD PKG.
SZ16.15 LEAD FREE PKG.

0.386[9.804]
0.393[9.982]

SEATING PLANE

0.010[0.254]
0.016[0.406]   X 45°

0.061[1.549]
0.068[1.727]

0.004[0.102]

0.050[1.270]
BSC

0.0138[0.350]
0.0192[0.487]

0.004[0.102]
0.0098[0.249]

0°~8°

0.016[0.406]
0.035[0.889]

0.0075[0.190]
0.0098[0.249]
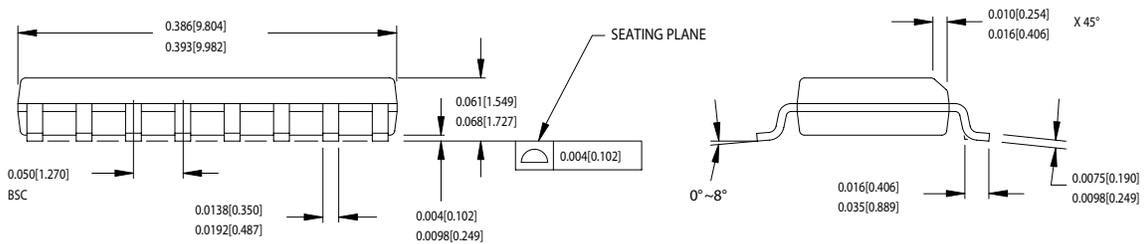
51-85068-*B

Package Drawing and Dimensions (continued)

**16-lead TSSOP 4.40 MM Body Z16.173**
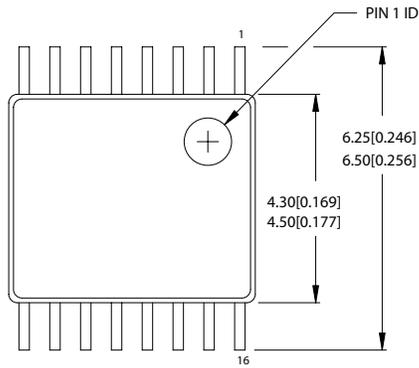
DIMENSIONS IN MM[INCHES] MIN.

MAX.

REFERENCE JEDEC MO-153

PACKAGE WEIGHT 0.05gms
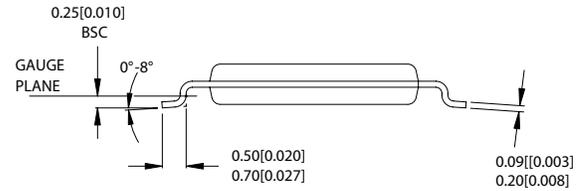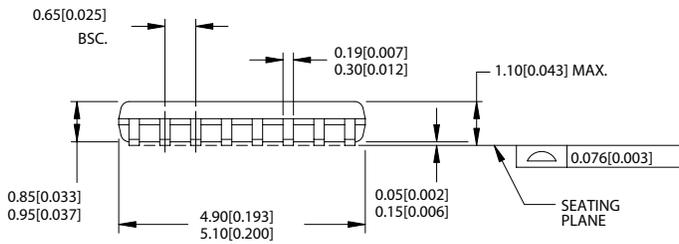
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Document History Page

Document Title: CY2305C/CY2309C Low-cost 3.3V Zero Delay Buffer				
Document Number: 38-07672				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	224421	See ECN	RGL	New data sheet
*A	268571	See ECN	RGL	Added bullet for 5V tolerant-inputs in the features
*B	276453	See ECN	RGL	Minor Change: Moved one sentence from the features to the Functional Description
*C	303063	See ECN	RGL	Updated data sheet as per characterization data
*D	318315	See ECN	RGL	Data sheet re-write
*E	344815	See ECN	RGL	Minor Error: Corrected the header of all the AC/DC tables with the right part numbers.