

APL6536



Four-Channel Supervisory IC

Features

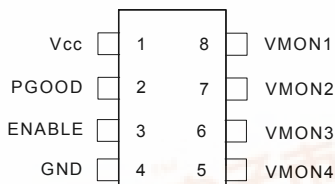
- 2.6V to 5.5V Input Voltage Range
- Low Quiescent Current : less than 50μA
- High Accuracy Detection Threshold : ±1.6%
- Adjustable Undervoltage Lockout for Each Supply
- Active high PGOOD Output
- Guaranteed PGOOD Valid to Falling V_{CC} < 1V
- VMON Glitch Immunity : 30μs
- Lead Free Available (RoHS Compliant)

Applications

- Graphics Cards
- Portable Battery-Powered Equipment
- μP Voltage Monitoring
- Set-Top Boxes
- Notebook Computer
- Multiple Supply System

Pinouts

SOP-8 Top View

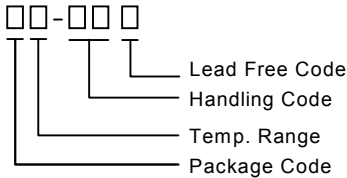
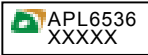


APL6536

General Description

The APL6536 is a four channel supervisory IC designed to monitor voltage supplies in μP and digital system. This IC can supervise any positive voltage using an external resistor divider to translate to a lower voltage for comparison to the internal 0.633V reference. Once any VMON input falls below 0.633V the PGOOD output is pulled low, the hysteresis of the internal reference is 15mV. The PGOOD pin has an internal 20kΩ pull-up to V_{CC} making an external pull-up resistor unnecessary. Each rail's VMON point is independently adjustable with a resistor divider. The PGOOD output is guaranteed to be valid with IC bias lower than 1V. This IC is designed to reject fast line transient glitches 30μs on VMON input. The PGOOD output is an open-drain to allow ORing of multiple signals. If less than four voltages are being monitored, connect the unused VMON pins to V_{CC}. The ENABLE input pin provides for a reset of the PGOOD output when it is pulled down below 0.5V. With an internal 10μA pull-up to V_{CC}, it can be signaled with common logic or pulled to ground with a push button switch. APL6536 come in a miniature SOP-8 package.

Ordering and Marking Information

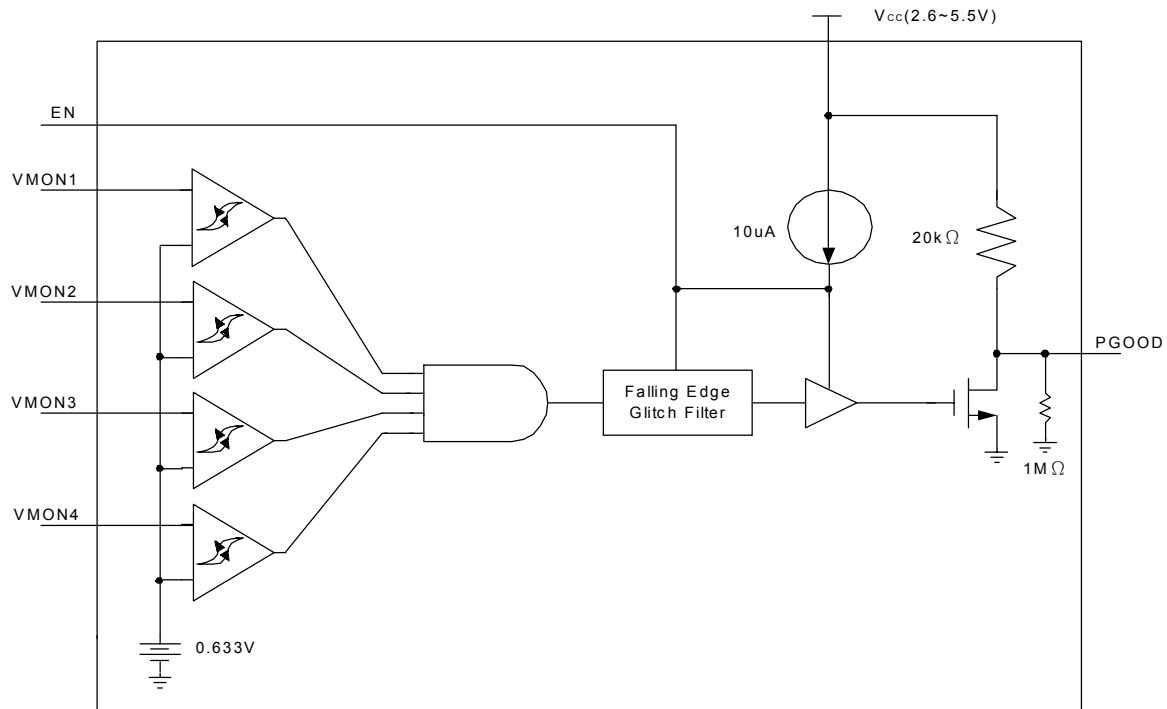
| | |
|---|---|
| <p>APL6536 □□-□□□</p>  <p>Lead Free Code Handling Code Temp. Range Package Code</p> | <p>Package Code K : SOP-8 Temp. Range I : -40 to 85 °C Handling Code TU : Tube TR : Tape & Reel Lead Free Code L : Lead Free Device Blank : Original Device</p> |
| <p>APL6536 : </p> | <p>XXXXX - Date Code</p> |

Notes : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte in plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldering operations. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

Pin Function Description

| PIN | | I/O | Description |
|-----|----------------------------------|-----|--|
| No. | Name | | |
| 1 | V _{CC} | | Supply Voltage (2.6V to 5V) |
| 2 | PGOOD | O | PGOOD is the AND function of all the VMON inputs being satisfied. This is an open drain output and can be pulled high to the appropriate level with an external resistor. Additionally a 20kΩ pull up to V _{CC} is provided internally. |
| 3 | ENABLE | I | Enabling input for supervisory function. Has a 10μA pull-up to V _{CC} . |
| 4 | GND | | Ground Connection |
| 5-8 | VMON1 VMON2 VMON3 VMON4 | I | These inputs provide for a programmable monitored voltage threshold referenced to an internal 0.633V reference. These inputs have a 30μs glitch filter to prevent transient upsets from being recognized by PGOOD. |

Block Diagram



Absolute Maximum Ratings

| Symbol | Parameter | Rating | Unit |
|------------------|------------------------------------|--------------------------------|------|
| V _{CC} | Input Voltage | 7 | V |
| VMON1-4,EN | All Input Pins | -0.3V to V _{CC} +0.3V | V |
| PGOOD | Output Pin | -0.3V to V _{CC} +0.3V | V |
| T _J | Maximum Junction Temperature | 150 | °C |
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| T _S | Soldering Temperature (10 seconds) | 260 | °C |
| ESD | Electrostatic Discharge | -3000 to 3000* ¹ | V |

Note:1.Human body model: C=100pF, R=1500Ω, 3 positives pulse plus 3 negative pulses.

Electrical Characteristics

Unless Otherwise noted these specifications apply over full temperature, $V_{CC} = 3.3V$, $T_J = -40^{\circ}C$ to $85^{\circ}C$
 Typical values refer to $T_J = 25^{\circ}C$

| Symbol | Parameter | Test condition | APL6536 | | | Unit |
|-------------------|--------------------------------------|---|---------|-------|-------|-------------------|
| | | | Min. | Typ. | Max. | |
| BIAS | | | | | | |
| I_{CC} | Supply Current (EN enable) | $VMON > VMON_{L2H}$ | | 40 | 400 | μA |
| | | $VMON < VMON_{H2L}$ | | 230 | 2000 | μA |
| I_{CC} | Supply Current (EN disable) | $VMON > VMON_{L2H}$ | | 50 | 500 | μA |
| | | $VMON < VMON_{H2L}$ | | 50 | 500 | μA |
| V_{CC_L2H} | V_{CC} Power On | V_{CC} low to high | | 2.6 | | V |
| V_{CC_POR} | V_{CC} Power On Reset | V_{CC} high to low | | 2.4 | | V |
| PGOOD | | | | | | |
| PGpd | Pull-Down Current | $V_{PGOOD} = 0.5V$ | | 10 | | mA |
| PGpu | Pull-Up Resistance | | | 20 | | $K\Omega$ |
| VPGI | Output Low | $V_{CC} = 1V$ | | 0 | 100 | mV |
| TPG del VMON | Delay From VMON Rising | Last valid input = V_{th} to PG release | | 3 | | μs |
| TPG del ENR | Delay From EN Rising | EN high to PG release | | 2 | | μs |
| TPG del ENF | Delay From EN Falling | EN low to PG pulling low | | 10 | | ns |
| ENABLE | | | | | | |
| V_{EN} | Rising Threshold Voltage | Enable low to high threshold | 1.30 | 1.65 | 2 | V |
| V_{EN_HYS} | Threshold Hysteresis Voltage | | | 80 | | mV |
| I_{ENpu} | Pull-up current | $V_{EN} = 0.5V$ | | 10 | | μA |
| VMON Input | | | | | | |
| $VMON_{H2L}$ | Falling Threshold Voltage | $T_J = 25^{\circ}C$ | 0.623 | 0.633 | 0.643 | V |
| $VMON_{TC}$ | Falling Threshold Temperature Coeff. | $T_J = -40^{\circ}C$ to $85^{\circ}C$ | | 100 | | $\mu V/^{\circ}C$ |
| $VVMON_{HYS}$ | Hysteresis Voltage | | | 15 | | mV |
| $VVMON_{RNG}$ | Range | | | 10 | | mV |
| T_{FIL} | Glitch Filter Duration | VMON glitch to PGOOD low filter | | 30 | | μs |

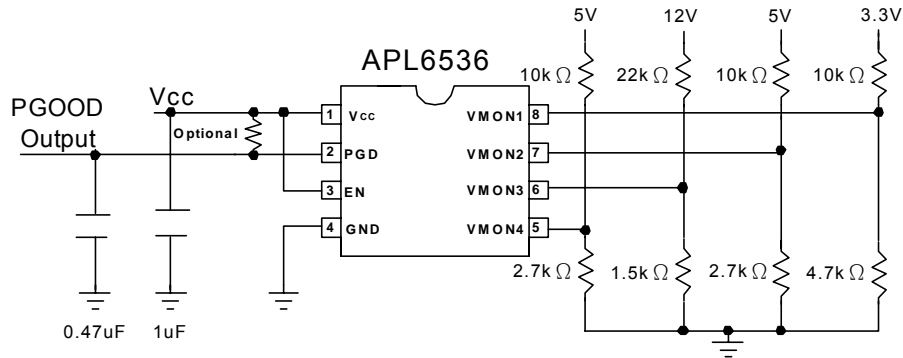
Electrical Characteristics

Unless Otherwise noted these specifications apply over full temperature, $V_{CC} = 5V$, $T_J = -40^\circ C$ to $85^\circ C$

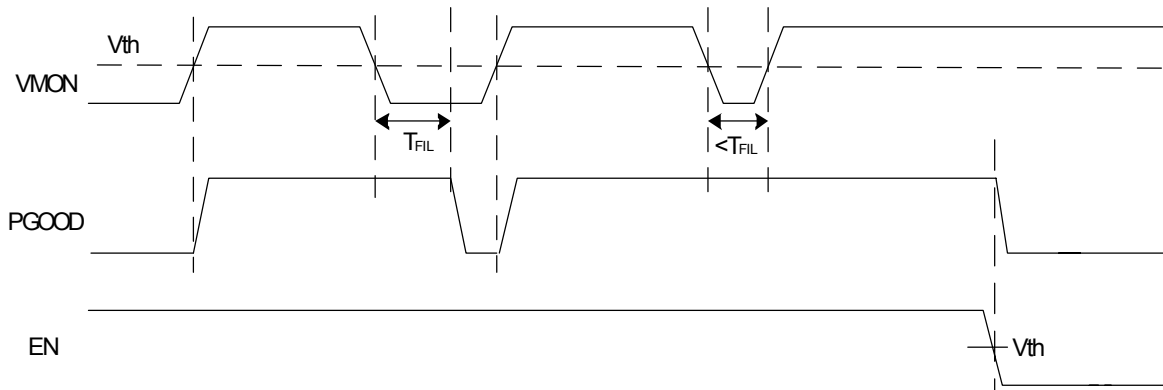
Typical values refer to $T_J = 25^\circ C$

| Symbol | Parameter | Test condition | APL6536 | | | Unit |
|-------------------|--------------------------------------|---|---------|-------|-------|------------------|
| | | | Min. | Typ. | Max. | |
| BIAS | | | | | | |
| I_{CC} | Supply Current (EN Enable) | $V_{MON} > V_{MON_L2H}$ | | 50 | 500 | μA |
| | | $V_{MON} < V_{MON_H2L}$ | | 230 | 2000 | μA |
| I_{CC} | Supply Current (EN Disable) | $V_{MON} > V_{MON_L2H}$ | | 60 | 600 | μA |
| | | $V_{MON} < V_{MON_H2L}$ | | 60 | 600 | μA |
| V_{CC_L2H} | V_{CC} Power On | V_{CC} low to high | | 2.6 | | V |
| V_{CC_POR} | V_{CC} Power On Reset | V_{CC} high to low | | 2.4 | | V |
| PGOOD | | | | | | |
| PGpd | Pull-Down Current | $V_{PGOOD} = 0.5V$ | | 10 | | mA |
| PGpu | Pull-Up Resistance | | | 20 | | $K\Omega$ |
| VPGI | Output Low | $V_{CC} = 1V$ | | 0 | 100 | mV |
| TPG del VMON | Delay From VMON Rising | Last valid input = V_{th} to PG release | | 5 | | μs |
| TPG del ENR | Delay From EN Rising | EN high to PG release | | 2 | | μs |
| TPG del ENF | Delay From EN Falling | EN low to PG pulling low | | 10 | | ns |
| ENABLE | | | | | | |
| V_{EN} | Rising Threshold Voltage | Enable low to high threshold | 2 | 2.5 | 3 | V |
| V_{EN_HYS} | Threshold Hysteresis Voltage | | | 80 | | mV |
| I_{ENpu} | Pull-Up Current | $V_{EN} = 0.5V$ | | 10 | | μA |
| VMON Input | | | | | | |
| V_{MON_H2L} | Falling Threshold Voltage | $T_J = 25^\circ C$ | 0.623 | 0.633 | 0.643 | V |
| V_{MON_TC} | Falling Threshold Temperature Coeff. | $T_J = -40^\circ C$ to $85^\circ C$ | | 100 | | $\mu V/^\circ C$ |
| V_{VMON_HYS} | Hysteresis Voltage | | | 15 | | mV |
| V_{VMON_RNG} | Range | | | 10 | | mV |
| T_{FIL} | Glitch Filter Duration | VMON glitch to PGOOD low filter | | 30 | | μs |

Application Circuit

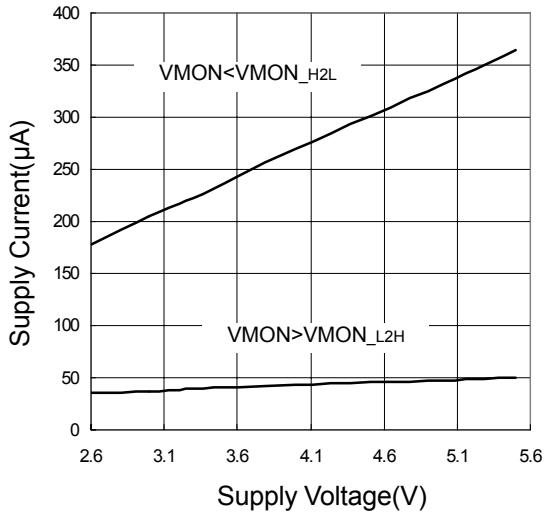


Timing Diagram

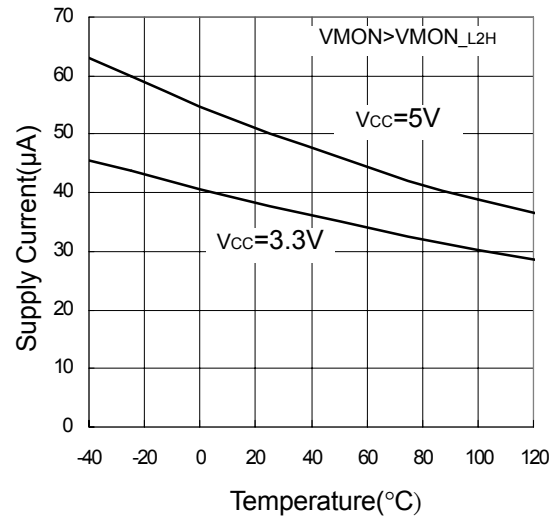


Typical Characteristics

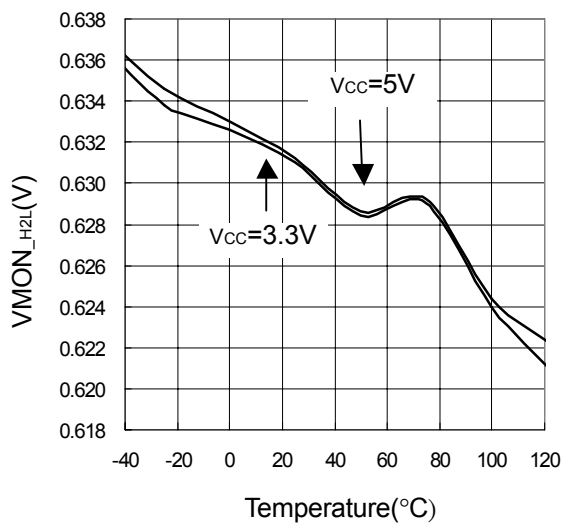
Supply Current vs. Supply Voltage



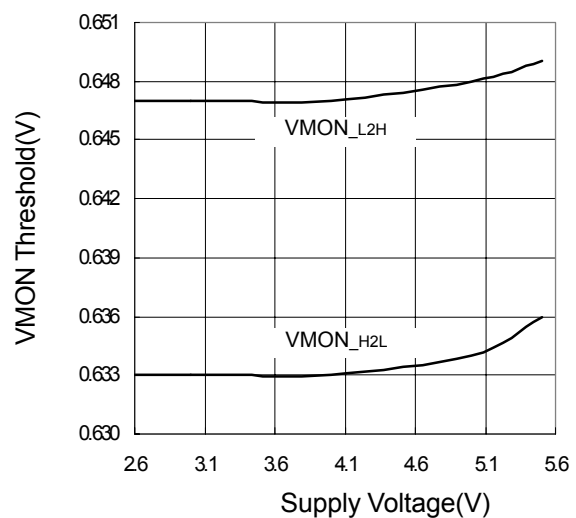
Supply Current vs. Temperature



VMON_H2L vs. Temperature

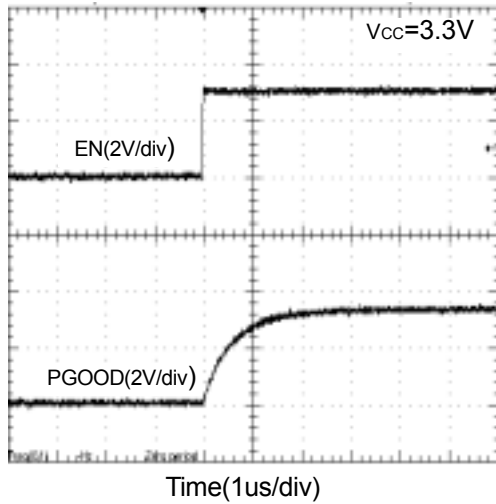


VMON Threshold vs. Supply Voltage

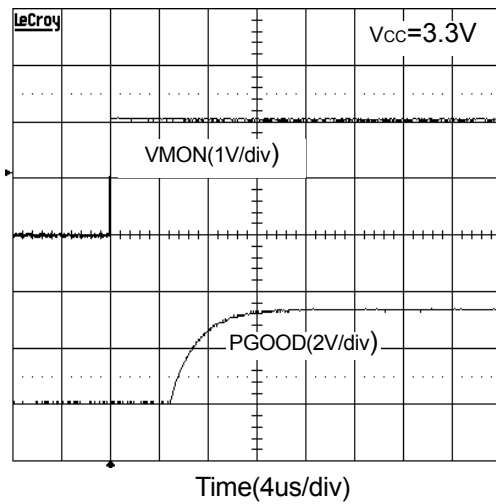


Typical Characteristics (Cont.)

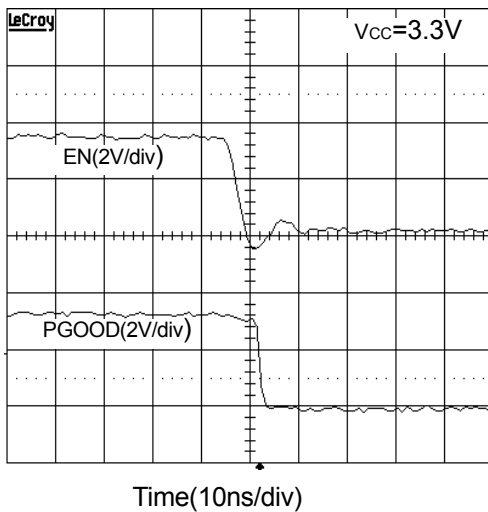
EN High to PGOOD



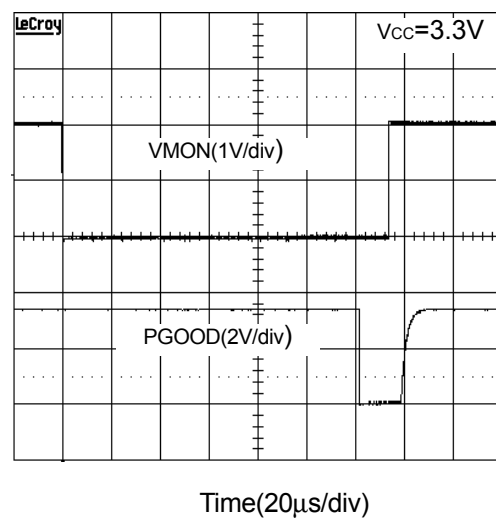
VMON High to PGOOD



EN Low to PGOOD



VMON Low to PGOOD



Application Information

PGOOD

The APL6536 is a four channel supervisory IC designed to monitor multiple voltages greater than 0.7V. This IC is suitable for both microprocessors or industrial system applications. Once biased to 2.6V and enabled the IC continuously monitors from one to four voltages independently through external resistor dividers comparing each VMON pin voltage to an internal 0.633V reference. The PGOOD output is an open-drain to allow ORing of the signals and interfacing to a wide range of logic levels. If less than four voltages are being monitored, connect the unused VMON pins to V_{CC} . The PGOOD pin has an internal 20k Ω pull-up to V_{CC} making an external pull-up resistor unnecessary.

Falling Edge Glitch Filter

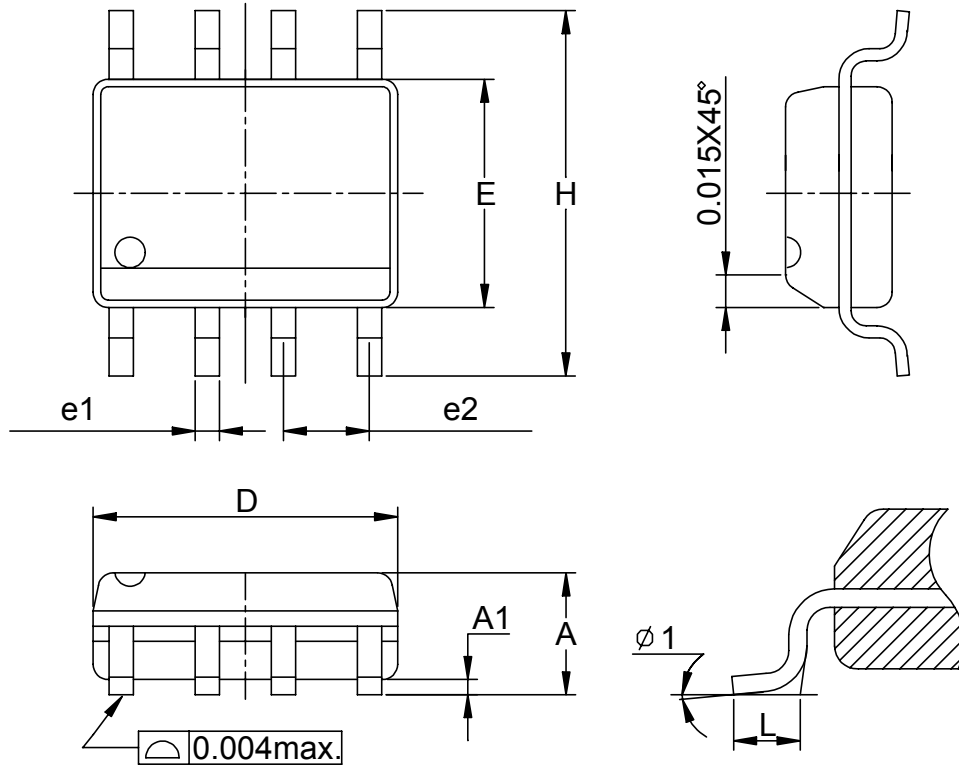
Once any VMON input falls below 0.633V the PGOOD output is pulled low, the VMON inputs are designed to reject fast transients (30us).

Enable

The APL6536 has an active high enable function. Force EN high ($\geq 0.5V_{CC}$) enables the PGOOD, EN low ($\leq 0.5V$) disables the PGOOD and enter the shutdown mode and it also causes the PGOOD to discharge through a 1M Ω resistance to ground. In shutdown mode, the quiescent current can reduce below 60uA. With an internal 10uA pull-up to V_{CC} , it can be signaled with common logic or pulled to ground with a push button switch.

Package Information

SOP-8 pin (Reference JEDEC Registration MS-012)

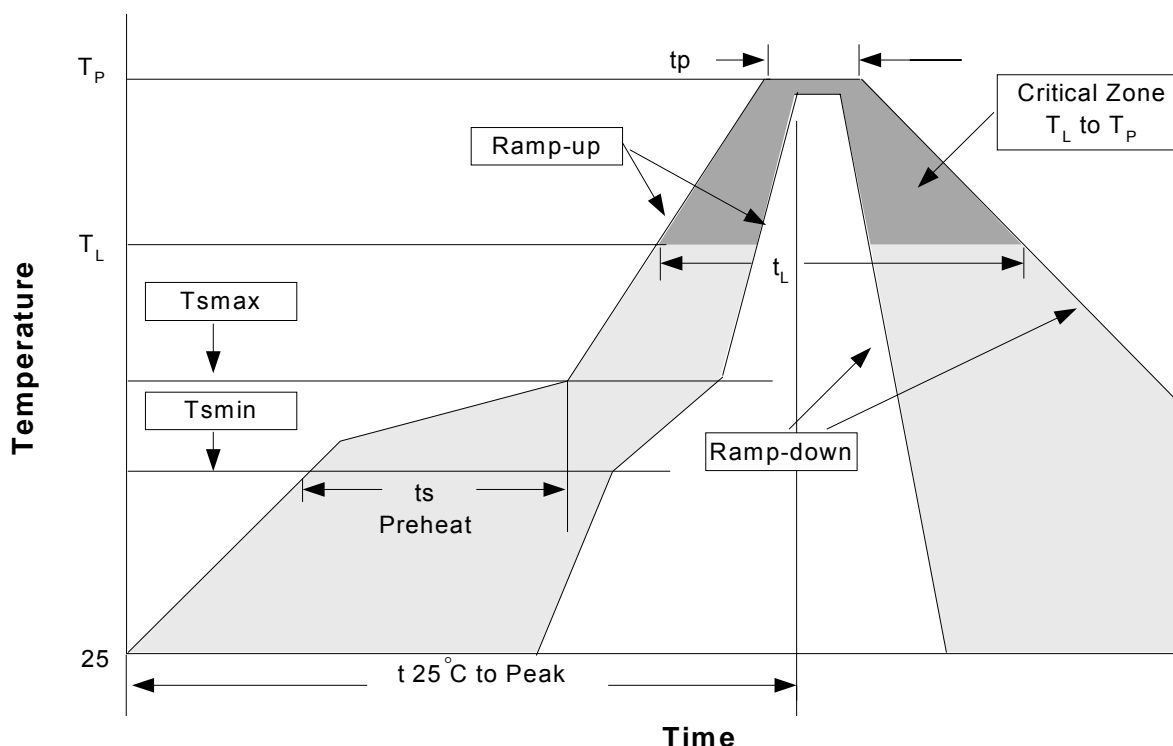


| Dim | Millimeters | | Inches | |
|-----|-------------|------|---------|-------|
| | Min. | Max. | Min. | Max. |
| A | 1.35 | 1.75 | 0.053 | 0.069 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| D | 4.80 | 5.00 | 0.189 | 0.197 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| L | 0.40 | 1.27 | 0.016 | 0.050 |
| e1 | 0.33 | 0.51 | 0.013 | 0.020 |
| e2 | 1.27BSC | | 0.50BSC | |
| φ 1 | 8° | | 8° | |

Physical Specifications

| | |
|--------------------|--|
| Terminal Material | Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn |
| Lead Solderability | Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3. |

Reflow Condition (IR/Convection or VPR Reflow)



Classification Reflow Profiles

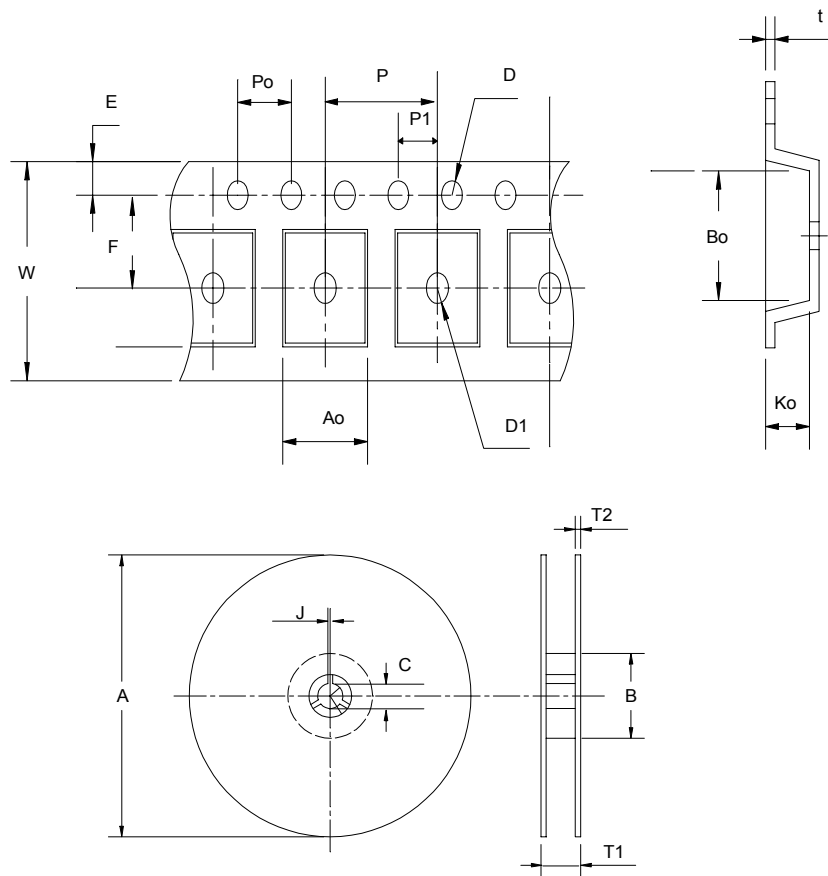
| Profile Feature | Sn-Pb Eutectic Assembly | | Pb-Free Assembly | |
|---|-------------------------|---------------|------------------|---------------|
| | Large Body | Small Body | Large Body | Small Body |
| Average ramp-up rate (T_L to T_P) | 3°C/second max. | | 3°C/second max. | |
| Preheat | | | | |
| - Temperature Min (T_{smin}) | 100°C | | 150°C | |
| - Temperature Mix (T_{smax}) | 150°C | | 200°C | |
| - Time (min to max)(t_s) | 60-120 seconds | | 60-180 seconds | |
| T_{smax} to T_L | | | 3°C/second max | |
| - Ramp-up Rate | | | | |
| T_{smax} to T_L | | | | |
| - Temperature(T_L) | 183°C | | 217°C | |
| - Time (t_L) | 60-150 seconds | | 60-150 seconds | |
| Peak Temperature(T_p) | 225 +0/-5°C | 240 +0/-5°C | 245 +0/-5°C | 250 +0/-5°C |
| Time within 5°C of actual Peak Temperature(t_p) | 10-30 seconds | 10-30 seconds | 10-30 seconds | 20-40 seconds |
| Ramp-down Rate | 6°C/second max. | | 6°C/second max. | |
| Time 25°C to Peak Temperature | 6 minutes max. | | 8 minutes max. | |

Note: All temperatures refer to topside of the package. Measured on the body surface.

Reliability test program

| Test item | Method | Description |
|---------------|---------------------|---------------------------|
| SOLDERABILITY | MIL-STD-883D-2003 | 245°C , 5 SEC |
| HOLT | MIL-STD-883D-1005.7 | 1000 Hrs Bias @ 125 °C |
| PCT | JESD-22-B, A102 | 168 Hrs, 100 % RH , 121°C |
| TST | MIL-STD-883D-1011.9 | -65°C ~ 150°C, 200 Cycles |
| ESD | MIL-STD-883D-3015.7 | VHBM > 2KV, VMM > 200V |
| Latch-Up | JESD 78 | 10ms , $I_{tr} > 100mA$ |

Carrier Tape



Reel Dimensions

| Application | A | B | C | J | T1 | T2 | W | P | E |
|-------------|---------|-----------|----------------|-----------|------------|-----------|-----------|-----------|-------------|
| SOP- 8 | 330 ± 1 | 62 +1.5 | 12.75+ 0.15 | 2 ± 0.5 | 12.4 ± 0.2 | 2 ± 0.2 | 12 ± 0.3 | 8 ± 0.1 | 1.75 ± 0.1 |
| | F | D | D1 | Po | P1 | Ao | Bo | Ko | t |
| | 5.5 ± 1 | 1.55 +0.1 | 1.55+ 0.25 | 4.0 ± 0.1 | 2.0 ± 0.1 | 6.4 ± 0.1 | 5.2 ± 0.1 | 2.1 ± 0.1 | 0.3 ± 0.013 |

(mm)

Cover Tape Dimensions

| Application | Carrier Width | Cover Tape Width | Devices Per Reel |
|-------------|---------------|------------------|------------------|
| SOP- 8 | 12 | 9.3 | 2500 |

Customer Service

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