APL1581

DUAL INPUT LOW DROPOUT REGULATOR

Features

- Adjustable or Fixed Output
- 520mV typ. Dropout at 5A in Dual Power Voltage Mode
- Remote Sense Pin Available
- 2% Accuracy Over Temperature Range
- Build-in Over Temperature Protection
- Build-in Current Limit
- 5 Pin TO-220 and TO-263, TO-252, SOP-8-P Packages
- Lead Free Available (RoHS Compliant)

Applications

- Microprocessor Supplies
- Chip Set Supplies
- VGA Card Power
- LCD Monitor Power

General Description

The APL1581 series of high performance positive voltage regulators are designed for use in applications requiring very low dropout voltage at 5Amp.

The APL1581 can provide a output voltage at the range of 1.25V to 2.55V, where both 5V and 3.3V voltage supplies are available.

The superior dropout characteristics result in reduced heat dissipation compared to regular LDOs. The APL1581 also provides excellent regulation over line, load, and temperature variations.

Current limit is trimmed to ensure specified output current and controlled short-circuit current. On-chip thermal limiting provides protection against any combination of overload that would create excessive junction temperature.

The APL1581 is available in both the through-hole and surface mount versions of the industry standard 5-Pin TO-220 and TO-263, TO-252, SOP-8-P power packages.

Ordering and Marking Information

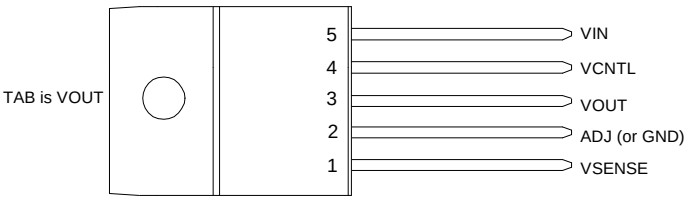
<table>
<tr>
<td>APL1581 - □□ □□ - □□ □
Lead Free Code
Handling Code
Temp. Range
Package Code
Voltage Code</td>
<td>Package Code
F : TO-220-5 G : TO-263-5 U :TO-252-5
KA : SOP-8-P
Temp. Range
C : 0 to 70 °C
Handling Code
TU : Tube TR : Tape & Reel
Voltage Code :
15 : 1.5V 18 : 1.8V
25 : 2.5V Blank : Adjustable Version
Lead Free Code
L : Lead Free Device Blank : Original Device</td>
</tr>
<tr>
<td>APL1581-15 F/G/U : 15 APL1581 XXXXX XXXXX - Date Code</td>
<td>APL1581 KA : APL1581 XXXXX XXXXX - Date Code</td>
</tr>
</table>

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldiering operations. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

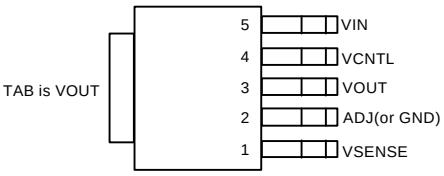
ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Rev. B.4 - Aug., 2005

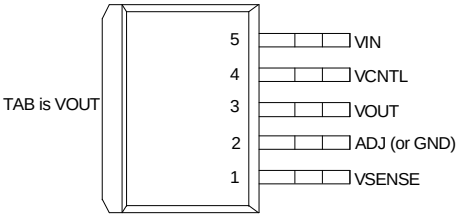
Pin Configuration



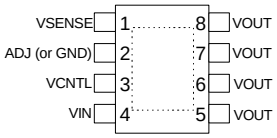
Front View of TO-220-5



Front View of TO-252-5



Front View of TO-263-5



SOP-8-P (Top View)

NC = No internal connection

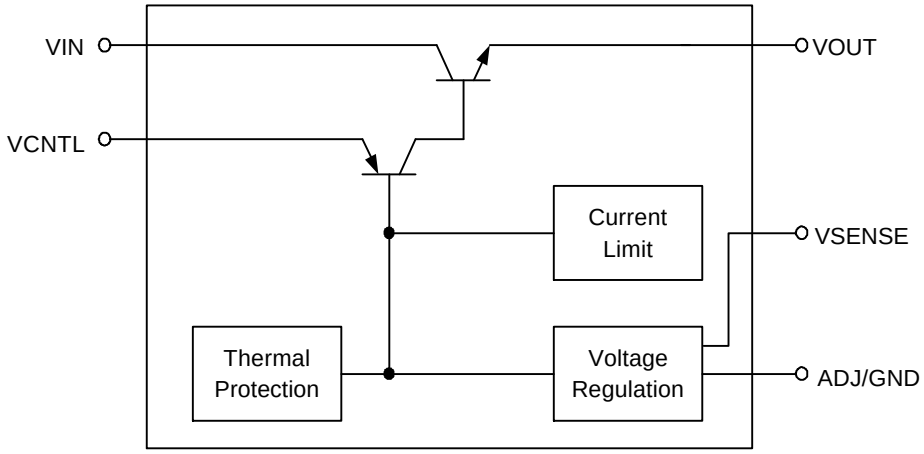
⬚ = Thermal Pad
(connected to VOUT plane for better heat dissipation)

Pin 5~8 must be connected together by a shortest wide track or plane.

Pin Description

PIN		Description
Name	I/O	
VSENSE	I	Positive side of the reference voltage, which allows remote sensing to obtain excellent load regulation.
ADJ	O	Negative side of the reference voltage, which allows to use resistor divider to set an expect output voltage. A small bypass capacitor can be connected from this pin to ground to improve PSRR performance.
GND	O	For fixed voltage devices this is the bottom of the resistor divider that sets the output voltage.
VOUT	O	Output pin of the regulator, which connects to the TAB. A minimum of 10µF capacitor must be connected from this pin to ground to ensure the stability.
VCNTL	I	Supply pin of the control circuitry, Which must be always higher than V_{OUT} for the device to regulate. (see electrical characteristics)
VIN	I	Power input pin of the regulator, which must be always higher than V_{OUT} for the device to regulate. (see electrical characteristics)

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{IN}	Input Voltage	7	V
V_{CNTL}	Control Voltage	13.2	V
P_D	Power Dissipation	Internally Limited	W
T_J	Operating Junction Temperature		°C
	Control Section	0 to 125	
	Power Transistor	0 to 150	
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature (Soldering, 10 second)	260	°C

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 1)		°C/W
	TO-263-5 (Toplayer plane size : 15mm x 15 mm)	28	
	TO-252-5 (Toplayer plane size : 10mm x 10 mm)	42	
	SOP-8-P (Toplayer plane size : 10mm x 10 mm)	68	
θ_{JC}	Junction-to-Case Resistance (Note 2)		°C/W
	TO-220-5	3	
	TO-263-5	4	
	TO-252-5	5	

Note 1: θJA is measured with the component mounted on a high effective thermal conductivity test board in free air. The sizes of the rectangular plane, where the devices are mounted, are shown in the table.

Note 2: The case temperature is measured on the TAB of the device mounted on the test board described in Note 1 except the package TO-220-5. The case temperature of the TO-220-5 is measured on the bottom of the case directly below the die.

Electrical Characteristics

Unless otherwise noted , these specifications apply over C_{IN} = 10uF, C_{CNTL} = 1uF, C_{OUT} = 10uF, and T_A = 0 to 70°C. Typical values refer to T_A = 25°C. V_{OUT} = V_{SENSE}.

Symbol	Parameter	Test Conditions	APL1581			UNIT
			MIN	TYP	MAX	
V_{REF}	Reference Voltage APL1581	V_{CNTL}=2.75~12V, V_{IN}=2.05~5.5V, I_O=10mA~5A, V_{ADJ}=0V	1.225	1.250	1.275	V
V_{OUT}	Output Voltage APL1581-15 APL1581-18 APL1581-25	(I_O =0~5A for fixed versions) V_{CNTL}=3~12V , V_{IN}=2.3~5.5V V_{CNTL}=3.3~12V , V_{IN}=2.6~5.5V V_{CNTL}=4~12V , V_{IN}=3.3~5.5V	1.470 1.764 2.450	1.500 1.800 2.500	1.530 1.836 2.550	V
REG_{LINE}	Line Regulation APL1581 APL1581-15 APL1581-18 APL1581-25	(I_O =0A for fixed versions) V_{CNTL}=2.75~12V, V_{IN}=1.75~5.5V, I_O=10mA, V_{ADJ}=0V V_{CNTL}=3~12V, V_{IN}=2.3~5.5V V_{CNTL}=3.3~12V, V_{IN}=2.6~5.5V V_{CNTL}=4~12V, V_{IN}=3~5.5V			3	mV
REG_{LOAD}	Load Regulation (note 1) APL1581 APL1581-15 APL1581-18 APL1581-25	(I_O =0~5A for fixed versions) V_{CNTL}=2.75V, V_{IN}=2.1V, V_{ADJ}=0V, I_O =10mA~5A V_{CNTL}=3V, V_{IN}=2.35V V_{CNTL}=3.3V, V_{IN}=2.65V V_{CNTL}=4V, V_{IN}=3.35V			5	mV
V_{CNTL}-V_{OUT}	Dropout Voltage (note 2) APL1581 APL1581-15 APL1581-18 APL1581-25	I_O=5A for all versions V_{IN}=2.05V, V_{ADJ}=0V V_{IN}=2.3V V_{IN}=2.6V V_{IN}=3.3V		1.20	1.35	V
V_{IN}-V_{OUT}	Dropout Voltage (note 2) APL1581 APL1581-15 APL1581-18 APL1581-25	I_O=5A for all versions V_{CNTL}=2.75V, V_{ADJ}=0V V_{CNTL}=3V V_{CNTL}=3.3V V_{CNTL}=4V		0.52	0.75	V
I_{LIMIT}	Current Limit	V_{CNTL}-V_{OUT}=1.5V, V_{IN}-V_{OUT}=0.6V	5			A
I_{LMIN}	Minimum Load Current (note 3) APL1581	V_{CNTL}=5V, V_{IN}=3.3V, V_{ADJ}=0V		0.8	10	mA
$REG_{THERMAL}$	Thermal Regulation	30mS Pulse		0.01		%/W
PSRR	Power Supply Ripple Rejection APL1581 APL1581-15 APL1581-18 APL1581-25	V_{RIPPLE}=1V_{PP} at 120Hz, I_O=5A V_{CNTL}=5V, V_{IN}=5V, V_{ADJ}=0V V_{CNTL}=5.25V, V_{IN}=5.25V V_{CNTL}=5.55V, V_{IN}=5.55V V_{CNTL}=6.25V, V_{IN}=6.25V	60	70		dB
I_{CNTL}	CNTL Pin Current	V_{CNTL}-V_{OUT}=1.5V , V_{IN}-V_{OUT}=0.8V, I_O =5A		45	120	mA
I_{GND}	Ground Pin Current APL1581-15 APL1581-18 APL1581-25	 V_{CNTL}=3V, V_{IN}=2.3V V_{CNTL}=3.3V, V_{IN}=2.6V V_{CNTL}=4V, V_{IN}=3.3V		8	13	mA
I_{ADJ}	Adjust Pin Current APL1581	 V_{CNTL}=2.75V , V_{IN}=2.05V , V_{ADJ}=0V		50	120	µA

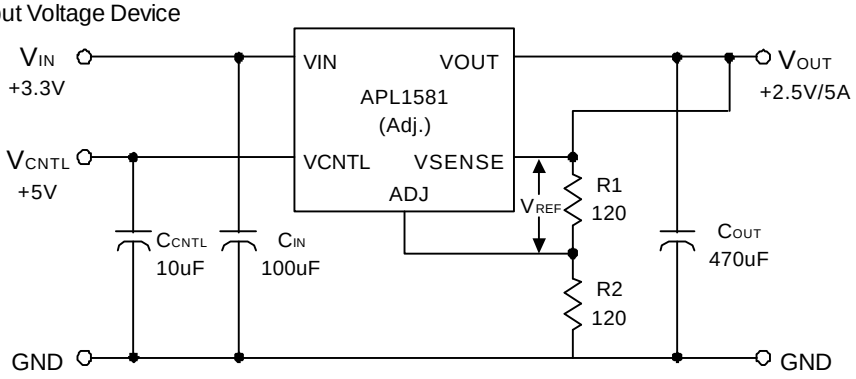
Note 1 : Low duty cycle pulse test with Kelvin connections are required to maintain data accuracy .

Note 2 : Dropout voltage is defined as the minimum difference between V_{IN} and V_{OUT} required to maintain 1% V_{OUT} regulation.

Note 3 : Minimum load current is defined as the minimum current required at the output to maintain V_{OUT} regulation.

Application Circuit

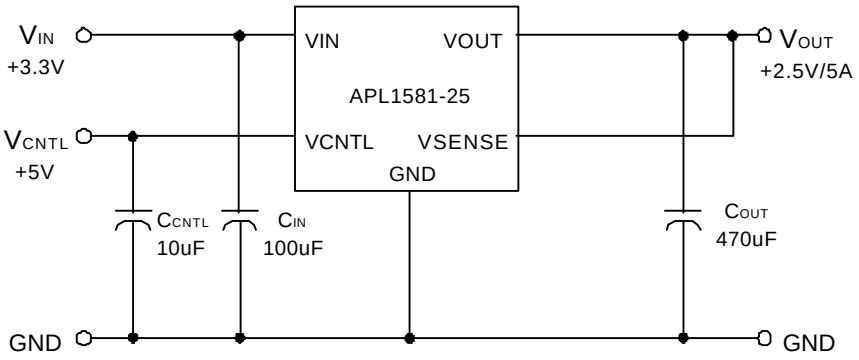
(1) Adjustable Output Voltage Device



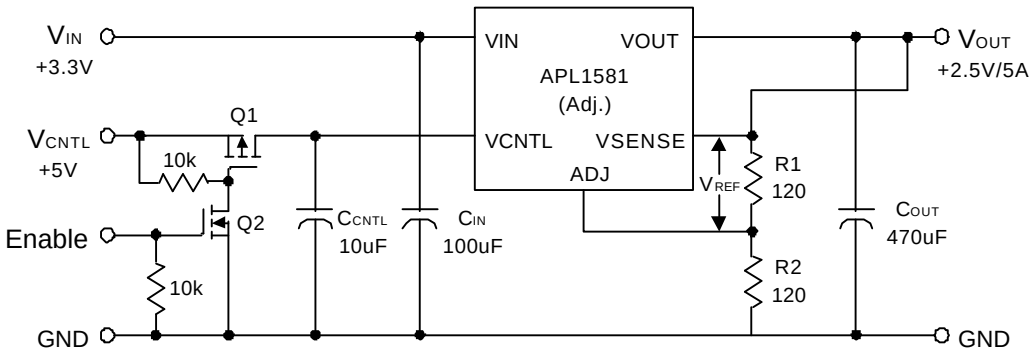
* $V_{OUT} = V_{REF} (1+ R2 / R1) + I_{ADJ} * R2$
where V_{REF} =1.25V (typical)
I_{ADJ}=50μA (typical)

* R1 is typically in range of 100Ω to 125 Ω to satisfy the minimum load current requirement.

(2) Fixed Output Voltage Device



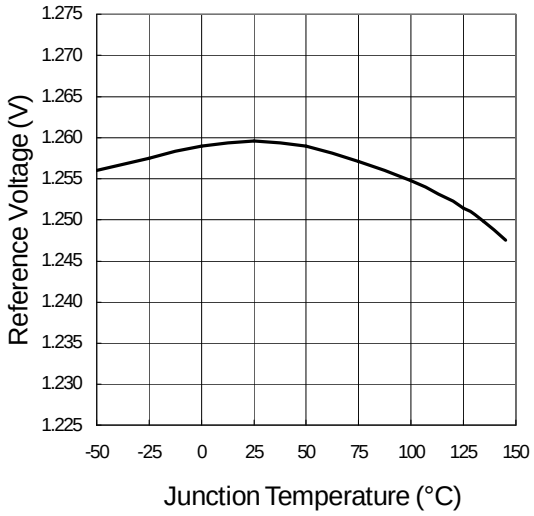
(3) With Enable Control Application



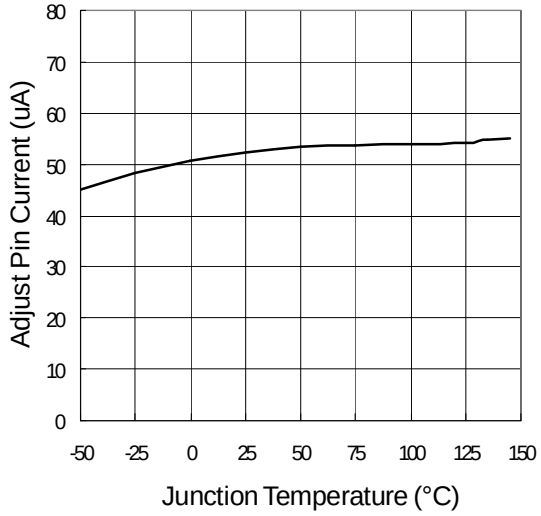
Q1 : APM2301A
Q2 : APM2300A

Typical Characteristics

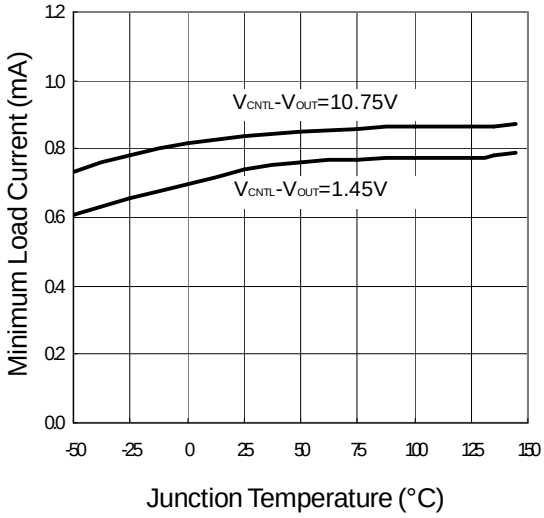
Reference Voltage vs Junction Temperature



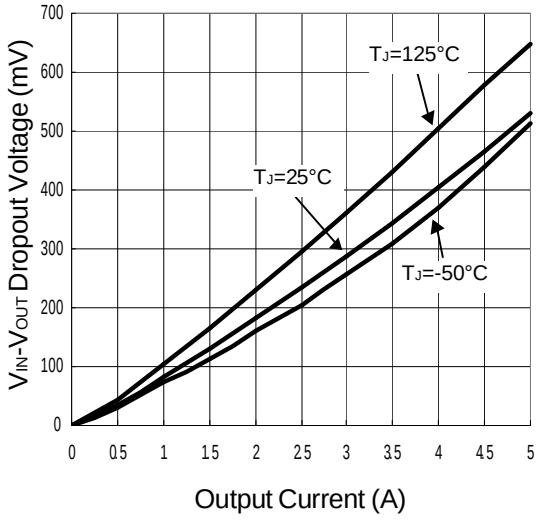
Adjust Pin Current vs Junction Temperature



Minimum Load Current vs Junction Temperature

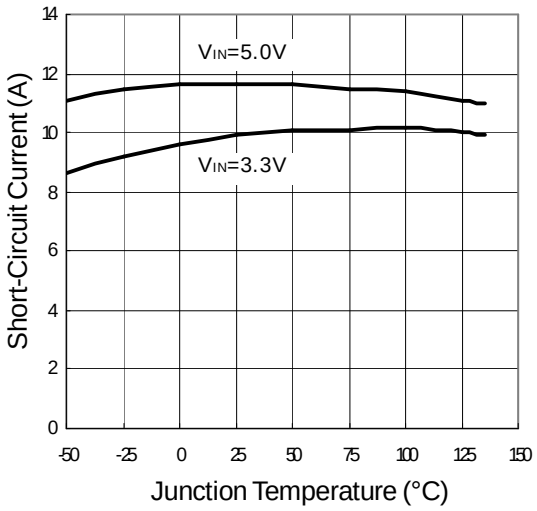


VIN-VOUT Dropout Voltage vs Output Current

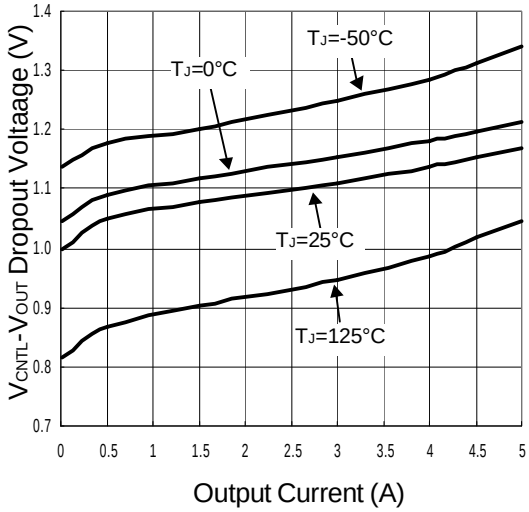


Typical Characteristics

Short-Circuit Current vs Junction Temperature

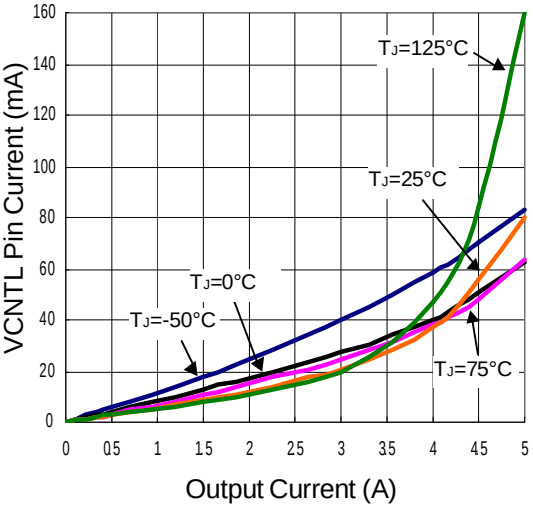


VCONTROL-VOUT Dropout Voltage vs Output Current



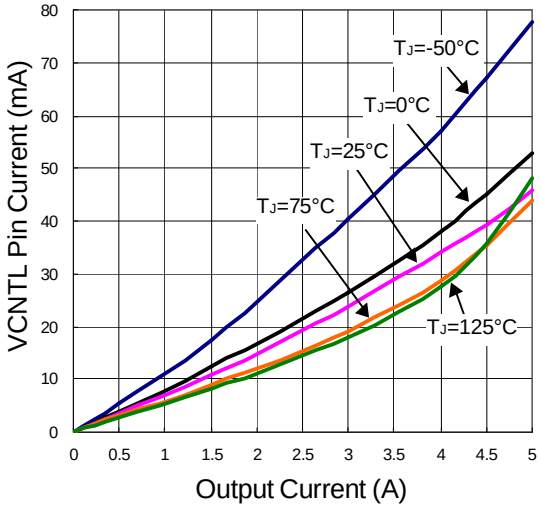
Control Pin Current vs Output Current

VIN-VOUT=0.6V



Control Pin Current vs Output Current

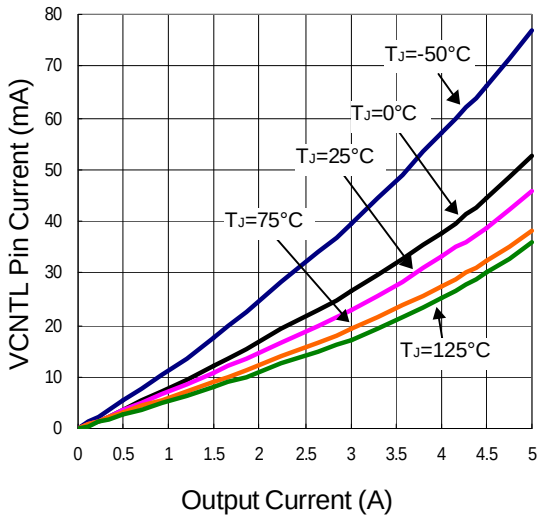
VIN-VOUT=0.8V



Typical Characteristics

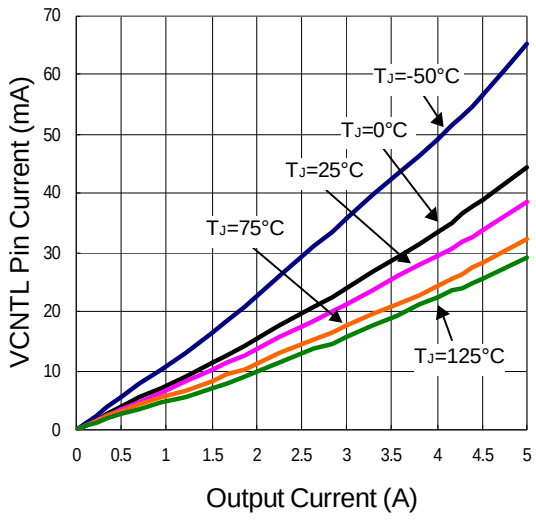
Control Pin Current vs Output Current

V_{IN}-V_{OUT}=1.0V



Control Pin Current vs Output Current

V_{IN}-V_{OUT}=4.25V



Application Information

General

The APL1581 (adjustable or fixed) regulator is a 5 terminal device designed specifically to provide extremely low dropout voltages comparable to the PNP type without the disadvantage of the extra power dissipation due to the base current associated with PNP regulators. This is done by bringing out the control pin of the regulator that provides the base current to the power NPN and connecting it to a voltage that is greater than the voltage present at the VIN pin. This flexibility makes APL1581 ideal for applications, where dual inputs are available, such as a computer motherboard with an ATX power supply that provides 5V and 3.3V to the board.

APL1581 is equipped with a 1.25V reference, precision and fast voltage regulations, on-chip current and thermal limits, and remote sensing capability to reduce system total cost.

APL1581 is available in SOP-8-P, TO-252-5, TO-263-5 and TO-220-5 packages to meet different power dissipation applications.

Output Voltage Setting

See figure 1. Adjustable APL1581 develops a 1.25V reference voltage between the VSENSE pin and the ADJ pin. Placing a resistor between these two terminals causes a constant current to flow through R1 and down through R2 to set the overall output voltage. In general R1 is chosen so that this current is the specified minimum load current of 10mA.The current out of the ADJ pin is small, typically 50μA and itadds to the current from R1. Because IADJ is very small, it needs to be considered only when very precise output voltage setting is required. For best regulation, the top of the resistor divider should be connected directly to

Application Information (Cont.)

Output Voltage Setting (Cont.)

the SENSE pin. The adjustable APL1581 can be programmable to any voltages in the range of 1.25V to 5.5V according to the following formula:

$$V_{OUT} = V_{REF} \times (1 + \frac{R2}{R1}) + I_{ADJ} \times R2$$

where V_{REF} = 1.25V (typical)

I_{ADJ} = 50µA (typical)

The recommended R1 is in range of 100Ω to125Ω to satisfy the minimum load current requirement. Proper sizes of R2 and R1 are also concerned for power dissipation.

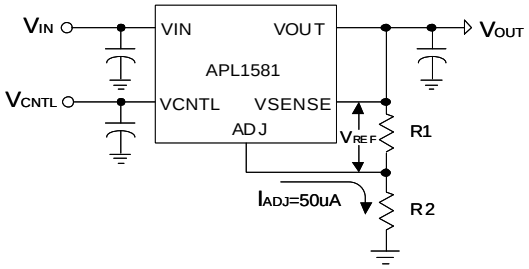


Figure 1 Setting Output Voltage

Grounding and Output Sensing

The APL1581 allows true Kelvin sensing for both the high and low side of the load. Figure 2 shows the device connected to take advantage of the remote sense feature. The SENSE pin and the top of the resistor divider are connected to the top of the load; the bottom of the resistor divider is connected to the bottom of the load. Typically the load is a microprocessor and parasitic resistance RP is made up of the PC traces and /or connector resistance between the regulator and the processor. RP is now connectedinside the regulation loop of the APL1581 and for reasonable values of RP the load regulation at the load will be negligible. Voltage drops due to RP are not eliminated; they will add to the dropout voltage of the regulator regardless of whether they are inside or outside the regulation loop.

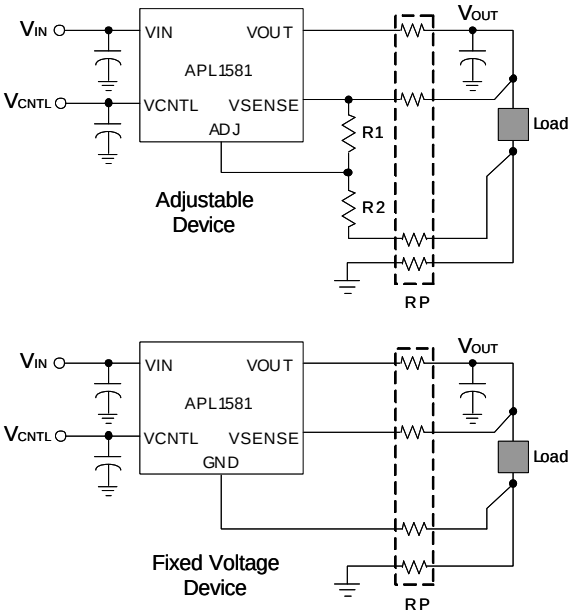
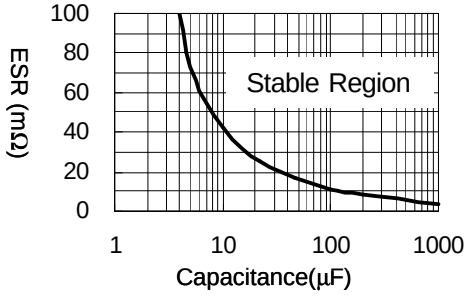


Figure 2 Remote Voltage Sensing

Stability and Output Capacitors

The circuit design of using the APL1581 series requires an output capacitor as part of the device frequency compensation. The following chart shows a stable region to select output capacitor for APL1581. This region above the curve indicates minimum required ESR and capacitance to maintain stability. However, the output capacitor should have an ESR less than1Ω.



Application Information (Cont.)

Stability and Output Capacitors (Cont.)

A low-ESR solid tantalum and aluminum electrolytic capacitor (ESR<1Ω) works extremely well and provides good transient response and stability over temperature. Ultra-low-ESR capacitors, such as ceramic chip capacitors, may promote unstable or under-damped transient response, but proper ceramic chip capacitors placed near loads can be used as decoupling capacitors.

The output capacitors are also used to reduce the slew rate of load current and help the APL1581 to minimize variations of the output voltage, improving transient response. For this purpose, the low-ESR capacitors are recommended.

Input Capacitors

The input capacitors of VCNTL and VIN pins are not required for stability but for supplying surge currents during large load transients, This will prevent the input rail from drooping and improve the performance of the APL1581. Because of parasitic inductors from

voltage sources or other bulk capacitors to the VCNTL and VIN pins will limit the slew rate of the surge currents during large load transients, resulting in voltage drop at VIN and VCNTL pins.

A capacitor of 1μF (ceramic chip capacitor) or greater (aluminum electrolytic capacitor) is recommended and connected near VCNTL pin. For VIN pin, an aluminum electrolytic capacitor (>33 μF) is recommended. It is not necessary to use low-ESR capacitors. More capacitance reduces the variations of the input voltage at VIN pin.

Layout and Thermal Considerations

The APL1581 series have internal power and thermal limiting (T_J=150°C typical) circuitry designed to protect the device under overload conditions. However maximum junction temperature ratings should not be exceeded under continuous normal load conditions. Careful consideration must be given to all sources of thermal resistance from junction to ambient, including junction-to-case, case-to-heat sink interface and heat sink resistance itself.

See Figure 3. The SOP-8-P is a cost-effective package featuring a small size as a standard SOP-8 and a bottom thermal pad to minimize the thermal resistance of the package, being applicable to high current applications. The thermal pad is soldered to the top VOUT plane which may be connected to internal or bottom VOUT plane by vias to reduce the heat sink thermal resistance. Therefore the printed circuit board (PCB) forms a heat sink and dissipates heat into ambient air.

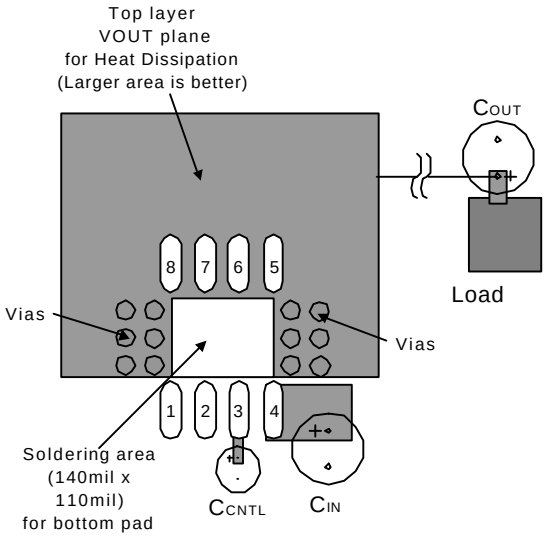
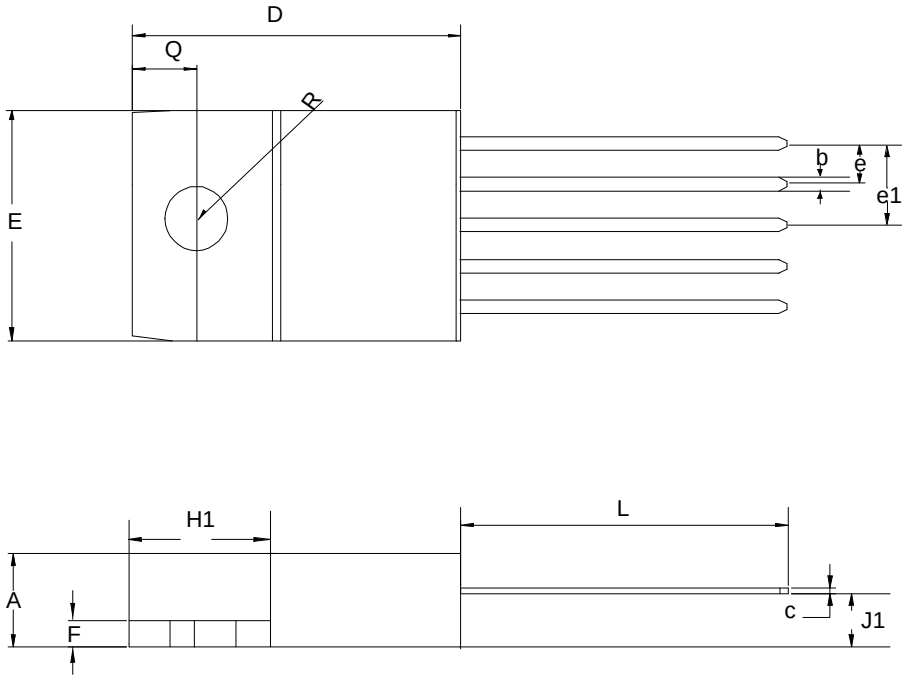


Figure 3 Recommended SOP-8-P Layout

Package Information

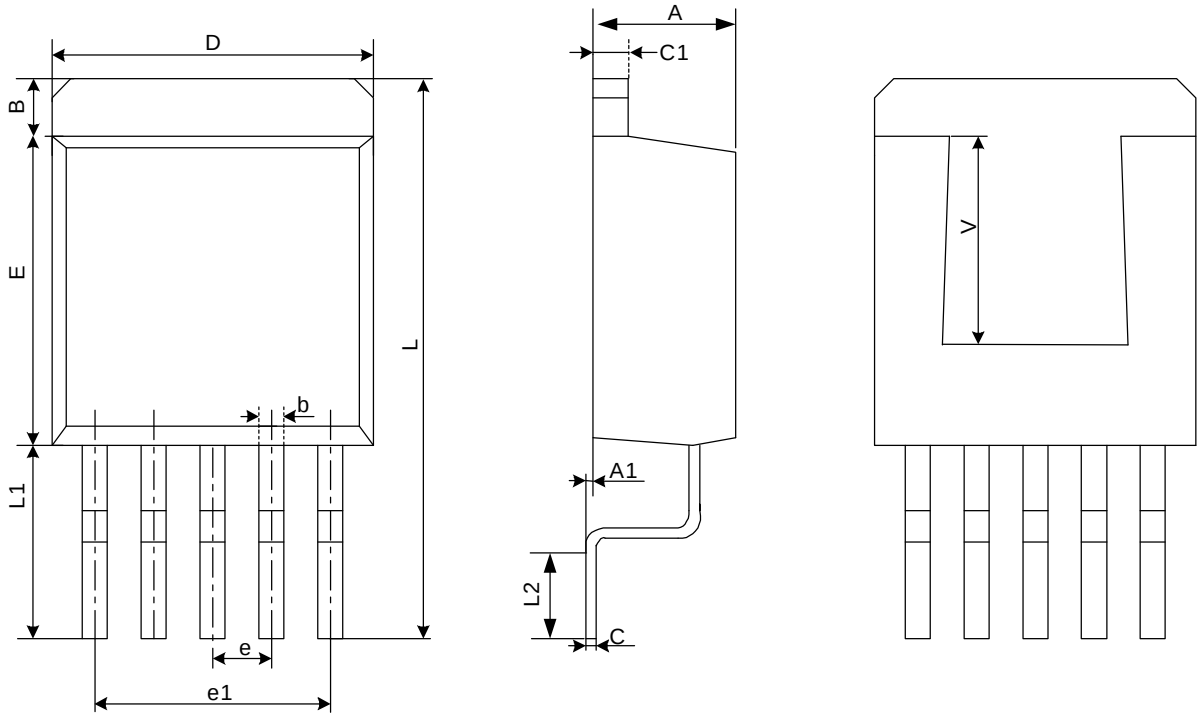
TO-220-5



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	3.55	4.83	0.140	0.190
b	0.63	1.02	0.025	0.040
c	0.35	0.56	0.014	0.022
D	14.22	16.51	0.560	0.650
e	1.57	1.83	0.062	0.072
e1	6.68	6.94	0.263	0.273
E	9.65	10.67	0.380	0.420
F	1.14	1.40	0.045	0.055
H1	5.84	6.60	0.230	0.260
J1	2.03	3.05	0.080	0.120
L	13.72	14.22	0.540	0.560
R	3.53	4.09	0.139	0.161
Q	2.54	3.43	0.100	0.135

Package Information

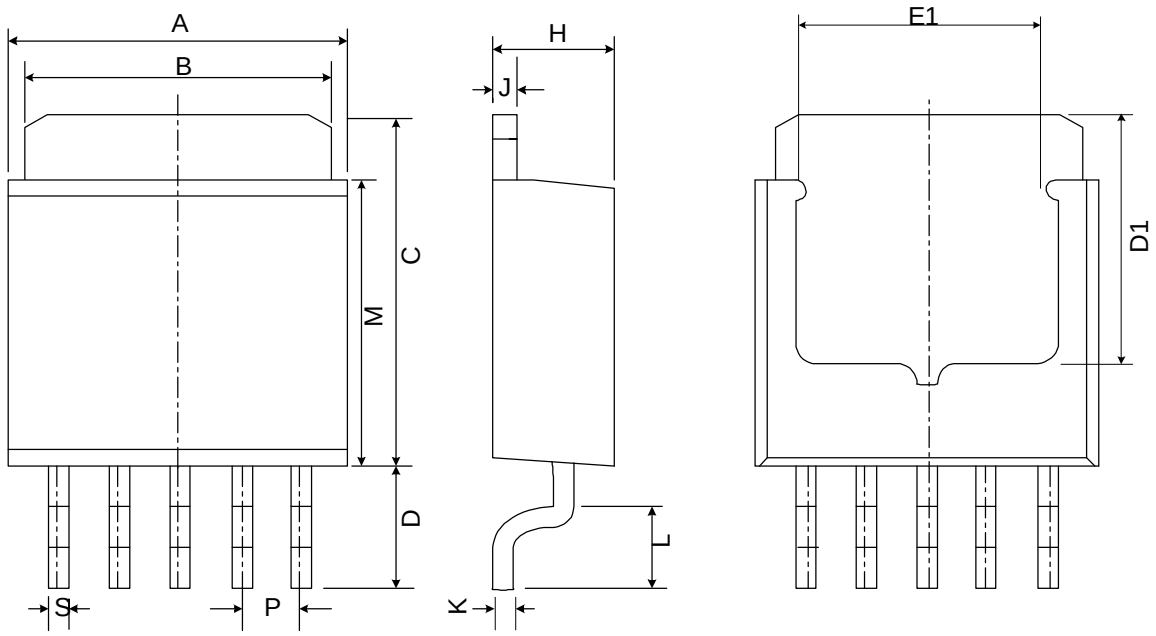
TO-263-5



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	4.06	4.83	0.160	0.190
A1	0.00	0.15	0.000	0.006
B	1.40	1.76	0.055	0.069
b	0.50	0.99	0.020	0.039
C	0.310	0.736	0.012	0.029
C1	1.14	1.40	0.045	0.055
D	9.65	10.29	0.380	0.405
E	8.20	9.66	0.323	0.380
e	1.52	1.83	0.060	0.072
e1	6.70	6.90	0.264	0.272
L	14.60	15.88	0.575	0.625
L1	5.08	5.48	0.200	0.216
L2	2.28	2.80	0.090	0.110
V	5.600REF		0.220REF	

Packaging Information

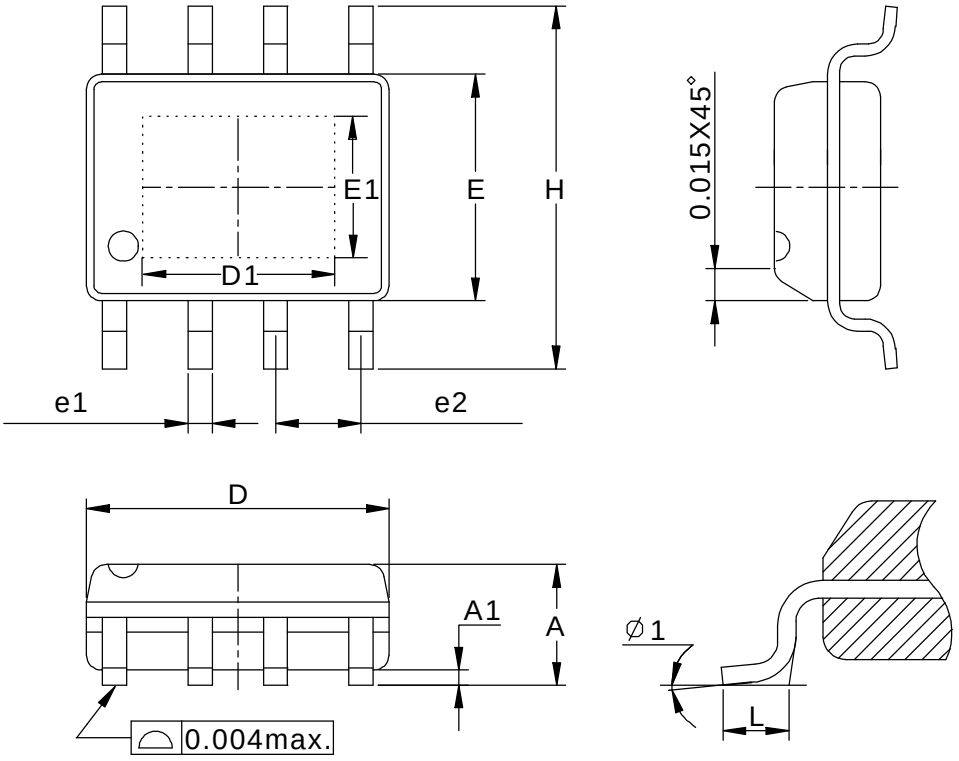
TO-252-5



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	6.40	6.80	0.25	0.26
B	5.20	5.50	0.20	0.21
C	6.80	7.20	0.26	0.27
D	2.20	2.80	0.08	0.11
D1	5.2REF		0.205REF	
E1	5.3REF		0.209REF	
P	1.27REF		0.05REF	
S	0.50	0.80	0.02	0.03
H	2.20	2.40	0.08	0.09
J	0.45	0.55	0.01	0.02
K	0.45	0.60	0.018	0.024
L	0.90	1.50	0.03	0.06
M	5.40	5.80	0.21	0.22

Packaging Information

SOP-8-P pin (Reference JEDEC Registration MS-012)

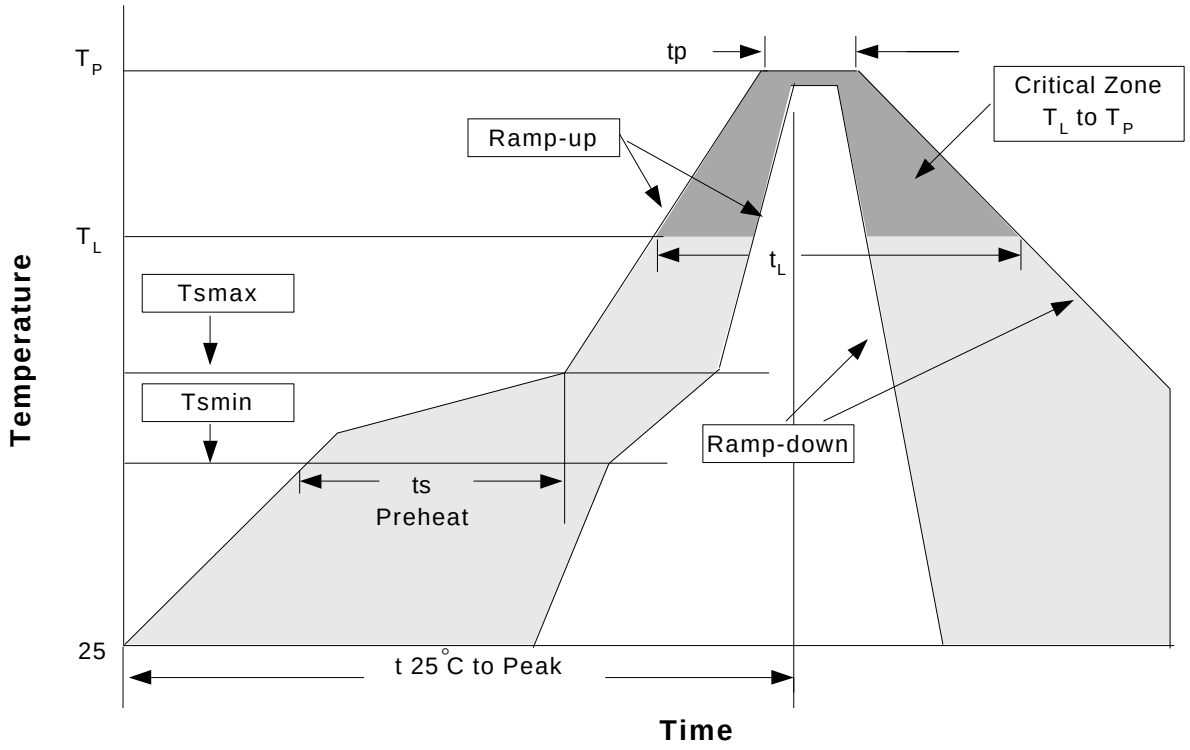


Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0	0.15	0	0.006
D	4.80	5.00	0.189	0.197
D1	3.00REF		0.118REF	
E	3.80	4.00	0.150	0.157
E1	2.60REF		0.102REF	
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
e1	0.33	0.51	0.013	0.020
e2	1.27BSC		0.50BSC	
ϕ 1	8°		8°	

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reflow Condition (IR/Convection or VPR Reflow)



Classificatin Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classificatioon Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package .Measured on the body surface.

Classificatin Reflow Profiles(Cont.)

Table 1. SnPb Entectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

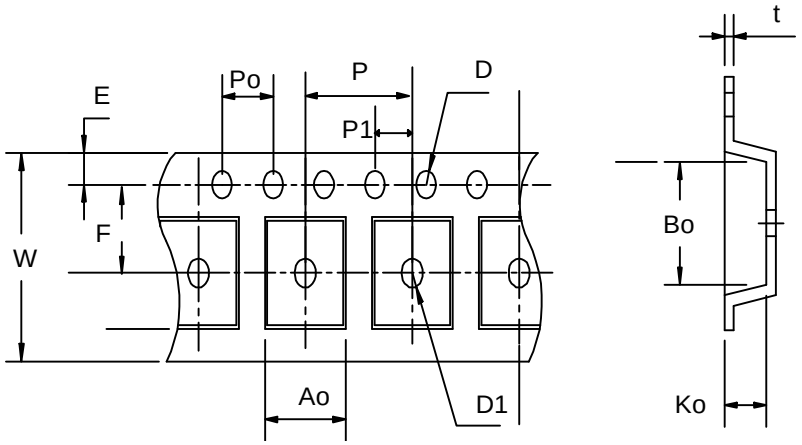
Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*
*Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.			

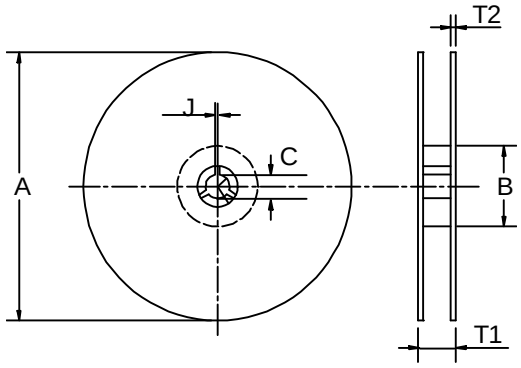
Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B,A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Carrier Tape & Reel Dimension



Carrier Tape & Reel Dimension(Cont.)



Application	A	B	C	J	T1	T2	W	P	E
TO-263	380±3	80 ± 2	13 ± 0. 5	2 ± 0.5	24 ± 4	2± 0.3	24 + 0.3 - 0.1	16 ± 0.1	1.75± 0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	11.5 ± 0.1	1.5 +0.1	1.5± 0.25	4.0 ± 0.1	2.0 ± 0.1	10.8 ± 0.1	16.1± 0.1	5.2± 0.1	0.35±0.013
Application	A	B	C	J	T1	T2	W	P	E
TO-252	330 ±3	100 ± 2	13 ± 0. 5	2 ± 0.5	16.4 + 0.3 -0.2	2.5± 0.5	16+ 0.3 - 0.1	8 ± 0.1	1.75± 0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	7.5 ± 0.1	1.5 +0.1	1.5± 0.25	4.0 ± 0.1	2.0 ± 0.1	6.8 ± 0.1	10.4± 0.1	2.5± 0.1	0.3±0.05
Application	A	B	C	J	T1	T2	W	P	E
SOP- 8-P	330 ± 1	62 +1.5	12.75+ 0.15	2 ± 0.5	12.4 ± 0.2	2 ± 0.2	12± 0. 3	8± 0.1	1.75±0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	5.5± 1	1.55 +0.1	1.55+ 0.25	4.0 ± 0.1	2.0 ± 0.1	6.4 ± 0.1	5.2± 0. 1	2.1± 0.1	0.3±0.013

Cover Tape Dimensions

(mm)

Application	Carrier Width	Cover Tape Width	Devices Per Reel
TO- 263	24	21.3	1000
TO- 252	16	13.3	2500
SOP- 8-P	12	9.3	2500

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