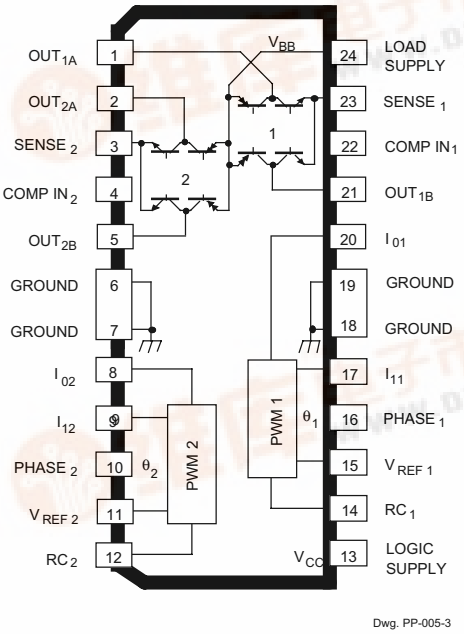
L6219DS

Data Sheet
29319.43D

DUAL FULL-BRIDGE PWM MOTOR DRIVER



ABSOLUTE MAXIMUM RATINGS at $T_J \leq 150°C$

Motor Supply Voltage, V_{BB} ..... **45 V**
Output Current, I_{OUT}
(Peak) ..... **+1.0 A**
(Continuous) ..... **+750 mA**
Logic Supply Voltage, V_{CC} ..... **7.0 V**
Logic Input Voltage Range,
V_{IN} ..... **-0.3 V to V_{CC}+0.3 V**
Output Emitter Voltage, V_{SENSE} ..... **1.5 V**
Package Power Dissipation,
P_D ..... **See Graph**
Operating Temperature Range,
T_A ..... **-20°C to +85°C**
Storage Temperature Range,
T_S ..... **-55°C to +150°C**

Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified peak current rating or a junction temperature of +150°C.

The L6219DS motor driver is designed to drive both windings of a bipolar stepper motor or bidirectionally control two dc motors. Both bridges are capable of sustaining 45 V and include internal pulse-width modulation (PWM) control of the output current to 750 mA. The outputs have been optimized for a low output saturation voltage drop (less than 1.8 V total source plus sink at 500 mA).

For PWM current control, the maximum output current is determined by the user's selection of a reference voltage and sensing resistor. Two logic-level inputs select output current limits of 0, 33, 67, or 100% of the maximum level. A PHASE input to each bridge determines load current direction.

The bridges include both ground clamp and flyback diodes for protection against inductive transients. Internally generated delays prevent cross-over currents when switching current direction. Special power-up sequencing is not required. Thermal protection circuitry disables the outputs if the chip temperature exceeds safe operating limits.

The L6219DS is supplied in a 24-pin surface-mountable SOIC. Its batwing construction provides for maximum package power dissipation in the smallest possible construction. This device is also available on special order for operation from -40°C to +85°C or to +105°C. A lead-free version (100% matte tin leadframe) is also available.

FEATURES

- Interchangeable with SGS L6219DS
- 750 mA Continuous Output Current
- 45 V Output Sustaining Voltage
- Internal Clamp Diodes
- Internal PWM Current Control
- Low Output Saturation Voltage
- Internal Thermal Shutdown Circuitry
- Similar to Dual PBL3717, UC3770

Always order by complete part number:

Part Number	Package
L6219DS	24-pin batwing SOIC
L6219DS-T	24-pin batwing SOIC; Lead-free

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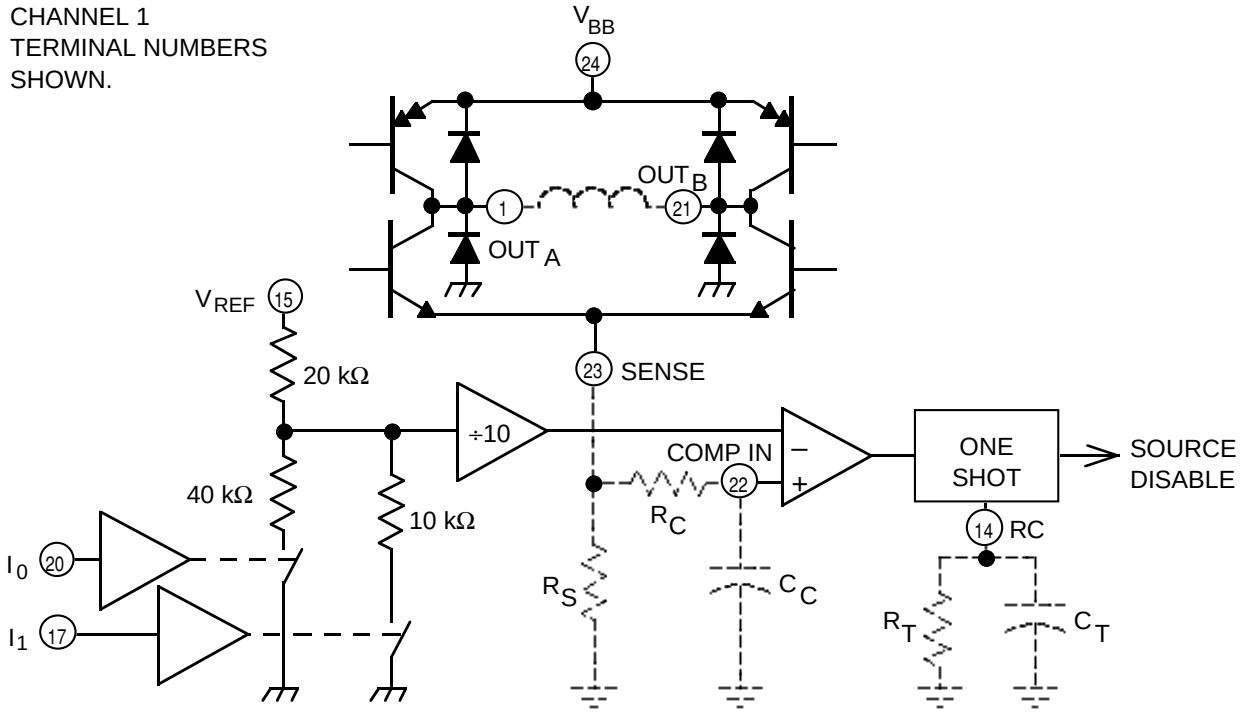
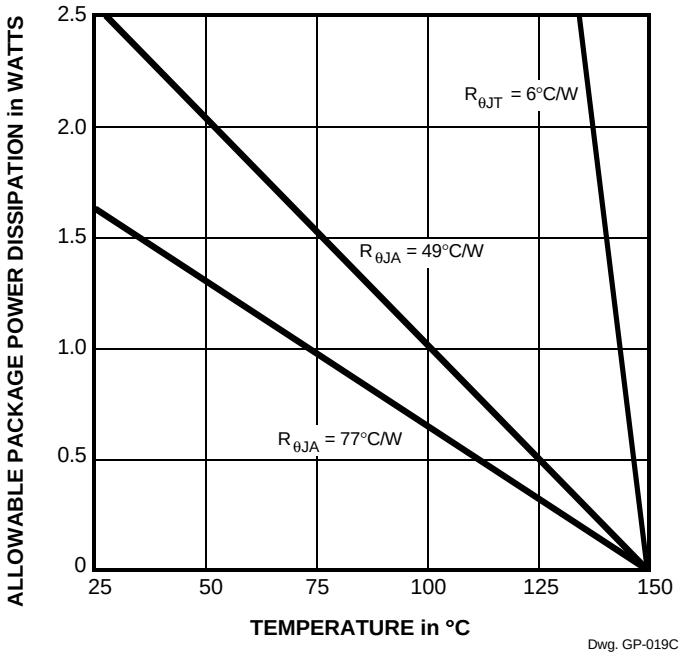
PWM CURRENT-CONTROL CIRCUITRY



Dwg. EP-007-5



Dwg. GP-019C

TRUTH TABLE

PHASE	OUT_A	OUT_B
H	H	L
L	L	H

$R_{\theta JA}$ is measured on typical two-sided PCB with minimal copper ground area (77°C/W) or with 3.57 in^2 copper ground area (49°C/W). See also, Application Note 29501.5, *Improving Batwing Power Dissipation.*

ELECTRICAL CHARACTERISTICS at T_A = +25°C, $T_J \leq$ 150°C, V_{BB} = 45 V, V_{CC} = 4.75 V to 5.25 V, V_{REF} = 5.0 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Drivers (OUT_A or OUT_B)						
Motor Supply Range	V_{BB}		10	—	45	V
Output Leakage Current	I_{CEX}	V_{OUT} = V_{BB}	—	< 1.0	50	µA
		V_{OUT} = 0	—	<-1.0	-50	µA
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = ±750 mA, L = 3.0 mH	45	—	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	Sink Driver, I_{OUT} = +500 mA	—	0.4	0.6	V
		Sink Driver, I_{OUT} = +750 mA	—	1.0	1.2	V
		Source Driver, I_{OUT} = -500 mA	—	1.0	1.2	V
		Source Driver, I_{OUT} = -750 mA	—	1.3	1.5	V
Clamp Diode Leakage Current	I_R	V_R = 45 V	—	< 1.0	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 750 mA	—	1.6	2.0	V
Driver Supply Current	$I_{BB(ON)}$	Both Bridges On, No Load	—	20	25	mA
	$I_{BB(OFF)}$	Both Bridges Off	—	5.0	10	mA
Control Logic						
Input Voltage	$V_{IN(1)}$	All inputs	2.4	—	—	V
	$V_{IN(0)}$	All inputs	—	—	0.8	V
Input Current	$I_{IN(1)}$	V_{IN} = 2.4 V	—	<1.0	20	µA
		V_{IN} = 0.8 V	—	- 3.0	-200	µA
Reference Voltage Range	V_{REF}	Operating	1.5	—	7.5	V
Current Limit Threshold (at trip point)	V_{REF}/V_{COMPIN}	I_0 = I_1 = 0.8 V	9.5	10	10.5	—
		I_0 = 2.4 V, I_1 = 0.8 V	13.5	15	16.5	—
		I_0 = 0.8 V, I_1 = 2.4 V	25.5	30	34.5	—
Thermal Shutdown Temperature	T_J		—	170	—	°C
Total Logic Supply Current	$I_{CC(ON)}$	I_0 = I_1 = 0.8 V, No Load	—	40	50	mA
	$I_{CC(OFF)}$	I_0 = I_1 = 2.4 V, No Load	—	10	14	mA
Fixed Off-Time	t_{off}	R_T = 56 kΩ, C_T = 820 pF	—	46	—	µs

APPLICATIONS INFORMATION

PWM CURRENT CONTROL

The L6219DS dual bridge is designed to drive both windings of a bipolar stepper motor. Output current is sensed and controlled independently in each bridge by an external sense resistor (R_S), internal comparator, and monostable multivibrator.

When the bridge is turned on, current increases in the motor winding and it is sensed by the external sense resistor until the sense voltage (V_{COMPIN}) reaches the level set at the comparator's input:

$$I_{TRIP} = V_{REF}/10\ R_S$$

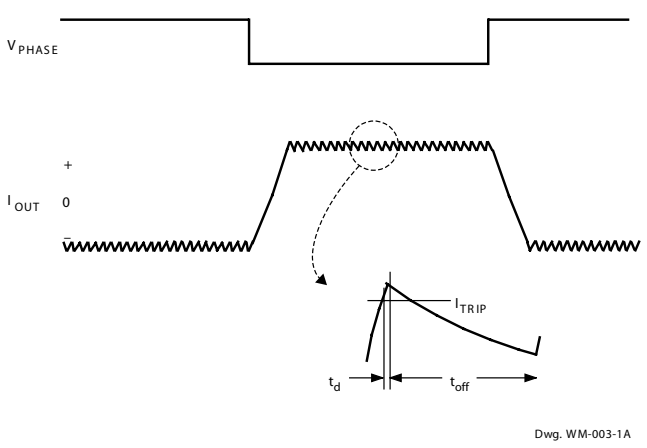
The comparator then triggers the monostable which turns off the source driver of the bridge. The actual load current peak will be slightly higher than the trip point (especially for low-inductance loads) because of the internal logic and switching delays. This delay (t_d) is typically 2 µs. After turn-off, the motor current decays, circulating through the ground-clamp diode and sink transistor. The source driver's off time (and therefore the magnitude of the current decrease) is determined by the monostable's external RC timing components, where $t_{off} = R_T C_T$ within the range of 20 kΩ to 100 kΩ and 100 pF to 1000 pF.

The fixed-off time should be short enough to keep the current chopping above the audible range (< 46 µs) and long enough to properly regulate the current. Because only slow-decay current control is available, short off times (< 10 µs) require additional efforts to ensure proper current regulation. Factors that can negatively affect the ability to properly regulate the current when using short off times include: higher motor-supply voltage, light load, and longer than necessary blank time.

When the source driver is re-enabled, the winding current (the sense voltage) is again allowed to rise to the comparator's threshold. This cycle repeats itself, maintaining the average motor winding current at the desired level.

Loads with high distributed capaci-tances may result in high turn-on current peaks. This peak (appearing across R_S) will attempt to trip the comparator, resulting in erroneous current control or high-frequency oscillations. An external $R_C C_C$ time delay should be used to further delay the action of the comparator. Depending on load type, many applications will not require these external components (SENSE connected to COMP IN).

PWM OUTPUT CURRENT WAVE FORM



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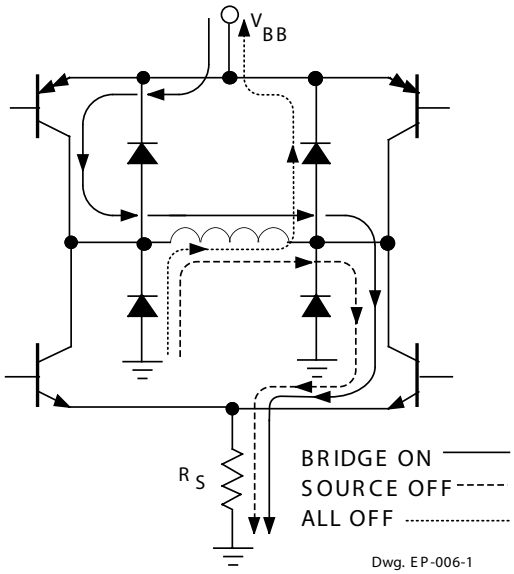
LOAD CURRENT PATHS



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LOGIC CONTROL OF OUTPUT CURRENT

Two logic level inputs (I_0 and I_1) allow digital selection of the motor winding current at 100%, 67%, 33%, or 0% of the maximum level per the table. The 0% output current condition turns off all drivers in the bridge and can be used as an OUTPUT ENABLE function.

CURRENT-CONTROL TRUTH TABLE

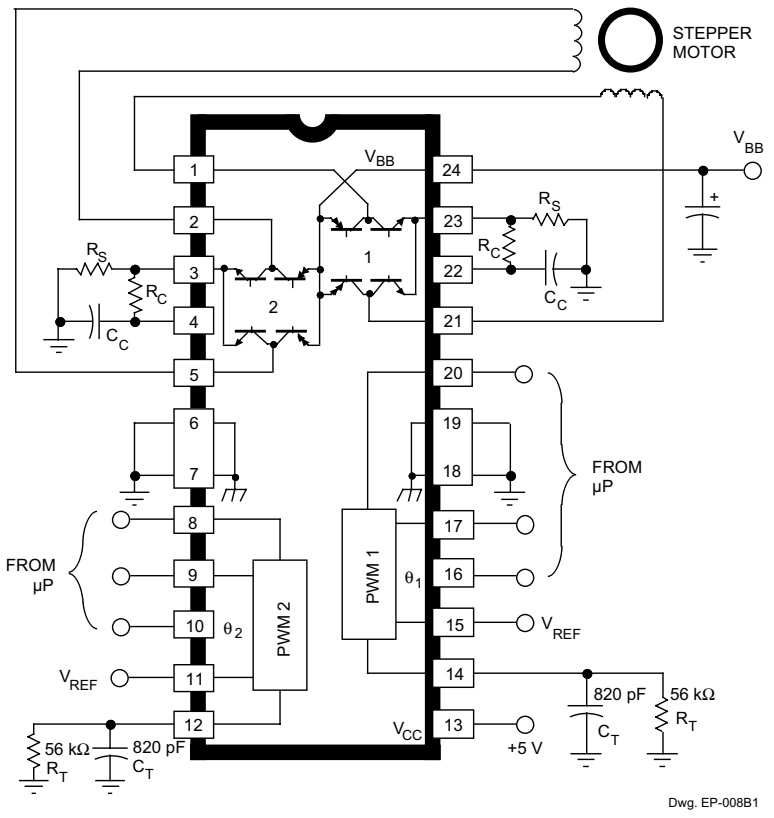
I_0	I_1	Output Current
L	L	$V_{REF}/10\ R_S = I_{TRIP}$
H	L	$V_{REF}/15\ R_S = 2/3\ I_{TRIP}$
L	H	$V_{REF}/30\ R_S = 1/3\ I_{TRIP}$
H	H	0

These logic level inputs greatly enhance the implementation of µP-controlled drive formats.

During half-step operations, the I_0 and I_1 allow the µP to control the motor at a constant torque between all positions in an eight-step sequence. This is accomplished by digitally selecting 100% drive current when only one phase is on and 67% drive current when two phases are on. Logic highs on both I_0 and I_1 turn off all drivers to allow rapid current decay when switching phases. This helps to ensure proper motor operation at high step rates.

The logic control inputs can also be used to select a reduced current level (and reduced power dissipation) for 'hold' conditions and/or increased current (and available torque) for start-up conditions.

TYPICAL APPLICATION



GENERAL

The PHASE input to each bridge determines the direction motor winding current flows. An internally generated deadtime (approximately 2 µs) prevents crossover currents that can occur when switching the PHASE input.

All four drivers in the bridge output can be turned off between steps ($I_0 = I_1 \bullet 2.4$ V) resulting in a fast current decay through the internal output clamp and flyback diodes. The fast current decay is desirable in half-step and high-speed applications. The PHASE, I_0,and I_1 inputs float high.

Varying the reference voltage (V_{REF}) provides continuous control of the peak load current for microstepping applications.

Thermal protection circuitry turns off all drivers when the junction temperature reaches +170°C. It is only intended to protect the device from failures due to excessive junction temperature and should not imply that output short circuits are permitted. The output drivers are re-enabled when the junction temperature cools to +145°C.

The L6219DS output drivers are optimized for low output saturation voltages—less than 1.8 V total (source plus sink) at 500 mA. Under normal operating conditions, when combined with the excellent thermal properties of the batwing package design, this allows continuous operation of both bridges simultaneously at 500 mA.

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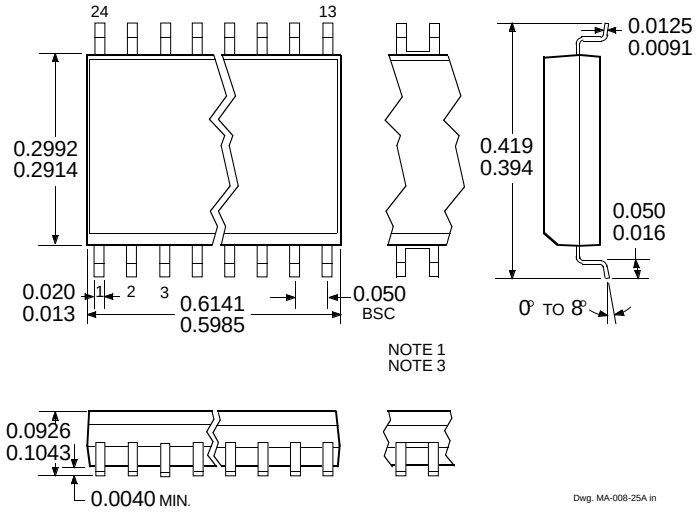
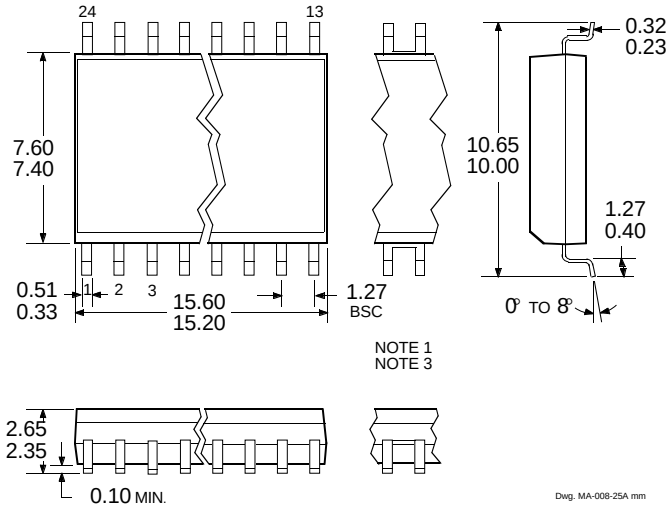
Dimensions in Inches
(for reference only)



Dimensions in Millimeters
(controlling dimensions)



NOTES:
1. Webbed lead frame. Leads indicated are internally one piece.
2. Lead spacing tolerance is non-cumulative.
3. Exact body and lead configuration at vendor's option within limits shown.
4. Supplied in standard sticks/tubes of 31 devices or add "TR" to part number for tape and reel.

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BRIDGE & HALF-BRIDGE DRIVERS

IN ORDER OF 1) OUTPUT CURRENT AND 2) OUTPUT VOLTAGE

Output Ratings *			Features			
mA	V	Description	Internal Diodes	Outputs	Internal Protection	Part Number †
±500	18	dual PWM full bridge	X	DMOS	X	3965
±650	30	dual PWM full bridge	X	bipolar	X	3966
	30	dual PWM full bridge	X	bipolar	X	3968
±750	30	dual microstepping full bridge	X	Darlington/Satlington™	X	3967
	45	dual PWM full bridge	X	bipolar	X	2916
	45	dual PWM full bridge	X	bipolar	X	2919
	45	dual PWM full bridge	X	bipolar	X	6219
±800	33	dual PWM full bridge	X	bipolar	X	3964
±1300	50	PWM full bridge	X	bipolar	X	3953
±1500	45	dual PWM full bridge	X	bipolar	X	2917
	50	PWM full bridge	sync rect	DMOS	X	3948
	50	microstepping full bridge	X	Darlington/Satlington™	X	3955
	50	microstepping full bridge	X	Darlington/Satlington™	X	3957
	50	dual PWM full bridge	sync rect	DMOS	X	3974
±2000	50	PWM full-bridge	X	Darlington	X	3952
	50	PWM full-bridge	sync rect	DMOS	X	3958
±2500	35	dual microstepping full bridge	sync rect	DMOS	X	3977
±3000	50	3-Ø PWM driver	sync rect	DMOS	X	3936
—	50	PWM full-bridge	sync rect	DMOS	X	3959
—	28	3-Ø MOSFET controller	–	DMOS	X	3933
—	40	3-Ø MOSFET controller	–	DMOS	X	3935
—	50	3-Ø MOSFET controller	–	DMOS	X	3932
—	50	3-Ø MOSFET controller	–	DMOS	X	3938

* Current is maximum specified test condition, voltage is maximum rating. See specification for sustaining voltage limits or over-current protection voltage limits.

† Complete part number includes additional characters to indicate operating temperature range and package style.

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DUAL FULL-BRIDGE MOTOR DRIVER

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