6818

DABiC-IV, 32-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER

The A6818– devices combine a 32-bit CMOS shift register, accompanying data latches and control circuitry with bipolar sourcing outputs and pnp active pull downs. Designed primarily to drive vacuum-fluorescent displays, the 60 V and - 40 mA output ratings also allow these devices to be used in many other peripheral power driver applications. The A6818– features an increased data input rate (compared with the older UCN/UCQ5818–F) and a controlled output slew rate.

The CMOS shift register and latches allow direct interfacing with micro-processor-based systems. With a 3.3 V or 5 V logic supply, typical serial-data input rates are up to 33 MHz.

A CMOS serial data output permits cascade connections in applications requiring additional drive lines. Similar devices are available as the A6810– (10 bits) and A6812– (20 bits).

The A6818– output source drivers are npn Darlingtons, capable of sourcing up to 40 mA. The controlled output slew rate reduces electromagnetic noise, which is an important consideration in systems that include telecommunications and/or microprocessors and to meet government emissions regulations. For inter-digit blanking, all output drivers can be disabled and all sink drivers turned on with a BLANKING input high. The pnp active pull-downs will sink at least 2.5 mA.

Three temperature ranges are available for optimum performance in commercial (suffix S-), industrial (E-), and extended industrial (K-) applications. The package style provided is the minimum-area surface-mount PLCC (suffix -EP). Copper lead frames, low logic-power dissipation, and low output-saturation voltages allow these devices to drive most multiplexed vacuum-fluorescent displays over the maximum operating temperature range.

The lead (Pb) free versions have 100% matte tin leadframe plating.

A6818xEP
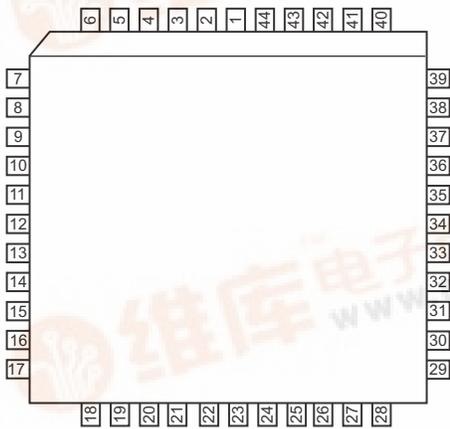
ABSOLUTE MAXIMUM RATINGS
at T_A = 25°C

Logic Supply Voltage, V_{DD} .... **7.0 V**
Driver Supply Voltage, V_{BB} .... **60 V**
Continuous Output Current Range,
    I_{OUT} .... **-40 mA to +15 mA**
Input Voltage Range,
    V_{IN} .... **-0.3 V to V_{DD} + 0.3 V**
Package Power Dissipation,
    P_D .... **See Graph**
Operating Temperature Range, T_A
    (Suffix 'E–') .... **-40°C to +85°C**
    (Suffix 'K–') .... **-40°C to +125°C**
    (Suffix 'S–') .... **-20°C to +85°C**
Storage Temperature Range,
    T_S .... **-55°C to +125°C**

Caution: These CMOS devices have input static protection (Class 2) but are still susceptible to damage if exposed to extremely high static electrical charges.

FEATURES

- Controlled Output Slew Rate
- 60 V Minimum Output Breakdown
- PNP Active Pull-Downs
- Low-Power CMOS Logic and Latches
- High-Speed Data Storage
- High Data Input Rate
- Low Output-Saturation Voltages
- Improved Replacements for SN75518N, SN75518NF, UCN5818–, and UCQ5818–
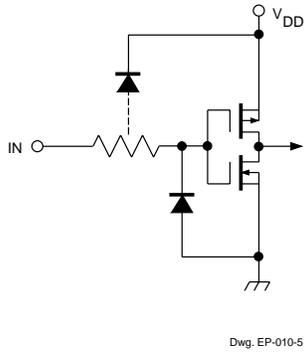
Always order by complete part number:

Part Number	Pb-free	Packing	Ambient Temperature, T_A (°C)
A6818EEP	–	27 pieces/tube	
A6818EEP-T	Yes		
A6818EEPTR	–	450 pieces/13-in. reel	–40 to 85
A6818EEPTR-T	Yes		
A6818KEP	–	27 pieces/tube	
A6818KEP-T	Yes		
A6818KEPTR	–	450 pieces/13-in. reel	–40 to 125
A6818KEPTR-T	Yes		
A6818SEP	–	27 pieces/tube	
A6818SEP-T	Yes		
A6818SEPTR	–	450 pieces/13-in. reel	–20 to 85
A6818SEPTR-T	Yes		

Allegro

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32-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER

TYPICAL INPUT CIRCUIT

Dwg. EP-010-5

A6818xEP

Dwg. PP-059-2

TYPICAL OUTPUT DRIVER

Dwg. EP-021-19

SUFFIX 'EP', $R_{\theta JA} = 54°C/W$

Dwg. GP-025B
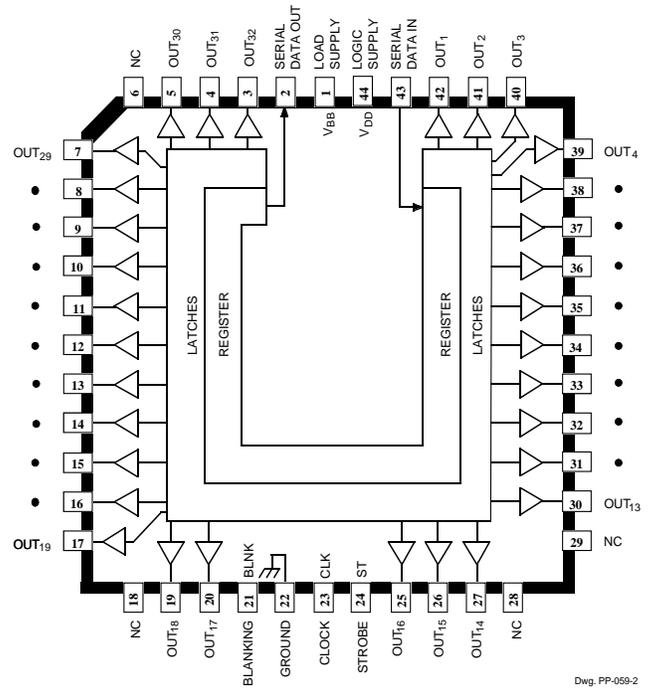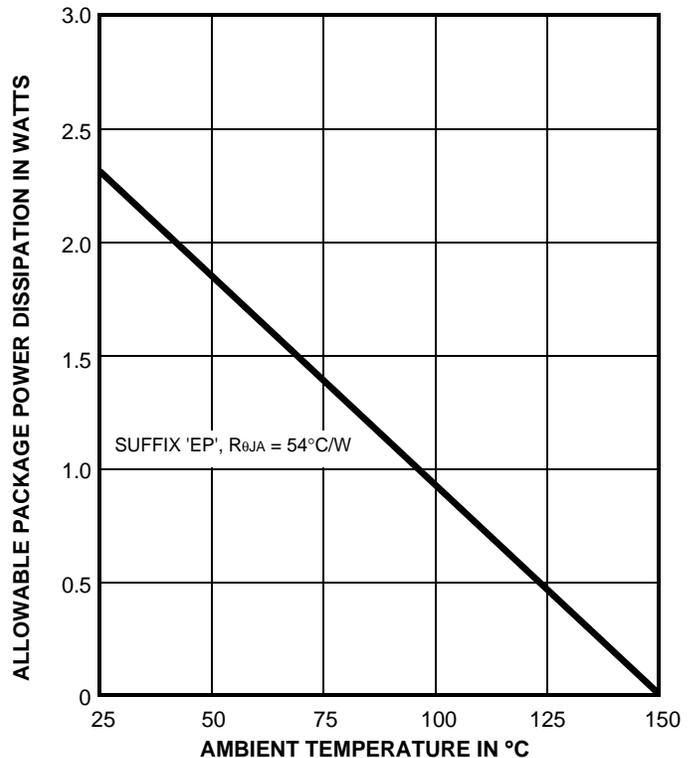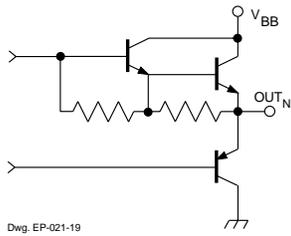
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32-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER

FUNCTIONAL BLOCK DIAGRAM

CLOCK

SERIAL DATA IN

STROBE

BLANKING

SERIAL-PARALLEL SHIFT REGISTER

LATCHES

V_{DD} — LOGIC SUPPLY

SERIAL DATA OUT

MOS
BIPOLAR

V_{BB} — LOAD SUPPLY

GROUND   OUT$_1$ OUT$_2$ OUT$_3$ OUT$_N$
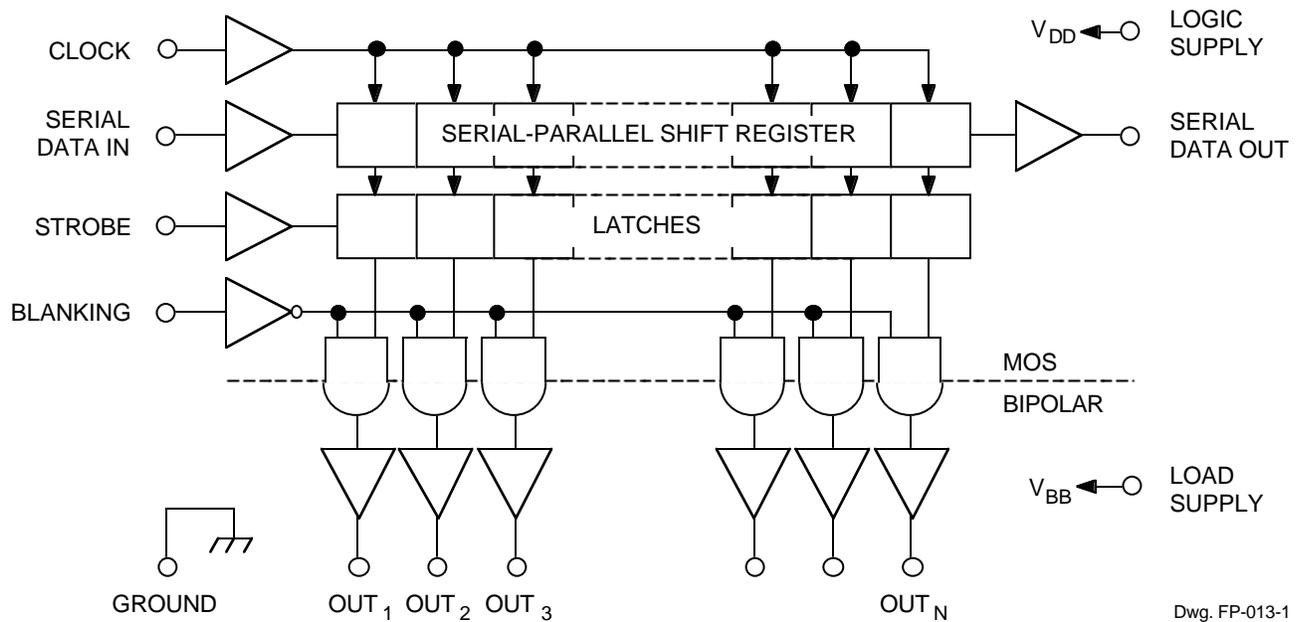
Dwg. FP-013-1

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents I_1 I_2 I_3 ... I_{N-1} I_N	Serial Data Output	Strobe Input	Latch Contents I_1 I_2 I_3 ... I_{N-1} I_N	Blanking	Output Contents I_1 I_2 I_3 ... I_{N-1} I_N
H	⌐	H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L	⌐	L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X	⌐	R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	L	P_1 P_2 P_3 ... P_{N-1} P_N
					X X X ... X X	H	L L L ... L L

L = Low Logic Level   H = High Logic Level   X = Irrelevant   P = Present State   R = Previous State

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32-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER

ELECTRICAL CHARACTERISTICS at T$_A$ = +25°C (A6818S-) or over operating temperature range (A6818E- and A6818K-), V$_{BB}$ = 60 V unless otherwise noted.

Characteristic	Symbol	Test Conditions	Limits @ V$_{DD}$ = 3.3 V			Limits @ V$_{DD}$ = 5 V			Units
			MIn.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I$_{CEX}$	V$_{OUT}$ = 0 V	—	<-0.1	-15	—	<-0.1	-15	µA
Output Voltage	V$_{OUT(1)}$	I$_{OUT}$ = -25 mA	57.5	58.3	—	57.5	58.3	—	V
	V$_{OUT(0)}$	I$_{OUT}$ = 1 mA	—	1.0	1.5	—	1.0	1.5	V
Output Pull-Down Current	I$_{OUT(0)}$	V$_{OUT}$ = 5 V to V$_{BB}$	2.5	5.0	—	2.5	5.0	—	mA
Input Voltage	V$_{IN(1)}$		2.2	—	—	3.3	—	—	V
	V$_{IN(0)}$		—	—	1.1	—	—	1.7	V
Input Current	I$_{IN(1)}$	V$_{IN}$ = V$_{DD}$	—	<0.01	1.0	—	<0.01	1.0	µA
	I$_{IN(0)}$	V$_{IN}$ = 0.8 V	—	<-0.01	-1.0	—	<-0.01	-1.0	µA
Input Clamp Voltage	V$_{IK}$	I$_{IN}$ = -200 µA	—	-0.8	-1.5	—	-0.8	-1.5	V
Serial Data Output Voltage	V$_{OUT(1)}$	I$_{OUT}$ = -200 µA	2.8	3.05	—	4.5	4.75	—	V
	V$_{OUT(0)}$	I$_{OUT}$ = 200 µA	—	0.15	0.3	—	0.15	0.3	V
Maximum Clock Frequency	f$_c$		10	33	—	10	33	—	MHz
Logic Supply Current	I$_{DD(1)}$	All Outputs High	—	0.25	0.75	—	0.3	1.0	mA
	I$_{DD(0)}$	All Outputs Low	—	0.25	0.75	—	0.3	1.0	mA
Load Supply Current	I$_{BB(1)}$	All Outputs High, No Load	—	4.5	9.0	—	4.5	9.0	mA
	I$_{BB(0)}$	All Outputs Low	—	0.2	20	—	0.2	20	µA
Blanking-to-Output Delay	t$_{dis(BQ)}$	C$_L$ = 30 pF, 50% to 50%	—	0.7	2.0	—	0.7	2.0	µs
	t$_{en(BQ)}$	C$_L$ = 30 pF, 50% to 50%	—	1.8	3.0	—	1.8	3.0	µs
Strobe-to-Output Delay	t$_{p(STH-QL)}$	R$_L$ = 2.3 kΩ, C$_L$ ≤ 30 pF	—	0.7	2.0	—	0.7	2.0	µs
	t$_{p(STH-QH)}$	R$_L$ = 2.3 kΩ, C$_L$ ≤ 30 pF	—	1.8	3.0	—	1.8	3.0	µs
Output Fall Time	t$_f$	R$_L$ = 2.3 kΩ, C$_L$ ≤ 30 pF	2.4	—	12	2.4	—	12	µs
Output Rise Time	t$_r$	R$_L$ = 2.3 kΩ, C$_L$ ≤ 30 pF	2.4	—	12	2.4	—	12	µs
Output Slew Rate	dV/dt	R$_L$ = 2.3 kΩ, C$_L$ ≤ 30 pF	4.0	—	20	4.0	—	20	V/µs
Clock-to-Serial Data Out Delay	t$_{p(CH-SQX)}$	I$_{OUT}$ = ±200 µA	—	50	—	—	50	—	ns

Negative current is defined as coming out of (sourcing) the specified device terminal.

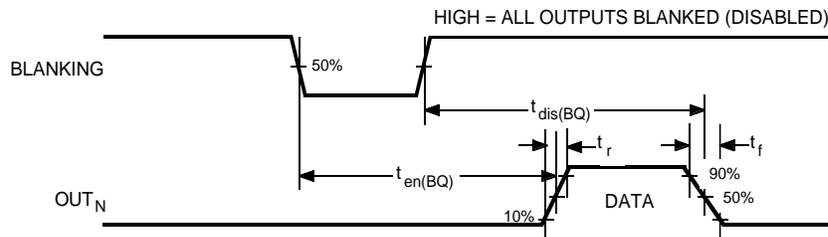Typical data is is for design information only and is at T$_A$ = +25°C.

TIMING REQUIREMENTS and SPECIFICATIONS
(Logic Levels are V_{DD} and Ground)
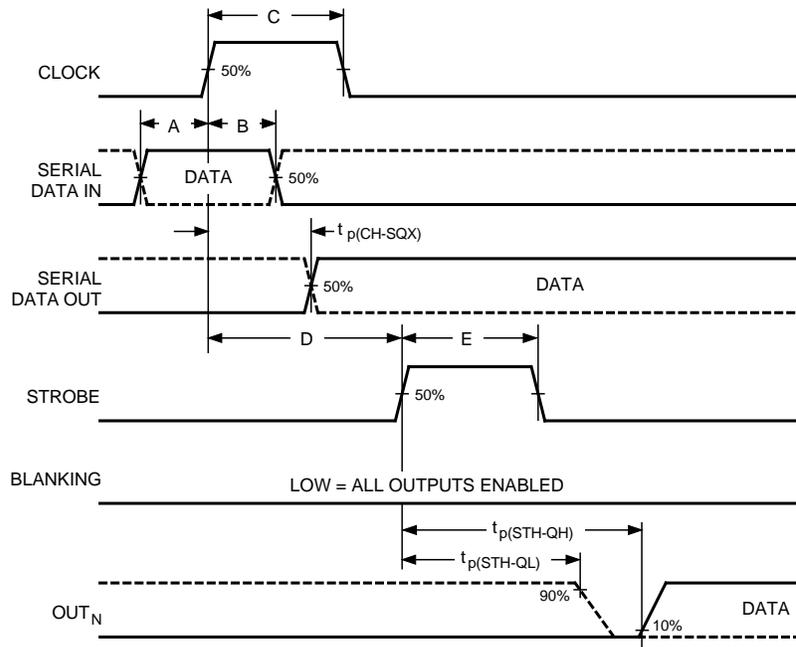
Dwg. WP-029

Dwg. WP-030A

A. Data Active Time Before Clock Pulse
(Data Set-Up Time), $t_{su(D)}$ .... **25 ns**
B. Data Active Time After Clock Pulse
(Data Hold Time), $t_{h(D)}$ .... **25 ns**
C. Clock Pulse Width, $t_{w(CH)}$ .... **50 ns**
D. Time Between Clock Activation and Strobe, $t_{su(C)}$ .... **100 ns**
E. Strobe Pulse Width, $t_{w(STH)}$ .... **50 ns**

NOTE – Timing is representative of a 10 MHz clock. Significantly higher speeds are attainable.

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.
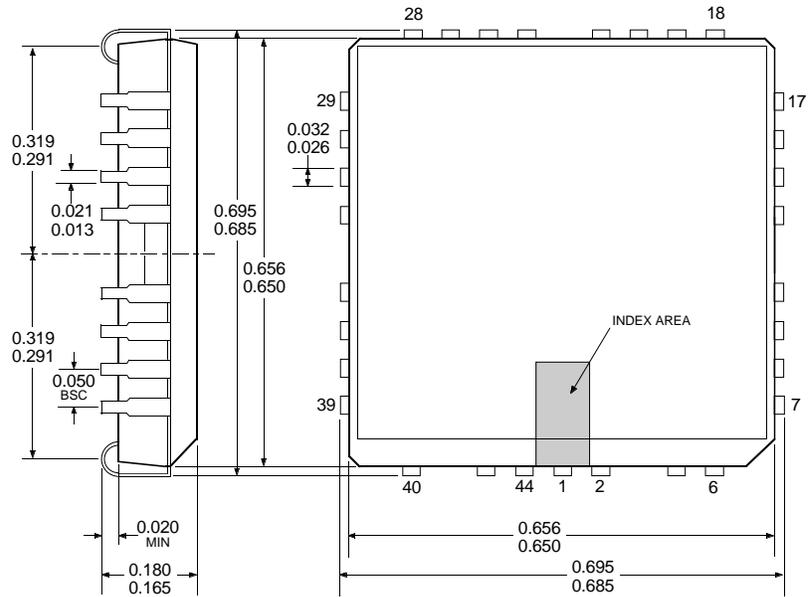
Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the pnp active pull-down sink drivers are ON. The information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

A6818EEP & A6818SEP

Dimensions in Inches
(controlling dimensions)

28   18

29

17

0.319
0.291

0.032
0.026

0.021
0.013

0.695
0.685

0.656
0.650

0.319
0.291

INDEX AREA

0.050
BSC

39   7

40   44   1   2   6

0.020
MIN

0.656
0.650

0.180
0.165

0.695
0.685

Dwg. MA-005-44A in

Dimensions in Millimeters
(for reference only)

28   18

29

17

8.10
7.39

0.812
0.661

0.533
0.331

17.65
17.40

16.662
16.510

8.10
7.39

INDEX AREA

1.27
BSC

39   7

40   44   1   2   6

0.51
MIN

16.662
16.510

4.57
4.20

17.65
17.40
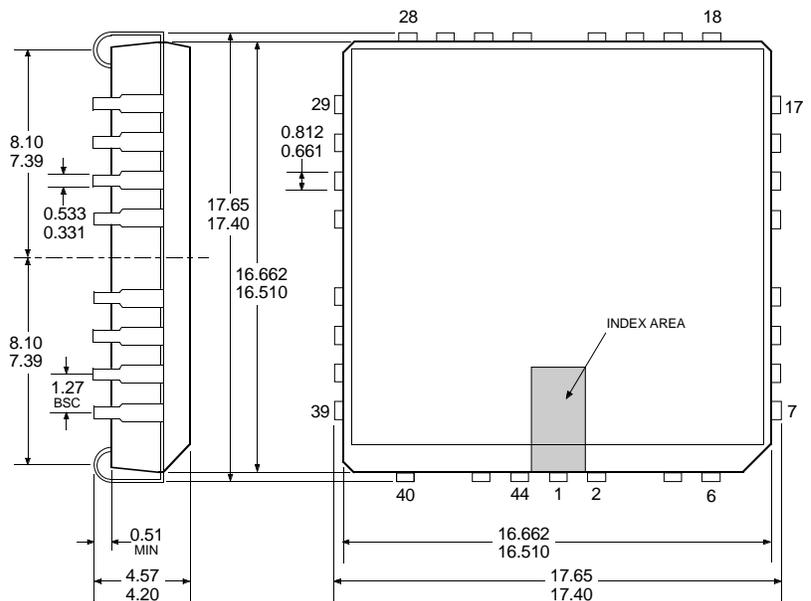
Dwg. MA-005-44A mm

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
        2. Lead spacing tolerance is non-cumulative.

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