*dB*Cool™ Remote Thermal Controller and Voltage Monitor

ADT7476

FEATURES

- Monitors up to 5 voltages
- Controls and monitors up to 4 fans
- High and low frequency fan drive signal
- 1 on-chip and 2 remote temperature sensors
- Series resistance cancellation on the remote channel
- Extended temperature measurement range up to 191°C
- Automatic fan speed control mode controls system cooling based on measured temperature
- Enhanced acoustic mode dramatically reduces user perception of changing fan speeds
- Thermal protection feature via $\overline{\text{THERM}}$ output
- Monitors performance impact of Intel® Pentium™ 4 processor
- Thermal control circuit via $\overline{\text{THERM}}$ input
- 3-wire, and 4-wire fan speed measurement
- Limit comparison of all monitored values
- Meets SMBus 2.0 electrical specifications

GENERAL DESCRIPTION

The ADT7476 *dB*COOL controller is a thermal monitor and multiple PWM fan controller for noise-sensitive or power-sensitive applications requiring active system cooling. The ADT7476 can drive a fan using either a low or high frequency drive signal, monitor the temperature of up to two remote sensor diodes plus its own internal temperature, and measure and control the speed of up to four fans, so they operate at the lowest possible speed for minimum acoustic noise.

The automatic fan speed control loop optimizes fan speed for a given temperature. The effectiveness of the system's thermal solution can be monitored using the $\overline{\text{THERM}}$ input. The ADT7476 also provides critical thermal protection to the system using the bidirectional $\overline{\text{THERM}}$ pin as an output to prevent system or component overheating.

FUNCTIONAL BLOCK DIAGRAM

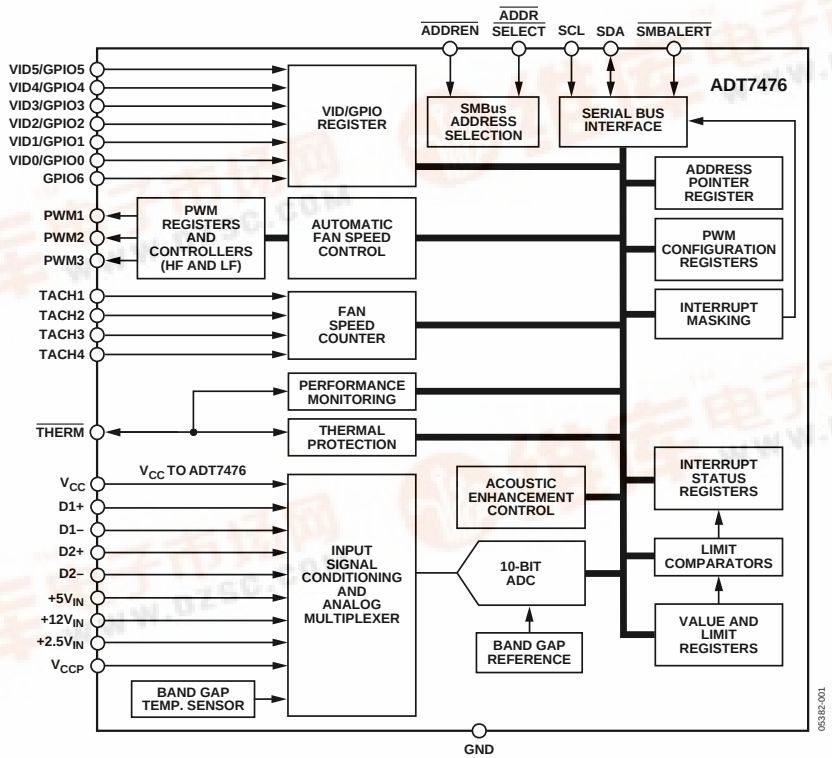

Figure 1.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com

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REVISION HISTORY

4/05—Revision 0: Initial Version

SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted.

All voltages are measured with respect to GND, unless otherwise specified. Typical voltages are $T_A = 25°C$ and probably represent a parametric norm. Logic inputs accept input high voltages up to V_{MAX}, even when the device is operating down to V_{MIN}. Timing specifications are tested at logic levels of $V_{IL} = 0.8$ V for a falling edge, and $V_{IH} = 2.0$ V for a rising edge. SMBus timing specifications are guaranteed by design and are not production tested.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY					
Supply Voltage	3.0	3.3	3.6	V	
Supply Current, I_{CC}		1.5	3	mA	Interface inactive, ADC active
TEMP-TO-DIGITAL CONVERTER					
Local Sensor Accuracy		±0.5	±1.5	°C	$0°C \le T_A \le 85°C$
			±2.5	°C	$-40°C \le T_A \le 125°C$
Resolution		0.25		°C	
Remote Diode Sensor Accuracy		±0.5	±1.5	°C	$0°C \le T_A \le 85°C$
			±2.5	°C	$-40°C \le T_A \le 125°C$
Resolution		0.25		°C	
Remote Sensor Source Current		180		µA	High level
		11		µA	Low level
ANALOG-TO-DIGITAL CONVERTER (INCLUDING MUX AND ATTENUATORS)					
Total Unadjusted Error (TUE)			±2	%	For 12 V channel
			±1.5	%	For all other channels
Differential Nonlinearity (DNL)			±1	LSB	8 bits
Power Supply Sensitivity		±0.1		%/V	
Conversion Time (Voltage Input)		11		ms	Averaging enabled
Conversion Time (Local Temperature)		12		ms	Averaging enabled
Conversion Time (Remote Temperature)		38		ms	Averaging enabled
Total Monitoring Cycle Time		145		ms	Averaging enabled
Total Monitoring Cycle Time		19		ms	Averaging disabled
Input Resistance	90	120		kΩ	For V_{CCP} channel
	90	114		kΩ	For all other channels
FAN RPM-TO-DIGITAL CONVERTER					
Accuracy			±6	%	$0°C \le T_A \le 70°C$
			±10	%	$-40°C \le T_A \le +120°C$
Full-Scale Count			65,535		
Nominal Input RPM		109		RPM	Fan count = 0xBFFF
		329		RPM	Fan count = 0x3FFF
		5,000		RPM	Fan count = 0x0438
		10,000		RPM	Fan count = 0x021C
OPEN-DRAIN DIGITAL OUTPUTS, PWM1 TO PWM3, XTO					
Current Sink, I_{OL}			8.0	mA	
Output Low Voltage, V_{OL}			0.4	V	$I_{OUT} = -8.0$ mA
High Level Output Current, I_{OH}		0.1	20	µA	$V_{OUT} = V_{CC}$
OPEN-DRAIN SERIAL DATA BUS OUTPUT (SDA)					
Output Low Voltage, V_{OL}			0.4	V	$I_{OUT} = -4.0$ mA
High Level Output Current, I_{OH}		0.1	1.0	µA	$V_{OUT} = V_{CC}$

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SMBus DIGITAL INPUTS (SCL, SDA)					
Input High Voltage, V_{IH}	2.0			V	
Input Low Voltage, V_{IL}			0.4	V	
Hysteresis		500		mV	
DIGITAL INPUT LOGIC LEVELS (TACH INPUTS)					
Input High Voltage, V_{IH}	2.0			V	
			3.6	V	Maximum input voltage
Input Low Voltage, V_{IL}			0.8	V	
	−0.3			V	Minimum input voltage
Hysteresis		0.5		V p-p	
DIGITAL INPUT LOGIC LEVELS ($\overline{THERM}$) ADTL+					
Input High Voltage, V_{IH}			$0.75 \times V_{CC}$	V	
Input Low Voltage, V_{IL}			0.4	V	
DIGITAL INPUT CURRENT					
Input High Current, I_{IH}		±1		µA	$V_{IN} = V_{CC}$
Input Low Current, I_{IL}		±1		µA	$V_{IN} = 0$
Input Capacitance, C_{IN}		5		pF	
SERIAL BUS TIMING					See Figure 2
Clock Frequency, f_{SCLK}	10		400	kHz	
Glitch Immunity, t_{SW}			50	ns	
Bus Free Time, t_{BUF}	4.7			µs	
SCL Low Time, t_{LOW}	4.7			µs	
SCL High Time, t_{HIGH}	4.0		50	µs	
SCL, SDA Rise Time, t_r			1,000	ns	
SCL, SDA Fall Time, t_f			300	µs	
Data Setup Time, $t_{SU;DAT}$	250			ns	
Detect Clock Low Timeout, $t_{TIMEOUT}$	15		35	ms	Can be optionally disabled

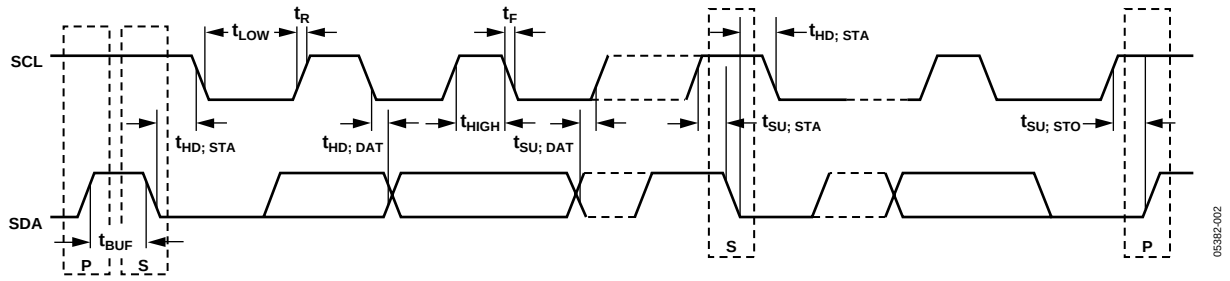


Figure 2. Serial Bus Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Positive Supply Voltage (V_{CC})	3.6 V
Maximum Voltage on +12V_{IN} Pin	16 V
Maximum Voltage on +5V_{IN} Pin	6.25V
Maximum Voltage on All Open-Drain Outputs	3.6 V
Voltage on Any Input or Output Pin	−0.3 V to +4.2 V
Input Current at Any Pin	±5 mA
Package Input Current	±20 mA
Maximum Junction Temperature ($T_{J\,max}$)	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature, Soldering	
IR Reflow Peak Temperature	220°C
Pb-free Peak Temperature	260°C
Lead Temperature (Soldering, 10 sec)	300°C
ESD rating	1,500 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

24-lead QSOP package:

θ_{JA} = 122°C/W
θ_{JC} = 31.25°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

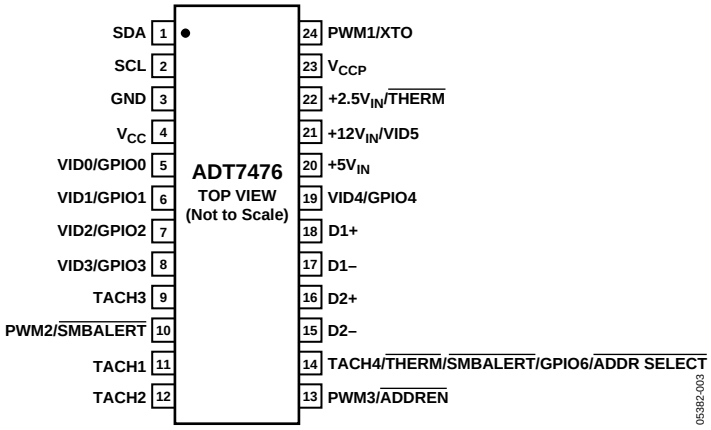


Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SDA	Digital I/O (Open Drain). SMBus bidirectional serial data. Requires SMBus pull-up.
2	SCL	Digital Input (Open Drain). SMBus serial clock input. Requires SMBus pull-up.
3	GND	Ground Pin.
4	V_{CC}	Power Supply. Powered by 3.3 V standby, if monitoring in low power states is required. V_{CC} is also monitored through this pin.
5	VID0/	Digital Input. Voltage supply readouts from CPU. This value is read into the VID register (Reg. 0x43).
	GPIO0	General Purpose Open Drain Digital I/O.
6	VID1/	Digital Input. Voltage supply readouts from CPU. This value is read into the VID register (Reg. 0x43).
	GPIO1	General Purpose Open Drain Digital I/O.
7	VID2/	Digital Input. Voltage supply readouts from CPU. This value is read into the VID register (Reg. 0x43).
	GPIO2	General Purpose Open Drain Digital I/O.
8	VID3/	Digital Input. Voltage supply readouts from CPU. This value is read into the VID register (Reg. 0x43).
	GPIO3	General Purpose Open Drain Digital I/O.
9	TACH3	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 3.
10	PWM2/	Digital Output (Open Drain). Requires 10 kΩ typical pull-up. Pulse width modulated output to control Fan 2 speed. Can be configured as a high or low frequency drive.
	$\overline{\text{SMBALERT}}$	Digital Output (Open Drain). This pin can be reconfigured as an $\overline{\text{SMBALERT}}$ interrupt output to signal out-of-limit conditions.
11	TACH1	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 1.
12	TACH2	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 2.
13	PWM3	Digital I/O (Open Drain). Pulse width modulated output to control Fan 3/4 speed. Requires 10 kΩ typical pull-up. Can be configured as a high or low frequency drive.
	$\overline{\text{ADDREN}}$	If pulled low on power-up, the ADT7476 enters address select mode, and the state of Pin 14 (ADDR SELECT) determines the ADT7476's slave address.
14	TACH4/	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 4.
	$\overline{\text{THERM}}$/	Alternatively, the pin can be reconfigured as a bi-directional $\overline{\text{THERM}}$ pin. Use to time and monitor assertions on the $\overline{\text{THERM}}$ input. For example, can be connected to the $\overline{\text{PROCHOT}}$ output of Intel's Pentium 4™ processor or to the output of a trip point temperature sensor. Can be used as an output to signal overtemperature conditions.
	$\overline{\text{SMBALERT}}$/	Digital Output (Open Drain). This pin can be reconfigured as an $\overline{\text{SMBALERT}}$ interrupt output to signal out-of-limit conditions.
	GPIO6/	General Purpose Open Drain Digital I/O.
	$\overline{\text{ADDR SELECT}}$	If in address select mode, the logic state of this pin defines the SMBus device address.

Pin No.	Mnemonic	Description
15	D2–	Cathode Connection to Second Thermal Diode.
16	D2+	Anode Connection to Second Thermal Diode.
17	D1–	Cathode Connection to First Thermal Diode.
18	D1+	Anode Connection to First Thermal Diode.
19	VID4/	Digital Input. Voltage supply readouts from CPU. This value is read into the VID register (Reg. 0x43).
	GPIO4	General Purpose Open Drain Digital I/O.
20	$+5V_{IN}$	Analog Input. Monitors +5 V power supply.
21	$+12V_{IN}$/	Analog Input. Monitors +12 V power supply.
	VID5	Digital Input. Voltage supply readouts from CPU. This value is read into the VID register (Reg. 0x43).
22	$+2.5V_{IN}$/	Analog Input. Monitors +2.5 V supply, typically a chipset voltage.
	$\overline{\text{THERM}}$	Alternatively, this pin can be reconfigured as a bi-/omni-directional $\overline{\text{THERM}}$ pin. Can be used to time and monitor assertions on the $\overline{\text{THERM}}$ input. For example, can be connected to the $\overline{\text{PROCHOT}}$ output of Intel's Pentium 4 processor or to the output of a trip point temperature sensor. Can be used as an output to signal overtemperature conditions.
23	V_{CCP}	Analog Input. Monitors processor core voltage (0 V to 3 V).
24	PWM1/	Digital Output (Open Drain). Pulse width modulated output to control Fan 1 speed. Requires 10 kΩ typical pull-up.
	XTO	Also functions as the output from the XOR tree in XOR test mode.

TYPICAL PERFORMANCE CHARACTERISTICS

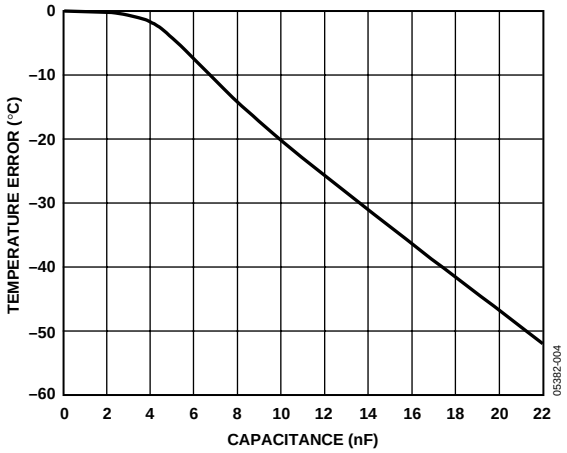


Figure 4. Temperature Error vs. Capacitance Between D+ and D–

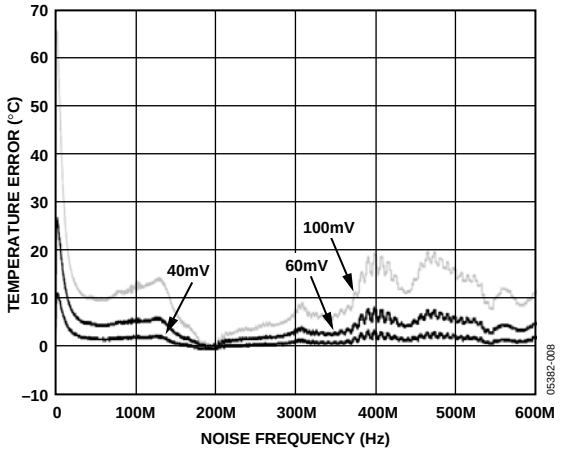


Figure 7. Remote Temperature Error vs. Differential Mode Noise Frequency

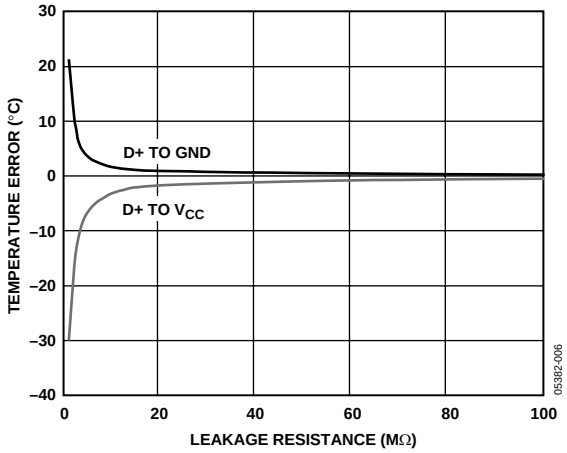


Figure 5. Remote Temperature Error vs. PCB Resistance

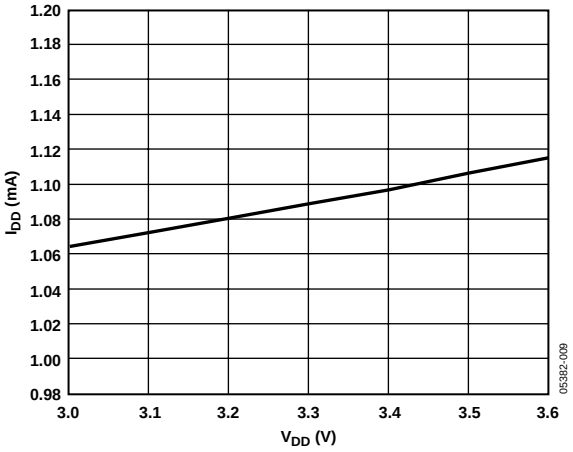


Figure 8. Normal I_{DD} vs. Power Supply

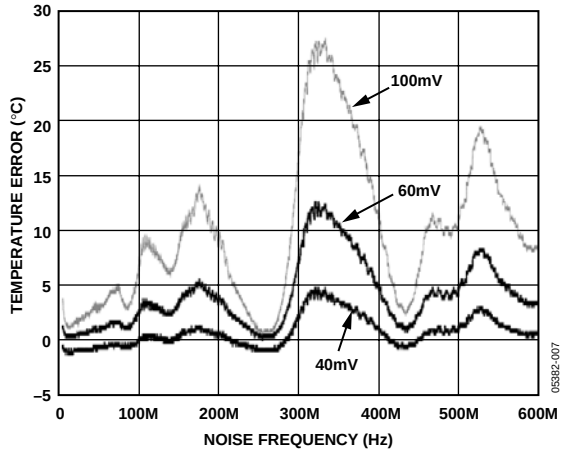


Figure 6. Remote Temperature Error vs. Common-Mode Noise Frequency

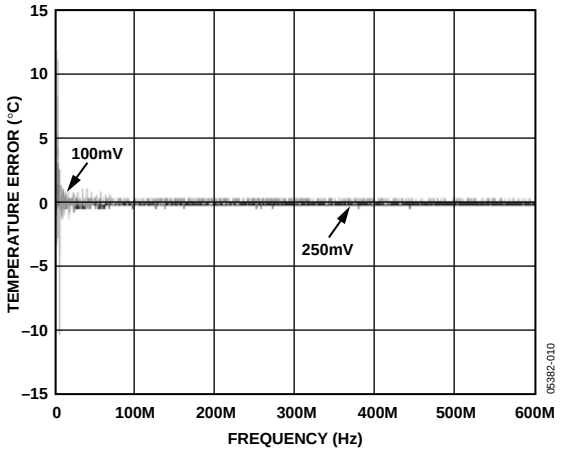


Figure 9. Internal Temperature Error vs. Power Supply

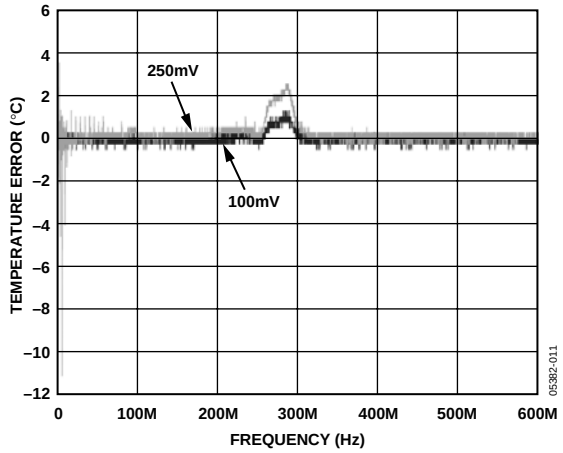


Figure 10. Remote Temperature Error vs. Power Supply Noise Frequency

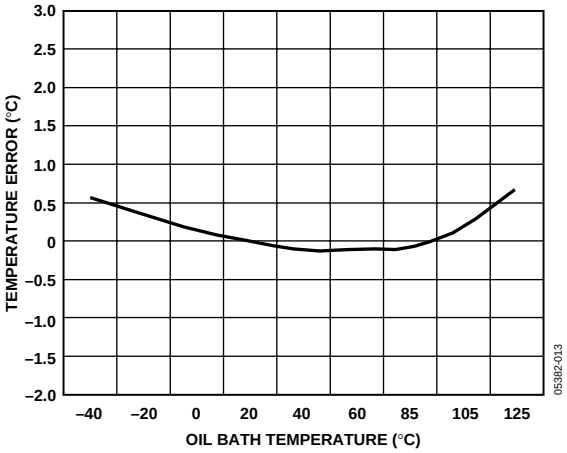


Figure 12. Remote Temperature Error vs. ADT7476 Temperature

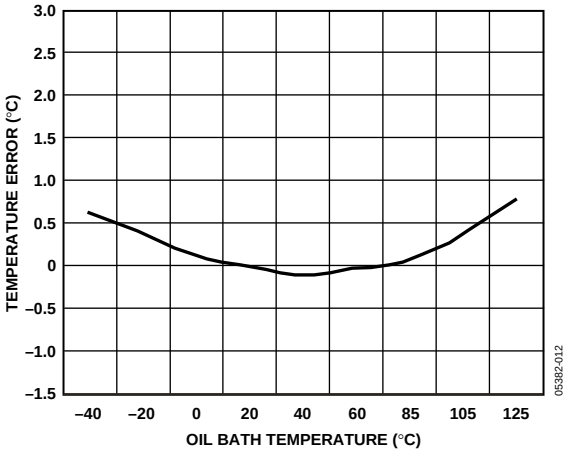


Figure 11. Internal Temperature Error vs. ADT7476 Temperature

PRODUCT DESCRIPTION

The ADT7476 is a complete thermal monitor and multiple fan controller for any system requiring thermal monitoring and cooling. The device communicates with the system via a serial system management bus. The serial bus controller has a serial data line for reading and writing addresses and data (Pin 1), and an input line for the serial clock (Pin 2). All control and programming functions for the ADT7476 are performed over the serial bus. In addition, a pin can be reconfigured as an $\overline{\text{SMBALERT}}$ output to signal out-of-limit conditions.

FEATURE COMPARISONS BETWEEN ADT7476 AND ADT7468

- Dynamic T_{MIN}, dynamic operating point and associated registers are no longer available. Related registers are gone.
  - Calibration Control 1 and 2 (0x36 and 0x37)
  - Operating Point (0x33, 0x34, and 0x35)
- Previously T_{RANGE} defined the slope of the automatic fan control algorithm. Trange now defines a true temperature range.
- Acoustic filtering is now assigned to temperature zones not to fans. Available smoothing times have been increased for better acoustic performance.
- Temperature measurements are now made with two switching currents instead of three. SRC is not available in the ADT7476.
- High frequency PWM can now be enabled/disabled on each PWM output individually.
- THERM can now be enabled/disabled on each temperature channel individually.
- The ADT7476 does not support full shutdown mode.
- Increased temperature accuracy on all temperature channels.
- The ADT7476 defaults to twos complement temperature measurement mode.
- Some pins have swapped/added functions.
- The power-up routine for the ADT7476 is simplified.
- Other minor changes include the following:
  - Vcore_low_enable has been reallocated to Bit 7 of Configuration Register 1 (0x40).
  - Dev ID register reads 0x76.
  - Rev ID register reads 0x69.

RECOMMENDED IMPLEMENTATION

Configuring the ADT7476 as in Figure 13 allows the system designer to use the following features:

- Two PWM outputs for fan control of up to three fans (the front and rear chassis fans are connected in parallel).
- Three TACH fan speed measurement inputs.
- V_{CC} measured internally through Pin 4.
- CPU temperature measured using Remote 1 temperature channel.
- Remote temperature zone measured through Remote 2 temperature channel.
- Local temperature zone measured through the internal temperature channel.
- Bidirectional $\overline{\text{THERM}}$ pin. This feature allows Intel Pentium 4 $\overline{\text{PROCHOT}}$ monitoring and can function as an overtemperature $\overline{\text{THERM}}$ output. It can alternatively be programmed as an $\overline{\text{SMBALERT}}$ system interrupt output.

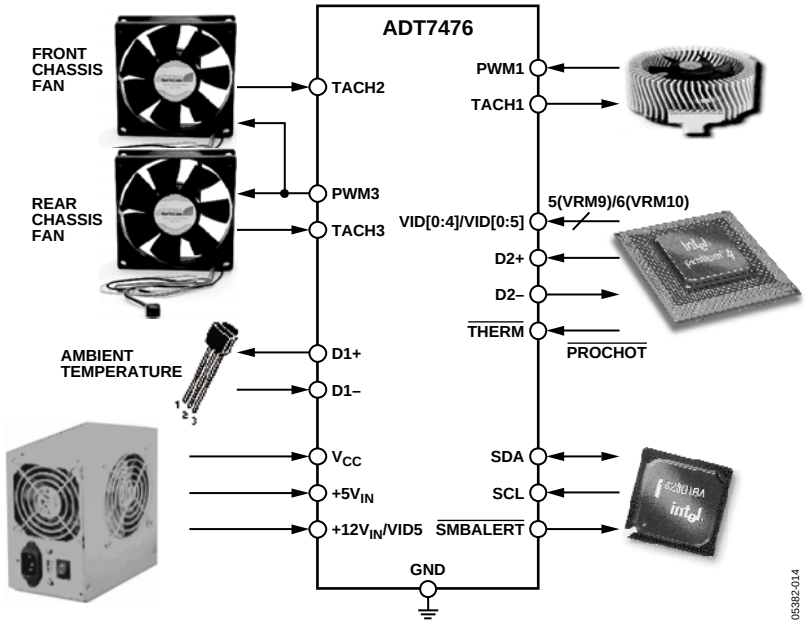


Figure 13. ADT7476 Configuration

SERIAL BUS INTERFACE

Control of the ADT7476 is carried out using the serial system management bus (SMBus). The ADT7476 is connected to this bus as a slave device, under the control of a master controller. The ADT7476 has a 7-bit serial bus address. When the device is powered up with Pin 13 (PWM3/$\overline{\text{ADDREN}}$) high, the ADT7476 has a default SMBus address of 0101110 or 0x2E. The read/write bit must be added to get the 8-bit address. If more than one ADT7476 is to be used in a system, each ADT7476 is placed in $\overline{\text{ADDR SELECT}}$ mode by strapping Pin 13 low on power-up. The logic state of Pin 14 then determines the device's SMBus address. The logic of these pins is sampled on power-up.

The device address is sampled on power-up and latched on the first valid SMBus transaction, more precisely on the low-to-high transition at the beginning of the 8th SCL pulse, when the serial bus address byte matches the selected slave address. The selected slave address is chosen using the $\overline{\text{ADDREN}}$ pin/$\overline{\text{ADDR SELECT}}$ pin. Any attempted changes in the address have no effect after this.

Table 4. Hardwiring the ADT7476 SMBus Device Address

Pin 13 State	Pin 14	Address
0	Low (10 kΩ to GND)	0101100 (0x2C)
0	High (10 kΩ Pull-Up)	0101101 (0x2D)
1	Don't Care	0101110 (0x2E)

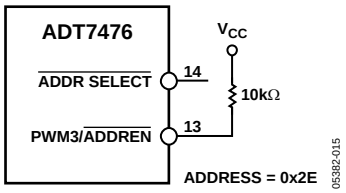


Figure 14. Default SMBus Address = 0x2E

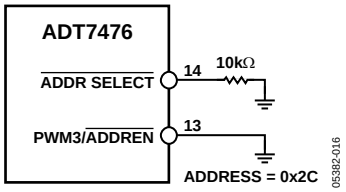


Figure 15. SMBus Address = 0x2C (Pin 14 = 0)

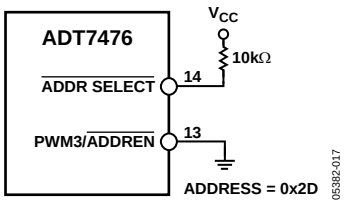


Figure 16. SMBus Address = 0x2D (Pin 14 = 1)

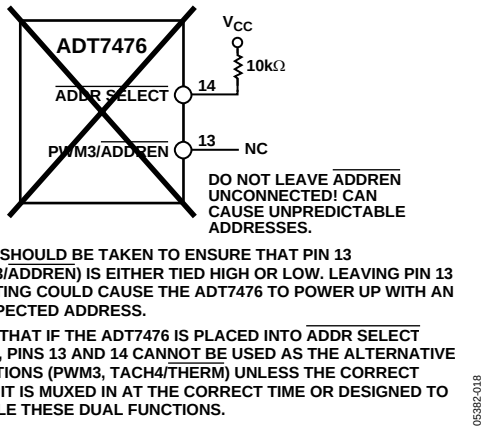


Figure 17. Unpredictable SMBus Address if Pin 13 is Unconnected

The ability to make hardwired changes to the SMBus slave address allows the user to avoid conflicts with other devices sharing the same serial bus, for example, if more than one ADT7476 is used in a system.

The serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition, defined as a high-to-low transition on the serial data line SDA while the serial clock line SCL remains high. This indicates an address/data stream follows. All slave peripherals connected to the serial bus respond to the start condition and shift in the next eight bits, consisting of a 7-bit address (MSB first), plus a R/$\overline{\text{W}}$ bit, which determines the direction of the data transfer, that is, whether data is written to or read from the slave device.

   The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the Acknowledge bit. All other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{\text{W}}$ bit is a 0, the master writes to the slave device. If the R/$\overline{\text{W}}$ bit is a 1, the master reads from the slave device.

2. Data is sent over the serial bus in sequences of nine clock pulses, eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period. A low-to-high transition, when the clock is high, can be interpreted as a stop signal. The number of data bytes transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.

3. When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the tenth clock pulse to assert a stop condition.

   In read mode, the master device overrides the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse. This is known as No Acknowledge. The master then takes the data line low during the low period before the tenth clock pulse, and then high during the tenth clock pulse to assert a stop condition. Any number of bytes of data can be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation. In ADT7476, write operations contain either one or two bytes, and read operations contain one byte and perform the following functions.

   To write data to one of the device data registers or read data from it, the address pointer register must be set, so the correct data register is addressed, then data can be written into that register or read from it. The first byte of a write operation always contains an address stored in the address pointer register. If data is to be written to the device, the write operation contains a second data byte that is written to the register selected by the address pointer register.

   This is illustrated in Figure 18. The device address is sent over the bus followed by R/$\overline{W}$ being set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the address pointer register. The second data byte is the data to be written to the internal data register.

On PCs and servers, control of the ADT7476 is carried out using the serial system management bus (SMBus). The ADT7476 is connected to this bus as a slave device, under the control of a master controller, which is usually (but not necessarily) the ICH.

The ADT7476 has three 7-bit serial bus addresses. The read/write bit must be added to get the 8-bit address (that is, 01011100 or 0x5C). Data is sent over the serial bus in sequences of nine clock pulses: eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low-to-high transition when the clock is high might be interpreted as a stop signal. The number of data bytes transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.

When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the tenth clock pulse to assert a stop condition. In read mode, the master device overrides the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse. This is known as No Acknowledge. The master then takes the data line low during the low period before the tenth clock pulse, and then high during the tenth clock pulse to assert a stop condition.

Any number of bytes of data can be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation, because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

In the ADT7476, write operations contain either one or two bytes, and read operations contain one byte and perform the following functions: To write data to one of the device data registers or read data from it, the address pointer register must be set so that the correct data register is addressed. Then, data can be written into that register or read from it. The first byte of a write operation always contains an address stored in the address pointer register. If data is to be written to the device, then the write operation contains a second data byte written to the register selected by the address pointer register.

This write operation is illustrated in Figure 18. The device address is sent over the bus, and then R/$\overline{W}$ is set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the address pointer register. The second data byte is the data to be written to the internal data register.

When reading data from a register, there are two possibilities:

- If the ADT7476's address pointer register value is unknown, or not the desired value, it must first be set to the correct value before data can be read from the desired data register. This is done by performing a write to the ADT7476 as before, but only the data byte containing the register address is sent, because no data is written to the register (see Figure 19).

  A read operation is then performed consisting of the serial bus address, R/$\overline{W}$ bit set to 1, followed by the data byte read from the data register (see Figure 20.)

- If the address pointer register is known to be already at the desired address, data can be read from the corresponding data register without first writing to the address pointer register (see Figure 20).

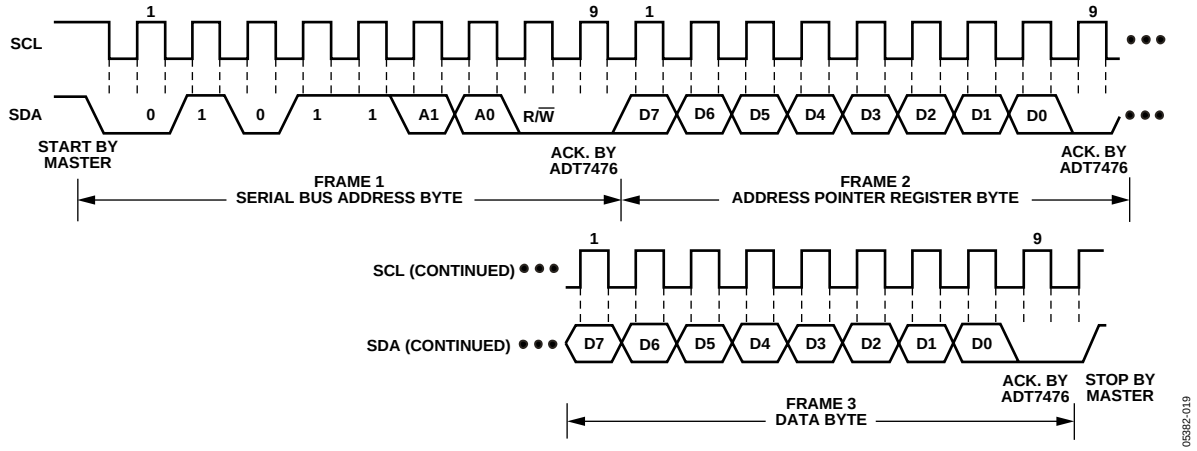


Figure 18. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

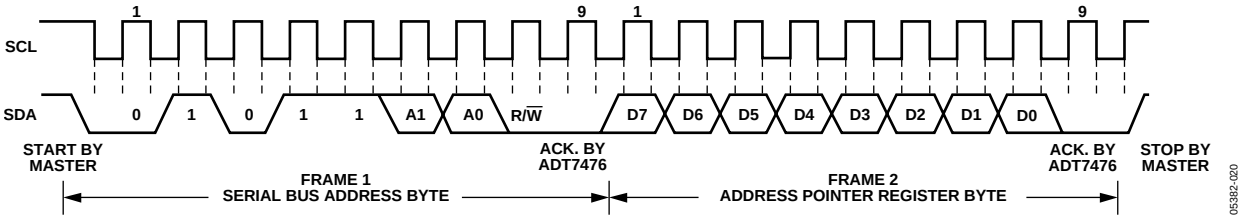


Figure 19. Writing to the Address Pointer Register Only

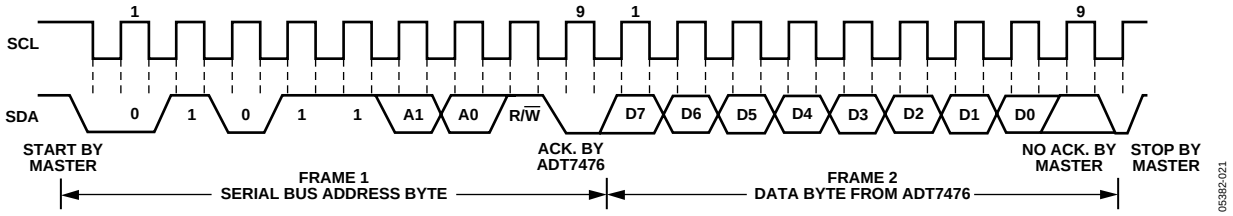


Figure 20. Reading Data from a Previously Selected Register

It is possible to read a data byte from a data register without first writing to the address pointer register, if the address pointer register is already at the correct value. However, it is not possible to write data to a register without writing to the address pointer register, because the first data byte of a write is always written to the address pointer register.

In addition to supporting the send byte and receive byte protocols, the ADT7476 also supports the read byte protocol. See Intel's *System Management Bus Specifications Rev. 2* for more information.

If several read or write operations must be performed in succession, the master can send a repeat start condition instead of a stop condition to begin a new operation.

WRITE OPERATIONS

The SMBus specification defines several protocols for different types of read and write operations. The ones used in the ADT7476 are discussed below. The following abbreviations are used in the diagrams:

S – START
P – STOP
R – READ
W – WRITE
A – ACKNOWLEDGE
$\overline{A}$ – NO ACKNOWLEDGE

The ADT7476 uses the following SMBus write protocols.

Send Byte

In this operation, the master device sends a single command byte to a slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA. The master sends a command code.
4. The slave asserts ACK on SDA.
5. The master asserts a stop condition on SDA, and the transaction ends.

For the ADT7476, the send byte protocol is used to write a register address to RAM for a subsequent single-byte read from the same address. This operation is illustrated in Figure 21.

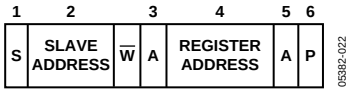


Figure 21. Setting a Register Address for Subsequent Read

If the master is required to read data from the register immediately after setting up the address, it can assert a repeat start condition immediately after the final ACK and carry out a single byte read without asserting an intermediate stop condition.

Write Byte

In this operation, the master device sends a command byte and one data byte to the slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master sends a data byte.
7. The slave asserts ACK on SDA.
8. The master asserts a stop condition on SDA, and the transaction ends.

This operation is illustrated in Figure 22.

Figure 22. Single Byte Write to a Register

READ OPERATIONS

The ADT7476 uses the following SMBus read protocols.

Receive Byte

This operation is useful when repeatedly reading a single register. The register address is set up previously. In this operation, the master device receives a single byte from a slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts ACK on SDA.
4. The master receives a data byte.
5. The master asserts NO ACK on SDA.
6. The master asserts a stop condition on SDA, and the transaction ends.

In the ADT7476, the receive byte protocol is used to read a single byte of data from a register whose address has previously been set by a send byte or write byte operation. This operation is illustrated in Figure 23.

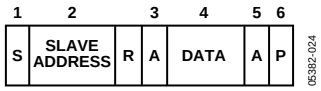


Figure 23. Singl- Byte Read from a Register

Alert Response Address

Alert response address (ARA) is a feature of SMBus devices, allowing an interrupting device to identify itself to the host when multiple devices exist on the same bus.

The $\overline{\text{SMBALERT}}$ output can be used as either an interrupt output or an $\overline{\text{SMBALERT}}$. One or more outputs can be connected to a common $\overline{\text{SMBALERT}}$ line connected to the master. If a device's $\overline{\text{SMBALERT}}$ line goes low, the following procedure occurs:

1. $\overline{\text{SMBALERT}}$ is pulled low.
2. The master initiates a read operation and sends the alert response address (ARA = 0001 100). This is a general call address that must not be used as a specific device address.
3. The device whose $\overline{\text{SMBALERT}}$ output is low responds to the alert response address, and the master reads its device address. The address of this device is now known and can be interrogated per usual.
4. If more than one device's $\overline{\text{SMBALERT}}$ output is low, the one with the lowest device address has priority in accordance with normal SMBus arbitration.
5. Once the ADT7476 has responded to the alert response address, the master must read the status registers, and the $\overline{\text{SMBALERT}}$ is cleared only if the error condition has gone away.

SMBus TIMEOUT

The ADT7476 includes an SMBus timeout feature. If there is no SMBus activity for 35 ms, the ADT7476 assumes the bus is locked and releases the bus. This prevents the device from locking or holding the SMBus expecting data. Some SMBus controllers cannot handle the SMBus timeout feature, so it can be disabled.

Configuration Register 1 (Reg. 0x40)

<6> TODIS = 0, SMBus timeout enabled (default).

<6> TODIS = 1, SMBus timeout disabled.

VIRUS PROTECTION

To prevent rogue programs or viruses from accessing critical ADT7476 register settings, the lock bit can be set. Setting Bit 1 of Configuration Register 1 (0x40) sets the lock bit and locks critical registers. In this mode, certain registers can no longer be written to until the ADT7476 is powered down and powered up again. For more information on which registers are locked, see the ADT7476 Registers.

VOLTAGE MEASUREMENT INPUT

The ADT7476 has four external voltage measurement channels. It can also measure its own supply voltage, V_{CC}.

Pin 20 to Pin 23 can measure 5 V, 12 V, and 2.5 V supplies, and the processor core voltage V_{CCP} (0 V to 3 V input). The V_{CC} supply voltage measurement is carried out through the V_{CC} pin (Pin 4). The 2.5 V input can be used to monitor a chipset supply voltage in computer systems.

ANALOG-TO-DIGITAL CONVERTER

All analog inputs are multiplexed into the on-chip, successive-approximation, analog-to-digital converter. This has a resolution of 10 bits. The basic input range is 0 V to 2.25 V, but the inputs have built-in attenuators to allow measurement of 2.5 V, 3.3 V, 5 V, 12 V, and the processor core voltage V_{CCP} without any external components. To allow the tolerance of these supply voltages, the ADC produces an output of 3/4 full scale (768 dec or 300 hex) for the nominal input voltage, and so has adequate headroom to cope with overvoltages.

INPUT CIRCUITRY

The internal structure for the analog inputs is shown in Figure 24. The input circuit consists of an input protection diode, an attenuator, plus a capacitor to form a first-order low-pass filter that gives input immunity to high frequency noise.

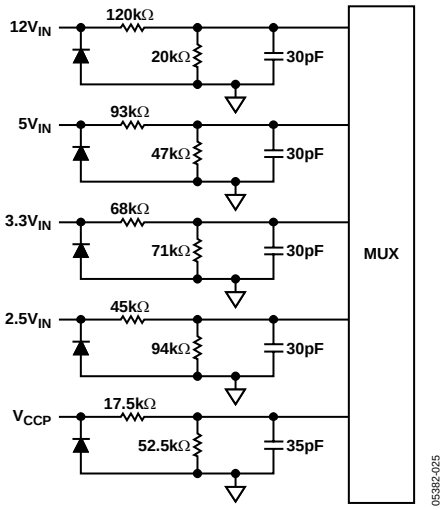


Figure 24. Structure of Analog Inputs

VOLTAGE MEASUREMENT REGISTERS

Reg. 0x20, **2.5 V Reading** = 0x00 default

Reg. 0x21, **V_{CCP} Reading** = 0x00 default

Reg. 0x22, **V_{CC} Reading** = 0x00 default

Reg. 0x23, **5 V Reading** = 0x00 default

Reg. 0x24, **12 V Reading** = 0x00 default

VOLTAGE LIMIT REGISTERS

Associated with each voltage measurement channel is a high and low limit register. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate $\overline{\text{SMBALERT}}$ interrupts.

Reg. 0x44, **2.5 V Low Limit** = 0x00 default

Reg. 0x45, **2.5 V High Limit** = 0xFF default

Reg. 0x46, **V_{CCP} Low Limit** = 0x00 default

Reg. 0x47, **V_{CCP} High Limit** = 0xFF default

Reg. 0x48, **V_{CC} Low Limit** = 0x00 default

Reg. 0x49, **V_{CC} High Limit** = 0xFF default

Reg. 0x4A, **5 V Low Limit** = 0x00 default

Reg. 0x4B, **5 V High Limit** = 0xFF default

Reg. 0x4C, **12 V Low Limit** = 0x00 default

Reg. 0x4D, **12 V High Limit** = 0xFF default

Table 8 shows the input ranges of the analog inputs and output codes of the 10-bit ADC.

When the ADC is running, it samples and converts a voltage input in 0.7 ms and averages 16 conversions to reduce noise; a measurement takes nominally 11 ms.

EXTENDED RESOLUTION REGISTERS

Voltage measurements can be made with higher accuracy using the extended resolution registers (0x76 and 0x77). Whenever the extended resolution registers are read, the corresponding data in the voltage measurement registers (0x20 to 0x 24) is locked until their data is read. That is, if extended resolution is required, the extended resolution register must be read first immediately followed by the appropriate voltage measurement register.

ADDITIONAL ADC FUNCTIONS FOR VOLTAGE MEASUREMENTS

A number of other functions are available on the ADT7476 to offer the system designer increased flexibility.

Turn-Off Averaging

For each voltage/temperature measurement read from a value register, 16 readings have actually been made internally and the results averaged, before being placed into the value register. When faster conversions are needed, setting Bit 4 of Configuration Register 2 (Reg. 0x73) turns averaging off. This effectively gives a reading 16 times faster, but the reading can be noisier. The default round-robin cycle time takes 146.5 ms.

Table 5. Conversion Time with Averaging Disabled

Channel	Measurement Time (ms)
Voltage Channels	0.7
Remote Temperature 1	7
Remote Temperature 2	7
Local Temperature	1.3

When Bit 7 of Configuration Register 6 (0x10) is set, the default round-robin cycle time increases to 240 ms.

Bypass All Voltage Input Attenuators

Setting Bit 5 of Configuration Register 2 (Reg. 0x73) removes the attenuation circuitry from the 2.5 V, V_{CCP}, V_{CC}, 5 V, and 12 V inputs. This allows the user to directly connect external sensors or rescale the analog voltage measurement inputs for other applications. The input range of the ADC without the attenuators is 0 V to 2.25 V.

Bypass Individual Voltage Input Attenuators

Bits <7:4> or Configuration Register 4 (0x7D) can be used to bypass individual voltage channel attenuators.

Table 6. Bypassing Individual Voltage Input Attenuators

Configuration Register 4 (0x7D)	
Bit	**Channel Attenuated**
4	Bypass 2.5 V attenuator
5	Bypass V_{CCP} attenuator
6	Bypass 5 V attenuator
7	Bypass 12 V attenuator

Configuration Register 2 (Reg. 0x73)

<4> = 1, averaging off.

<5> = 1, bypass input attenuators.

<6> = 1, single-channel convert mode.

TACH1 Minimum High Byte (Reg. 0x55)

<7:5> Selects ADC channel for single-channel convert mode.

Single-Channel ADC Conversion

While single-channel mode is intended as a test mode that can be used to increase sampling times for a specific channel, therefore helping to analyze that channel s performance in greater detail, it can also have other applications.

Setting Bit 6 of Configuration Register 2 (Reg. 0x73) places the ADT7476 into single-channel ADC conversion mode. In this mode, the ADT7476 can read a single voltage channel only. The selected voltage input is read every 0.7 ms. The appropriate ADC channel is selected by writing to Bits <7:5> of the TACH1 minimum high byte register (0x55).

Table 7. Programming Single-Channel ADC Mode

Bits <7:5> Reg. 0x55	Channel Selected[1]
000	2.5 V
001	V_{CCP}
010	V_{CC}
011	5 V
100	12 V
101	Remote 1 temperature
110	Local temperature
111	Remote 2 temperature

[1] In the process of configuring single-channel ADC conversion mode, the TACH1 minimum high byte is also changed, possibly trading off TACH1 minimum high byte functionality with single-channel mode functionality.

Table 8. 10-Bit A/D Output Code vs. V_{IN}

Input Voltage					A/D Output	
12 V_{IN}	**5 V_{IN}**	**V_{CC} (3.3 V_{IN})**	**2.5 V_{IN}**	**V_{CCP}**	**Decimal**	**Binary (10 Bits)**
<0.0156	<0.0065	<0.0042	<0.0032	<0.00293	0	00000000 00
0.0156–0.0312	0.0065–0.0130	0.0042–0.0085	0.0032–0.0065	0.0293–0.0058	1	00000000 01
0.0312–0.0469	0.0130–0.0195	0.0085–0.0128	0.0065–0.0097	0.0058–0.0087	2	00000000 10
0.0469–0.0625	0.0195–0.0260	0.0128–0.0171	0.0097–0.0130	0.0087–0.0117	3	00000000 11
0.0625–0.0781	0.0260–0.0325	0.0171–0.0214	0.0130–0.0162	0.0117–0.0146	4	00000001 00
0.0781–0.0937	0.0325–0.0390	0.0214–0.0257	0.0162–0.0195	0.0146–0.0175	5	00000001 01
0.0937–0.1093	0.0390–0.0455	0.0257–0.0300	0.0195–0.0227	0.0175–0.0205	6	00000001 10
0.1093–0.1250	0.0455–0.0521	0.0300–0.0343	0.0227–0.0260	0.0205–0.0234	7	00000001 11
0.1250–0.14060	0.0521–0.0586	0.0343–0.0386	0.0260–0.0292	0.0234–0.0263	8	00000010 00
	•					
	•					
	•					
4.0000–4.0156	1.6675–1.6740	1.1000–1.1042	0.8325–0.8357	0.7500–0.7529	256 (1/4 scale)	01000000 00
	•					
	•					
	•					
8.0000–8.0156	3.3300–3.3415	2.2000–2.2042	1.6650–1.6682	1.5000–1.5029	512 (1/2 scale)	10000000 00
	•					
	•					
	•					
12.0000–12.0156	5.0025–5.0090	3.3000–3.3042	2.4975–2.5007	2.2500–2.2529	768 (3/4 scale)	11000000 00
	•					
	•					
	•					
15.8281–15.8437	6.5983–6.6048	4.3527–4.3570	3.2942–3.2974	2.9677–2.9707	1013	11111101 01
15.8437–15.8593	6.6048–6.6113	4.3570–4.3613	3.2974–3.3007	2.9707–2.9736	1014	11111101 10
15.8593–15.8750	6.6113–6.6178	4.3613–4.3656	3.3007–3.3039	2.9736–2.9765	1015	11111101 11
15.8750–15.8906	6.6178–6.6244	4.3656–4.3699	3.3039–3.3072	2.9765–2.9794	1016	11111110 00
15.8906–15.9062	6.6244–6.6309	4.3699–4.3742	3.3072–3.3104	2.9794–2.9824	1017	11111110 01
15.9062–15.9218	6.6309–6.6374	4.3742–4.3785	3.3104–3.3137	2.9824–2.9853	1018	11111110 10
15.9218–15.9375	6.6374–6.4390	4.3785–4.3828	3.3137–3.3169	2.9853–2.9882	1019	11111110 11
15.9375–15.9531	6.6439–6.6504	4.3828–4.3871	3.3169–3.3202	2.9882–2.9912	1020	11111111 00
15.9531–15.9687	6.6504–6.6569	4.3871–4.3914	3.3202–3.3234	2.9912–2.9941	1021	11111111 01
15.9687–15.9843	6.6569–6.6634	4.3914–4.3957	3.3234–3.3267	2.9941–2.9970	1022	11111111 10
>15.9843	>6.6634	>4.3957	>3.3267	>2.9970	1023	11111111 11

VID CODE MONITORING

The ADT7476 has five dedicated voltage ID (VID code) inputs. These are digital inputs that can be read back through the VID register (Reg. 0x43) to determine the processor voltage required or being used in the system. Five VID code inputs support VRM9.x solutions. In addition, Pin 21 (12 V input) can be reconfigured as a sixth VID input to satisfy future VRM requirements.

VID Code Register (Reg. 0x43)

<0> = VID0, reflects logic state of Pin 5.

<1> = VID1, reflects logic state of Pin 6.

<2> = VID2, reflects logic state of Pin 7.

<3> = VID3, reflects logic state of Pin 8.

<4> = VID4, reflects logic state of Pin 19.

<5> = VID5, reconfigurable 12 V input. This bit reads 0 when Pin 21 is configured as the 12 V input. This bit reflects the logic state of Pin 21 when the pin is configured as VID5.

VID CODE INPUT THRESHOLD VOLTAGE

The switching threshold for the VID code inputs is approximately 1 V. To enable future compatibility, it is possible to reduce the VID code input threshold to 0.6 V. Bit 6 (THLD) of the VID register (Reg. 0x43) controls the VID input threshold voltage.

VID CODE REGISTER (Reg. 0x43)

<6> THLD = 0, VID switching threshold = 1 V,
V_{OL} < 0.8 V, V_{IH} > 1.7 V, V_{MAX} = 3.3 V

<6> THLD = 1, VID switching threshold = 0.6 V,
V_{OL} < 0.4 V, V_{IH} > 0.8 V, V_{MAX} = 3.3 V

Reconfiguring Pin 21 as VID5 Input

Pin 21 can be reconfigured as a sixth VID code input (VID5) for VRM10 compatible systems. Because the pin is configured as VID5, it is not possible to monitor a 12 V supply.

Bit 7 of the VID register (Reg. 0x43) determines the function of Pin 21. System or BIOS software can read the state of Bit 7 to determine whether the system is designed to monitor 12 V or is monitoring a sixth VID input.

VID Code Register (Reg. 0x43)

<7> VIDSEL = 0, Pin 21 functions as a 12 V measurement input. Software can read this bit to determine there are five VID inputs being monitored. Bit 5 of Register 0x43 (VID5) always reads back 0. Bit 0 of Status Register 2 (Reg. 0x42) reflects 12 V out-of-limit measurements.

<7> VIDSEL = 1, Pin 21 functions as the sixth VID code input (VID5). Software can read this bit to determine there are six VID inputs being monitored. Bit 5 of Register 0x43 reflects the logic state of Pin 21. Bit 0 of Status Register 2 (Reg. 0x42) reflects VID code changes.

VID CODE CHANGE DETECT FUNCTION

The ADT7476 has a VID code change detect function. When Pin 21 is configured as the VID5 input, VID code changes are detected and reported back by the ADT7476. Bit 0 of Status Register 2 (Reg. 0x42) is the 12 V/VC bit and denotes a VID change when set. The VID code change bit is set when the logic states on the VID inputs are different than they were 11 µs previously. The change of VID code is used to generate an $\overline{\text{SMBALERT}}$ interrupt. If an $\overline{\text{SMBALERT}}$ interrupt is not required, Bit 0 of Interrupt Mask Register 2 (Reg. 0x75), when set, prevents $\overline{\text{SMBALERT}}$s from occurring on VID code changes.

Status Register 2 (Reg. 0x42)

<0> 12V/VC = 0, if Pin 21 is configured as VID5, Logic 0 denotes no change in VID code within the last 11 µs.

<0> 12V/VC = 1, if Pin 21 is configured as VID5, Logic 1 means that a change has occurred on the VID code inputs within the last 11 µs. An $\overline{\text{SMBALERT}}$ is generated, if this function is enabled.

PROGRAMMING THE GPIOS

The ADT7476 follows an upgrade path from the ADM1027 to ADT7476. In order to maintain consistency between versions, it is necessary to omit references to GPIO5. As a result, there are six GPIOs as follows: GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, and GPIO6.

Setting Bit 4 of Configuration Register 5 (0x7C) to 1 enables GPIO functionality. This turns all pins configured as VID inputs into general-purpose outputs. Writing to the corresponding VID bit in the VID register (0x43) sets the polarity for the corresponding GPIO. GPIO6 can be programmed independently as an input/output/etc. using Bits <3:2> of Configuration Register 5 (0x7C).

TEMPERATURE MEASUREMENT METHOD

Local Temperature Measurement

The ADT7476 contains an on-chip band gap temperature sensor whose output is digitized by the on-chip, 10-bit ADC. The 8-bit MSB temperature data is stored in the temperature registers (Addresses 0x25, 0x26, and 0x27). Because both positive and negative temperatures can be measured, the temperature data is stored in Offset 64 format or twos complement format, as shown in Table 9 and Table 10. Theoretically, the temperature sensor and ADC can measure temperatures from −63°C to +127°C (or −61°C to +191°C in the extended temperature range) with a resolution of 0.25°C. However, this exceeds the operating temperature range of the device, so local temperature measurements outside the ADT7476 operating temperature range are not possible.

Remote Temperature Measurement

The ADT7476 can measure the temperature of two remote diode sensors or diode-connected transistors connected to Pin 17 and Pin 18, or Pin 15 and Pin 16.

The forward voltage of a diode or diode-connected transistor operated at a constant current exhibits a negative temperature coefficient of about −2 mV/°C. Unfortunately, the absolute value of V_{BE} varies from device to device and individual calibration is required to null this out, so the technique is unsuitable for mass production. The technique used in the ADT7476 is to measure the change in V_{BE} when the device is operated at two different currents.

This is given by

$$\Delta V_{BE} = KT/q \times 1n(\mathrm{N})$$

where:

K is Boltzmann's constant.
q is the charge on the carrier.
T is the absolute temperature in Kelvin.
N is the ratio of the two currents.

Figure 25 shows the input signal conditioning used to measure the output of a remote temperature sensor. This figure shows the external sensor as a substrate transistor, provided for temperature monitoring on some microprocessors. It could also be a discrete transistor such as a 2N3904/2N3906.

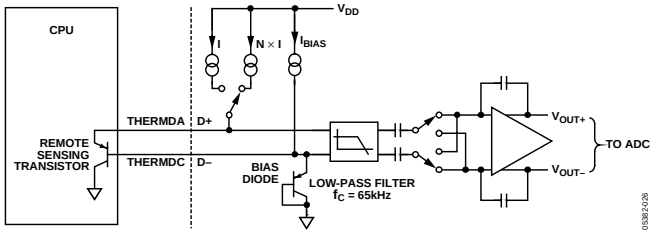


Figure 25. Signal Conditioning for Remote Diode Temperature Sensors

If a discrete transistor is used, the collector is not grounded and should be linked to the base. If a PNP transistor is used, the base is connected to the D– input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D– input and the base to the D+ input. Figure 26 and Figure 27 show how to connect the ADT7476 to an NPN or PNP transistor for temperature measurement. To prevent ground noise from interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal diode at the D– input.

To measure ΔV_{BE}, the sensor is switched between operating currents of I and N × I. The resulting waveform is passed through a 65 kHz low-pass filter to remove noise and to a chopper-stabilized amplifier that performs the functions of amplification and rectification of the waveform to produce a dc voltage proportional to ΔV_{BE}. This voltage is measured by the ADC to give a temperature output in 10-bit, twos complement format. To further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles.

A remote temperature measurement takes nominally 38 ms. The results of remote temperature measurements are stored in 10-bit, twos complement format, as illustrated in Table 9. The extra resolution for the temperature measurements is held in the Extended Resolution Register 2 (Reg. 0x77). This gives temperature readings with a resolution of 0.25°C.

Noise Filtering

For temperature sensors operating in noisy environments, previous practice was to place a capacitor across the D+ pin and the D– pin to help combat the effects of noise. However, large capacitances affect the accuracy of the temperature measurement, leading to a recommended maximum capacitor value of 1000 pF.

This capacitor reduces the noise, but does not eliminate it, making use the sensor difficult in a very noisy environment. In most cases, a capacitor is not required as differential inputs by their very nature have a high immunity to noise.

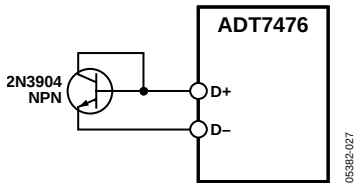


Figure 26. Measuring Temperature Using an NPN Transistor

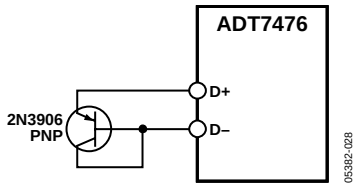


Figure 27. Measuring Temperature Using a PNP Transistor

FACTORS AFFECTING DIODE ACCURACY

Remote Sensing Diode

The ADT7476 is designed to work with either substrate transistors built into processors or with discrete transistors. Substrate transistors are generally PNP types with the collector connected to the substrate. Discrete types can be either PNP or NPN transistors connected as a diode (base-shorted to the collector). If an NPN transistor is used, the collector and base are connected to D+ and the emitter to D−. If a PNP transistor is used, the collector and base are connected to D− and the emitter is connected to D+.

To reduce the error due to variations in both substrate and discrete transistors, a number of factors should be taken into consideration:

- The ideality factor, n_f, of the transistor is a measure of the deviation of the thermal diode from ideal behavior. The ADT7476 is trimmed for an n_f value of 1.008. Use the following equation to calculate the error introduced at a temperature T (°C), when using a transistor whose n_f does not equal 1.008. See the processor data sheet for the n_f values.

  $$\Delta T = (n_f - 1.008) \times (273.15\ \text{K} + T)$$

  To factor this in, the user can write the ΔT value to the offset register. The ADT7476 then automatically adds it to or subtracts it from the temperature measurement.

- Some CPU manufacturers specify the high and low current levels of the substrate transistors. The high current level of the ADT7476, I_{HIGH}, is 180 µA and the low level current, I_{LOW}, is 11 µA. If the ADT7476 current levels do not match the current levels specified by the CPU manufacturer, it might be necessary to remove an offset. The CPUs data sheet advises whether this offset needs to be removed and how to calculate it. This offset can be programmed to the offset register. It is important to note that, if more than one offset must be considered, the algebraic sum of these offsets must be programmed to the offset register.

If a discrete transistor is used with the ADT7476, the best accuracy is obtained by choosing devices according to the following criteria:

- Base-emitter voltage greater than 0.25 V at 11 µA, at the highest operating temperature.
- Base-emitter voltage less than 0.95 V at 180 µA, at the lowest operating temperature.
- Base resistance less than 100 Ω.
- Small variation in h_{FE} (approximately 50 to 150) that indicates tight control of V_{BE} characteristics.

Transistors, such as 2N3904, 2N3906, or equivalents in SOT-23 packages, are suitable devices to use.

Table 9. Twos Complement Temperature Data Format

Temperature	Digital Output (10-Bit)[1]
−128°C	1000 0000 **00** (diode fault)
−50°C	1100 1110 **00**
−25°C	1110 0111 **00**
−10°C	1111 0110 **00**
0°C	0000 0000 **00**
10.25°C	0000 1010 **01**
25.5°C	0001 1001 **10**
50.75°C	0011 0010 **11**
75°C	0100 1011 **00**
100°C	0110 0100 **00**
125°C	0111 1101 **00**
127°C	0111 1111 **00**

[1] Bold numbers denote 2 LSB of measurement in Extended Resolution Register 2 (Reg. 0x77) with 0.25°C resolution.

Table 10. Extended Range, Temperature Data Format

Temperature	Digital Output (10-Bit)[1]
−64°C	0000 0000 **00** (diode fault)
−1°C	0011 1111 **00**
0°C	0100 0000 **00**
1°C	0100 0001 **00**
10°C	0100 1010 **00**
25°C	0101 1001 **00**
50°C	0111 0010 **00**
75°C	1000 1001 **00**
100°C	1010 0100 **00**
125°C	1011 1101 **00**
191°C	1111 1111 **00**

[1] Bold numbers denote 2 LSB of measurement in Extended Resolution Register 2 (Reg. 0x77) with 0.25°C resolution.

Nulling Out Temperature Errors

As CPUs run faster, it is more difficult to avoid high frequency clocks when routing the D+/D− traces around a system board. Even when recommended layout guidelines are followed, some temperature errors can still be attributable to noise coupled onto the D+/D− lines. Constant high frequency noise usually attenuates, or increases, temperature measurements by a linear, constant value.

The ADT7476 has temperature offset registers at Addresses 0x70, 0x72 for the Remote 1 and Remote 2 temperature channels. By doing a one-time calibration of the system, the user can determine the offset caused by system board noise and null it out using the offset registers. The offset registers automatically add a twos complement 8-bit reading to every temperature measurement.

Changing Bit 1 of Configuration Register 5 (0x7C) changes the resolution and therefore the range of the temperature offset as either having a range of −63°C to +127°C with a resolution of 1°C or having a range of −63°C to +64°C with a resolution of 0.5°C. This temperature offset can be used to compensate for linear temperature errors introduced by noise.

Temperature Offset Registers

Reg. 0x70, **Remote 1 Temperature Offset** = 0x00 (0°C default)

Reg. 0x71, **Local Temperature Offset** = 0x00 (0°C default)

Reg. 0x72, **Remote 2 Temperature Offset** = 0x00 (0°C default)

ADT7463/ADT7476 Backwards Compatible Mode

By setting Bit 0 of Configuration Register 5 (0x7C), all temperature measurements are stored in the zone temperature value registers (0x25, 0x26, and 0x27) in twos complement in the range −63°C to +127°C. The temperature limits must be reprogrammed in twos complement.

If a twos complement temperature below −63°C is entered, the temperature is clamped to −63°C. In this mode, the diode fault condition remains −128°C = 1000 0000, while in the extended temperature range (−63°C to +191°C), the fault condition is represented by −64°C = 0000 0000.

Temperature Measurement Registers

Reg. 0x25, **Remote 1 Temperature**

Reg. 0x26, **Local Temperature**

Reg. 0x27, **Remote 2 Temperature**

Reg. 0x77, **Extended Resolution 2** = 0x00 default

<7:6> TDM2, Remote 2 temperature LSBs.

<5:4> LTMP, Local temperature LSBs.

<3:2> TDM1, Remote 1 temperature LSBs.

Temperature Measurement Limit Registers

Associated with each temperature measurement channel are high and low limit registers. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate $\overline{\text{SMBALERT}}$ interrupts (depending on the way the interrupt mask register is programmed and assuming that $\overline{\text{SMBALERT}}$ is set as an output on the appropriate pin).

Reg. 0x4E, **Remote 1 Temperature Low Limit** = 0x81 default

Reg. 0x4F, **Remote 1 Temperature High Limit** = 0x7F default

Reg. 0x50, **Local Temperature Low Limit** = 0x81 default

Reg. 0x51, **Local Temperature High Limit** = 0x7F default

Reg. 0x52, **Remote 2 Temperature Low Limit** = 0x81 default

Reg. 0x53, **Remote 2 Temperature High Limit** = 0x7F default

Reading Temperature from the ADT7476

It is important to note that temperature can be read from the ADT7476 as an 8-bit value (with 1°C resolution) or as a 10-bit value (with 0.25°C resolution). If only 1°C resolution is required, the temperature readings can be read back at any time and in no particular order.

If the 10-bit measurement is required, this involves a 2-register read for each measurement. The extended resolution register (Reg. 0x77) should be read first. This causes all temperature reading registers to be frozen until all temperature reading registers have been read from. This prevents an MSB reading from being updated while its two LSBs are being read and vice versa.

ADDITIONAL ADC FUNCTIONS FOR TEMPERATURE MEASUREMENT

A number of other functions are available on the ADT7476 to offer the system designer increased flexibility.

Turn-Off Averaging

For each temperature measurement read from a value register, 16 readings have actually been made internally, and the results averaged, before being placed into the value register. Sometimes it is necessary to take a very fast measurement. Setting Bit 4 of Configuration Register 2 (Reg. 0x73) turns averaging off. The default round-robin cycle time takes 146.5 ms.

Table 11. Conversion Time with Averaging Disabled

Channel	Measurement Time (ms)
Voltage Channels	0.7
Remote Temperature 1	7
Remote Temperature 2	7
Local Temperature	1.3

When bit 7 of Configuration Register 6 (0x10) is set, the default round-robin cycle time increases to 240 ms.

Table 12. Conversion Time with Averaging Enabled

Channel	Measurement Time (ms)
Voltage Channels	11
Remote Temperature	39
Local Temperature	12

Single-Channel ADC Conversions

Setting Bit 6 of Configuration Register 2 (Reg. 0x73) places the ADT7476 into single-channel ADC conversion mode. In this mode, the ADT7476 can be made to read a single temperature channel only. The appropriate ADC channel is selected by writing to Bits <7:5> of the TACH1 minimum high byte register (0x55).

Table 13. Programming Single Channel ADC Mode for Temperatures

Bits <7:5> Reg. 0x55	Channel Selected
101	Remote 1 temperature
110	Local temperature
111	Remote 2 temperature

Configuration Register 2 (Reg. 0x73)

<4> = 1, averaging off.

<6> = 1, single-channel convert mode.

TACH1 Minimum High Byte (Reg. 0x55)

<7:5> selects ADC channel for single-channel convert mode.

Overtemperature Events

Overtemperature events on any of the temperature channels can be detected and dealt with automatically in automatic fan speed control mode. Register 0x6A to Register 0x6C are the $\overline{\text{THERM}}$ temperature limits. When a temperature exceeds its $\overline{\text{THERM}}$ temperature limit, all PWM outputs run at the maximum PWM duty cycle (Reg. 0x38, Reg. 0x39, and Reg. 0x3A). This effectively runs the fans at the fastest allowed speed. The fans run at this speed until the temperature drops below $\overline{\text{THERM}}$ minus hysteresis. This can be disabled by setting the boost bit in Configuration Register 3, Bit 2 (Reg. 0x78). The hysteresis value for the $\overline{\text{THERM}}$ temperature limit is the value programmed into the hysteresis registers (Reg. 0x6D and Reg. 0x6E). The default hysteresis value is 4°C.

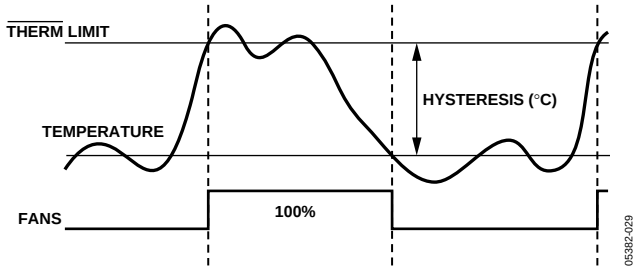


Figure 28. $\overline{\text{THERM}}$ Temperature Limit Operation

$\overline{\text{THERM}}$ can be disabled on specific temperature channels using bits <7:5> of Configuration Register 5 (0x7C). $\overline{\text{THERM}}$ can also be disabled by:

- In offset 64 mode, writing −64°C to the appropriate $\overline{\text{THERM}}$ temperature limit.
- In twos complement mode, writing −128°C to the appropriate $\overline{\text{THERM}}$ temperature limit.

LIMITS, STATUS REGISTERS, AND INTERRUPTS

LIMIT VALUES

Associated with each measurement channel on the ADT7476 are high and low limits. These can form the basis of system status monitoring; a status bit can be set for any out-of-limit condition and is detected by polling the device. Alternatively, $\overline{\text{SMBALERT}}$ interrupts can be generated to flag out-iof-limit conditions to a processor or microcontroller.

8-Bit Limits

The following is a list of 8-bit limits on the ADT7476.

Voltage Limit Registers

Reg. 0x44, **2.5 V Low Limit** = 0x00 default

Reg. 0x45, **2.5 V High Limit** = 0xFF default

Reg. 0x46, **V_{CCP} Low Limit** = 0x00 default

Reg. 0x47, **V_{CCP} High Limit** = 0xFF default

Reg. 0x48, **V_{CC} Low Limit** = 0x00 default

Reg. 0x49, **V_{CC} High Limit** = 0xFF default

Reg. 0x4A, **5 V Low Limit** = 0x00 default

Reg. 0x4B, **5 V High Limit** = 0xFF default

Reg. 0x4C, **12 V Low Limit** = 0x00 default

Reg. 0x4D, **12 V High Limit** = 0xFF default

Temperature Limit Registers

Reg. 0x4E, **Remote 1 Temperature Low Limit** = 0x81 default

Reg. 0x4F, **Remote 1 Temperature High Limit** = 0x7F default

Reg. 0x6A, **Remote 1 $\overline{\text{THERM}}$ Limit** = 0x64 default

Reg. 0x50, **Local Temperature Low Limit** = 0x81 default

Reg. 0x51, **Local Temperature High Limit** = 0x7F default

Reg. 0x6B, **Local $\overline{\text{THERM}}$ Limit** = 0x64 default

Reg. 0x52, **Remote 2 Temperature Low Limit** = 0x81 default

Reg. 0x53, **Remote 2 Temperature High Limit** = 0x7F default

Reg. 0x6C, **Remote 2 $\overline{\text{THERM}}$ Limit** = 0x64 default

$\overline{\text{THERM}}$ Limit Register

Reg. 0x7A, **$\overline{\text{THERM}}$ Limit** = 0x00 default

16-Bit Limits

The fan TACH measurements are 16-bit results. The fan TACH limits are also 16 bits, consisting of a high byte and low byte. Because fans running under speed or stalled are normally the only conditions of interest, only high limits exist for fan TACHs. Because the fan TACH period is actually being measured, exceeding the limit indicates a slow or stalled fan.

Fan Limit Registers

Reg. 0x54, **TACH1 Minimum Low Byte** = 0xFF default

Reg. 0x55, **TACH1 Minimum High Byte** = 0xFF default

Reg. 0x56, **TACH2 Minimum Low Byte** = 0xFF default

Reg. 0x57, **TACH2 Minimum High Byte** = 0xFF default

Reg. 0x58, **TACH3 Minimum Low Byte** = 0xFF default

Reg. 0x59, **TACH3 Minimum High Byte** = 0xFF default

Reg. 0x5A, **TACH4 Minimum Low Byte** = 0xFF default

Reg. 0x5B, **TACH4 Minimum High Byte** = 0xFF default

Out-of-Limit Comparisons

Once all limits have been programmed, the ADT7476 can be enabled for monitoring. The ADT7476 measures all voltage and temperature measurements in round-robin format and sets the appropriate status bit for out-of-limit conditions. TACH measurements are not part of this round-robin cycle. Comparisons are done differently depending on whether the measured value is being compared to a high or low limit.

High Limit: > Comparison Performed

Low Limit: ≤ Comparison Performed

Voltage and temperature channels use a window comparator for error detecting and, therefore, have high and low limits. Fan speed measurements use only a low limit. This fan limit is needed only in manual fan control mode.

Analog Monitoring Cycle Time

The analog monitoring cycle begins when a 1 is written to the start bit (Bit 0) of Configuration Register 1 (Reg. 0x40). The ADC measures each analog input in turn, and, as each measurement is completed, the result is automatically stored in the appropriate value register. This round-robin monitoring cycle continues unless disabled by writing a 0 to Bit 0 of Configuration Register 1.

As the ADC is normally left to free-run in this manner, the time taken to monitor all the analog inputs is normally not of interest, because the most recently measured value of any input can be read out at any time.

For applications where the monitoring cycle time is important, it can easily be calculated.

The total number of channels measured is

- Four dedicated supply voltage inputs
- Supply voltage (V_{CC} pin)
- Local temperature
- Two remote temperatures

As mentioned previously, the ADC performs round-robin conversions and takes 11 ms for each voltage measurement, 12 ms for a local temperature reading, and 39 ms for each remote temperature reading. The total monitoring cycle time for averaged voltage and temperature monitoring is, therefore, nominally

$$(5 \times 11) + 12 + (2 \times 39) = 145 \text{ ms}$$

Fan TACH measurements are made in parallel and are not synchronized with the analog measurements in any way.

STATUS REGISTERS

The results of limit comparisons are stored in Status Register 1 and Status Register 2. The status register bit for each channel reflects the status of the last measurement and limit comparison on that channel. If a measurement is within limits, the corresponding status register bit is cleared to 0. If the measurement is out-of-limits, the corresponding status register bit is set to 1.

The state of the various measurement channels can be polled by reading the status registers over the serial bus. In Bit 7 (OOL) of Status Register 1 (Reg. 0x41), 1 means an out-of-limit event has been flagged in Status Register 2. This means the user also needs to read Status Register 2. Alternatively, Pin 10 or Pin 14 can be configured as an $\overline{\text{SMBALERT}}$ output. This hard interrupt automatically notifies the system supervisor of an out-of-limit condition. Reading the status registers clears the appropriate status bit as long as the error condition that caused the interrupt has cleared. Status register bits are *sticky*. Whenever a status bit is set, indicating an out-of-limit condition, it remains set even if the event that caused it has gone away (until read).

The only way to clear the status bit is to read the status register after the event has gone away. Interrupt status mask registers (Reg. 0x74, and Reg. 0x75) allow individual interrupt sources to be masked from causing an $\overline{\text{SMBALERT}}$. However, if one of these masked interrupt sources goes out-of-limit, its associated status bit is set in the interrupt status registers.

Status Register 1 (Reg. 0x41)

Bit 7 (OOL) = 1, denotes a bit in Status Register 2 is set and Status Register 2 should be read.

Bit 6 (R2T) = 1, Remote 2 temperature high or low limit has been exceeded.

Bit 5 (LT) = 1, Local temperature high or low limit has been exceeded.

Bit 4 (R1T) = 1, Remote 1 temperature high or low limit has been exceeded.

Bit 3 (5 V) = 1, 5 V high or low limit has been exceeded.

Bit 2 (V_{CC}) = 1, V_{CC} high or low limit has been exceeded.

Bit 1 (V_{CCP}) = 1, V_{CCP} high or low limit has been exceeded.

Bit 0 (2.5 V) = 1, 2.5 V high or low limit has been exceeded. If the 2.5 V input is configured as $\overline{\text{THERM}}$, this bit represents the status of $\overline{\text{THERM}}$.

Status Register 2 (Reg. 0x42)

Bit 7 (D2) = 1, indicates an open or short on D2+/D2– inputs.

Bit 6 (D1) = 1, indicates an open or short on D1+/D1– inputs.

Bit 5 (F4P) = 1, indicates Fan 4 has dropped below minimum speed. Alternatively, indicates that the $\overline{\text{THERM}}$ limit has been exceeded, if the $\overline{\text{THERM}}$ function is used. Alternatively, indicates the status of GPIO6.

Bit 4 (FAN3) = 1, indicates Fan 3 has dropped below minimum speed.

Bit 3 (FAN2) = 1, indicates Fan 2 has dropped below minimum speed.

Bit 2 (FAN1) = 1, indicates Fan 1 has dropped below minimum speed.

Bit 1 (OVT) = 1, indicates a $\overline{\text{THERM}}$ overtemperature limit has been exceeded.

Bit 0 (12V/VC) = 1, indicates a 12 V high or low limit has been exceeded. If the VID code change function is used, this bit indicates a change in VID code on the VID0 to VID5 inputs.

$\overline{\text{SMBALERT}}$ Interrupt Behavior

The ADT7476 can be polled for status, or an $\overline{\text{SMBALERT}}$ interrupt can be generated for out-of-limit conditions. It is important to note how the $\overline{\text{SMBALERT}}$ output and status bits behave when writing interrupt handler software.

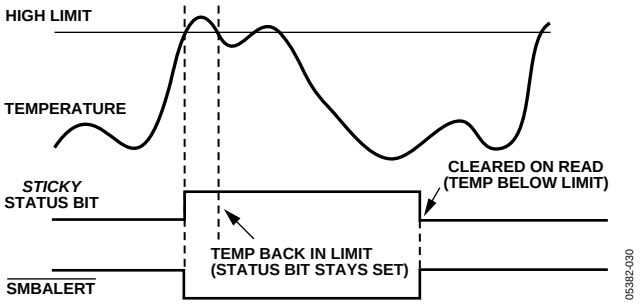


Figure 29. SMBALERT and Status Bit Behavior

Figure 29 shows how the SMBALERT output and *sticky* status bits behave. Once a limit is exceeded, the corresponding status bit is set to 1. The status bit remains set until the error condition subsides and the status register is read. The status bits are referred to as *sticky,* because they remain set until read by software. This ensures that an out-of-limit event cannot be missed, if software is polling the device periodically.

Note: The SMBALERT output remains low for the entire duration that a reading is out-of-limit and until the status register has been read. This has implications on how software handles the interrupt.

Handling SMBALERT Interrupts

To prevent the system from being tied up servicing interrupts, it is recommend to handle the SMBALERT interrupt as follows:

1. Detect the SMBALERT assertion.
2. Enter the interrupt handler.
3. Read the status registers to identify the interrupt source.
4. Mask the interrupt source by setting the appropriate mask bit in the interrupt mask registers (Reg. 0x74 and Reg. 0x75).
5. Take the appropriate action for a given interrupt source.
6. Exit the interrupt handler.
7. Periodically poll the status registers. If the interrupt status bit has cleared, reset the corresponding interrupt mask bit to 0. This causes the SMBALERT output and status bits to behave as shown in Figure 30.

Masking Interrupt Sources

Interrupt Mask Register 1 and Interrupt Mask Register 2 are located at Addresses 0x74 and 0x75. These allow individual interrupt sources to be masked out to prevent SMBALERT interrupts. Note: Masking an interrupt source prevents only the SMBALERT output from being asserted; the appropriate status bit is set normally.

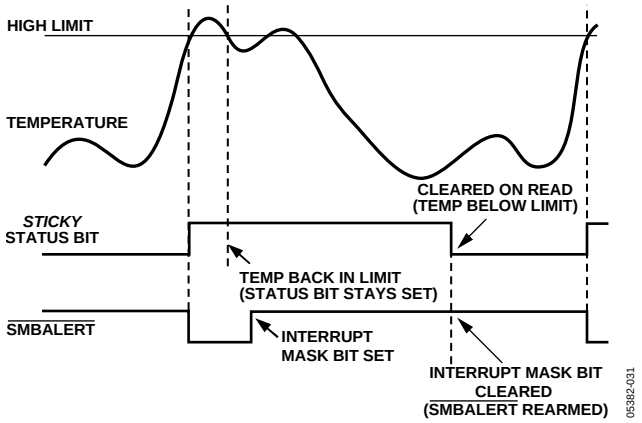


Figure 30. How Masking the Interrupt Source Affects SMBALERT Output

Interrupt Mask Register 1 (Reg. 0x74)

Bit 7 (OOL) = 1, masks SMBALERT for any alert condition flagged in Status Register 2.

Bit 6 (R2T) = 1, masks SMBALERT for Remote 2 temperature.

Bit 5 (LT) = 1, masks SMBALERT for local temperature.

Bit 4 (R1T) = 1, masks SMBALERT for Remote 1 temperature.

Bit 3 (5 V) = 1, masks SMBALERT for 5 V channel.

Bit 2 (V_{CC}) = 1, masks SMBALERT for V_{CC} channel.

Bit 1 (V_{CCP}) = 1, masks SMBALERT for V_{CCP} channel.

Bit 0 (2.5V) = 1, masks SMBALERT for 2.5V/ THERM.

Interrupt Mask Register 2 (Reg. 0x75)

Bit 7 (D2) = 1, masks SMBALERT for Diode 2 errors.

Bit 6 (D1) = 1, masks SMBALERT for Diode 1 errors.

Bit 5 (FAN4) = 1, masks SMBALERT for Fan 4 failure.

If the TACH4 pin is being used as the THERM input, this bit masks SMBALERT for a THERM event. If the TACH4 pin is being used as GPIO6, setting this bit masks interrupts related to GPIO6.

Bit 4 (FAN3) = 1, masks SMBALERT for Fan 3.

Bit 3 (FAN2) = 1, masks SMBALERT for Fan 2.

Bit 2 (FAN1) = 1, masks SMBALERT for Fan 1.

Bit 1 (OVT) = 1, masks SMBALERT for overtemperature (exceeding THERM temperature limits).

Bit 0 (12V/VC) = 1, masks SMBALERT for 12 V channel or for a VID code change, depending on the function used.

Enabling the $\overline{\text{SMBALERT}}$ Interrupt Output

The $\overline{\text{SMBALERT}}$ interrupt function is disabled by default. Pin 10 or Pin 14 can be reconfigured as an $\overline{\text{SMBALERT}}$ output to signal out-of-limit conditions.

Table 14. Configuring Pin 10 as $\overline{\text{SMBALERT}}$ Output

Register	Bit Setting
Configuration Register 3 (Reg. 0x78)	<1> Pin 10 = $\overline{\text{SMBALERT}}$
	<0> Pin 10 = PWM2

Assigning $\overline{\text{THERM}}$ Functionality to a Pin

Pin 14 on the ADT7476 has four possible functions: $\overline{\text{SMBALERT}}$, $\overline{\text{THERM}}$, GPIO6, and TACH4. The user chooses the required functionality by setting Bit 0 and Bit 1 of Configuration Register 4 at Address 0x7D.

If $\overline{\text{THERM}}$ is enabled (Bit 1, Configuration Register 3 at Address 0x78):

- Pin 22 becomes $\overline{\text{THERM}}$.
- If Pin 14 is configured as $\overline{\text{THERM}}$ (Bit 0 and Bit 1 of Configuration Register 4 at Address 0x7D), $\overline{\text{THERM}}$ is enabled on this pin.

If $\overline{\text{THERM}}$ is not enabled:

- Pin 22 becomes a 2.5 V measurement input.
- If Pin 14 is configured as $\overline{\text{THERM}}$, then $\overline{\text{THERM}}$ is disabled on this pin.

Table 15. Configuring Pin 14

Bit 0	Bit 1	Function
0	0	TACH4
0	1	$\overline{\text{THERM}}$
1	0	$\overline{\text{SMBALERT}}$
1	1	GPIO6

$\overline{\text{THERM}}$ as an Input

When $\overline{\text{THERM}}$ is configured as an input, the user can time assertions on the $\overline{\text{THERM}}$ pin. This can be useful for connecting to the $\overline{\text{PROCHOT}}$ output of a CPU to gauge system performance.

The user can also set up the ADT7476, so that, when the $\overline{\text{THERM}}$ pin is driven low externally, the fans run at 100%. The fans run at 100% for the duration of the time that the $\overline{\text{THERM}}$ pin is pulled low. This is done by setting the BOOST bit (Bit 2) in Configuration Register 3 (Address 0x78) to 1. This works only if the fan is already running, for example, in manual mode when the current duty cycle is above 0x00, or in automatic mode when the temperature is above T_{MIN}.

If the temperature is below T_{MIN} or if the duty cycle in manual mode is set to 0x00, pulling the $\overline{\text{THERM}}$ low externally has no effect. See Figure 31 for more information.

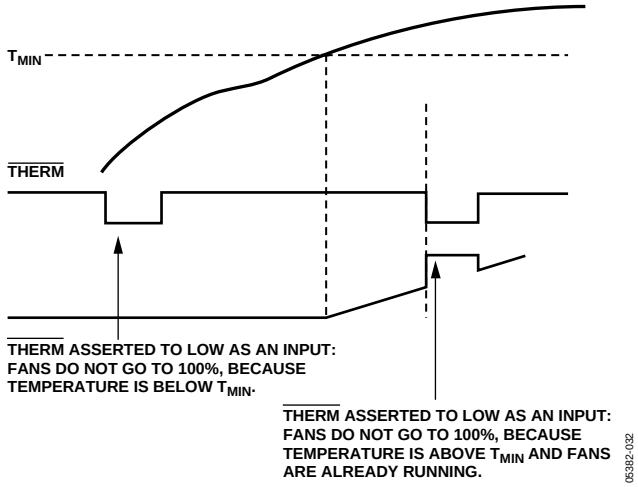


Figure 31. Asserting $\overline{\text{THERM}}$ Low as an Input in Automatic Fan Speed Control Mode

$\overline{\text{THERM}}$ TIMER

The ADT7476 has an internal timer to measure $\overline{\text{THERM}}$ assertion time. For example, the $\overline{\text{THERM}}$ input can be connected to the $\overline{\text{PROCHOT}}$ output of a Pentium 4™ CPU to measure system performance. The $\overline{\text{THERM}}$ input can also be connected to the output of a trip point temperature sensor.

The timer is started on the assertion of the ADT7476's $\overline{\text{THERM}}$ input and stopped when $\overline{\text{THERM}}$ is de-asserted. The timer counts $\overline{\text{THERM}}$ times cumulatively, that is, the timer resumes counting on the next $\overline{\text{THERM}}$ assertion. The $\overline{\text{THERM}}$ timer continues to accumulate $\overline{\text{THERM}}$ assertion times until the timer is read (it is cleared on read), or until it reaches full scale. If the counter reaches full scale, it stops at that reading until cleared.

The 8-bit $\overline{\text{THERM}}$ timer register (Reg. 0x79) is designed, so that Bit 0 is set to 1 on the first $\overline{\text{THERM}}$ assertion. Once the cumulative $\overline{\text{THERM}}$ assertion time has exceeded 45.52 ms, Bit 1 of the $\overline{\text{THERM}}$ timer is set and Bit 0 now becomes the LSB of the timer with a resolution of 22.76 ms (see Figure 32).

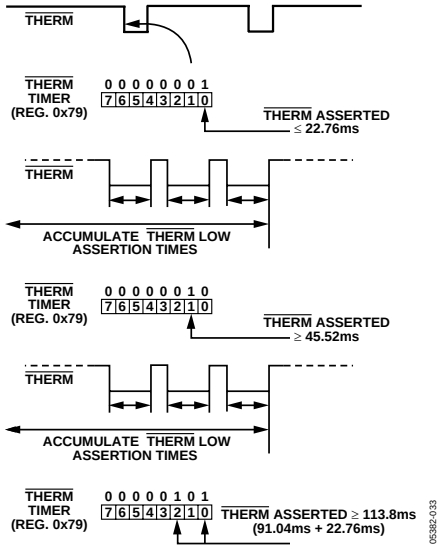


Figure 32.Understanding the THERM Timer

When using the THERM timer, be aware of the following.

After a THERM timer read (Reg. 0x79):

1. The contents of the timer are cleared on read.
2. The F4P bit (Bit 5) of Status Register 2 needs to be cleared (assuming that the THERM timer limit has been exceeded).

If the THERM timer is read during a THERM assertion, the following happens:

1. The contents of the timer are cleared.
2. Bit 0 of the THERM timer is set to 1, because a THERM assertion is occurring.
3. The THERM timer increments from zero.
4. If the THERM timer limit (Reg. 0x7A) = 0x00, the F4P bit is set.

Generating SMBALERT Interrupts from THERM Timer Events

The ADT7476 can generate SMBALERTs when a programmable THERM timer limit has been exceeded. This allows the system designer to ignore brief, infrequent THERM assertions, while capturing longer THERM timer events. Register 0x7A is the THERM timer limit register. This 8-bit register allows a limit from 0s (first THERM assertion) to 5.825 sec to be set before an SMBALERT is generated. The THERM timer value is compared with the contents of the THERM timer limit register. If the THERM timer value exceeds the THERM timer limit value, then the F4P bit (Bit 5) of Status Register 2 is set and an SMBALERT is generated.

Note: Depending on which pins are configured as a THERM timer, setting the F4P bit (Bit 5) of Mask Register 2 (Reg. 0x75), or bit 0 of or Mask Register 1 (Reg. 0x74), masks out SMBALERT; although the F4P bit of Interrupt Status Register 2 still is set, if the THERM timer limit is exceeded.

Figure 33 is a functional block diagram of the THERM timer, limit, and associated circuitry. Writing a value of 0x00 to the THERM timer limit register (Reg. 0x7A) causes an SMBALERT to be generated on the first THERM assertion. A THERM timer limit value of 0x01 generates an SMBALERT, once cumulative THERM assertions exceed 45.52 ms.

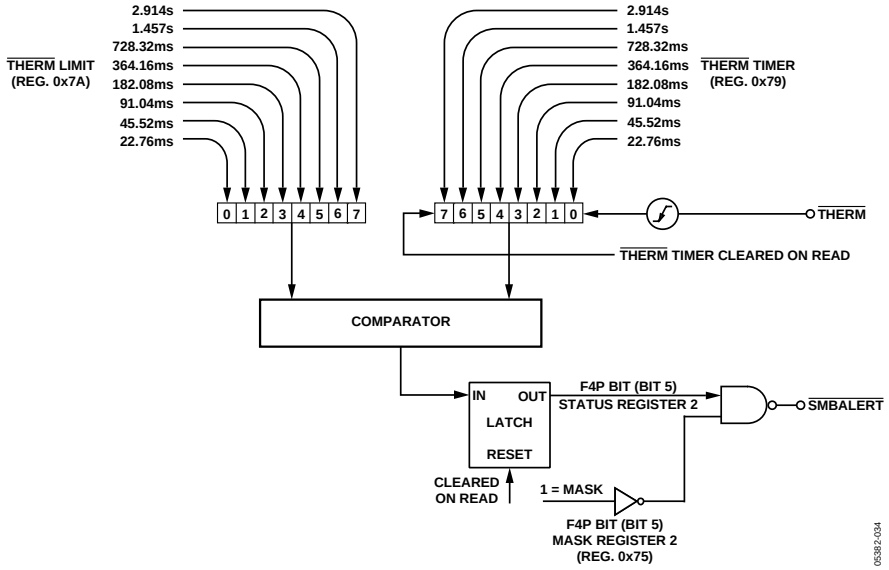


Figure 33. Functional Block Diagram of THERM Monitoring Circuitry

Configuring the Relevant $\overline{\text{THERM}}$ Behavior

1. Configure the desired pin as the $\overline{\text{THERM}}$ timer input.

   Setting Bit 1 ($\overline{\text{THERM}}$ timer enable) of Configuration Register 3 (Reg. 0x78) enables the $\overline{\text{THERM}}$ timer monitoring functionality. This is disabled on Pin 14 and Pin 22 by default.

   Setting Bit 0 and Bit 1 (PIN14FUNC) of Configuration Register 4 (Reg. 0x7D) enables $\overline{\text{THERM}}$ timer output functionality on Pin 22 (Bit 1 of Configuration Register 3, $\overline{\text{THERM}}$, must also be set). Pin 14 can also be used as TACH4.

2. Select the desired fan behavior for $\overline{\text{THERM}}$ timer events.

   Assuming the fans are running, setting Bit 2 (BOOST bit) of Configuration Register 3 (Reg. 0x78) causes all fans to run at 100% duty cycle whenever $\overline{\text{THERM}}$ is asserted. This allows fail-safe system cooling. If this bit is 0, the fans run at their current settings and are not affected by $\overline{\text{THERM}}$ events. If the fans are not already running when $\overline{\text{THERM}}$ is asserted, the fans do not run to full speed.

3. Select whether $\overline{\text{THERM}}$ timer events should generate $\overline{\text{SMBALERT}}$ interrupts.

   Bit 5 (F4P) of Mask Register 2 (Reg. 0x75) or Bit 0 of Mask Register 1 (Reg. 0x74) (depending on which pins are configured as a THERM timer), when set, masks out $\overline{\text{SMBALERT}}$s when the $\overline{\text{THERM}}$ timer limit value is exceeded. This bit should be cleared, if $\overline{\text{SMBALERT}}$s based on $\overline{\text{THERM}}$ events are required.

4. Select a suitable $\overline{\text{THERM}}$ limit value.

   This value determines whether an $\overline{\text{SMBALERT}}$ is generated on the first $\overline{\text{THERM}}$ assertion, or only if a cumulative $\overline{\text{THERM}}$ assertion time limit is exceeded. A value of 0x00 causes an $\overline{\text{SMBALERT}}$ to be generated on the first $\overline{\text{THERM}}$ assertion.

5. Select a $\overline{\text{THERM}}$ monitoring time.

   This value specifies how often OS- or BIOS-level software checks the $\overline{\text{THERM}}$ timer. For example, BIOS can read the $\overline{\text{THERM}}$ timer once an hour to determine the cumulative $\overline{\text{THERM}}$ assertion time. If, for example, the total $\overline{\text{THERM}}$ assertion time is <22.76 ms in Hour 1, >182.08 ms in Hour 2, and >5.825 s in Hour 3, this indicates that system performance is degrading significantly, because $\overline{\text{THERM}}$ is asserting more frequently on an hourly basis.

   Alternatively, OS- or BIOS-level software can timestamp when the system is powered on. If an $\overline{\text{SMBALERT}}$ is generated due to the $\overline{\text{THERM}}$ timer limit being exceeded, another timestamp can be taken. The difference in time can be calculated for a fixed $\overline{\text{THERM}}$ timer limit time. For example, if it takes one week for a $\overline{\text{THERM}}$ timer limit of 2.914 s to be exceeded, and the next time it takes only 1 hour, this is an indication of a serious degradation in system performance.

Configuring the $\overline{\text{THERM}}$ Pin as an Output

In addition to monitoring $\overline{\text{THERM}}$ as an input, the ADT7476 can optionally drive $\overline{\text{THERM}}$ low as an output. When $\overline{\text{PROCHOT}}$ is bidirectional, $\overline{\text{THERM}}$ can be used to throttle the processor by asserting $\overline{\text{PROCHOT}}$. The user can preprogram system-critical thermal limits. If the temperature exceeds a thermal limit by 0.25°C, $\overline{\text{THERM}}$ asserts low. If the temperature is still above the thermal limit on the next monitoring cycle, $\overline{\text{THERM}}$ stays low. $\overline{\text{THERM}}$ remains asserted low until the temperature is equal to or below the thermal limit. Because the temperature for that channel is measured only once for every monitoring cycle, after $\overline{\text{THERM}}$ asserts it is guaranteed to remain low for at least one monitoring cycle.

The $\overline{\text{THERM}}$ pin can be configured to assert low, if the Remote 1, local, or Remote 2 $\overline{\text{THERM}}$ temperature limits are exceeded by 0.25°C. The $\overline{\text{THERM}}$ temperature limit registers are at Registers 0x6A, 0x6B, and 0x6C, respectively. Setting Bits <5:7> of Configuration Register 5 (0x7C) enables the $\overline{\text{THERM}}$ output feature for the Remote 1, local, and Remote 2 temperature channels, respectively. Figure 34 shows how the $\overline{\text{THERM}}$ pin asserts low as an output in the event of a critical overtemperature.

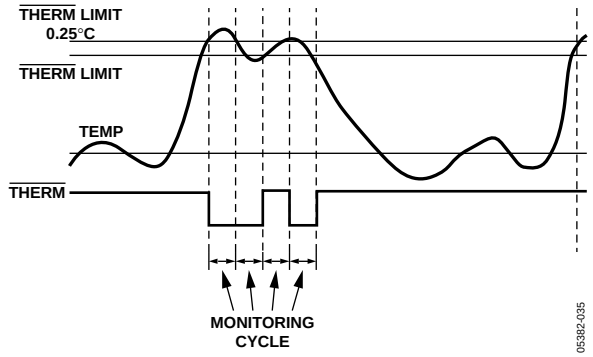


Figure 34. Asserting $\overline{\text{THERM}}$ as an Output, Based on Tripping $\overline{\text{THERM}}$ Limits

An alternative method of disabling $\overline{\text{THERM}}$ is to program the $\overline{\text{THERM}}$ temperature limit to −63°C or less in Offset 64 mode, or −128°C or less in twos complement mode; that is, for $\overline{\text{THERM}}$ temperature limit values less than −63°C or −128°C, respectively, $\overline{\text{THERM}}$ is disabled.

Enabling and Disabling THERM on individual Channels.

$\overline{\text{THERM}}$ can be enabled/disabled for individual or combinations of temperature channels using bits <7:5> of Configuration Register 5 (0x7C).

$\overline{\text{THERM}}$ Hysteresis

Setting Bit 0 of Configuration Register 7 (0x11) disables $\overline{\text{THERM}}$ hysteresis.

If $\overline{\text{THERM}}$ hysteresis is enabled and $\overline{\text{THERM}}$ is disabled (Bit 2 of Configuration Register 4, 0x7D), the $\overline{\text{THERM}}$ pin does not assert low when a $\overline{\text{THERM}}$ event occurs. If $\overline{\text{THERM}}$ hysteresis is disabled and $\overline{\text{THERM}}$ is disabled (Bit 2 of Configuration Register 4, 0x7D)and assuming the appropriate pin is configured as $\overline{\text{THERM}}$), the $\overline{\text{THERM}}$ pin asserts low when a $\overline{\text{THERM}}$ event occurs.

If $\overline{\text{THERM}}$ and $\overline{\text{THERM}}$ hysterisis are both enabled, the $\overline{\text{THERM}}$ output asserts as expected.

$\overline{\text{THERM}}$ Operation in Manual Mode

In manual mode, $\overline{\text{THERM}}$ events do not cause fans to go to full speed, unless Bit 3 of Configuration Register 6 (0x10) is set to 1.

Additionally, Bit 3 of Configuration Register 4 (0x7D) can be used to select PWM speed on THERM event (100% or maximum PWM).

Bit 2 in Configuration Register 4 (0x7D) can be set to disable $\overline{\text{THERM}}$ events from affecting the fans.

FAN DRIVE USING PWM CONTROL

The ADT7476 uses pulse-width modulation (PWM) to control fan speed. This relies on varying the duty cycle (or on/off ratio) of a square wave applied to the fan to vary the fan speed. The external circuitry required to drive a fan using PWM control is extremely simple. For 4-wire fans, the PWM drive might need only a pull-up resistor. In many cases, the 4-wire fan PWM input has a built-in, pull-up resistor.

The ADT7476 PWM frequency can be set to a selection of low frequencies or a single high PWM frequency. The low frequency options are used for 3-wire fans, while the high frequency option is usually used with 4-wire fans.

For 3-wire fans, a single N-channel MOSFET is the only drive device required. The specifications of the MOSFET depend on the maximum current required by the fan being driven and the input capacitance of the FET. Because a 10 kΩ (or greater) resistor must be used as a PWM pull-up, an FET with large input capacitance can cause the PWM output to become distorted and adversely affect the fan control range. This is a requirement only when using high frequency PWM mode.

Typical notebook fans draw a nominal 170 mA, so SOT devices can be used where board space is a concern. In desktops, fans typically draw 250 mA to 300 mA each. If you drive several fans in parallel from a single PWM output or drive larger server fans, the MOSFET must handle the higher current requirements. The only other stipulation is that the MOSFET should have a gate voltage drive, V_{GS} < 3.3 V, for direct interfacing to the PWM output pin. The MOSFET should also have a low on resistance to ensure that there is not a significant voltage drop across the FET, which would reduce the voltage applied across the fan and, therefore, the maximum operating speed of the fan.

Figure 35 shows how to drive a 3-wire fan using PWM control.

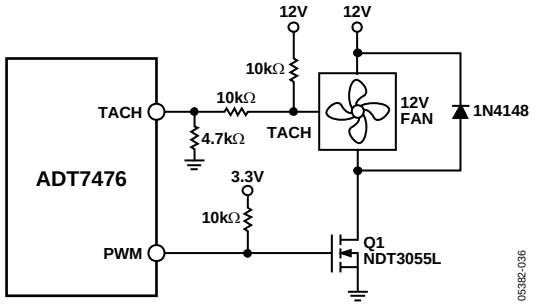


Figure 35. Driving a 3-Wire Fan Using an N-Channel MOSFET

Figure 35 uses a 10 kΩ pull-up resistor for the TACH signal. This assumes that the TACH signal is an open-collector from the fan. In all cases, the TACH signal from the fan must be kept below 3.6 V maximum to prevent damaging the ADT7476.

Figure 36 shows a fan drive circuit using an NPN transistor such as a general-purpose MMBT2222. While these devices are inexpensive, they tend to have much lower current handling capabilities and higher on resistance than MOSFETs. When choosing a transistor, care should be taken to ensure that it meets the fan's current requirements. Ensure that the base resistor is chosen, so the transistor is saturated when the fan is powered on.

Because in 4-wire fans the fan drive circuitry is not switched on or off, as with previous PWM driven/powered fans, the internal drive circuit is always on and uses the PWM input as a signal instead of a power supply. This enables the internal fan drive circuit to perform better than 3-wire fans, especially for high frequency applications.

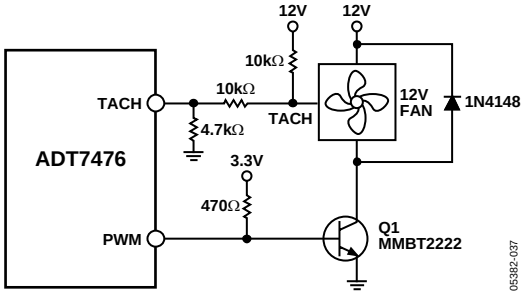


Figure 36. Driving a 3-Wire Fan Using an NPN Transistor

Figure 37 shows a typical drive circuit for 4-wire fans.

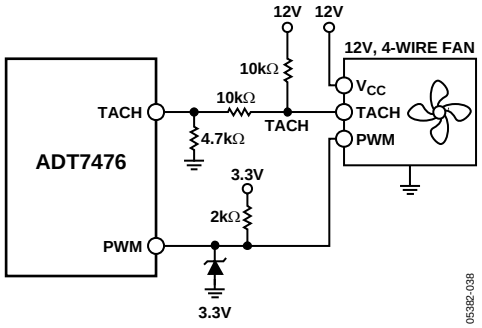


Figure 37. Driving a 4-Wire Fan

Driving Two Fans from PWM3

The ADT7476 has four TACH inputs available for fan speed measurement, but only three PWM drive outputs. If a fourth fan is being used in the system, it should be driven from the PWM3 output in parallel with the third fan.

Figure 38 shows how to drive two fans in parallel using low cost NPN transistors. Figure 39 shows the equivalent circuit using a MOSFET.

Because the MOSFET can handle up to 3.5 A, it is simply a matter of connecting another fan directly in parallel with the first. Care should be taken in designing drive circuits with transistors and FETs to ensure the PWM outputs are not required to source current, and they sink less than the 5 mA maximum current specified on the data sheet.

Driving up to Three Fans from PWM3

TACH measurements for fans are synchronized to particular PWM channels; for example, TACH1 is synchronized to PWM1. TACH3 and TACH4 are both synchronized to PWM3, so PWM3 can drive two fans. Alternatively, PWM3 can be programmed to synchronize TACH2, TACH3, and TACH4 to the PWM3 output. This allows PWM3 to drive two or three fans. In this case, the drive circuitry looks the same, as shown in Figure 38 and Figure 39. The SYNC bit in Register 0x62 enables this function.

Synchronization is not required in high frequency mode when used with 4-wire fans.

(SYNC) Enhance Acoustics Register 1 (Reg. 0x62)

<4>SYNC = 1, synchronizes TACH2, TACH3, and TACH4 to PWM3.

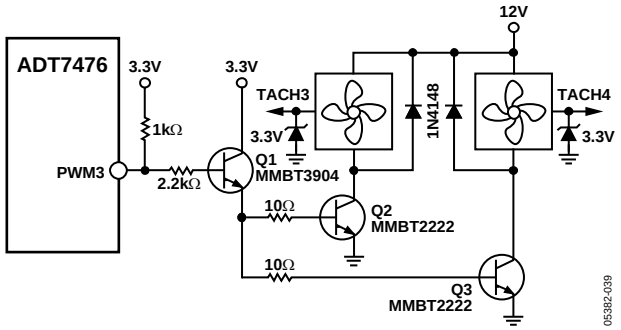


Figure 38. Interfacing Two Fans in Parallel to the PWM3 Output Using Low Cost NPN Transistors

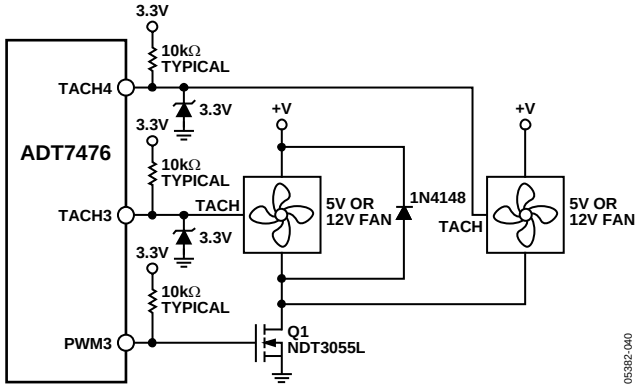


Figure 39. Interfacing Two Fans in Parallel to the PWM3 Output Using a Single N-Channel MOSFET

LAYING OUT 3-WIRE FANS

Figure 40 shows how to lay out a common circuit arrangement for 3-wire fans.

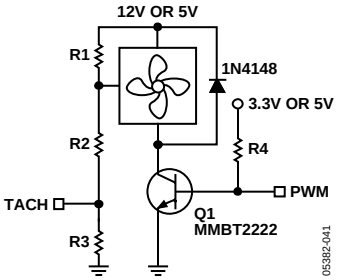


Figure 40. Planning for 3-Wire Fans on a PCB

TACH Inputs

Pins 9, 11, 12, and 14 (when configured as TACH inputs) are high impedance inputs intended for fan speed measurement.

Signal conditioning in the ADT7476 accommodates the slow rise and fall times typical of fan tachometer outputs. The maximum input signal range is 0 V to 3.6 V, even though V_{CC} is 3.3 V. In the event that these inputs are supplied from fan outputs that exceed 0 V to 3.6 V, either resistive attenuation of the fan signal or diode clamping must be included to keep inputs within an acceptable range.

Figure 41 to Figure 44 show circuits for most common fan TACH outputs.

If the fan TACH output has a resistive pull-up to V_{CC}, it can be connected directly to the fan input, as shown in Figure 41.

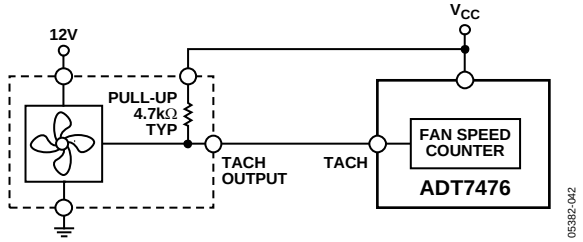


Figure 41. Fan with TACH Pull-Up to V_{CC}

If the fan output has a resistive pull-up to 12 V, or other voltage greater than 3.6 V, the fan output can be clamped with a Zener diode, as shown in Figure 42. The Zener diode voltage should be chosen so that it is greater than V_{IH} of the TACH input but less than 3.6 V, allowing for the voltage tolerance of the Zener. A value of between 3 V and 3.6 V is suitable.

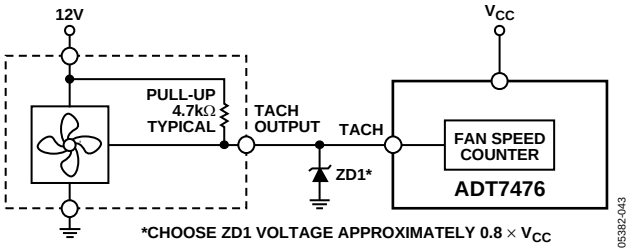


Figure 42. Fan with TACH Pull-Up to Voltage > 3.6 V, for example, 12 V) Clamped with Zener Diode

If the fan has a strong pull-up (less than 1 kΩ) to 12 V or a totem-pole output, a series resistor can be added to limit the Zener current, as shown in Figure 43.

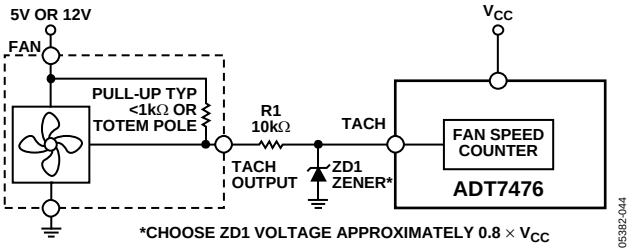


Figure 43. Fan with Strong TACH Pull-Up to > V_{CC} or Totem-Pole Output, Clamped with Zener Diode and Resistor

Alternatively, a resistive attenuator can be used, as shown in Figure 44. R1 and R2 should be chosen such that

$$2\text{ V} < V_{PULL\text{-}UP} \times R2/(R_{PULL\text{-}UP} + R1 + R2) < 3.6\text{ V}$$

The fan inputs have an input resistance of nominally 160 kΩ to ground, which should be taken into account when calculating resistor values.

With a pull-up voltage of 12 V and pull-up resistor less than 1 kΩ, suitable values for R1 and R2 are 100 kΩ and 40 kΩ, respectively. This gives a high input voltage of 3.42 V.

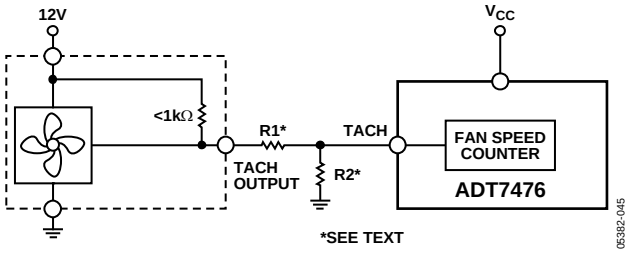


Figure 44. Fan with Strong TACH Pull-Up to > V_{CC} or Totem-Pole Output, Attenuated with R1/R2

The fan counter does not count the fan TACH output pulses directly, because the fan speed could be less than 1,000 RPM and it takes several seconds to accumulate a reasonably large and accurate count. Instead, the period of the fan revolution is measured by gating an on-chip 90 kHz oscillator into the input of a 16-bit counter for *N* periods of the fan TACH output (Figure 45), so the accumulated count is actually proportional to the fan tachometer period and inversely proportional to the fan speed.

N, the number of pulses counted, is determined by the settings of TACH pulses per revolution register (Reg. 0x7B). This register contains two bits for each fan, allowing one, two (default), three, or four TACH pulses to be counted.

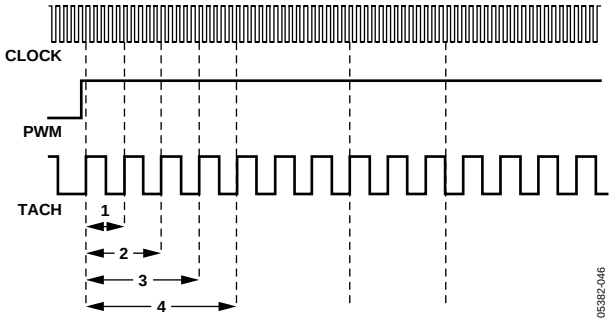


Figure 45. Fan Speed Measurement

Fan Speed Measurement Registers

The fan tachometer readings are 16-bit values consisting of a 2-byte read from the ADT7476.

Reg. 0x28, **TACH1 Low Byte** = 0x00 default

Reg. 0x29, **TACH1 High Byte** = 0x00 default

Reg. 0x2A, **TACH2 Low Byte** = 0x00 default

Reg. 0x2B, **TACH2 High Byte** = 0x00 default

Reg. 0x2C, **TACH3 Low Byte** = 0x00 default

Reg. 0x2D, **TACH3 High Byte** = 0x00 default

Reg. 0x2E, **TACH4 Low Byte** = 0x00 default

Reg. 0x2F, **TACH4 High Byte** = 0x00 default

Reading Fan Speed from the ADT7476

The measurement of fan speeds involves a 2-register read for each measurement. The low byte should be read first. This causes the high byte to be frozen until both high and low byte registers have been read, preventing erroneous TACH readings. The fan tachometer reading registers report back the number of 11.11 µs period clocks (90 kHz oscillator) gated to the fan speed counter, from the rising edge of the first fan TACH pulse to the rising edge of the third fan TACH pulse (assuming two pulses per revolution are being counted).

Because the device is essentially measuring the fan TACH period, the higher the count value, the slower the fan is actually running. A 16-bit fan tachometer reading of 0xFFFF indicates that either the fan has stalled or is running very slowly (<100 RPM).

High Limit: > Comparison Performed

Because the actual fan TACH period is being measured, falling below a fan TACH limit by 1 sets the appropriate status bit and can be used to generate an $\overline{\text{SMBALERT}}$.

Fan TACH Limit Registers

The fan TACH limit registers are 16-bit values consisting of two bytes.

Reg. 0x54, **TACH1 Minimum Low Byte** = 0xFF default

Reg. 0x55, **TACH1 Minimum High Byte** = 0xFF default

Reg. 0x56, **TACH2 Minimum Low Byte** = 0xFF default

Reg. 0x57, **TACH2 Minimum High Byte** = 0xFF default

Reg. 0x58, **TACH3 Minimum Low Byte** = 0xFF default

Reg. 0x59, **TACH3 Minimum High Byte** = 0xFF default

Reg. 0x5A, **TACH4 Minimum Low Byte** = 0xFF default

Reg. 0x5B, **TACH4 Minimum High Byte** = 0xFF default

Fan Speed Measurement Rate

The fan TACH readings are normally updated once every second.

The FAST bit (Bit 3) of Configuration Register 3 (Reg. 0x78), when set, updates the fan TACH readings every 250 ms.

DC Bits

If any of the fans are not being driven by a PWM channel but are powered directly from 5 V or 12 V, their associated dc bit in Configuration Register 3 should be set. This allows TACH readings to be taken on a continuous basis for fans connected directly to a dc source. For 4-wire fans, once high frequency mode is enabled, the DC bits do not need to be set as this is done automatically internally.

Calculating Fan Speed

Assuming a fan with a two pulses per revolution, and with the ADT7476 programmed to measure two pulses per revolution, fan speed is calculated by

$$\textit{Fan Speed (RPM)} = (90{,}000 \times 60)/\textit{Fan TACH Reading}$$

where *Fan TACH Reading* is the 16-bit fan tachometer reading.

Example

TACH1 High Byte (Reg. 0x29) = 0x17

TACH1 Low Byte (Reg. 0x28) = 0xFF

What is Fan 1 speed in RPM?

Fan 1 TACH Reading = 0x17FF = 6143 (decimal)

RPM = (*f* × 60)/*Fan 1 TACH Reading*

RPM = (90000 × 60)/6143

Fan Speed = 879 RPM

Fan Pulses per Revolution

Different fan models can output either one, two, three, or four TACH pulses per revolution. Once the number of fan TACH pulses has been determined, it can be programmed into the fan pulses per revolution register (Reg. 0x7B) for each fan. Alternatively, this register can be used to determine the number or pulses per revolution output by a given fan. By plotting fan speed measurements at 100% speed with different pulses per revolution setting, the smoothest graph with the lowest ripple determines the correct pulses per revolution value.

Fan Pulses per Revolution Register

<1:0> Fan 1 default = 2 pulses per revolution.

<3:2> Fan 2 default = 2 pulses per revolution.

<5:4> Fan 3 default = 2 pulses per revolution.

<7:6> Fan 4 default = 2 pulses per revolution.

00 = 1 pulse per revolution.

01 = 2 pulses per revolution.

10 = 3 pulses per revolution.

11 = 4 pulses per revolution.

Fan Spin-Up

The ADT7476 has a unique fan spin-up function. It spins the fan at 100% PWM duty cycle until two TACH pulses are detected on the TACH input. Once two TACH pulses have been detected, the PWM duty cycle goes to the expected running value, for example, 33%. The advantage is that fans have different spin-up characteristics and take different times to overcome inertia. The ADT7476 runs the fans just fast enough to overcome inertia and is quieter on spin-up than fans programmed to spin up for a given spin-up time.

Fan Startup Timeout

To prevent the generation of false interrupts as a fan spins up, because it is below running speed, the ADT7476 includes a fan startup timeout function. During this time, the ADT7476 looks for two TACH pulses. If two TACH pulses are not detected, then an interrupt is generated.

Fan startup timeout can be disabled by setting Bit 5 (FSPDIS) of Configuration Register 1 (0x40).

PWM1, PWM2, PWM3 Configuration (Reg. 0x5C, 0x5D, 0x5E)

<2:0> SPIN, startup timeout for PWM1 = 0x5C, PWM2 = 0x5D, and PWM3 = 0x5E.

000 = No startup timeout

001 = 100 ms

010 = 250 ms default

011 = 400 ms

100 = 667 ms

101 = 1 s

110 = 2 s

111 = 4 s

Disabling Fan Startup Timeout

Although fan startup makes fan spin-ups much quieter than fixed-time spin-ups, the option exists to use fixed spin-up times. Setting Bit 5 (FSPDIS) to 1 in Configuration Register 1 (Reg. 0x40) disables the spin-up for two TACH pulses. Instead, the fan spins up for the fixed time as selected in Reg. 0x5C to Reg. 0x5E.

PWM Logic State

The PWM outputs can be programmed high for 100% duty cycle (noninverted) or low for 100% duty cycle (inverted).

PWM1 Configuration (Reg. 0x5C)

<4> INV.
0 = Logic high for 100% PWM duty cycle.
1 = Logic low for 100% PWM duty cycle.

PWM2 Configuration (Reg. 0x5D)

<4> INV.
0 = Logic high for 100% PWM duty cycle.
1 = Logic low for 100% PWM duty cycle.

PWM3 Configuration (Reg. 0x5E)

<4> INV.
0 = Logic high for 100% PWM duty cycle.
1 = Logic low for 100% PWM duty cycle.

Low Frequency Mode PWM Drive Frequency

The PWM drive frequency can be adjusted for the application. Register 0x5F to Register 0x61 configure the PWM frequency for PWM1 to PWM3, respectively.

PWM1, PWM 2, PWM3 Frequency Registers (Reg. 0x5F to Reg. 0x61)

<2:0> FREQ

000 = 11.0 Hz

001 = 14.7 Hz

010 = 22.1 Hz

011 = 29.4 Hz

100 = 35.3 Hz default

101 = 44.1 Hz

110 = 58.8 Hz

111 = 88.2 Hz

High Frequency Mode PWM Drive

Setting Bit 3 of Registers 0x5F, 0x60, 0x61 enables high frequency mode for Fan1, Fan 2, and Fan 3 respectively.

In high frequency mode, the PWM drive frequency is always 22.5 kHz. When high frequency mode is enabled, the DC bits are asserted internally automatically and do not need to be changed.

Fan Speed Control

The ADT7476 controls fan speed using automatic and manual modes:

In automatic fan speed control mode, fan speed is automatically varied with temperature and without CPU intervention, once initial parameters are set up. The advantage is that, if the system hangs, the user is guaranteed that the system is protected from overheating.

In manual fan speed control mode, the ADT7476 allows the duty cycle of any PWM output to be manually adjusted. This can be useful, if the user wants to change fan speed in software or adjust PWM duty cycle output for test purposes. Bits <7:5> of Reg. 0x5C to Reg. 0x5E (PWM Configuration) control the behavior of each PWM output.

PWM Configuration Registers (Reg. 0x5C to Reg. 0x5E)

<7:5> BHVR.

111 = manual mode

Once under manual control, each PWM output can be manually updated by writing to Reg. 0x30 to Reg. 0x32 (PWMx current duty cycle registers).

Programming the PWM Current Duty Cycle Registers

The PWM current duty cycle registers are 8-bit registers that allow the PWM duty cycle for each output to be set anywhere from 0% to 100% in steps of 0.39%. The value to be programmed into the PWM_{MIN} register is given by

Value (decimal) = PWM_{MIN}/0.39

Example 1: For a PWM duty cycle of 50%,

Value (decimal) = 50/0.39 = 128 (decimal)
Value = 128 (decimal) or 0x80 (hex)

Example 2: For a PWM duty cycle of 33%,

Value (decimal) = 33/0.39 = 85 (decimal)
Value = 85 (decimal) or 0x54 (hex)

PWM Duty Cycle Registers

Reg. 0x30 **PWM1 Duty Cycle** = 0xFF (100% default)

Reg. 0x31 **PWM2 Duty Cycle** = 0xFF (100% default)

Reg. 0x32 **PWM3 Duty Cycle** = 0xFF (100% default)

By reading the PWMx current duty cycle registers, the user can keep track of the current duty cycle on each PWM output, even when the fans are running in automatic fan speed control mode or acoustic enhancement mode.

PROGRAMMING TRANGE

T_{RANGE} defines the distance between T_{MIN} and 100% PWM. For the ADT7467, ADT7468 and ADT7473, T_{RANGE} is effectively a slope. For the ADT7475 andADT7476, T_{RANGE} is no longer a slope but defines the temperature region where the PWM output linearly ramps from PWM_{MIN} to 100% PWM.

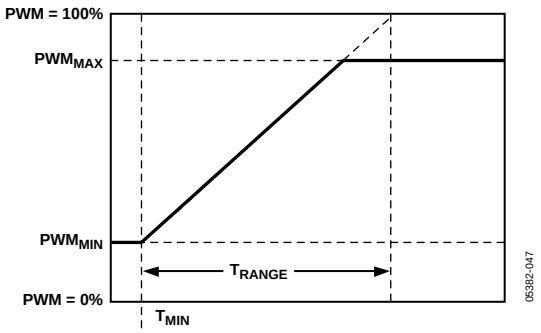


Figure 46. T_{RANGE}

PROGRAMMING THE AUTOMATIC FAN SPEED CONTROL LOOP

To more efficiently understand the automatic fan speed control loop, it is recommended using the ADT7476 evaluation board and software while reading this section.

This section provides the system designer with an understanding of the automatic fan control loop, and provides step-by-step guidance on effectively evaluating and selecting critical system parameters. To optimize the system characteristics, the designer needs to give some thought to system configuration, including the number of fans, where they are located, and what temperatures are being measured in the particular system.

The mechanical or thermal engineer who is tasked with the system thermal characterization should also be involved at the beginning of the system development process.

MANUAL FAN CONTROL OVERVIEW

In unusual circumstances, it can be necessary to manually control the speed of the fans. As the ADT7476 has an SMBus interface, a system can read back all necessary voltage, fan speed and temperature information, and use this information to control the speed of the fans by writing to the current PWM duty cycle register (0x30, 0x31, and 0x32) of the appropriate fan. Bits <7:5> of the PWMX configuration registers (0x5C, 0x5D, 0x5E) are used to set fans up for manual control.

THERM OPERATION IN MANUAL MODE

In manual mode, if the temperature increases above the programmed $\overline{\text{THERM}}$ temperature limit, the fans automatically speed up to Maximum PWM or100% PWM, whichever way the appropriate fan channel is configured.

AUTOMATIC FAN CONTROL OVERVIEW

The ADT7476 can automatically control the speed of fans based on the measured temperature. This is done independently of CPU intervention once initial parameters are set up.

The ADT7476 has a local temperature sensor and two remote temperature channels that can be connected to a CPU on-chip thermal diode (available on Intel Pentium class and other CPUs). These three temperature channels can be used as the basis for automatic fan speed control to drive fans using pulse-width modulation (PWM).

Automatic fan speed control reduces acoustic noise by optimizing fan speed according to accurately measured temperature. Reducing fan speed can also decrease system current consumption. The automatic fan speed control mode is very flexible owing to the number of programmable parameters, including T_{MIN} and T_{RANGE}. The T_{MIN} and T_{RANGE} values for a temperature channel and, therefore, for a given fan are critical, because they define the thermal characteristics of the system. The thermal validation of the system is one of the most important steps in the design process, so these values should be selected carefully.

Figure 47 gives a top-level overview of the automatic fan control circuitry on the ADT7476. From a systems-level perspective, up to three system temperatures can be monitored and used to control three PWM outputs. The three PWM outputs can be used to control up to four fans. The ADT7476 allows the speed of four fans to be monitored. Each temperature channel has a thermal calibration block, allowing the designer to individually configure the thermal characteristics of each temperature channel. For example, one can decide to run the CPU fan when CPU temperature increases above 60°C and a chassis fan when the local temperature increases above 45°C.

At this stage, the designer has not assigned these thermal calibration settings to a particular fan drive (PWM) channel. The right side of Figure 47 shows controls that are fan-specific. The designer has individual control over parameters such as minimum PWM duty cycle, fan speed failure thresholds, and even ramp control of the PWM outputs. Automatic fan control, then, ultimately allows graceful fan speed changes that are less perceptible to the system user.

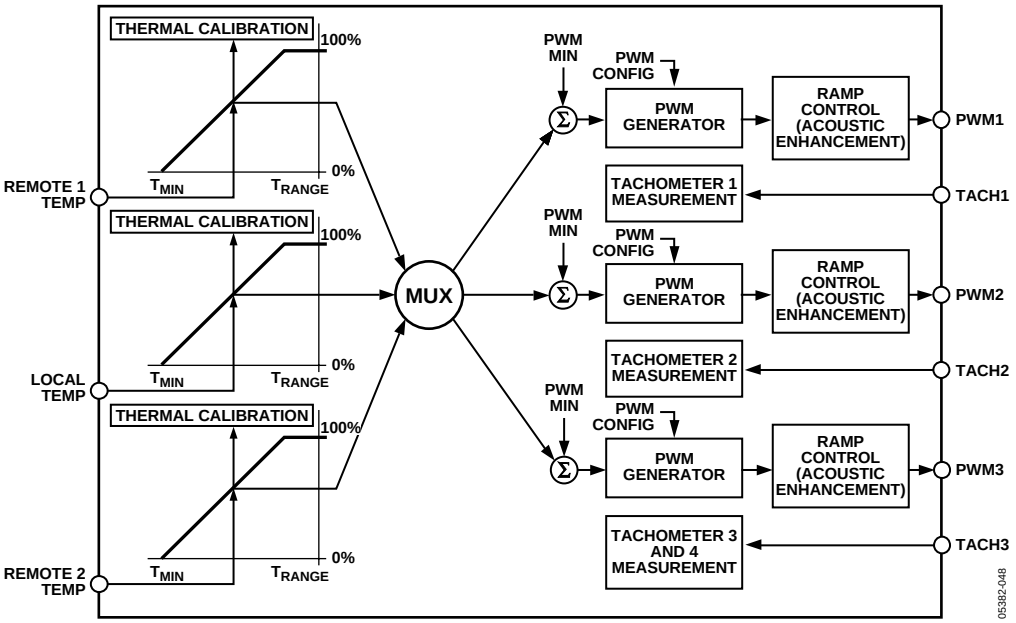


Figure 47. Automatic Fan Control Block Diagram

STEP 1: HARDWARE CONFIGURATION

During system design, the motherboard sensing and control capabilities should be addressed early in the design stages. Decisions about how these capabilities are used should involve the system thermal/mechanical engineer. Ask the following questions:

1. What ADT7476 functionality is used?
   - PWM2 or $\overline{\text{SMBALERT}}$?
   - $\overline{\text{TACH4}}$ fan speed measurement or overtemperature $\overline{\text{THERM}}$ function?
   - 2.5 V voltage monitoring or overtemperature $\overline{\text{THERM}}$ function?
   - 12 V voltage monitoring or VID5 input?

   The ADT7476 offers multifunctional pins that can be reconfigured to suit different system requirements and physical layouts. These multifunction pins are software programmable.

2. How many fans are supported in system, three or four? This influences the choice of whether to use the $\overline{\text{TACH4}}$ pin or to reconfigure it for the $\overline{\text{THERM}}$ function.

3. Is the CPU fan to be controlled using the ADT7476, or will the CPU fan run at full speed 100% of the time?

   If run at 100%, this frees up a PWM output, but the system is louder.

4. Where will the ADT7476 be physically located in the system?

   This influences the assignment of the temperature measurement channels to particular system thermal zones. For example, locating the ADT7476 close to the VRM controller circuitry allows the VRM temperature to be monitored using the local temperature channel.

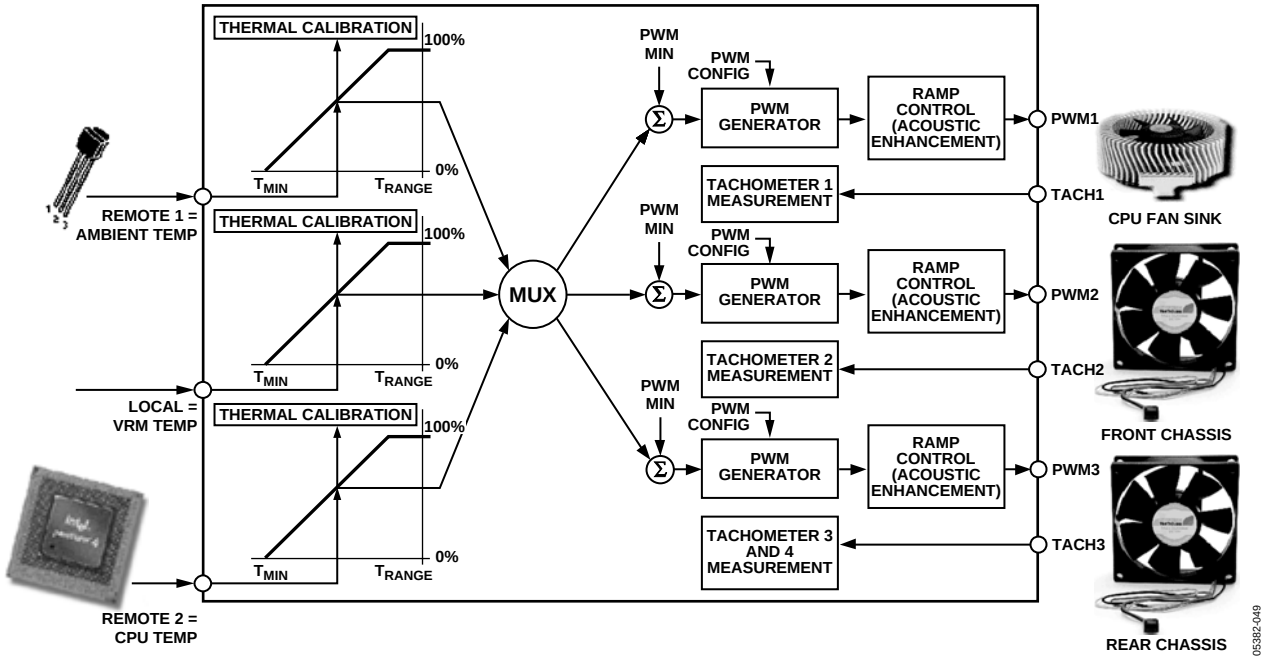


Figure 48. Hardware Configuration Example

Recommended Implementation 1

Configuring the ADT7476 as in Figure 49 provides the system designer with the following features:

- Six VID inputs (VID0 to VID5) for VRM10 support.
- Two PWM outputs for fan control of up to three fans. The front and rear chassis fans are connected in parallel.
- Three TACH fan speed measurement inputs.
- V_{CC} measured internally through Pin 4.
- CPU core voltage measurement (V_{CORE}).
- 2.5 V measurement input used to monitor CPU current (connected to V_{COMP} output of ADP316x VRM controller). This is used to determine CPU power consumption.
- 5 V measurement input.
- VRM temperature using local temperature sensor.
- CPU temperature measured using the Remote 1 temperature channel.
- Ambient temperature measured through the Remote 2 temperature channel.
- If not using VID5, it can be reconfigured as the 12 V monitoring input.
- Bidirectional $\overline{\text{THERM}}$ pin allows the monitoring of $\overline{\text{PROCHOT}}$ output from an Intel® P4 processor, for example, or can be used as an overtemperature $\overline{\text{THERM}}$ output.
- $\overline{\text{SMBALERT}}$ system interrupt output.

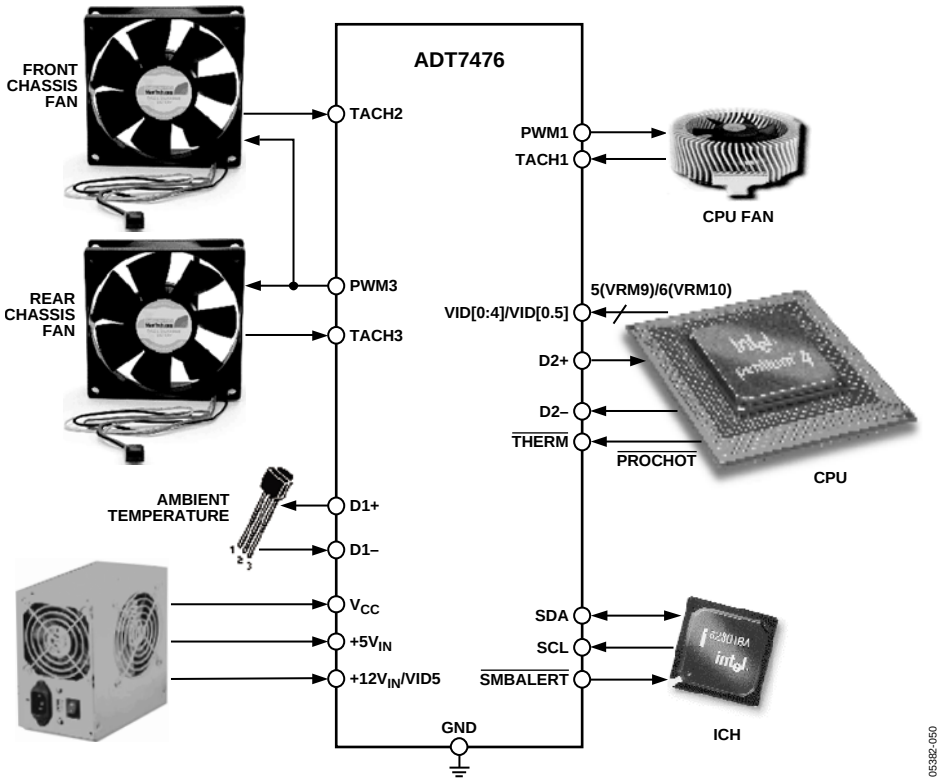


Figure 49. Recommended Implementation 1

Recommended Implementation 2

Configuring the ADT7476 as in Figure 50 provides the system designer with the following features:

- Six VID inputs (VID0 to VID5) for VRM10 support.
- Three PWM outputs for fan control of up to three fans. All three fans can be individually controlled.
- Three TACH fan speed measurement inputs.
- V_{CC} measured internally through Pin 4.
- CPU core voltage measurement (V_{CORE}).
- 2.5 V measurement input used to monitor CPU current (connected to V_{COMP} output of ADP316x VRM controller). This is used to determine CPU power consumption.
- 5 V measurement input.
- VRM temperature using local temperature sensor.
- CPU temperature measured using the Remote 1 temperature channel.
- Ambient temperature measured through the Remote 2 temperature channel.
- If not using VID5, it can be reconfigured as the 12 V monitoring input.
- Bidirectional $\overline{\text{THERM}}$ pin allows the monitoring of $\overline{\text{PROCHOT}}$ output/input from an Intel P4 processor, for example, or can be used as an overtemperature $\overline{\text{THERM}}$ output.

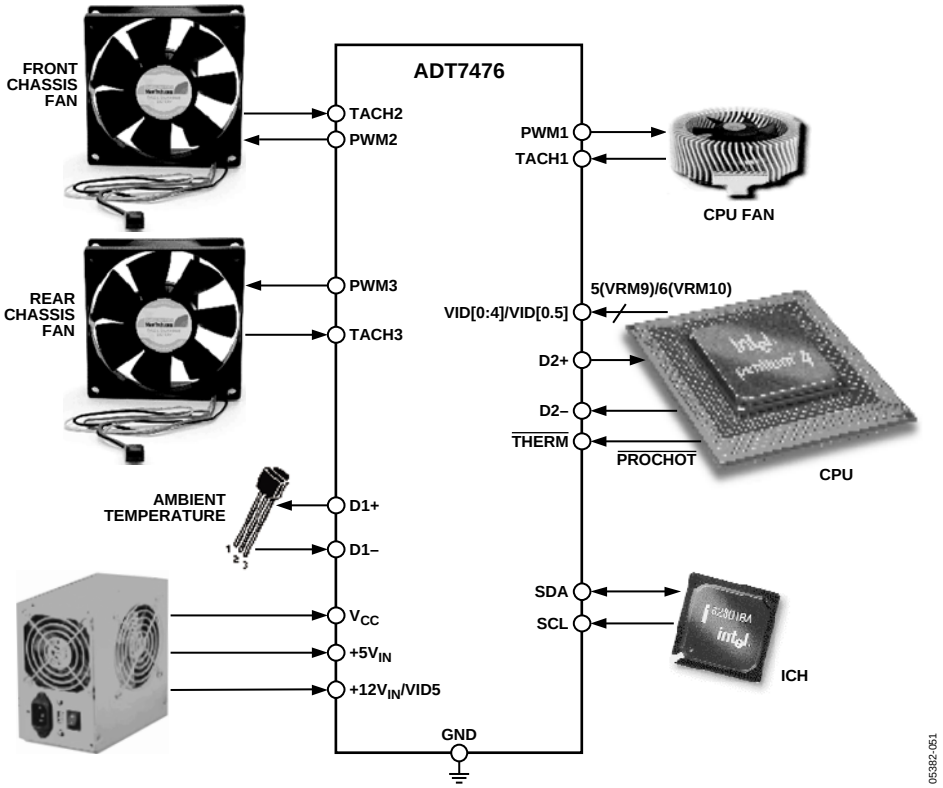


Figure 50. Recommended Implementation 2

STEP 2: CONFIGURING THE MUX

After the system hardware configuration is determined, the fans can be assigned to particular temperature channels. Not only can fans be assigned to individual channels, but the behavior of the fans is also configurable. For example, fans can be run under automatic fan control, can be run manually (under software control), or can be run at the fastest speed calculated by multiple temperature channels. The mux is the bridge between temperature measurement channels and the three PWM outputs.

Bits <7:5> (BHVR) of Registers 0x5C, 0x5D, and 0x5E (PWM configuration registers) control the behavior of the fans connected to the PWM1, PWM2, and PWM3 outputs. The values selected for these bits determine how the mux connects a temperature measurement channel to a PWM output.

Automatic Fan Control Mux Options

<7:5> (BHVR), Registers 0x5C, 0x5D, 0x5E.

000 = Remote 1 temperature controls PWMx

001 = local temperature controls PWMx

010 = Remote 2 temperature controls PWMx

101 = Fastest speed calculated by local and Remote 2 temperature controls PWMx

110 = Fastest speed calculated by all three temperature channels controls PWMx

The Fastest Speed Calculated options pertain to controlling one PWM output based on multiple temperature channels. The thermal characteristics of the three temperature zones can be set to drive a single fan. An example would be the fan turning on when Remote 1 temperature exceeds 60°C or if the local temperature exceeds 45°C.

Other Mux Options

<7:5> (BHVR), Registers 0x5C, 0x5D, 0x5E.

011 = PWMx runs full speed

100 = PWMx disabled (default)

111 = manual mode. PWMx is running under software control. In this mode, PWM duty cycle registers (Registers 0x30 to 0x32) are writable and control the PWM outputs.

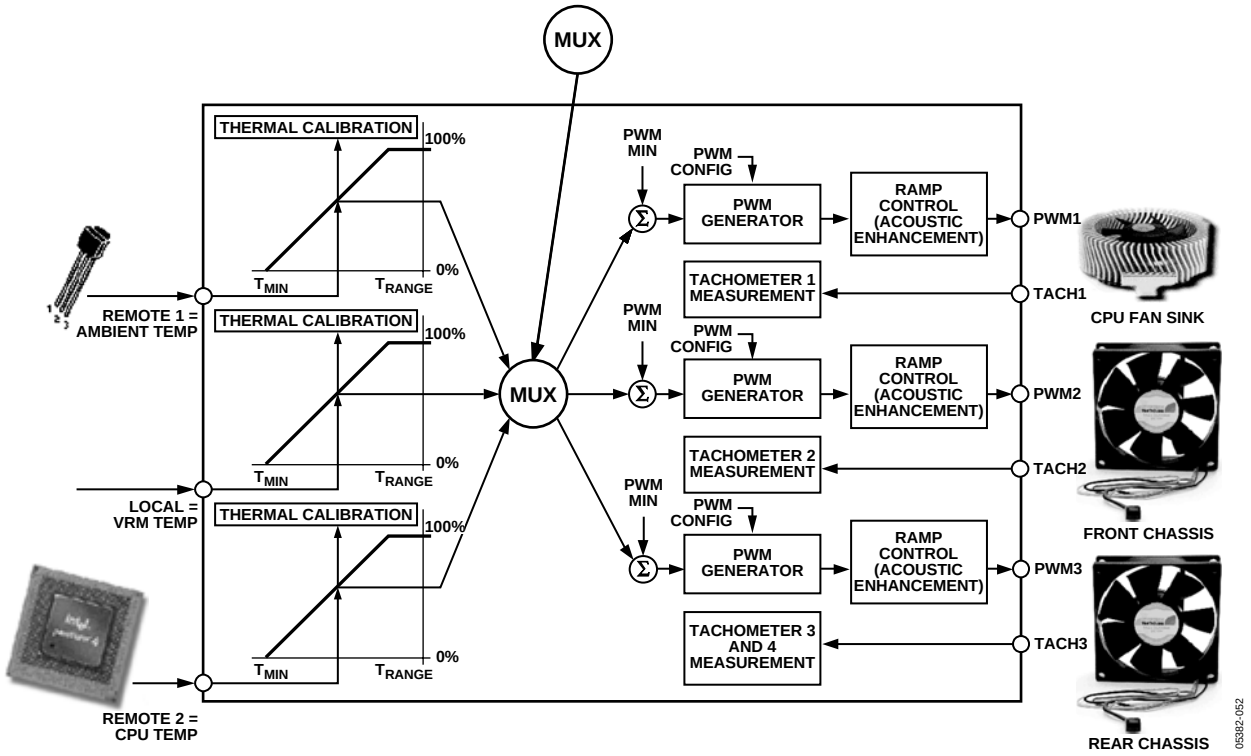


Figure 51. Assigning Temperature Channels to Fan Channels

Mux Configuration Example

This is an example of how to configure the mux in a system using the ADT7476 to control three fans. The CPU fan sink is controlled by PWM1, the front chassis fan is controlled by PWM2, and the rear chassis fan is controlled by PWM3. The mux is configured for the following fan control behavior:

- PWM1 (CPU fan sink) is controlled by the fastest speed calculated by the local (VRM temperature) and Remote 2 (processor) temperature. In this case, the CPU fan sink is also being used to cool the VRM.
- PWM2 (front chassis fan) is controlled by the Remote 1 temperature (ambient).
- PWM3 (rear chassis fan) is controlled by the Remote 1 temperature (ambient).

Example Mux Settings

<7:5> (BHVR), PWM1 Configuration Register 0x5C.

101 = Fastest speed calculated by local and Remote 2 temperature controls PWM1

<7:5> (BHVR), PWM2 Configuration Register 0x5D.

000 = Remote 1 temperature controls PWM2

<7:5> (BHVR), PWM3 Configuration Register 0x5E.

000 = Remote 1 temperature controls PWM3

These settings configure the mux, as shown in Figure 52.

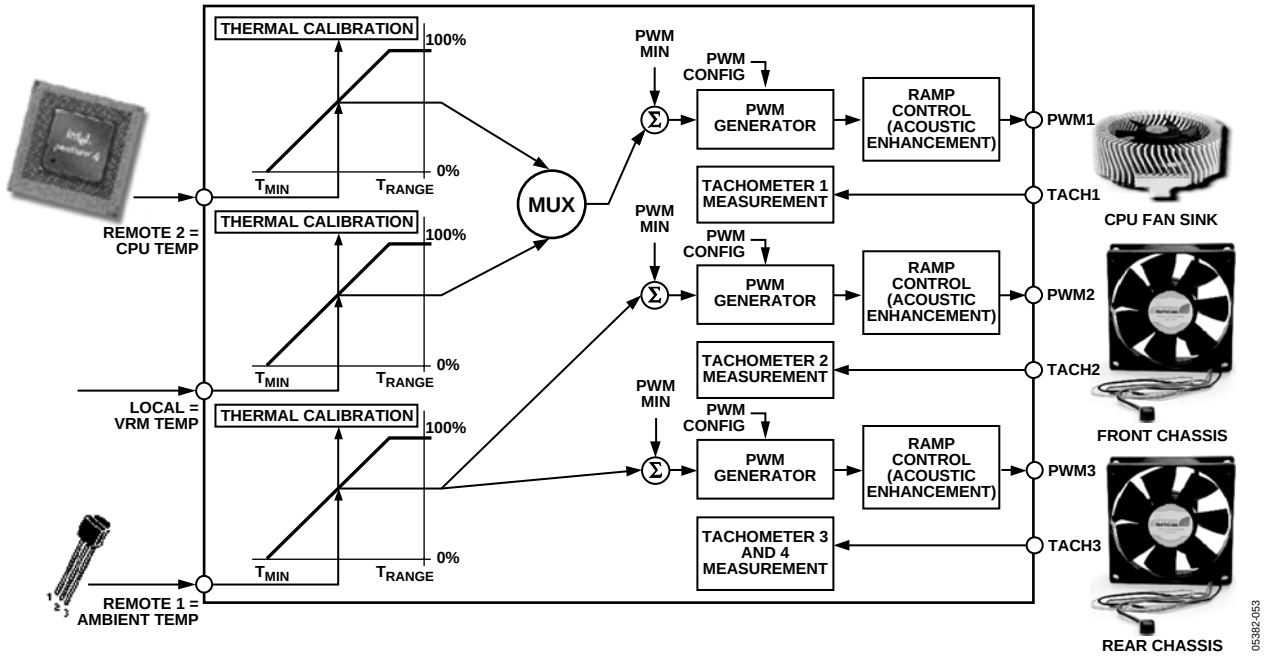


Figure 52. MUX Configuration Example

STEP 3: T_{MIN} SETTINGS FOR THERMAL CALIBRATION CHANNELS

T_{MIN} is the temperature at which the fans start to turn on under automatic fan control. The speed at which the fan runs at T_{MIN} is programmed later. The T_{MIN} values chosen are temperature channel specific, for example, 25°C for ambient channel, 30°C for VRM temperature, and 40°C for processor temperature.

T_{MIN} is an 8-bit value, either twos complement or Offset 64, that can be programmed in 1°C increments. A T_{MIN} register is associated with each temperature measurement channel: Remote 1 local, and Remote 2 Temperature. Once the T_{MIN} value is exceeded, the fan turns on and runs at the minimum PWM duty cycle. The fan turns off once the temperature has dropped below $T_{MIN} - T_{HYST}$.

To overcome fan inertia, the fan is spun up until two valid TACH rising edges are counted. See the Fan Startup Timeout section for more details. In some cases, primarily for psycho-acoustic reasons, it is desirable that the fan never switch off below T_{MIN}. Bits <7:5> of Enhanced Acoustics Register 1 (Reg. 0x62), when set, keep the fans running at the PWM minimum duty cycle, if the temperature should fall below T_{MIN}.

T_{MIN} Registers

Reg. 0x67, **Remote 1 Temperature T_{MIN}** = 0x5A (90°C)

Reg. 0x68, **Local Temperature T_{MIN}** = 0x5A (90°C)

Reg. 0x69, **Remote 2 Temperature T_{MIN}** = 0x5A (90°C)

Enhance Acoustics Register 1 (Reg. 0x62)

Bit 7 (MIN3) = 0, PWM3 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 7 (MIN3) = 1, PWM3 runs at PWM3 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 0, PWM2 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 1, PWM2 runs at PWM2 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 0, PWM1 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 1, PWM1 runs at PWM1 minimum duty cycle below $T_{MIN} - T_{HYST}$.

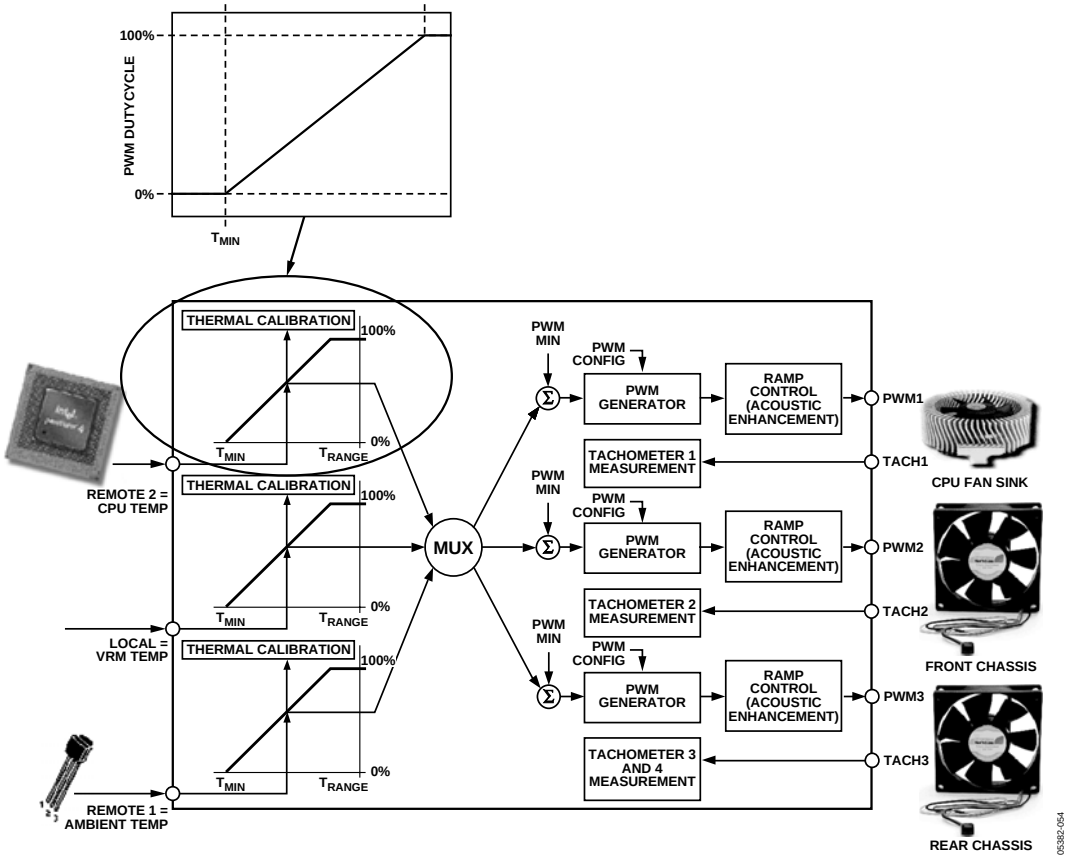


Figure 53. Understanding the T_{MIN} Parameter

STEP 4: PWM_{MIN} FOR EACH PWM (FAN) OUTPUT

PWM_{MIN} is the minimum PWM duty cycle at which each fan in the system runs. It is also the start speed for each fan under automatic fan control once the temperature rises above T_{MIN}. For maximum system acoustic benefit, PWM_{MIN} should be as low as possible. Depending on the fan used, the PWM_{MIN} setting is usually in the 20% to 33% duty cycle range. This value can be found through fan validation.

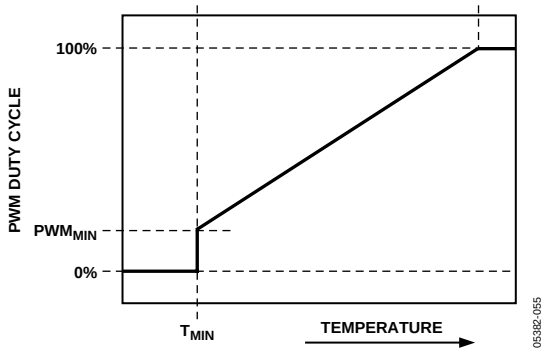


Figure 54. PWM_{MIN} Determines Minimum PWM Duty Cycle

More than one PWM output can be controlled from a single temperature measurement channel. For example, Remote 1 Temperature can control PWM1 and PWM2 outputs. If two different fans are used on PWM1 and PWM2, the fan characteristics can be set up differently. As a result, Fan 1 driven by PWM1 can have a different PWM_{MIN} value than that of Fan 2 connected to PWM2. Figure 55 illustrates this as $PWM1_{MIN}$ (front fan) is turned on at a minimum duty cycle of 20%, while $PWM2_{MIN}$ (rear fan) turns on at a minimum of 40% duty cycle. Note: Both fans turn on at exactly the same temperature, defined by T_{MIN}.

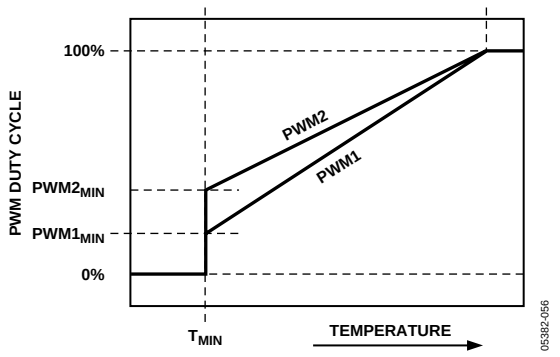


Figure 55. Operating Two Different Fans from a Single Temperature Channel

Programming the PWM_{MIN} Registers

The PWM_{MIN} registers are 8-bit registers that allow the minimum PWM duty cycle for each output to be configured anywhere from 0% to 100%. This allows the minimum PWM duty cycle to be set in steps of 0.39%.

The value to be programmed into the PWM_{MIN} register is given by

Value (decimal) = PWM_{MIN}/0.39

Example 1: For a minimum PWM duty cycle of 50%,

Value (decimal) = 50/0.39 = 128 (decimal)
Value = 128 (decimal) or 80 (hex)

Example 2: For a minimum PWM duty cycle of 33%,

Value (decimal) = 33/0.39 = 85 (decimal)
Value = 85 (decimal)l or 54 (hex)

PWM_{MIN} Registers

Reg. 0x64, **PWM1 Minimum Duty Cycle** = 0x80 (50% default)

Reg. 0x65 **PWM2 Minimum Duty Cycle** = 0x80 (50% default)

Reg. 0x66, **PWM3 Minimum Duty Cycle** = 0x80 (50% default)

Note on Fan Speed and PWM Duty Cycle

The PWM duty cycle does not directly correlate to fan speed in RPM. Running a fan at 33% PWM duty cycle does not equate to running the fan at 33% speed. Driving a fan at 33% PWM duty cycle actually runs the fan at closer to 50% of its full speed. This is because fan speed in %RPM generally relates to the square root of PWM duty cycle. Given a PWM square wave as the drive signal, fan speed in RPM approximates to

$$\%\, fanspeed = \sqrt{PWM\ Duty\ Cycle \times 10}$$

STEP 5: PWM_{MAX} FOR PWM (FAN) OUTPUTS

PWM_{MAX} is the maximum duty cycle that each fan in the system runs at under the automatic fan speed control loop. For maximum system acoustic benefit, PWM_{MAX} should be as low as possible, but should be capable of maintaining the processor temperature limit at an acceptable level. If the $\overline{\text{THERM}}$ temperature limit is exceeded, the fans are still boosted to 100% for fail-safe cooling.

There is a PWM_{MAX} limit for each fan channel. The default value of this register is 0xFF and has no effect unless it is programmed.

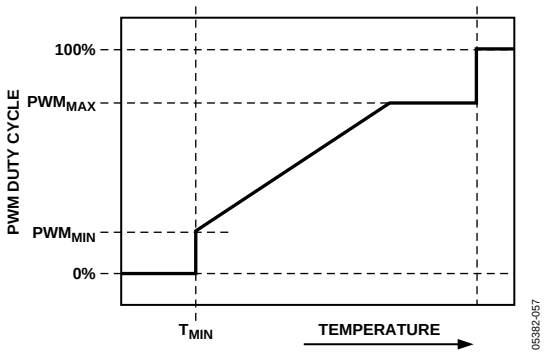


Figure 56. PWM_{MAX} Determines Maximum PWM Duty Cycle below the $\overline{\text{THERM}}$ Temperature Limit

Programming the PWM_{MAX} Registers

The PWM_{MAX} registers are 8-bit registers that allow the maximum PWM duty cycle for each output to be configured anywhere from 0% to 100%. This allows the maximum PWM duty cycle to be set in steps of 0.39%.

The value to be programmed into the PWM_{MAX} register is given by

Value (decimal) = PWM_{MAX}/0.39

Example 1: For a maximum PWM duty cycle of 50%,

Value (decimal) – 50/0.39 = 128 (decimal)
Value = 128 (decimal) or 80 (hex)

Example 2: For a minimum PWM duty cycle of 75%,

Value (decimal) = 75/0.39 = 85 (decimal)

Value = 192 (decimal) or C0 (hex)

PWM_{MAX} Registers

Reg. 0x38, **PWM1 Maximum Duty Cycle** = 0xFF (100% default)

Reg. 0x39, **PWM2 Maximum Duty Cycle** = 0xFF (100% default)

Reg. 0x3A, **PWM3 Maximum Duty Cycle** = 0xFF (100% default)

STEP 6: T_{RANGE} FOR TEMPERATURE CHANNELS

T_{RANGE} is the range of temperature over which automatic fan control occurs once the programmed T_{MIN} temperature has been exceeded. T_{RANGE} is the temperature range between PWM_{MIN} and 100% PWM where the fan speed changes linearly. Otherwise stated, it is the line drawn between the T_{MIN}/PWM_{MIN} and the (T_{MIN} + T_{RANGE})/PWM100% intersection points.

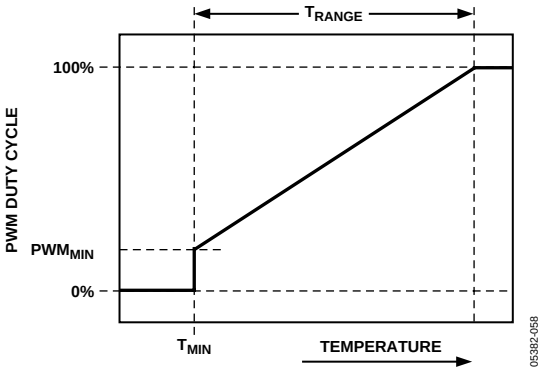


Figure 57. T_{RANGE} Parameter Affects Cooling Slope

The T_{RANGE} is determined by the following procedure:

1. Determine the maximum operating temperature for that channel (for example, 70°C).
2. Determine experimentally the fan speed (PWM duty cycle value) that does not exceed the temperature at the worst-case operating points. For example, 70°C is reached when the fans are running at 50% PWM duty cycle.
3. Determine the slope of the required control loop to meet these requirements.
4. Using the ADT7476 evaluation software, you can graphically program and visualize this functionality. Ask your local Analog Devices representative for details.

As PWM_{MIN} is changed, the automatic fan control slope changes.

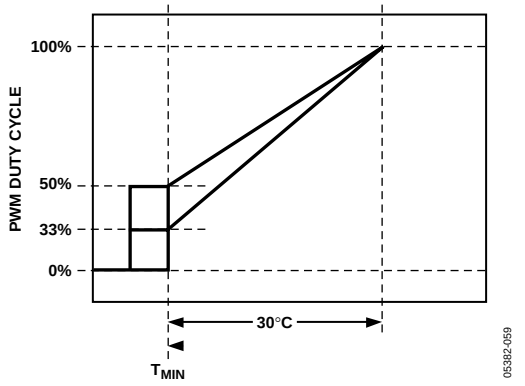


Figure 58. Adjusting PWM_{MIN} Changes the Automatic Fan Control Slope.

As T_{RANGE} is changed, the slope changes. As T_{RANGE} gets smaller, the fans will reach 100% speed with a smaller temperature change.

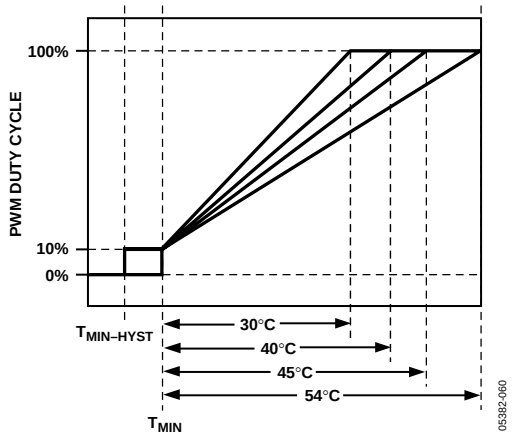


Figure 59. Increasing T_{RANGE} Changes the AFC slope

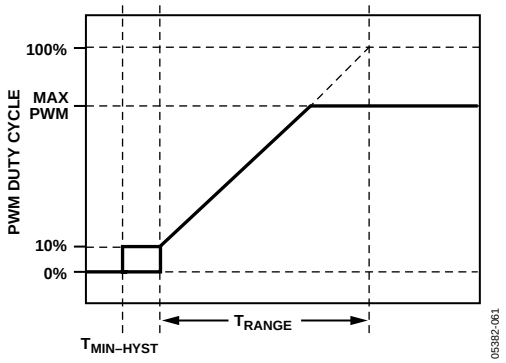


Figure 60. Changing PWM Max Does Not Change the AFC Slope

Selecting T_{RANGE}

The T_{RANGE} value can be selected for each temperature channel: Remote 1, local, and Remote 2 temperature. Bits <7:4> (T_{RANGE}) of Registers 0x5F to 0x61 define the T_{RANGE} value for each temperature channel.

Table 16. Selecting a T_{RANGE} Value

Bits <7:4>[1]	T_{RANGE} (°C)
0000	2
0001	2.5
0010	3.33
0011	4
0100	5
0101	6.67
0110	8
0111	10
1000	13.33
1001	16
1010	20
1011	26.67
1100	32 (default)
1101	40
1110	53.33
1111	80

[1] Register 0x5F configures Remote 1 T_{RANGE}; Register 0x60 configures local T_{RANGE}; Register 0x61 configures Remote 2 T_{RANGE}.

Actual Changes in PWM Output (Advanced Acoustics Settings)

While the automatic fan control algorithm describes the general response of the PWM output, it is also necessary to note the enhanced acoustics registers (0x62 and 0x63) can be used to set/clamp the maximum rate of change of PWM output for a given temperature zone. This means that if T_{RANGE} is programmed with an AFC slope that is quite steep, a relatively small change in temperature could cause a large change in PWM output and possibly an audible change in fan speed, which can be noticeable/annoying to end users.

Decreasing the speed the PWM output changes, by programming the smoothing on the appropriate temperature channels (Register 0x62 and Register 0x63), will change how fast the fan speed increases/decreases in the event of a temperature spike Slowly the PWM duty cycle increases until the PWM duty cycle reaches the appropriate duty cycle as defined by the AFC curve.

Figure 61 shows PWM duty cycle vs. temperature for each T_{RANGE} setting. The lower graph shows how each T_{RANGE} setting affects fan speed vs. temperature. As can be seen from the graph, the effect on fan speed is nonlinear.

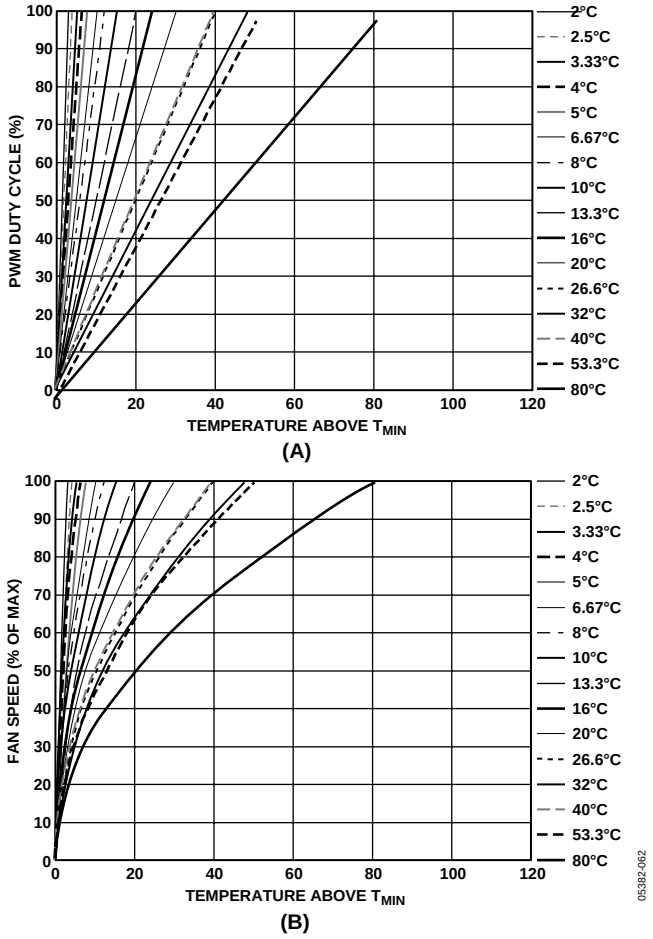


Figure 61. T_{RANGE} vs. Actual Fan Speed (Not PWM Drive) Profile

The graphs in Figure 61 assume the fan starts from 0% PWM duty cycle. Clearly, the minimum PWM duty cycle, PWM_{MIN}, needs to be factored in to see how the loop actually performs in the system. Figure 62 shows how T_{RANGE} is affected when the PWM_{MIN} value is set to 20%. It can be seen that the fan actually runs at about 45% fan speed when the temperature exceeds T_{MIN}.

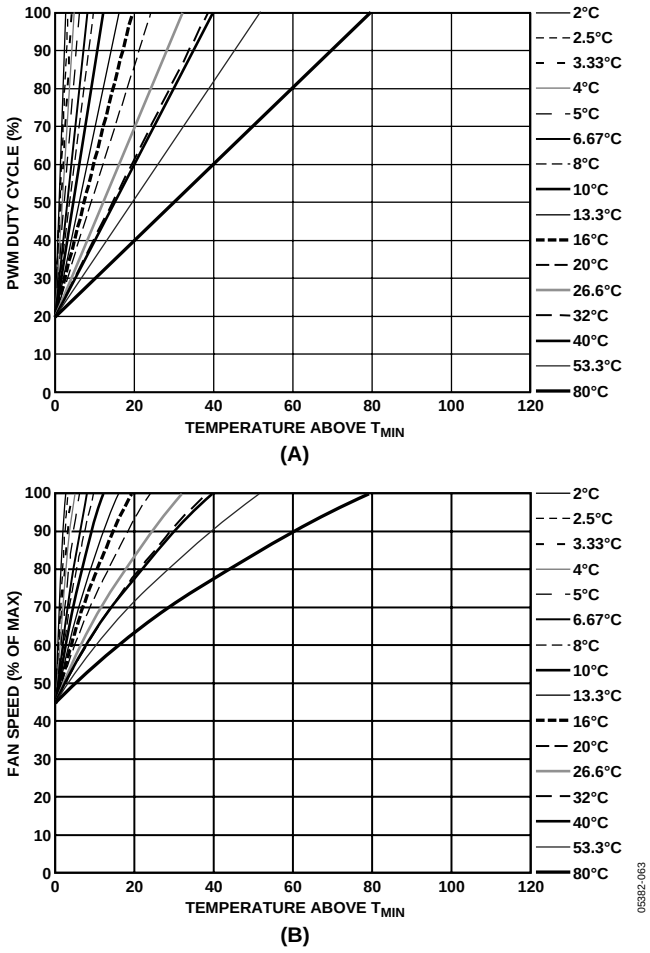


Figure 62. T_{RANGE} and % Fan Speed Slopes with PWM_{MIN} = 20%

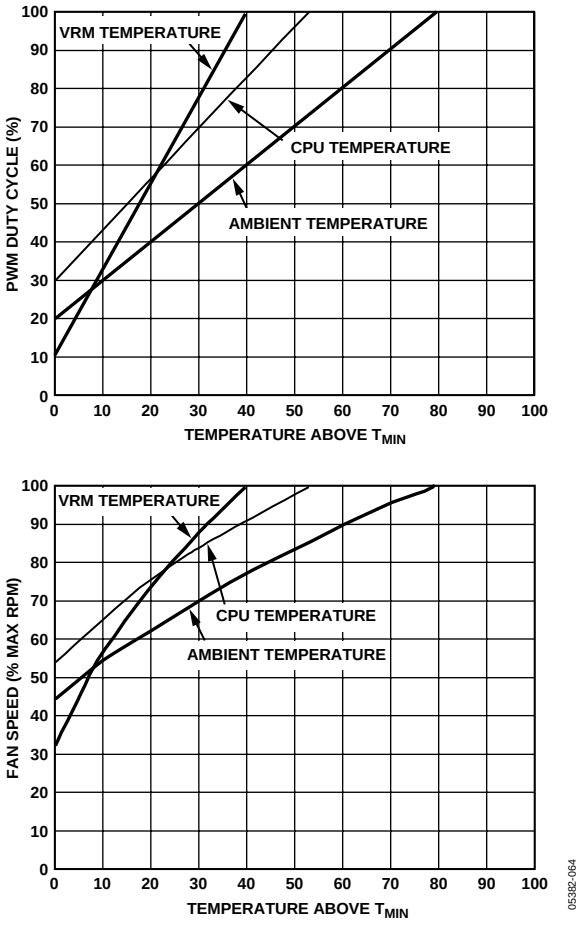


Figure 63. T_{RANGE} and % Fan Speed Slopes for VRM, Ambient, and CPU Temperature Channels

Example: Determining T_{RANGE} for Each Temperature Channel

The following example shows how the different T_{MIN} and T_{RANGE} settings can be applied to three different thermal zones. In this example, the following T_{RANGE} values apply:

T_{RANGE} = 80°C for ambient temperature
T_{RANGE} = 53.33°C for CPU temperature
T_{RANGE} = 40°C for VRM temperature

This example uses the MUX configuration described in Step 2, with the ADT7476 connected as shown in Figure 52. Both CPU temperature and VRM temperature drive the CPU fan connected to PWM1. Ambient temperature drives the front chassis fan and rear chassis fan connected to PWM2 and PWM3. The front chassis fan is configured to run at PWM_{MIN} = 20%. The rear chassis fan is configured to run at PWM_{MIN} = 30%. The CPU fan is configured to run at PWM_{MIN} = 10%.

Note: The control range for 4-wire fans is much wider than that of 3-wire fans. In many cases, 4-wire fans can start with a PWM drive of as little as 20% or less. In extreme cases, some 3-wire fans can not run unless a PWM drive of 60% or more is applied.

STEP 7: $T_{\overline{THERM}}$ FOR TEMPERATURE CHANNELS

$T_{\overline{THERM}}$ is the absolute maximum temperature allowed on a temperature channel. Above this temperature, a component such as the CPU or VRM might be operating beyond its safe operating limit. When the temperature measured exceeds $T_{\overline{THERM}}$, all fans are driven at 100% PWM duty cycle (full speed) to provide critical system cooling.

The fans remain running at 100% until the temperature drops below $T_{\overline{THERM}}$ minus hysteresis, where hysteresis is the number programmed into the hysteresis registers (0x6D and 0x6E). The default hysteresis value is 4°C.

The $T_{\overline{THERM}}$ limit should be considered the maximum worst-case operating temperature of the system. Because exceeding any $T_{\overline{THERM}}$ limit runs all fans at 100%, it has very negative acoustic effects. Ultimately, this limit should be set up as a fail-safe, and one should ensure that it is not exceeded under normal system operating conditions.

Note: $T_{\overline{THERM}}$ limits are nonmaskable and affect the fan speed no matter how automatic fan control settings are configured. This allows some flexibility, because a T_{RANGE} value can be selected based on its slope, while a hard limit (such as 70°C), can be programmed as T_{MAX} (the temperature at which the fan reaches full speed) by setting $T_{\overline{THERM}}$ to that limit (for example, 70°C).

$\overline{THERM}$ Registers

Reg. 0x6A, **Remote 1 $\overline{THERM}$ limit** = 0x64 (100°C default)

Reg. 0x6B, **Local $\overline{THERM}$ limit** = 0x64 (100°C default)

Reg. 0x6C, **Remote 2 $\overline{THERM}$ limit** = 0x64 (100°C default)

$\overline{THERM}$ Hysteresis

$\overline{THERM}$ hysteresis on a particular channel is configured via the hysteresis settings below (0x6D and 0x6E). For example, setting hysteresis on the Remote 1 channel also sets the hysteresis on Remote 1 $\overline{THERM}$.

Hysteresis Registers

Reg. 0x6D, **Remote 1, Local Hysteresis Register**

<7:4>, Remote 1 Temperature hysteresis (4°C default).

<3:0>, Local Temperature hysteresis (4°C default).

Reg. 0x6E**, Remote 2 Temperature Hysteresis Register**

<7:4>, Remote 2 Temperature hysteresis (4°C default).

Because each hysteresis setting is four bits, hysteresis values are programmable from 1°C to 15°C. It is not recommended that hysteresis values ever be programmed to 0°C, because this disables hysteresis. In effect, this would cause the fans to cycle (during a $\overline{THERM}$ event) between normal speed and 100% speed, or, while operating close to T_{MIN}, between normal speed and off, creating unsettling acoustic noise.

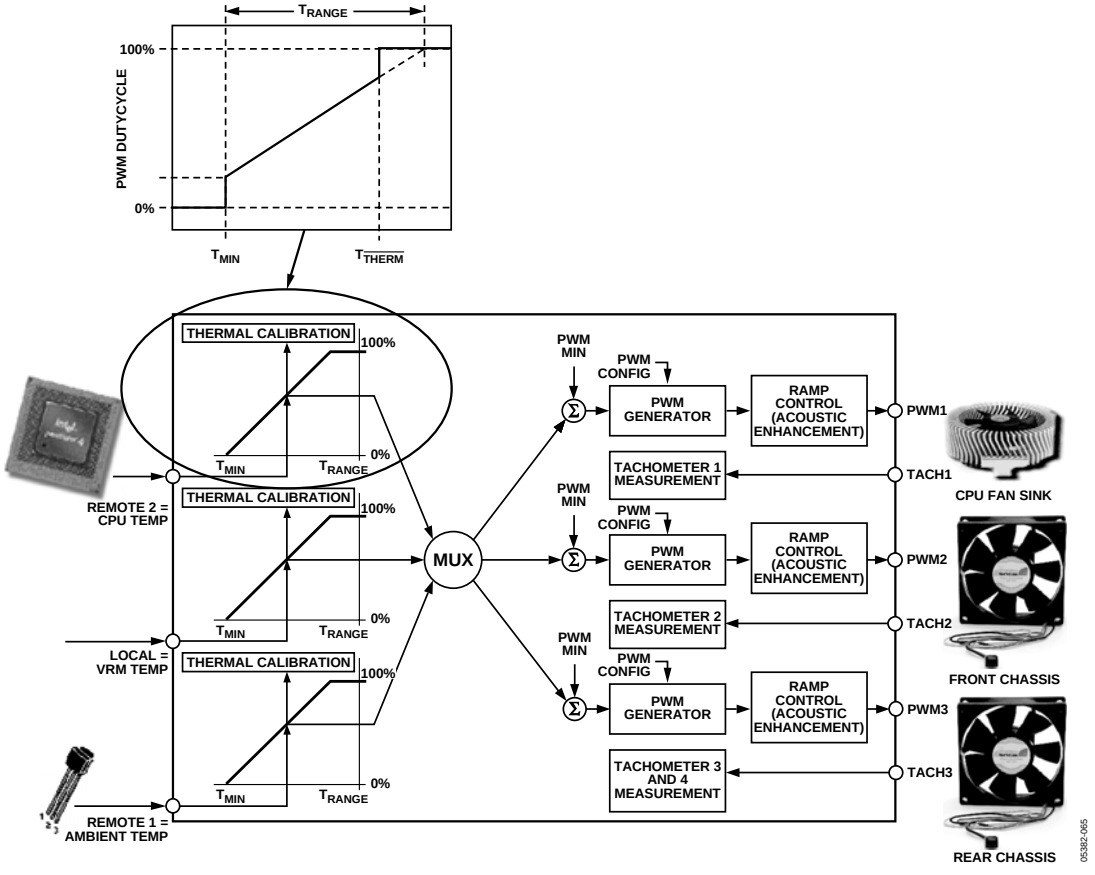


Figure 64. How $T_{\overline{THERM}}$ Relates to Automatic Fan Control

STEP 8: T_{HYST} FOR TEMPERATURE CHANNELS

T_{HYST} is the amount of extra cooling a fan provides after the temperature measured has dropped back below T_{MIN} before the fan turns off. The premise for temperature hysteresis (T_{HYST}) is that, without it, the fan would merely chatter, or cycle on and off regularly, whenever the temperature is hovering at about the T_{MIN} setting.

The T_{HYST} value chosen determines the amount of time needed for the system to cool down or heat up as the fan is turning on and off. Values of hysteresis are programmable in the range 1°C to 15°C. Larger values of T_{HYST} prevent the fans from chattering on and off. The T_{HYST} default value is set at 4°C.

The T_{HYST} setting applies not only to the temperature hysteresis for fan on/off, but the same setting is used for the $T_{\overline{THERM}}$ hysteresis value, described in Step 6. Therefore, programming Registers 0x6D and 0x6E sets the hysteresis for both fan on/off and the $\overline{THERM}$ function.

In some applications, it is required that fans not turn off below T_{MIN}, but remain running at PWM_{MIN}. Bits <7:5> of Enhanced Acoustics Register 1 (Reg. 0x62) allow the fans to be turned off or to be kept spinning below T_{MIN}. If the fans are always on, the T_{HYST} value has no effect on the fan when the temperature drops below T_{MIN}.

$\overline{THERM}$ Hysteresis

Any hysteresis programmed via Registers 0x6D and 0x6E also applies hysteresis on the appropriate $\overline{THERM}$ channel.

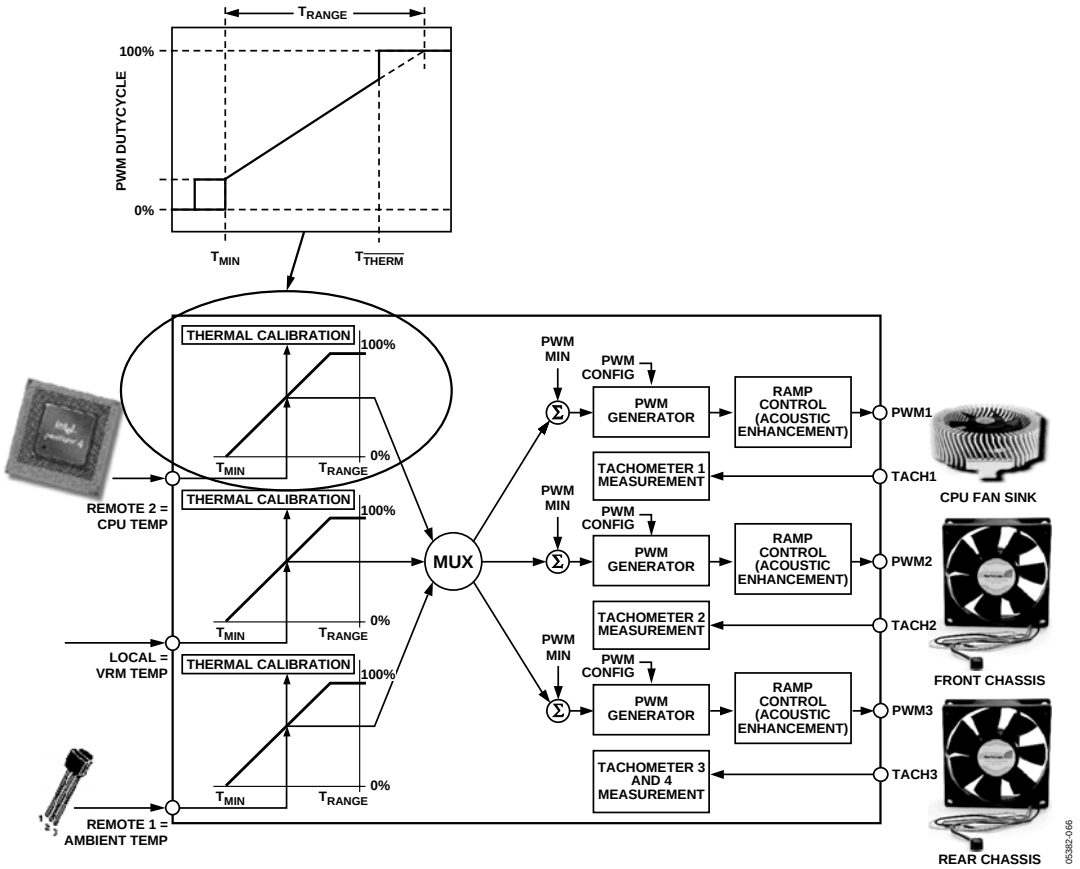


Figure 65. The T_{HYST} Value Applies to Fan On/Off Hysteresis and $\overline{THERM}$ Hysteresis

Enhance Acoustics Register 1 (Reg. 0x62)

Bit 7 (MIN3) = 0, PWM3 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 7 (MIN3) = 1, PWM3 runs at PWM3 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 0, PWM2 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 1, PWM2 runs at PWM2 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 0, PWM1 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 1, PWM1 runs at PWM1 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Configuration Register 6 (Reg. 0x10)

<0> SLOW, 1 slows the ramp rate for PWM changes associated with the Remote 1 temperature channel by 4. Configuration Register 6(Reg. 0x10)

<1> SLOW, 1 slows the ramp rate for PWM changes associated with the Local temperature channel by 4.

Configuration Register 6(Reg. 0x10)

<2> SLOW, 1 slows the ramp rate for PWM changes associated with the Remote 2 temperature channel by 4.

Configuration Register 6 (Reg. 0x10)

<7> ExtraSlow, 1 slows the ramp rate for all fans by a factor of 39.2%.

The following sections list the ramp-up times when the SLOW bit is set for each temperature monitoring channel.

Enhanced Acoustics Register 1 (Reg. 0x62)

<2:0> ACOU, selects the ramp rate for PWM outputs associated with the Remote Temperature 1 input.

000 = 37.5 sec
001 = 18.8 sec
010 = 12.5 sec
011 = 7.5 sec
100 = 4.7 sec
101 = 3.1 sec
110 = 1.6 sec
111 = 0.8 sec

Enhance Acoustics Register 2 (Reg. 0x63)

<2:0> ACOU3, selects the ramp rate for PWM outputs associated with the local temperature channel.

000 = 37.5 sec
001 = 18.8 sec
010 = 12.5 sec
011 = 7.5 sec
100 = 4.7 sec
101 = 3.1 sec
110 = 1.6 sec
111 = 0.8 sec

<6:4> ACOU2, selects the ramp rate for PWM outputs associated with the Remote Temperature 2 input.

000 = 37.5 sec
001 = 18.8 sec
010 = 12.5 sec
011 = 7.5 sec
100 = 4.7 sec
101 = 3.1 sec
110 = 1.6 sec
111 = 0.8 sec

When Bit 7 of Configuration Register 6 (0x10) =1, the above ramp rates change to the values below.

000=52.2 sec
001=26.1 sec
010=17.4 sec
011=10.4 sec
100=6.5 sec
101=4.4 sec
110=2.2 sec
111=1.1 sec

Setting the appropriate slow bit <2:0> of Configuration Register 6 (0x10) slows the ramp rate further by a factor of 4.

FAN PRESENCE DETECT

This feature is used to determine if a 4-wire fan is directly connected to a PWM output. This feature does not work for 3-wire fans. To detect whether a 4-wire fan is connected directly to a PWM output, the following must be performed in this order:

1. Drive the appropriate PWM outputs to 100% duty cycle.
2. Set Bit 0 of Configuration Register 2 (0x73) .
3. Wait 5 ms.
4. Program fans to run at a different speed if necessary.
5. Read the state of Bits <3:1> of Configuration Register 2 (0x73). The state of these bits reflects whether a 4-wire fan is directly connected to the PWM output.

As the detection time only takes 5ms, programming the PWM outputs to 100% and then back to its normal speed is not noticeable, in most cases.

How Fan Presence Detect Works

4-wire fans typically have an internal pull up to 4.75V ±10%, which typically sources 5 mA. While the detection cycle is on, an internal current sink is turned on, sinking current from the fan's internal pull-up. By driving some of the current from the fan's internal pull-up (~100 µA) the logic buffer switches to a defined logic state. If this state is high, a fan is present; if the state is low, no fan is present.

Note: The PWM input voltage should be clamped to 3.3 V. This ensures the PWM output is not pulled to a voltage higher than the maximum allowable voltage on that pin (3.6 V).

FAN SYNC

When two ADT7476s are used in a system, it is possible to synchronize them so that one PWM channel from each device can be effectively OR'ed together to create a PWM output that reflects the maximum speed of the two OR'ed PWMs. This OR'ed PWM can in turn be used to drive a chassis fan. See the Analog Devices website for information on the Fan SYNC function.

STANDBY MODE

The ADT7476 has been specifically designed to respond to the STBY supply. In computers that support S3 and S5 states, the core voltage of the processor is lowered in these states. When monitoring $\overline{\text{THERM}}$, the $\overline{\text{THERM}}$ timer should be disabled during these states.

When the V_{CCP} voltage drops below the V_{CCP} low limit, the following occurs:

1. Status Bit 1 (V_{CCP}) in Status Register 1 is set.
2. $\overline{\text{SMBALERT}}$ is generated, if enabled.
3. $\overline{\text{THERM}}$ monitoring is disabled. The $\overline{\text{THERM}}$ timer should hold its value prior to the S3 or S5 state.

Once the core voltage, V_{CCP}, goes above the V_{CCP} low limit, everything is re-enabled and the system resumes normal operation.

XNOR TREE TEST MODE

The ADT7476 includes an XNOR tree test mode. This mode is useful for in-circuit test equipment at board-level testing. By applying stimulus to the pins included in the XNOR tree, it is possible to detect opens, or shorts, on the system board.

The XNOR tree test is invoked by setting Bit 0 (XEN) of the XNOR tree test enable register (Reg. 0x6F).

Figure 66 shows the signals that are exercised in the XNOR tree test mode.

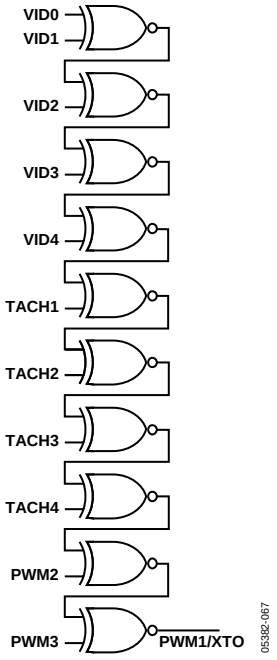


Figure 66. XNOR Tree Test

POWER-ON DEFAULT

When the ADT7476 is powered up, monitoring is off by default and the PWM outputs go to 100%. All necessary registers then need to be configured via the SMBus for the appropriate functions to operate.

REGISTER TABLES

Table 17. ADT7476 Registers

Address	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Lockable?
0x10	R/W	Config. 6	ExtraSlow	V_{CCP} Low	MasterEn	SlaveEn	THERM in Manual	SLOW Remote 2	SLOW Local	SLOW Remote 1	0x00	Yes
0x11	R	Config. 7	RES	RES	RES	RES	RES	RES	RES	DisTHERMHys	0x00	Yes
0x20	R	2.5 V measurement	9	8	7	6	5	4	3	2	0x00	
0x21	R	V_{CCP} measurement	9	8	7	6	5	4	3	2	0x00	
0x22	R	V_{CC} measurement	9	8	7	6	5	4	3	2	0x00	
0x23	R	5 V measurement	9	8	7	6	5	4	3	2	0x00	
0x24	R	12 V measurement	9	8	7	6	5	4	3	2	0x00	
0x25	R	Remote 1 Temperature	9	8	7	6	5	4	3	2	0x80	
0x26	R	Local Temperature	9	8	7	6	5	4	3	2	0x80	
0x27	R	Remote 2 Temperature	9	8	7	6	5	4	3	2	0x80	
0x28	R	TACH 1 Low Byte	7	6	5	4	3	2	1	0	0x00	
0x29	R	TACH 1 High Byte	15	14	13	12	11	10	9	8	0x00	
0x2A	R	TACH 2 Low Byte	7	6	5	4	3	2	1	0	0x00	
0x2B	R	TACH 2 High Byte	15	14	13	12	11	10	9	8	0x00	
0x2C	R	TACH 3 Low Byte	7	6	5	4	3	2	1	0	0x00	
0x2D	R	TACH 3 High Byte	15	14	13	12	11	10	9	8	0x00	
0x2E	R	TACH 4 Low Byte	7	6	5	4	3	2	1	0	0x00	
0x2F	R	TACH 4 High Byte	15	14	13	12	11	10	9	8	0x00	
0x30	R/W	PWM1 Current Duty Cycle	7	6	5	4	3	2	1	0	0xFF	
0x31	R/W	PWM2 Current Duty Cycle	7	6	5	4	3	2	1	0	0xFF	
0x32	R/W	PWM3 Current Duty Cycle	7	6	5	4	3	2	1	0	0xFF	
0x38	R/W	Max PWM 1 Duty Cycle	7	6	5	4	3	2	1	0	0xFF	Yes
0x39	R/W	Max PWM 2 Duty Cycle	7	6	5	4	3	2	1	0	0xFF	Yes
0x3A	R/W	Max PWM 3 Duty Cycle	7	6	5	4	3	2	1	0	0xFF	Yes
0x3D	R	Device ID Register	7	6	5	4	3	2	1	0	0x76	
0x3E	R	Company ID Number	7	6	5	4	3	2	1	0	0x41	
0x3F	R	Revision Number	VER	VER	VER	VER	STP	STP	STP	STP	0x69	
0x40	R/W	Configuration 1	RES	TODIS	FSPDIS	Vx1	FSPD	RDY	LOCK	STRT	0x04	Yes
0x41	R	Interrupt Status 1	OOL	R2T	LT	R1T	5 V	V_{CC}	V_{CCP}	2.5 V /THERM	0x00	

Address	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Lockable?
0x42	R	Interrupt Status 2	D2 FAULT	D1 FAULT	FAN4/ $\overline{\text{THERM}}$ /GPIO4	FAN3	FAN2	FAN1	$\overline{\text{THERM}}$ Temp Limit	12 V/VC	0x00	
0x43	R/W	VID Config	VIDSEL	THLD	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	0x1F	
0x44	R/W	2.5 V Low Limit	7	6	5	4	3	2	1	0	0x00	
0x45	R/W	2.5 V High Limit	7	6	5	4	3	2	1	0	0xFF	
0x46	R/W	V_{CCP} Low Limit	7	6	5	4	3	2	1	0	0x00	
0x47	R/W	V_{CCP} High Limit	7	6	5	4	3	2	1	0	0xFF	
0x48	R/W	V_{CC} Low Limit	7	6	5	4	3	2	1	0	0x00	
0x49	R/W	V_{CC} High Limit	7	6	5	4	3	2	1	0	0xFF	
0x4A	R/W	5 V Low Limit	7	6	5	4	3	2	1	0	0x00	
0x4B	R/W	5 V High Limit	7	6	5	4	3	2	1	0	0xFF	
0x4C	R/W	12 V Low Limit	7	6	5	4	3	2	1	0	0x00	
0x4D	R/W	12 V High Limit	7	6	5	4	3	2	1	0	0xFF	
0x4E	R/W	Remote 1 Temp Low Limit	7	6	5	4	3	2	1	0	0x81	
0x4F	R/W	Remote 1 Temp High Limit	7	6	5	4	3	2	1	0	0x7F	
0x50	R/W	Local Temp Low Limit	7	6	5	4	3	2	1	0	0x81	
0x51	R/W	Local Temp High Limit	7	6	5	4	3	2	1	0	0x7F	
0x52	R/W	Remote 2 Temp Low Limit	7	6	5	4	3	2	1	0	0x81	
0x53	R/W	Remote 2 Temp High Limit	7	6	5	4	3	2	1	0	0x7F	
0x54	R/W	TACH1 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	
0x55	R/W	TACH1 Minimum High Byte	15	14	13	12	11	10	9	8	0xFF	
0x56	R/W	TACH2 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	
0x57	R/W	TACH2 Minimum High Byte	15	14	13	12	11	10	9	8	0xFF	
0x58	R/W	TACH3 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	
0x59	R/W	TACH3 Minimum High Byte	15	14	13	12	11	10	9	8	0xFF	
0x5A	R/W	TACH4 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	
0x5B	R/W	TACH4 Minimum High Byte	15	14	13	12	11	10	9	8	0xFF	
0x5C	R/W	PWM1 Configuration Register	BHVR	BHVR	BHVR	INV	RES	SPIN	SPIN	SPIN	0x62	Yes
0x5D	R/W	PWM2 Configuration Register	BHVR	BHVR	BHVR	INV	RES	SPIN	SPIN	SPIN	0x62	Yes

Address	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Lockable?
0x5E	R/W	PWM3 Configuration Register	BHVR	BHVR	BHVR	INV	RES	SPIN	SPIN	SPIN	0x62	Yes
0x5F	R/W	Remote 1 T_{RANGE}/PWM 1 Frequency	RANGE	RANGE	RANGE	RANGE	HF/LF	FREQ	FREQ	FREQ	0XC4	Yes
0x60	R/W	Local T_{RANGE}/PWM 2 Frequency	RANGE	RANGE	RANGE	RANGE	HF/LF	FREQ	FREQ	FREQ	0XC4	Yes
0x61	R/W	Remote 2 T_{RANGE}/PWM3 Frequency	RANGE	RANGE	RANGE	RANGE	HF/LF	FREQ	FREQ	FREQ	0XC4	Yes
0x62	R/W	Enhance Acoustics Reg. 1	MIN3	MIN2	MIN1	SYNC	EN1	ACOU	ACOU	ACOU	0X00	Yes
0x63	R/W	Enhance Acoustics Reg. 2	EN2	ACOU2	ACOU2	ACOU2	EN3	ACOU3	ACOU3	ACOU3	0X00	Yes
0x64	R/W	PWM1 Min Duty Cycle	7	6	5	4	3	2	1	0	0X80	Yes
0x65	R/W	PWM2 Min Duty Cycle	7	6	5	4	3	2	1	0	0X80	Yes
0x66	R/W	PWM3 Min Duty Cycle	7	6	5	4	3	2	1	0	0X80	Yes
0x67	R/W	Remote 1 Temp T_{MIN}	7	6	5	4	3	2	1	0	0X5A	Yes
0x68	R/W	Local Temp T_{MIN}	7	6	5	4	3	2	1	0	0X5A	Yes
0x69	R/W	Remote 2 Temp T_{MIN}	7	6	5	4	3	2	1	0	0X5A	Yes
0x6A	R/W	Remote 1 $\overline{\text{THERM}}$ Temp Limit	7	6	5	4	3	2	1	0	0X64	Yes
0x6B	R/W	Local $\overline{\text{THERM}}$ Temp Limit	7	6	5	4	3	2	1	0	0X64	Yes
0x6C	R/W	Remote 2 $\overline{\text{THERM}}$ Temp Limit	7	6	5	4	3	2	1	0	0X64	Yes
0x6D	R/W	Remote 1 and Local Temp/T_{MIN} Hysteresis	HYSR1	HYSR1	HYSR1	HYSR1	HYSL	HYSL	HYSL	HYSL	0X44	Yes
0x6E	R/W	Remote 2 Temp/T_{MIN} Hysteresis	HYSR2	HYSR2	HYSR2	HYRS	RES	RES	RES	RES	0X40	Yes
0x6F	R/W	XNOR Tree Test Enable	RES	RES	RES	RES	RES	RES	RES	XEN	0X00	Yes
0x70	R/W	Remote 1 Temperature Offset	7	6	5	4	3	2	1	0	0X00	Yes
0x71	R/W	Local Temperature Offset	7	6	5	4	3	2	1	0	0X00	Yes
0x72	R/W	Remote 2 Temperature Offset	7	6	5	4	3	2	1	0	0X00	Yes
0x73	R/W	Configuration Register 2	RES	CONV	ATTN	AVG	Fan3Detect	Fan2Detect	Fan1Detect	FanPresenceDT	0X00	Yes
0x74	R/W	Interrupt Mask 1 Register	OOL	R2T	LT	RIT	5 V	V_{CC}	V_{CCP}	2.5 V/ $\overline{\text{THERM}}$	0X00	
0x75	R/W	Interrupt Mask 2 Register	D2	D1	F4P	FAN3	FAN2	FAN1	OVT	12 V / VC	0X00	
0x76	R/W	Extended Resolution 1	5 V	5 V	V_{CC}	V_{CC}	V_{CCP}	V_{CCP}	2.5 V	2.5 V	0X00	
0x77	R/W	Extended Resolution 2	TDM2	TDM2	LTMP	LTMP	TDM1	TDM1	12 V	12 V	0X00	

Address	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Lockable?
0x78	R/W	Config. 3	DC4	DC3	DC2	DC1	FAST	BOOST	$\overline{\text{THERM}}$ /2.5V	ALERT Enable	0x00	Yes
0x79	R	$\overline{\text{THERM}}$ Timer Status	TMR	TMR	TMR	TMR	TMR	TMR	TMR	ASRT/TMRO	0x00	
0x7A	R/W	$\overline{\text{THERM}}$ Timer Limit	LIMT	LIMT	LIMT	LIMT	LIMT	LIMT	LIMT	LIMT	0x00	
0x7B	R/W	TACH Pulses per Revolution	FAN4	FAN4	FAN3	FAN3	FAN2	FAN2	FAN1	FAN1	0x55	
0x7C	R/W	Config. 5	R2 $\overline{\text{THERM}}$ O/P Only	Local $\overline{\text{THERM}}$ O/P Only	R1 $\overline{\text{THERM}}$ O/P Only	VID/ GPIO	GPIO6P	GPIO6D	Temp Offset	TWOS COMPL	0x01	Yes
0x7D	R/W	Config. 4	BpAtt 12 V	BpAtt 5 V	BpAtt V_{CCP}	BpAtt 2.5 V	Max/Full on $\overline{\text{THERM}}$	$\overline{\text{THERM}}$ Disable	Pin 14 Func	Pin 14 Func	0x00	Yes
0x7E	R	Test 1	do not write to these registers								0x00	Yes
0x7F	R	Test 2	do not write to these registers								0x00	Yes

Table 18. Register 0x10—Configuration Register 6 (Power-On Default = 0x00)[1, 2]

Bit	Mneumonic	R/W	Description
<0>	SlowFan Remote 1	Read/write	When this bit is set, Fan 1 smoothing times are multiplied ×4 for Remote 1 temperature channel (as defined in Register 0x62).
<1>	SlowFan Local	Read/write	When this bit is set, Fan 2 smoothing times are multiplied ×4 for local temperature channel (as defined in Register 0x63).
<2>	SlowFan Remote 2	Read/write	When this bit is set, Fan 3 smoothing times are multiplied ×4 for Remote 2 temperature channel (as defined in Register 0x63).
<3>	THERM in Manual	Read/write	When this bit is set, THERM is enabled in manual mode[1].
<4>	SlaveEn	Read/write	Setting this bit configures the ADT7476 as a slave for use in fan sync mode.
<5>	MasterEn	Read/write	Setting this bit configures the ADT7476 as a master for use in fan sync mode.
<6>	VccpLow	Read/write	V_{CCP}LO = 1. When the power is supplied from 3.3 V STANDBY and the core voltage (V_{CCP}) drops below its V_{CCP} low limit value (Reg. 0x46), the following occurs: • Status Bit 1 in Status Register 1 is set. • $\overline{\text{SMBALERT}}$ is generated, if enabled. • $\overline{\text{PROCHOT}}$ monitoring is disabled. • Everything is re-enabled once V_{CCP} increases above the V_{CCP} low limit. When V_{CCP} increases above the low limit: • $\overline{\text{PROCHOT}}$ monitoring is enabled. • Fans return to their programmed state after a spin-up cycle.
<7>	ExtraSlow	Read/write	When this bit is set, all fan smoothing times are increased by a further 39.2%

[1] A $\overline{\text{THERM}}$ event always overrides any fan setting (even when fans are disabled).
[2] This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any subsequent attempts to write to this register fail.

Table 19. Register 0x11—Configuration Register 7 (Power-On Default = 0x00) [1]

Bit	Mneumonic	R/W	Description
<0>	DisTHERMHys	Read/write	Setting this bit to 1 disables $\overline{\text{THERM}}$ hysteresis.
<7:1>	Reserved	N/A	Reserved. Do not write to these bits.

[1] This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any subsequent attempts to write to this register fail.

Table 20. Voltage Reading Registers (Power-On Default = 0x00)[1]

Register Address	R/W	Description
0x20	Read-only	Reflects the voltage measurement at the 2.5 V input on Pin 22 (8 MSBs of reading).
0x21	Read-only	Reflects the voltage measurement[2] at the V_{CCP} input on Pin 23 (8 MSBs of reading).
0x22	Read-only	Reflects the voltage measurement[3] at the V_{CC} input on Pin 4 (8 MSBs of reading).
0x23	Read-only	Reflects the voltage measurement at the 5 V input on Pin 20 (8 MSBs of reading.
0x24	Read-only	Reflects the voltage measurement at the 12 V input on Pin 21 (8 MSBs of reading).

[1] If the extended resolution bits of these readings are also being read, the extended resolution registers (Reg. 0x76, 0x77) must be read first. Once the extended resolution registers have been read, the associated MSB reading registers are frozen until read. Both the extended resolution registers and the MSB registers are frozen.
[2] If V_{CCP}Low (Bit 7 of 0x40) is set, V_{CCP} can control the sleep state of the ADT7476.
[3] V_{CC} (Pin 4) is the supply voltage for the ADT7476.

Table 21. Temperature Reading Registers (Power-On Default = 0x80)[1, 2, 3]

Register Address	R/W	Description
0x25	Read-only	Remote 1 temperature reading[3, 4] (8 MSB of reading).
0x26	Read-only	Local temperature reading (8 MSB of reading).
0x27	Read-only	Remote 2 temperature reading[3, 4] (8 MSB of reading).

[1] If the extended resolution bits of these readings are also being read, the extended resolution registers (Reg. 0x76, 0x77) must be read first. Once the extended resolution registers have been read, all associated MSB reading registers are frozen until read. Both the extended resolution registers and the MSB registers are frozen.
[2] These temperature readings can be in twos complement or Offset 64 format; this interpretation is determined by Bit 0 of Configuration Register 5 (0x7C).
[3] In twos complement mode, a temperature reading of −128°C (0x80) indicates a diode fault (open or short) on that channel.
[4] In Offset 64 mode, a temperature reading of −64°C (0x00) indicates a diode fault (open or short) on that channel.

Table 22. Fan Tachometer Reading Registers (Power-On Default = 0x00)[1]

Register Address	R/W	Description
0x28	Read-only	TACH1 low byte.
0x29	Read-only	TACH1 high byte.
0x2A	Read-only	TACH2 low byte.
0x2B	Read-only	TACH2 high byte.
0x2C	Read-only	TACH3 low byte.
0x2D	Read-only	TACH3 high byte.
0x2E	Read-only	TACH4 low byte.
0x2F	Read-only	TACH4 high byte.

[1] These registers count the number of 11.11 µs periods (based on an internal 90 kHz clock) that occur between a number of consecutive fan TACH pulses (default = 2). The number of TACH pulses used to count can be changed using the fan pulses per revolution register (Reg. 0x7B). This allows the fan speed to be accurately measured. Because a valid fan tachometer reading requires that two bytes are read, the low byte *must* be read first. Both the low and high bytes are then frozen until read. At power-on, these registers contain 0x0000 until such time as the first valid fan TACH measurement is read into these registers. This prevents false interrupts from occurring while the fans are spinning up. A count of 0xFFFF indicates that a fan is one of the following:
Stalled or blocked (object jamming the fan).
Failed (internal circuitry destroyed).
Not populated. (The ADT7476 expects to see a fan connected to each TACH. If a fan is not connected to that TACH, its TACH minimum high and low bytes should be set to 0xFFFF.)
Alternate function, for example, TACH4 reconfigured as $\overline{\text{THERM}}$ pin.

Table 23. Current PWM Duty Cycle Registers (Power-On Default = 0xFF)[1]

Register Address	R/W	Description
0x30	Read/write	PWM1 current duty cycle (0% to 100% duty cycle = 0x00 to 0xFF).
0x31	Read/write	PWM2 current duty cycle (0% to 100% duty cycle = 0x00 to 0xFF).
0x32	Read/write	PWM3 current duty cycle (0% to 100% duty cycle = 0x00 to 0xFF).

[1] These registers reflect the PWM duty cycle driving each fan at any given time. When in automatic fan speed control mode, the ADT7476 reports the PWM duty cycles back through these registers. The PWM duty cycle values vary according to temperature in automatic fan speed control mode. During fan startup, these registers report back 0x00. In manual mode, the PWM duty cycle outputs can be set to any duty cycle value by writing to these registers.

Table 24. Maximim PWM Duty Cycle (Power-On Default = 0xFF)[1, 2]

Register Address	R/W[2]	Description
0x38	Read/write	Maximum duty cycle for PWM1 output, default = 100% (0xFF.)
0x39	Read/write	Maximum duty cycle for PWM2 output, default = 100% (0xFF).
0x3A	Read/Write	Maximum duty cycle for PWM3 output, default = 100% (0xFF).

[1] These registers set the maximum PWM duty cycle of the PWM output.
[2] This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any subsequent attempts to write to this register fail.

Table 25. Register 0x40—Configuration Register 1 (Power-On Default = 0x04)

Bit	Name	R/W	Description
<0>	STRT[1,2]	Read/write	Logic 1 enables monitoring and PWM control outputs based on the limit settings programmed. Logic 0 disables monitoring and PWM control based on the default power-up limit settings. Note that the limit values programmed are preserved even if a Logic 0 is written to this bit and the default settings are enabled. This bit does not become locked once Bit 1 (LOCK bit) has been set.
<1>	LOCK	Write once	Logic 1 locks all limit values to their current settings. Once this bit is set, all lockable registers become read-only and cannot be modified until the ADT7476 is powered down and powered up again. This prevents rogue programs such as viruses from modifying critical system limit settings. (Lockable.)
<2>	RDY	Read-only	This bit is set to 1 by the ADT7476 to indicate only that the device is fully powered-up and ready to begin system monitoring.
<3>	FSPD	Read/write	When set to 1, this bit runs all fans at full speed. Power-on default = 0. This bit never gets locked.
<4>	Vx1	Read/write	BIOS should set this bit to a 1 when the ADT7476 is configured to measure current from an ADI ADOPT™ VRM controller and to measure the CPU's core voltage. This bit allows monitoring software to display CPU watts usage. (Lockable.)
<5>	FSPDIS	Read/write	Logic 1 disables fan spin-up for two TACH pulses. Instead, the PWM outputs go high for the entire fan spin-up timeout selected.
<6>	TODIS	Read/write	When this bit is set to 1, the SMBus timeout feature is enabled. In this state, if at any point during an SMBus transaction involving the ADT7476 activity ceases for more than 35 ms, the ADT7476 assumes the bus is locked and releases the bus. This allows the ADT7476 to be used with SMBus controllers that cannot handle SMBus timeouts. (Lockable.)

[1] Bit 0 (STRT) of 0x40, Configuration Register 1 remains writable after lock bit is set.
[2] When monitoring (STRT) is disabled, PWM outputs always go to 100% for thermal protection.

Table 26. Register 0x41—Interrupt Status Register 1 (Power-On Default = 0x00)

Bit	Name	R/W	Description
<0>	2.5 V/ $\overline{\text{THERM}}$ timer	Read-only	2.5 V = 1 indicates that the 2.5 V high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided. If Pin 22 is configured as $\overline{\text{THERM}}$, this bit is asserted when the timer limit has been exceeded.
<1>	V_{CCP}	Read-only	V_{CCP} = 1 indicates that the V_{CCP} high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<2>	V_{CC}	Read-only	V_{CC} = 1 indicates that the V_{CC} high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<3>	5 V	Read-only	A 1 indicates the 5 V high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<4>	RIT	Read-only	RIT = 1 indicates that the Remote 1 low or high temperature has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<5>	LT	Read-only	LT =1 indicates that the local low or high temperature has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<6>	R2T	Read-only	R2T = 1 indicates that the Remote 2 low or high temperature has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
<7>	OOL	Read-only	OOL = 1 indicates that an out-of-limit event has been latched in Status Register 2. This bit is a logical OR of all status bits in Status Register 2. Software can test this bit in isolation to determine whether any of the voltage, temperature, or fan speed readings represented by Status Register 2 are out-of-limit, which saves the need to read Status Register 2 during every interrupt or polling cycle.

Table 27. Register 0x42—Interrupt Status Register 2 (Power-On Default = 0x00)

Bit	Name	R/W	Description
<0>	12V/VC	Read-only	A 1 indicates that the 12 V high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided. If Pin 21 is configured as VID5, this bit is the VID change bit. This bit is set when the levels on VID0 to VID5 are different than they were 11 µs previously. This pin can be used to generate an $\overline{\text{SMBALERT}}$ whenever the VID code changes.
<1>	OVT	Read-only	OVT = 1 indicates that one of the $\overline{\text{THERM}}$ overtemperature limits has been exceeded. This bit is cleared on a read of the status register when the temperature drops below $\overline{\text{THERM}} - T_{HYST}$.
<2>	FAN1	Read-only	FAN1 = 1 indicates that Fan 1 has dropped below minimum speed or has stalled. This bit is not set when the PWM 1 output is off.
<3>	FAN2	Read-only	FAN2 = 1 indicates that Fan 2 has dropped below minimum speed or has stalled. This bit is not set when the PWM 2 output is off.
<4>	FAN3	Read-only	FAN3 = 1 indicates that Fan 3 has dropped below minimum speed or has stalled. This bit is not set when the PWM 3 output is off.
<5>	F4P	Read-only	When Pin 14 is programmed as a TACH4 input, F4P = 1 indicates that Fan 4 has dropped below minimum speed or has stalled. This bit is not set when the PWM3 output is off.
		Read/write	When Pin 14 is programmed as the GPIO6 output, writing to this bit determines the logic output of GPIO6. When GPIO6 is programmed as an input, this bit reflects the value read by GPIO6.
		Read-only	If Pin 14 is configured as the $\overline{\text{THERM}}$ timer input for $\overline{\text{THERM}}$ monitoring, then this bit is set when the $\overline{\text{THERM}}$ assertion time exceeds the limit programmed in the $\overline{\text{THERM}}$ limit register (Reg. 0x7A).
<6>	D1	Read-only	D1 = 1 indicates either an open or short circuit on the Thermal Diode 1 inputs.
<7>	D2	Read-only	D2 = 1 indicates either an open or short circuit on the Thermal Diode 2 inputs.

Table 28. Register 43H—VID Register (Power-On Default = 0x1F)

Bit	Name	R/W	Description
<4:0>	VID[4:0]	Read-only	The VID[4:0] inputs from the CPU indicate the expected processor core voltage. On power-up, these bits reflect the state of the VID pins, even if monitoring is not enabled.
<5>	VID5	Read-only	Reads VID5 from the CPU when Bit 7 = 1. If Bit 7 = 0, the VID5 bit always reads back 0 (power-on default).
<6>	THLD	Read/write	Selects the input switching threshold for the VID inputs.
			THLD = 0 selects a threshold of 1 V (V_{OL} < 0.8 V, V_{IH} > 1.7 V).
			THLD = 1 lowers the switching threshold to 0.6 V (V_{OL} < 0.4 V, V_{IH} > 0.8 V).
<7>	VIDSEL	Read/write	VIDSEL = 0 configures Pin 21 as the 12 V measurement input (default).

Table 29. Voltage Limit Registers[1]

Register Address	R/W	Description[2]	Power-On Default
0x44	Read/write	2.5 V low limit.	0x00
0x45	Read/write	2.5 V high limit.	0xFF
0x46	Read/write	V_{CCP} low limit.	0x00
0x47	Read/write	V_{CCP} high limit.	0xFF
0x48	Read/write	V_{CC} low limit.	0x00
0x49	Read/write	V_{CC} high limit.	0xFF
0x4A	Read/write	5 V low limit.	0x00
0x4B	Read/write	5 V high limit.	0xFF
0x4C	Read/write	12 V low limit.	0x00
0x4D	Read/write	12 V high limit.	0xFF

[1] Setting the Configuration Register 1 lock bit has no effect on these registers.
[2] High limits: An interrupt is generated when a value exceeds its high limit (> comparison). Low limits: An interrupt is generated when a value is equal to or below its low limit (≤ comparison).

Table 30. Temperature Limit Registers[1]

Register Address	R/W	Description[2]	Power-On Default
0x4E	Read/write	Remote 1 temperature low limit.	0x81
0x4F	Read/write	Remote 1 temperature high limit.	0x7F
0x50	Read/write	Local temperature low limit.	0x81
0x51	Read/write	Local temperature high limit.	0x7F
0x52	Read/write	Remote 2 temperature low limit.	0x81
0x53	Read/write	Remote 2 temperature high limit.	0x7F

[1] Exceeding any of these temperature limits by 1°C causes the appropriate status bit to be set in the interrupt status register. Setting the Configuration Register 1 lock bit has no effect on these registers.
[2] High limits: An interrupt is generated when a value exceeds its high limit (> comparison). Low limits: An interrupt is generated when a value is equal to or below its low limit (≤ comparison).

Table 31. Fan Tachometer Limit Registers[1]

Register Address	R/W	Description	Power-On Default
0x54	Read/write	TACH1 minimum low byte.	0xFF
0x55	Read/write	TACH1 minimum high byte/single-channel ADC channel select.	0xFF
0x56	Read/write	TACH2 minimum low byte.	0xFF
0x57	Read/write	TACH2 minimum high byte.	0xFF
0x58	Read/write	TACH3 minimum low byte.	0xFF
0x59	Read/write	TACH3 minimum high byte.	0xFF
0x5A	Read/write	TACH4 minimum low byte.	0xFF
0x5B	Read/write	TACH4 minimum high byte.	0xFF

[1] Exceeding any of the TACH limit registers by 1 indicates that the fan is running too slowly or has stalled. The appropriate status bit is set in Interrupt Status Register 2 to indicate the fan failure. Setting the Configuration Register 1 lock bit has no effect on these registers.

Table 32. Register 0x55—TACH 1 Minimum High Byte (Power-On Default = 0xFF)

Bits	Name	R/W	Description
<4:0>	Reserved	Read-only	These bits are reserved when Bit 6 of Config 2 Register (0x73) is set (single-channel ADC mode). Otherwise, these bits represent Bits <4:0> of the TACH1 minimum high byte.
<7:5>	SCADC	Read/write	When Bit 6 of Config 2 Register (0x73) is set (single-channel ADC mode), these bits are used to select the only channel from which the ADC will take measurements. Otherwise, these bits represent Bits <7:5> of the TACH1 minimum high byte.

Table 33. PWM Configuration Registers

Register Address		R/W[1]	Description	Power-On Default
0x5C		Read/write	PWM1 configuration.	0x62
0x5D		Read/write	PWM2 configuration.	0x62
0x5E		Read/write	PWM3 configuration.	0x62
Bit	**Name**	**R/W**	**Description**	
<2:0>	SPIN	Read/write	These bits control the startup timeout for PWMx. The PWM output stays high until two valid TACH rising edges are seen from the fan. If there is not a valid TACH signal during the fan TACH measurement directly after the fan startup timeout period, then the TACH measurement reads 0xFFFF and Status Register 2 reflects the fan fault. If the TACH minimum high and low bytes contain 0xFFFF or 0x0000, then the Status Register 2 bit is not set, even if the fan has not started. 000 = No startup timeout 001 = 100 ms 010 = 250 ms (default) 011 = 400 ms 100 = 667 ms 101 = 1 sec 110 = 2 sec 111 = 4 sec	
<4>	INV	Read/write	This bit inverts the PWM output. The default is 0, which corresponds to a logic high output for 100% duty cycle. Setting this bit to 1 inverts the PWM output, so 100% duty cycle corresponds to a logic low output.	
<7:5>	BHVR	Read/write	These bits assign each fan to a particular temperature sensor for localized cooling. 000 = Remote 1 temperature controls PWMx (automatic fan control mode). 001 = local temperature controls PWMx (automatic fan control mode). 010 = Remote 2 temperature controls PWMx (automatic fan control mode). 011 = PWMx runs full speed (default). 100 = PWMx disabled. 101 = fastest speed calculated by local and Remote 2 temperature controls PWMx. 110 = fastest speed calculated by all three temperature channel controls PWMx. 111 = manual mode. PWM duty cycle registers (Reg. 0x30 to Reg. 0x32) become writable.	

[1] These registers become read-only when the Configuration Register 1 lock bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 34. TEMP TRANGE/PWM Frequency Registers

Register Address		R/W[1]	Description	Power-On Default
0x5F		Read/write	Remote 1 T_{RANGE}/PWM1 frequency.	0xC4
0x60		Read/write	Local temperature T_{RANGE}/PWM2 frequency.	0xC4
0x61		Read/write	Remote 2 T_{RANGE}/PWM3 frequency.	0xC4
Bit	**Name**	**R/W**	**Description**	
<2:0>	FREQ	Read/write	These bits control the PWMx frequency (only apply when PWM channel is in low frequency mode). 000 = 11.0 Hz 001 = 14.7 Hz 010 = 22.1 Hz 011 = 29.4 Hz 100 = 35.3 Hz (default) 101 = 44.1 Hz 110 = 58.8 Hz 111 = 88.2 Hz	
<3>	HF/LF	Read/write	HF/LF = 1, High frequency PWM mode is enabled for PWM X. HF/LF = 0, Low frequency PWM mode is enabled for PWM X.	
<7:4>	RANGE	Read/write	These bits determine the PWM duty cycle vs. the temperature range for automatic fan control. 0000 = 2°C 0001 = 2.5°C 0010 = 3.33°C 0011 = 4°C 0100 = 5°C 0101 = 6.67°C 0110 = 8°C 0111 = 10°C 1000 = 13.33°C 1001 = 16°C 1010 = 20°C 1011 = 26.67°C 1100 = 32°C (Default) 1101 = 40°C 1110 = 53.33°C 1111 = 80°C	

[1]These registers become read-only when the Configuration Register 1 lock bit is set. Any further attempts to write to these registers have no effect.

Table 35. Register 0x62—Enhanced Acoustics Register 1 (Power-On Default = 0x00)

Bit	Name	R/W[1]	Description	
<2:0>	ACOU[2]	Read/write	Assuming that PWM X is associated with the Remote 1 temperature channel, these bits define the maximum rate of change of the PWM X output for Remote 1 temperature-related changes. Instead of the fan speed jumping instantaneously to its newly determined speed, it ramps gracefully at the rate determined by these bits. This feature ultimately enhances the acoustics of the fan.	
			When Bit 7 of Configuration Register 6 (0x10) is 0	
			Time Slot Increase	**Time for 0% to 100%**
			000 = 1	37.5 sec
			001 = 2	18.8 sec
			010 = 3	12.5 sec
			011 = 4	7.5 sec
			100 = 8	4.7 sec
			101 = 12	3.1 sec
			110 = 24	1.6 sec
			111 = 48	0.8 sec
			When Bit 7 of Configuration Register 6 (0x10) is 1	
			Time Slot Increase	**Time for 0% to 100%**
			000 = 1	52.2 sec
			001 = 2	26.1 sec
			010 = 3	17.4 sec
			011 = 4	10.4 sec
			100 = 8	6.5 sec
			101 = 12	4.4 sec
			110 = 24	2.2 sec
			111 = 48	1.1 sec
<3>	EN1	Read/write	When this bit is 1, smoothing is enabled on Remote 1 temperature channel.	
<4>	SYNC	Read/write	SYNC = 1 synchronizes fan speed measurements on TACH2, TACH3, and TACH4 to PWM3. This allows up to three fans to be driven from PWM3 output and their speeds to be measured.	
			SYNC = 0 synchronizes only TACH3 and TACH4 to PWM3 output.	
<5>	MIN1	Read/write	When the ADT7476 is in automatic fan control mode, this bit defines whether PWM1 is off (0% duty cycle) or at PWM1 minimum duty cycle when the controlling temperature is below its T_{MIN} – hysteresis value.	
			0 = 0% duty cycle below T_{MIN} – hysteresis.	
			1 = PWM1 minimum duty cycle below T_{MIN} – hysteresis.	
<6>	MIN2	Read/write	When the ADT7476 is in automatic fan speed control mode, this bit defines whether PWM2 is off (0% duty cycle) or at PWM2 minimum duty cycle when the controlling temperature is below its T_{MIN} – hysteresis value.	
			0 = 0% duty cycle below T_{MIN} – hysteresis.	
			1 = PWM 2 minimum duty cycle below T_{MIN} – hysteresis.	
<7>	MIN3	Read/write	When the ADT7476 is in automatic fan speed control mode, this bit defines whether PWM3 is off (0% duty cycle) or at PWM3 minimum duty cycle when the controlling temperature is below its T_{MIN} – hysteresis value.	
			0 = 0% duty cycle below T_{MIN} – hysteresis.	
			1 = PWM3 minimum duty cycle below T_{MIN} – hysteresis.	

[1] This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.
[2] Setting the relevant bit of configuration register 6, (0x10, <2:0>), will further decrease these ramp rates by a factor of 4.

Table 36. Register 0x63—Enhanced Acoustics Register 2 (Power-On Default = 0x00)

Bit	Name	R/W[1]	Description	
<2:0>	ACOU3	Read/write	Assuming that PWM X is associated with the Local temperature channel, these bits define the maximum rate of change of the PWM X output for local temperature-related changes. Instead of the fan speed jumping instantaneously to its newly determined speed, it ramps gracefully at the rate determined by these bits. This feature ultimately enhances the acoustics of the fan.	
			When Bit 7 of Configuration Register 6 (0x10) is 0	
			Time Slot Increase	**Time for 0% to 100%**
			000 = 1	37.5 sec
			001 = 2	18.8 sec
			010 = 3	12.5 sec
			011 = 4	7.5 sec
			100 = 8	4.7 sec
			101 = 12	3.1 sec
			110 = 24	1.6 sec
			111 = 48	0.8 sec
			When Bit 7 of Configuration Register 6 (0x10) is 1	
			Time Slot Increase	**Time for 0% to 100%**
			000 = 1	52.2 sec
			001 = 2	26.1 sec
			010 = 3	17.4 sec
			011 = 4	10.4 sec
			100 = 8	6.5 sec
			101 = 12	4.4 sec
			110 = 24	2.2 sec
			111 = 48	1.1 sec
< 3 >	EN3	Read/write	When this bit is 1, smoothing is enabled on the Local temperature channel.	
<6:4>	ACOU2	Read/write	Assuming that PWM X is associated with the Remote 2 temperature channel, these bits define the maximum rate of change of the PWM X output for Remote 2 Temperature related changes. Instead of the fan speed jumping instantaneously to its newly determined speed, it ramps gracefully at the rate determined by these bits. This feature ultimately enhances the acoustics of the fan.	
			When Bit 7 of Configuration Register 6 (0x10) is 0	
			Time Slot Increase	**Time for 0% to 100%**
			000 = 1	37.5 sec
			001 = 2	18.8 sec
			010 = 3	12.5 sec
			011 = 4	7.5 sec
			100 = 8	4.7 sec
			101 = 12	3.1 sec
			110 = 24	1.6 sec
			111 = 48	0.8 sec
			When Bit 7 of Configuration Register 6 (0x10) is 1	
			Time Slot Increase	**Time for 0% to 100%**
			000 = 1	52.2 sec
			001 = 2	26.1 sec
			010 = 3	17.4 sec
			011 = 4	10.4 sec
			100 = 8	6.5 sec
			101 = 12	4.4 sec
			110 = 24	2.2 sec
			111 = 48	1.1 sec
<7>	EN2	Read/write	When this bit is 1, smoothing is enabled on the Remote 2 temperature channel.	

[1] This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 37. PWM Minimum Duty Cycle Registers

Register Address		R/W[1]	Description	Power-On Default
0x64		Read/write	PWM1 minimum duty cycle.	0x80 (50% duty cycle)
0x65		Read/write	PWM2 minimum duty cycle.	0x80 (50% duty cycle)
0x66		Read/write	PWM3 minimum duty cycle.	0x80 (50% duty cycle)
Bit	**Name**	**R/W[1]**	**Description**	
<7:0>	PWM duty cycle	Read/write	These bits define the PWM_{MIN} duty cycle for PWMx. 0x00 = 0% duty cycle (fan off). 0x40 = 25% duty cycle. 0x80 = 50% duty cycle. 0xFF = 100% duty cycle (fan full speed).	

[1]These registers become read-only when the ADT7476 is in automatic fan control mode.

Table 38. T_{MIN} Registers[1]

Register Address	R/W[2]	Description	Power-On Default
0x67	Read/write	Remote 1 Temperature T_{MIN}.	0x5A (90°C)
0x68	Read/write	Local Temperatue T_{MIN}.	0x5A (90°C)
0x69	Read/write	Remote 2 Temperature T_{MIN}.	0x5A (90°C)

[1] These are the T_{MIN} registers for each temperature channel. When the temperature measured exceeds T_{MIN}, the appropriate fan runs at minimum speed and increases with temperature according to T_{RANGE}.
[2] These registers become read-only when the Configuration Register 1 lock bit is set. Any further attempts to write to these registers have no effect.

Table 39. $\overline{\text{THERM}}$ Limit Registers[1]

Register Address	R/W[2]	Description	Power-On Default
0x6A	Read/write	Remote 1 $\overline{\text{THERM}}$ limit.	0x64 (100°C)
0x6B	Read/write	Local $\overline{\text{THERM}}$ limit.	0x64 (100°C)
0x6C	Read/write	Remote 2 $\overline{\text{THERM}}$ limit.	0x64 (100°C)

[1] If any temperature measured exceeds its $\overline{\text{THERM}}$ limit, all PWM outputs drive their fans at 100% duty cycle. This is a fail-safe mechanism incorporated to cool the system in the event of a critical overtemperature. It also ensures some level of cooling in the event that software or hardware locks up. If set to 0x80, this feature is disabled. The PWM output remains at 100% until the temperature drops below $\overline{\text{THERM}}$ limit – hysteresis. If the $\overline{\text{THERM}}$ pin is programmed as an output, exceeding these limits by 0.25°C can cause the $\overline{\text{THERM}}$ pin to assert low as an output.
[2] These registers become read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to these registers have no effect.

Table 40. Temperature/T_{MIN} Hysteresis Registers[1]

Register Address	R/W[2]	Description	Power-On Default
0x6D	Read/write	Remote 1 and Local Temperature hysteresis.	0x44
<3:0>	HYSL	Local Temperature hyseresis. 0°C to 15°C of hysteresis can be applied to the Local temperature AFC control loops.	
<7:4>	HYSR1	Remote 1 Temperature hyseresis. 0°C to 15°C of hysteresis can be applied to the Remote 1 Temperature AFC control loops.	
0x6E	Read/write	Remote 2 temperature hysteresis.	0x40
<7:4>	HYSR2	Local Temperature hyseresis. 0°C to 15°C of hysteresis can be applied to the Local Temperature AFC control loops.	

[1] Each 4-bit value controls the amount of temperature hysteresis applied to a particular temperature channel. Once the temperature for that channel falls below its T_{MIN} value, the fan remains running at PWM_{MIN} duty cycle until the temperature = T_{MIN} – hysteresis. Up to 15°C of hysteresis can be assigned to any temperature channel. The hysteresis value chosen also applies to that temperature channel, if its $\overline{\text{THERM}}$ limit is exceeded. The PWM output being controlled goes to 100%, if the $\overline{\text{THERM}}$ limit is exceeded and remains at 100% until the temperature drops below $\overline{\text{THERM}}$ – hysteresis. For acoustic reasons, it is recommended the hysteresis value not be programmed less than 4°C. Setting the hysteresis value lower than 4°C causes the fan to switch on and off regularly when the temperature is close to T_{MIN}.
[2] These registers become read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to these registers have no effect.

Table 41. XNOR Tree Test Enable

Register Address	R/W[1]	Description	Power-On Default
0x6F	Read/write	XNOR tree test enable register.	0x00
<0>	XEN	If the XEN bit is set to 1, the device enters the XNOR tree test mode. Clearing the bit removes the device from the XNOR tree test mode.	
<7:1>	Reserved	Unused. Do not write to these bits.	

[1] This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 42. Remote 1 Temperature Offset[1]

Register Address	R/W[1]	Description	Power-On Default
0x70	Read/write	Remote 1 temperature offset.	0x00
<7:0>	Read/write	Allows a temperature offset to be automatically applied to the remote temperature 1 channel measurement. Bit 1 of 0x7C (Configuration Register 5) determines the range and resolution of this register.	

[1] This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 43. Local Temperature Offset[1]

Register Address	R/W[1]	Description	Power-On Default
0x71	Read/write	Local temperature offset.	0x00
<7:0>	Read/write	Allows a temperature offset to be automatically applied to the local temperature measurement. Bit 1 of 0x7C (Configuration Register 5) determines the range and resolution of this register.	

[1] This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 44. Remote 2 Temperature Offset[1]

Register Address	R/W[1]	Description	Power-On Default
0x72	Read/write	Remote 2 temperature offset.	0x00
<7:0>	Read/write	Allows a temperature offset to be automatically applied to the remote temperature 2 channel measurement. Bit 1 of 0x7C (Configuration Register 5) determines the range and resolution of this register.	

[1] This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 45. Register 0x73—Configuration Register 2 (Power-On Default = 0x00)[1]

Bit	Name	R/W[1]	Description
0	FanPresenceDT	Read/write	When FanPresenceDT = 1, the state of bits <3:1> of 0x73 reflects the presence of a 4-wire fan on the appropriate TACH channel.
1	Fan1Detect	Read	Fan1Detect = 1 indicates that a 4-wire fan is connected to the TACH 1 input.
2	Fan2Detect	Read	Fan2Detect = 1 indicates that a 4-wire fan is connected to the TACH 2 input.
3	Fan3Detect	Read	Fan3Detect = 1 indicates that a 4-wire fan is connected to the TACH 3 input.
4	AVG	Read/write	AVG = 1, averaging on the temperature and voltage measurements is turned off. This allows measurements on each channel to be made much faster. (x16).
5	ATTN	Read/write	ATTN = 1, the ADT7476 removes the attenuators from the 2.5 V, V_{CCP}, 5 V, and 12 V inputs. These inputs can be used for other functions such as connecting up external sensors. It is also possible to remove attenuators from individual channels using Bits <7:4> of Configuration Register 4 (0x7D).
6	CONV	Read/write	CONV = 1, the ADT7476 is put into a single-channel ADC conversion mode. In this mode, the ADT7476 can be made to read continuously from one input only, for example, Remote 1 temperature. The appropriate ADC channel is selected by writing to Bits <7:5> of TACH1 minimum high byte register (0x55).
			Bits <7:5> Reg. 0x55
			000 2.5 V
			001 V_{CCP}
			010 V_{CC} (3.3 V)
			011 5 V
			100 12 V
			101 Remote 1 temperature
			110 Local temperature
			111 Remote 2 temperature
7	Res		This bit is reserved and should not be changed.

[1] This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 46. Register 0x74—Interrupt Mask Register 1 (Power-On Default <7:0> = 0x00)

Bit	Name	R/W	Description
0	2.5V/$\overline{\text{THERM}}$	Read/write	2.5V/ $\overline{\text{THERM}}$ = 1, masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the 2.5 V/ $\overline{\text{THERM}}$ timer channel.
1	V_{CCP}	Read/write	V_{CCP} = 1, masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the V_{CCP} channel.
2	V_{CC}	Read/write	V_{CC} = 1, masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the V_{CC} channel.
3	5V	Read/write	5 V = 1, masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the 5 V channel.
4	RIT	Read/write	RIT = 1, masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the Remote 1 Temperature channel.
5	LT	Read/write	LT = 1, masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the Local Temperature channel.
6	R2T	Read/write	R2T = 1, masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the Remote 2 Temperature channel.
7	OOL	Read/write	OOL = 1, masks $\overline{\text{SMBALERT}}$ for any out-of-limit condition in Status Register 2.

Table 47. Register 0x75—Interrupt Mask Register 2 (Power-On Default <7:0> = 0x00)

Bit	Name	R/W	Description
0	12V/VC	Read/write	When Pin 21 is configured as a 12 V input, 12V/VC = 1 masks $\overline{\text{SMBALERT}}$ for out-of-limit conditions on the 12 V channel. When Pin 21 is programmed as VID5, this bit masks an $\overline{\text{SMBALERT}}$, if the VID5 VID code bit changes.
1	OVT	Read only	OVT = 1, masks $\overline{\text{SMBALERT}}$ for overtemperature $\overline{\text{THERM}}$ conditions.
2	FAN1	Read/write	FAN1 = 1, masks $\overline{\text{SMBALERT}}$ for a Fan 1 fault.
3	FAN2	Read/write	FAN2 = 1, masks $\overline{\text{SMBALERT}}$ for a Fan 2 fault.
4	FAN3	Read/write	FAN3 = 1, masks $\overline{\text{SMBALERT}}$ for a Fan 3 fault.
5	F4P	Read/write	If Pin 14 is configured as TACH 4, F4P = 1 masks $\overline{\text{SMBALERT}}$ for a Fan 4 fault. If Pin 14 is configured as $\overline{\text{THERM}}$, F4P = 1 masks $\overline{\text{SMBALERT}}$ for an exceeded $\overline{\text{THERM}}$ timer limit. If Pin 14 is configured as GPIO, F4P = 1 masks $\overline{\text{SMBALERT}}$ when GPIO is an input and GPIO is asserted.
6	D1	Read/write	D1 = 1 masks $\overline{\text{SMBALERT}}$ for a diode open or short on a Remote 1 channel.
7	D2	Read/write	D2 = 1 masks $\overline{\text{SMBALERT}}$ for a diode open or short on a Remote 2 channel.

Table 48. Register 0x76—Extended Resolution Register 1[1] (Power-On Default <7:0> = 0x00)

Bit	Name	R/W	Description
<1:0>	2.5V	Read-only	2.5 V LSBs. Holds the 2 LSBs of the 10-bit 2.5 V measurement.
<3:2>	V_{CCP}	Read-only	V_{CCP} LSBs. Holds the 2 LSBs of the 10-bit V_{CCP} measurement.
<5:4>	V_{CC}	Read-only	V_{CC} LSBs. Holds the 2 LSBs of the 10-bit V_{CC} measurement.
<7:6>	5 V	Read-only	5 V LSBs. Holds the 2 LSBs of the 10-bit 5 V measurement.

[1] If this register is read, this register and the registers holding the MSB of each reading are frozen until read.

Table 49. Register 0x77—Extended Resolution Register 2[1] (Power-On Default <7:0> = 0x00)

Bit	Name	R/W	Description
<1:0>	12 V	Read-only	12 V LSBs. Holds the 2 LSBs of the 10-bit 12 V measurement.
<3:2>	TDM1	Read-only	Remote 1 Temperature LSBs. Holds the 2 LSBs of the 10-bit Remote 1 temperature measurement.
<5:4>	LTMP	Read-only	Local Temperature LSBs. Holds the 2 LSBs of the 10-bit local temperature measurement.
<7:6>	TDM2	Read-only	Remote 2 Temperature LSBs. Holds the 2 LSBs of the 10-bit Remote 2 temperature measurement.

[1] If this register is read, this register and the registers holding the MSB of each reading are frozen until read.

Table 50. Register 0x78—Configuration Register 3 (Power-On Default = 0x00)

Bit	Name	R/W[1]	Description
<0>	ALERT	Read/write	ALERT = 1, Pin 10 (PWM2/$\overline{\text{SMBALERT}}$) is configured as an $\overline{\text{SMBALERT}}$ interrupt output to indicate out-of-limit error conditions. ALERT = 0, Pin 10 (PWM2/$\overline{\text{SMBALERT}}$) is configured as the PWM2 output.
<1>	$\overline{\text{THERM}}$ /2.5 V	Read/write	$\overline{\text{THERM}}$ = 1 enables $\overline{\text{THERM}}$ functionality on Pin 22 and Pin 14, if Pin 14 is configured as $\overline{\text{THERM}}$, determined by Bits 0 and 1 (PIN14FUNC) of Configuration Register 4. When $\overline{\text{THERM}}$ is asserted, if the fans are running and the boost bit is set, the fans run at full speed. Alternatively, $\overline{\text{THERM}}$ can be programmed so that a timer is triggered to time how long $\overline{\text{THERM}}$ has been asserted. $\overline{\text{THERM}}$ = 0 enables 2.5V measurement on Pin 22 and disables $\overline{\text{THERM}}$. If bits <5:7> of configuration register 5 are set, $\overline{\text{THERM}}$ is bidirectional. If they are 0, $\overline{\text{THERM}}$ is a timer input only.

Pin14FUNC	$\overline{\text{THERM}}$/2.5 V	Pin 22	Pin 14
00	0	2.5 V	TACH4
01	0	2.5 V	$\overline{\text{THERM}}$
10	0	2.5 V	$\overline{\text{SMBALERT}}$
11	0	2.5 V	GPIO
00	1	$\overline{\text{THERM}}$	TACH4
01	1	2.5 V	$\overline{\text{THERM}}$
10	1	$\overline{\text{THERM}}$	$\overline{\text{SMBALERT}}$
11	1	$\overline{\text{THERM}}$	GPIO

<2>	BOOST	Read/write	When $\overline{\text{THERM}}$ is an input and BOOST = 1, assertion of $\overline{\text{THERM}}$ causes all fans to run at the maximum programmed duty cycle for fail-safe cooling.
<3>	FAST	Read/write	FAST = 1, enables fast TACH measurements on all channels. This increases the TACH measurement rate from once per second to once every 250 ms (4 ×).
<4>	DC1	Read/write	DC1 = 1, enables TACH measurements to be continuously made on TACH1. Fans must be driven by dc. Setting this bit prevents pulse stretching, because it is not required for dc-driven motors.
<5>	DC2	Read/write	DC2 = 1, enables TACH measurements to be continuously made on TACH2. Fans must be driven by dc. Setting this bit prevents pulse stretching, because it is not required for dc-driven motors.
<6>	DC3	Read/write	DC3 = 1, enables TACH measurements to be continuously made on TACH3. Setting this bit prevents pulse stretching, because it is not required for dc-driven motors.
<7>	DC4	Read/write	DC4 = 1, enables TACH measurements to be continuously made on TACH4. Setting this bit prevents pulse stretching, because it is not required for dc-driven motors.

[1] This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 51. Register 0x79—$\overline{\text{THERM}}$ Timer Status Register (Power-On Default = 0x00)

Bit	Name	R/W	Description
<7:1>	TMR	Read-only	Times how long $\overline{\text{THERM}}$ input is asserted. These seven bits read zero until the $\overline{\text{THERM}}$ assertion time exceeds 45.52 ms.
<0>	ASRT/ TMR0	Read-only	This bit is set high on the assertion of the $\overline{\text{THERM}}$ input and is cleared on read. If the $\overline{\text{THERM}}$ assertion time exceeds 45.52 ms, this bit is set and becomes the LSB of the 8-bit TMR reading. This allows $\overline{\text{THERM}}$ assertion times from 45.52 ms to 5.82 sec to be reported back with a resolution of 22.76 ms.

Table 52. Register 0x7A—$\overline{\text{THERM}}$ Timer Limit Register (Power-On Default = 0x00)

Bit	Name	R/W	Description
<7:0>	LIMT	Read/write	Sets maximum $\overline{\text{THERM}}$ assertion length allowed before an interrupt is generated. This is an 8-bit limit with a resolution of 22.76 ms allowing $\overline{\text{THERM}}$ assertion limits of 45.52 ms to 5.82 s to be programmed. If the $\overline{\text{THERM}}$ assertion time exceeds this limit, Bit 5 (F4P) of Interrupt Status Register 2 (Reg. 0x42) is set. If the limit value is 0x00, an interrupt is generated immediately on the assertion of the $\overline{\text{THERM}}$ input.

Table 53. Register 0x7B—TACH Pulses per Revolution Register (Power-On Default = 0x55)

Bit	Name	R/W	Description
<1:0>	FAN1	Read/write	Sets number of pulses to be counted when measuring Fan 1 speed. Can be used to determine fan pulses per revolution for unknown fan type.
			Pulses Counted
			00 = 1
			01 = 2 (default)
			10 = 3
			11 = 4
<3:2>	FAN2	Read/write	Sets number of pulses to be counted when measuring Fan 2 speed. Can be used to determine fan pulses per revolution for unknown fan type.
			Pulses Counted
			00 = 1
			01 = 2 (default)
			10 = 3
			11 = 4
<5:4>	FAN3	Read/write	Sets number of pulses to be counted when measuring Fan 3 speed. Can be used to determine fan pulses per revolution for unknown fan type.
			Pulses Counted
			00 = 1
			01 = 2 (default)
			10 = 3
			11 = 4
<7:6>	FAN4	Read/write	Sets number of pulses to be counted when measuring Fan 4 speed. Can be used to determine fan pulses per revolution for unknown fan type.
			Pulses Counted
			00 = 1
			01 = 2 (default)
			10 = 3
			11 = 4

Table 54. Register 0x7C—Configuration Register 5 (Power-On Default = 0x01)

Bit	Name	R/W[1]	Description
<0>	2sC	Read/write	2sC = 1, sets the temperature range to the twos complement temperature range.
			2sC = 0, changes the temperature range to the Offset 64 temperature range. When this bit is changed, the ADT7476 interprets all relevant temperature register values as defined by this bit.
<1>	TempOffset	Read/write	TempOffset = 0 Sets offset range to −63C to +64C with 0.5°C resolution.
			TempOffset = 1 Sets offset range to −63°C to +127°C with 1°C resolution.
			These settings apply to registers 0x70, 0x71 and 0x72 (remote 1, internal and Remote2 Temperature offset registers.
<2>	GPIO6D	Read/write	GPIO 6 direction. When GPIO 6 function is enabled, this determines whether GPIO 6 is an input (0) or an output (1).
<3>	GPIO6P	Read/write	GPIO 6 polarity. When the GPIO 6 function is enabled and is programmed as an output, this bit determines whether the GPIO 6 is active low (0) or high (1).
<4>	VID/GPIO	Read/write	VID/GPIO = 0, VID functionality is enabled on pins 5, 6, 7, 8 and 19.
			VID/GPIO = 1, GPIO functionality is enabled on pins 5, 6, 7, 8 and 19.
<5>	R1 $\overline{\text{THERM}}$	Read/write	R1 $\overline{\text{THERM}}$ = 1 , $\overline{\text{THERM}}$ temperature limit functionality enabled for Remote 1 temperature channel, that is $\overline{\text{THERM}}$ is bi-directional. R1 $\overline{\text{THERM}}$ = 0, $\overline{\text{THERM}}$ is a timer input only.
			$\overline{\text{THERM}}$ can also be disabled on any channel by;
			In offset 64 mode, writing −64˚C to the appropriate $\overline{\text{THERM}}$ temperature limit
			In twos complement mode, writing −128˚C to the appropriate $\overline{\text{THERM}}$ temperature limit

Bit	Name	R/W[1]	Description
<6>	Local $\overline{\text{THERM}}$	Read/write	Local $\overline{\text{THERM}}$ = 1 , $\overline{\text{THERM}}$ temperature limit functionality enabled for Local temperature channel, that is $\overline{\text{THERM}}$ is bi-directional. Local $\overline{\text{THERM}}$ = 0, $\overline{\text{THERM}}$ is a timer input only. $\overline{\text{THERM}}$ can also be disabled on any channel by; In offset 64 mode, writing −64˚C to the appropriate $\overline{\text{THERM}}$ temperature limit In twos complement mode, writing −128˚C to the appropriate $\overline{\text{THERM}}$ temperature limit
<7>	R2 $\overline{\text{THERM}}$	Read/write	R2 $\overline{\text{THERM}}$ = 1 , $\overline{\text{THERM}}$ temperature limit functionality enabled for Remote 2 temperature channel, that is. $\overline{\text{THERM}}$ is bi-directional. R2 $\overline{\text{THERM}}$ = 0, $\overline{\text{THERM}}$ is a timer input only. $\overline{\text{THERM}}$ can also be disabled on any channel by; In offset 64 mode, writing −64°C to the appropriate $\overline{\text{THERM}}$ temperature limit In twos complement mode, writing −128°C to the appropriate $\overline{\text{THERM}}$ temperature limit

[1]This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 55. Register 0x7D—Configuration Register 4 (Power-On Default = 0x00)

Bit	Name	R/W[1]	Description
<1:0>	PIN14FUNC	Read/write	These bits set the functionality of Pin 14: 00 = TACH4 (default) 01 = $\overline{\text{THERM}}$ 10 = $\overline{\text{SMBALERT}}$ 11 = GPIO
<2>	$\overline{\text{THERM}}$ Disable	Read/write	$\overline{\text{THERM}}$ Disable=0, $\overline{\text{THERM}}$ overtemperature output is enabled assuming $\overline{\text{THERM}}$ is correctly configured (registers 0x78, 0x7C, 0x7D). $\overline{\text{THERM}}$ Disable=1, $\overline{\text{THERM}}$ overtemperature output is disabled on all channels. $\overline{\text{THERM}}$ can also be disabled on any channel by; In offset 64 mode, writing −64°C to the appropriate $\overline{\text{THERM}}$ temperature limit. In twos complement mode, writing −128°C to the appropriate $\overline{\text{THERM}}$ temperature limit.
<3>	MaxSpeed on $\overline{\text{THERM}}$	Read/write	MaxSpeed on $\overline{\text{THERM}}$=0, Fans go to full speed when $\overline{\text{THERM}}$ temperature limit is exceeded. MaxSpeed on $\overline{\text{THERM}}$=1, Fans go to max speed (0x38, 0x39, 0x3A) when $\overline{\text{THERM}}$ temperature limit is exceeded.
<4>	BpAtt2.5V	Read/write	Bypass 2.5 V attenuator. When set, the measurement scale for this channel changes from 0 V (0x00) to 2.25 V (0xFF).
<5>	BpAttV_{CCP}	Read/write	Bypass V_{CCP} attenuator. When set, the measurement scale for this channel changes from 0 V (0x00) to 2.25 V (0xFF).
<6>	BpAtt5V	Read/write	Bypass 5 V attenuator. When set, the measurement scale for this channel changes from 0 V (0x00) to 2.25 V (0xFF).
<7>	BpAtt12V	Read/write	Bypass 12 V attenuator. When set, the measurement scale for this channel changes from 0 V (0x00) to 2.25 V (0xFF).

[1]This register becomes read-only when the Configuration Register 1 lock bit is set to 1. Any further attempts to write to this register have no effect.

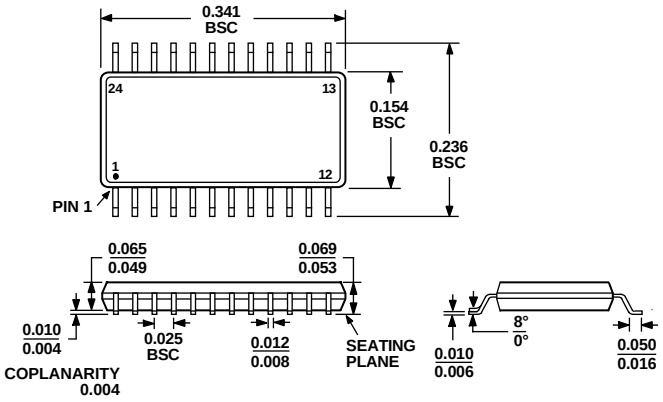
Table 56. Register 0x7E—Manufacturer's Test Register 1 (Power-On Default = 0x00)

Bit	Name	R/W	Description
<7:0>	Reserved	Read-only	Manufacturer's test register. These bits are reserved for manufacturer's test purposes and should *not* be written to under normal operation.

Table 57. Register 0x7F—Manufacturer's Test Register 2 (Power-On Default = 0x00)

Bit	Name	R/W	Description
<7:0>	Reserved	Read-only	Manufacturer's test register. These bits are reserved for manufacturer's test purposes and should *not* be written to under normal operation.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-137AE

Figure 67. 24-Lead Shrink Small Outline Package [QSOP]
(RQ-24)
Dimensions shown in inches

ORDERING GUIDE

Model	Termperature Range	Package Description	Package Option
ADT7476ARQZ[1]	–40°C to +125°C	24-Lead QSOP	RQ-24
ADT7476ARQZ-REEL[1]	–40°C to +125°C	24-Lead QSOP	RQ-24
ADT7476ARQZ-REEL7[1]	–40°C to +125°C	24-Lead QSOP	RQ-24

[1] Z = Pb-free part.

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