LCD Level Shifters with VCOM, NRS Buffers, and High Voltage Edge Detector

ADSY8401

FEATURES

- Complete suite of level shifters
- Eight inverting and three complementary level shifters for LCD timing
- High voltage edge detector
- Integrated low offset buffer for VCOM drives high capacitive loads
- MUXed input, low offset buffer for 2-level precharge drives high capacitive loads
- High current buffer for precharge provides high current drive into large capacitive loads
- Low power dissipation: 576 mW
- Available in 48-lead 7 mm × 7 mm LFCSP E-pad

PRODUCT DESCRIPTION

The ADSY8401 provides fast, 3 V to 15 V level shifters for LCD panel timing signals. An integrated low offset analog buffer is capable of driving the high capacitive loads. A 2:1 MUX input, low offset buffer simplifies application of 2-level precharge signals. A high current buffer provides high slew rates for large capacitive loads.

The ADSY8401 is fabricated on ADI's fast, 26 V XFHV process, providing fast input logic, high voltage level shifters, and precision drive amplifiers on the same chip.

The ADSY8401 dissipates 576 mW nominal static power.

The ADSY8401 is offered in a 48-lead 7 mm × 7 mm LFCSP E-pad package and operates over the commercial temperature range of 0°C to 85°C.

FUNCTIONAL BLOCK DIAGRAM

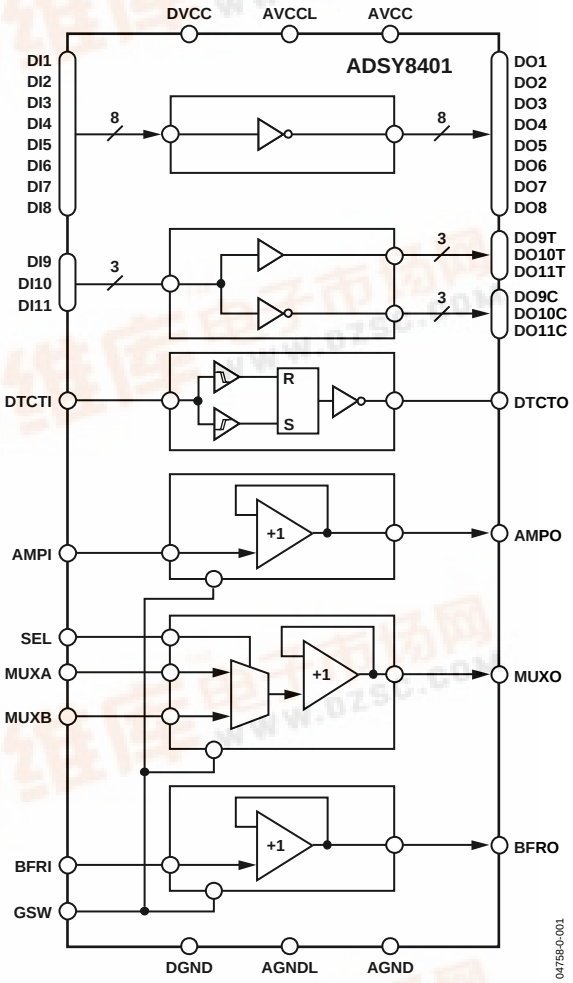

Figure 1.

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REVISION HISTORY

7/04—Revision 0: Initial Version

SPECIFICATIONS

At 25°C, AVCC = AVCCL = 15.5 V, DVCC = 3.3 V, T_A min = 0°C, T_A max = 85°C, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
Amp Section					
INPUT/OUTPUT CHARACTERISTICS					
Voltage Range					
V_H	AVCC – V_H		1.5	2.5	V
V_L	V_L – AGND		1.1	1.5	V
Output Voltage Grounded Mode	GSW = LOW		45		mV
Input Current			100		nA
Output Current			20		mA
Output Offset Voltage	VAMPI = 6 V, T_A = 25°C		1.5	8	mV
Output Offset Voltage	VAMPI = 6 V, T_A min to T_A max			11	mV
PSRR	AVCC ± 10%, T_A min to T_A max		0.1		mV/V
Gain Error	VAMPI = 3 V to 10 V, T_A min to T_A max		0.07	0.12	%
OUTPUT DYNAMIC PERFORMANCE	T_A min to T_A max, V_O = 5 V step, C_L = 1 nF				
−3 dB Bandwidth (Small Signal)	V_O = 0.25 V p-p		5.2		MHz
Slew Rate			13		V/µs
Settling Time to 0.5%	T_A min to T_A max		0.5	1	µs
Overshoot			0.05		%
MUX Section					
INPUT/OUTPUT CHARACTERISTICS					
Voltage Range					
V_H	AVCC – V_H		1.5	2.5	V
V_L	V_L – AGND		1.1	1.5	V
Output Voltage Grounded Mode	GSW = LOW		45		mV
Input Current					
I_I MUXA, MUXB			100		nA
Output Current			20		mA
Output Offset Voltage	VMUXA, B = 7.5 V, T_A = 25°C		1.5	8	mV
Output Offset Voltage	VMUXA, B = 7.5 V, T_A min to T_A max			11	mV
PSRR	AVCC ± 10%, T_A min to T_A max		0.1		mV/V
Gain Error	VMUXA, B 1.5 V to 12 V, T_A min to T_A max		0.07	0.12	%
SEL INPUT CHARACTERISTICS					
I_{IH} SEL			0.05		µA
I_{IL} SEL			−0.7		µA
V_{TH} SEL			1.65		V
V_{IH} SEL		2			V
V_{IL} SEL				0.8	V
OUTPUT DYNAMIC PERFORMANCE	V_O = 5 V step, C_L = 1 nF				
−3 dB Bandwidth (Small Signal)	V_O = 0.25 V p-p		5.2		MHz
Slew Rate			13		V/µs
Settling Time to 0.5%	T_A min to T_A max		0.5	1	µs
Overshoot			0.05		%
OUTPUT DYNAMIC PERFORMANCE	V_O = 5 V step, C_L = 15 pF				
−3 dB Bandwidth (Small Signal)	V_O = 0.25 V p-p		27		MHz
Slew Rate			13		V/µs
Settling Time to 0.5%	T_A min to T_A max		0.4	0.7	µs
Overshoot			0.1		%

Parameter	Conditions	Min	Typ	Max	Unit
BFR Section					
INPUT/OUTPUT CHARACTERISTICS					
Voltage Range					
V_H	AVCC – V_H		1.5	2.5	V
V_L	V_L – AGND		1.1	1.5	V
Output Voltage Grounded Mode	GSW = LOW		90		mV
Input Current			0.3		µA
Output Current			100		mA
Output Offset Voltage	BFRI = 7.5 V, T_A = 25°C		6	20	mV
Output Offset Voltage	BFRI = 7.5 V, T_A min to T_A max			30	mV
PSRR, T_A min to T_A max	AVCC ± 10%		1		mV/V
Gain Error, T_A min to T_A max	BFRI = 1.5 V to 12 V		0.5	0.65	%
OUTPUT DYNAMIC PERFORMANCE	V_O = 6 V step, C_L = 10 nF				
−3 dB Bandwidth (Small Signal)	V_O = 0.25 V p-p		1.3		MHz
Slew Rate			12		V/µs
Settling Time to 0.5%	T_A min to T_A max		0.7	1	µs
Overshoot			0.3		%
MUX and BFR Sections as NRS Buffer	See Figure 4				
Settling Time to 0.5%	C_L = 10 nF		0.9	1.5	µs
Level Shifter Section					
LEVEL SHIFTER LOGIC INPUTS					
C_{IN}				3	pF
I_{IH}			0.05		µA
I_{IL}			−0.6		µA
V_{IH}		2			V
V_{IL}				0.8	V
V_{TH}			1.65		V
LEVEL SHIFTER OUTPUTS					
V_{OH}		AVCCL – 0.5	AVCCL – 0.25		V
V_{OL}			0.25	0.5	V
LEVEL SHIFTER DYNAMIC PERFORMANCE	T_A min to T_A max				
Output Rise, Fall Times, tr, tf	10% to 90%				
DO1–DO8, DO9T–DO11T, DO9C–DO11C	C_L = 40 pF		20	30	ns
DO1–DO8	C_L = 300 pF		130	150	ns
Propagation Delay times, t_{11}, t_{12}, t_{13}, t_{14}					
DO1–DO8, DO9T–DO11T, DO9C–DO11C	C_L = 40 pF		23	50	ns
DO1–DO8	C_L = 300 pF		60	80	ns
Propagation Delay Skew, t_{15}, t_{16}	C_L = 40 pF				
DO1–DO8				2	ns
Propagation Delay Skew, t_{15}, t_{16}, t_{17}, t_{18}	C_L = 40 pF				
DO1–DO8, DO9T–DO11T, DO9C–DO11C			4		ns

Parameter	Conditions	Min	Typ	Max	Unit
Level Shifting Edge Detector Section	C_L = 10 pF				
Input Low Voltage, V_{IL}				AGND + 1.5	V
Input High Voltage, V_{IH}		AVCC − 1.5			V
Input Rising Edge Threshold Voltage, V_{TH} LH			AGND + 3		V
Input Falling Edge Threshold Voltage, V_{TH} HL			AVCC − 3		V
Output High Voltage, V_{OH}		DVCC − 0.5	DVCC − 0.25		V
Output Low Voltage, V_{OL}			0.25	0.5	V
Input Current High State, I_{IH}			1.2	2.5	µA
Input Current, I_{IL}		−2.5	−1.2		µA
Input Rising Edge Propagation Delay Time, t_{19}			15.5		ns
Input Falling Edge Propagation Delay Time, t_{20}			16.5		ns
t_{20} Variation with Temperature, Δt_{20}	T_A = 25°C to 85°C		2		ns
Output Rise, Fall Time, t_r	10% to 90%		6		ns
Grounded-Mode Switch					
GSW INPUT CHARACTERISTICS					
C_{IN}				3	pF
R_{IN}			50		kΩ
I_{IH}			0.6		µA
I_{IL}			−70		µA
V_{IH}		2			V
V_{IL}				0.8	V
V_{TH}			1.65		V
Power Supplies					
Operating Range, DVCC		3	3.3	3.6	V
Quiescent Current, DVCC			20	25	mA
Operating Range, AVCC, AVCCL1, 2, 3				18	V
Quiescent Current, AVCCL1			12.5	15.5	mA
Quiescent Current, AVCCL2	DI1 − DI11 ≤ V_{IL}		5.2	6.6	mA
Quiescent Current, AVCCL3	DI1 − DI11 ≤ V_{IL}		5.2	6.6	mA
Quiescent Current, AVCCL2	DI1 − DI11 ≥ V_{IH}		11.5	14.3	mA
Quiescent Current, AVCCL3	DI1 − DI11 ≥ V_{IH}		11.5	14.3	mA
Quiescent Current, AVCC			10	12.8	mA
Operating Temperature					
Ambient Temperature Range, T_A	In still air	0		85	°C

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameters	Rating
Supply Voltages	
AVCC to AGND	18 V
AVCCL to AGNDL	18 V
AGND to AGNDL	±0.5 V
AGND to DGND	±0.5 V
DVCC to DGND	4.5 V
Input Voltages	
Maximum Digital Input Voltages	DVCC + 0.5 V
Minimum Digital Input Voltages	DGND − 0.5 V
Maximum Analog Input Voltages	AVCCx + 0.5 V
Minimum Analog Input Voltages	AGNDx − 0.5 V
Internal Power Dissipation[1]	
LFCSP Package at 25°C, Ambient	3.8 W
Operating Temperature Range	0°C to 85°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature Range (Soldering 10 s)	300°C

[1] 48-lead LFCSP package:
θ_{JA} = 26°C/W (still air): JEDEC STD, 4-layer PCB, 0 CFM airflow
θ_{JC} = 20°C/W
Ψ_{JB} =11.0°C/W (still air)
Ψ_{JT} =0.4°C/W (still air)

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

Junction Temperature

The maximum power that can be safely dissipated by the ADSY8401 is limited by its junction temperature. The maximum safe junction temperature for plastic encapsulated devices as determined by the glass transition temperature of the plastic is approximately 150°C. Exceeding this limit temporarily might cause a shift in the parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 150°C for an extended period can result in device failure.

Exposed Paddle

The die paddle must be in good thermal contact with at least a partial plane for proper operation in high ambient temperature environments. The partial plane must be in good electrical contact with AVCC or AGND for reliable electrical operation. See the PCB Design for Optimized Thermal Performance section for more information on the use of the exposed paddles to dissipate excess heat.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

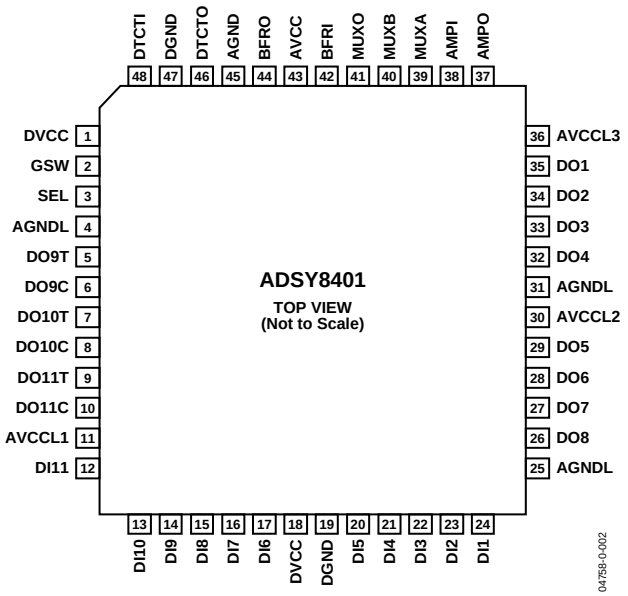

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 18	DVCC	Digital Power Supply.
2	GSW	Grounded Mode Switch. When the voltage on the GSW pin is tied to DGND, the AMPO, MUXO, and BFRO outputs are pulled to near AGND. When the GSW input is left unconnected or tied to DVCC, all outputs operate normally. The level shifters are not affected by the GSW input.
3, 39–41	SEL, MUXA, MUXB, MUXO	Analog Precharge. Low offset unity gain amplifier with MUXed inputs. Drives large capacitive loads. For driving large capacitive loads at high slew rates, connect MUXO to BFRI and the load capacitance to BFRO. SEL = HIGH selects MUXA.
4, 25, 31	AGNDL	Level Shifter Ground.
5–10	DO9–11T, DO9–11C	Complementary Level Shifter Outputs. While the corresponding input voltage of these level shifters is below the threshold voltage, the voltage at the noninverting output pins is at V_{OL} and the voltage at the inverting outputs is at V_{OH}. While the corresponding input voltage of these level shifters is above the threshold voltage, the voltage at the noninverting output pins is at V_{OH} and the voltage at the inverting outputs is at V_{OL}.
11, 30, 36	AVCCL1, 2, 3	Level Shifter Power Supply.
12–14	DI9–11	Complementary Level Shifter Inputs. Low voltage input of the complementary level shifters.
15–17, 20–24	DI1–8	Inverting Level Shifter Inputs. Low voltage input of the inverting level shifters.
19, 47	DGND	Digital Ground. This pin is normally connected to the digital ground plane.
26–29, 32–35	DO1-8	Inverting Level Shifter Outputs. While the corresponding input voltage of these level shifters is below the threshold voltage, the output voltage at these pins is at V_{OH}. While the corresponding input voltage of these level shifters is above the threshold voltage, the output voltage at these pins is at V_{OL}.
37–38	AMPO, AMPI	Analog Amplifier. Low offset unity gain amplifier. Drives large capacitive loads such as VCOM.
42, 44	BFRI, BFRO	Analog Buffer. High current output buffer.
43	AVCC	Analog Power Supplies. Analog power supplies for the level shifter and the amplifiers.
45	AGND	Analog Supply Returns. Analog supply returns for the level shifter and the amplifiers.
46	DTCTO	Edge Detecting Level Shifter Output. Logic output of the inverting level shifting edge detector.
48	DTCTI	Edge Detecting Level Shifter Input. High voltage input of the inverting level shifting edge detector.

AMPLIFIER APPLICATIONS

AMP SECTION AS VCOM BUFFER

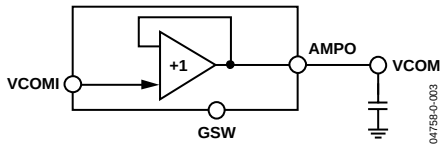

Figure 3. Amp Section as VCOM Buffer

MUX AND BFR SECTIONS AS NRS BUFFER

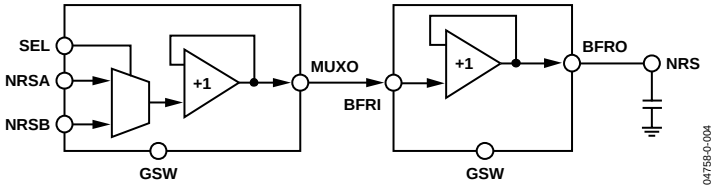

Figure 4. MUX and BFR Sections as NRS Buffer

MUX SECTION AS VCOM BUFFER

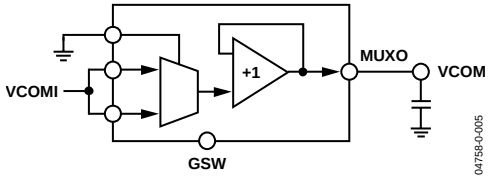

Figure 5. MUX Section as VCOM Buffer

LEVEL SHIFTER CHARACTERISTICS

LEVEL SHIFTER TIMING CHARACTERISTICS

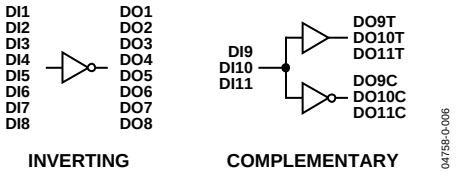

Figure 6. Level Shifter Timing Characteristics

INVERTING AND COMPLEMENTARY LEVEL SHIFTER TIMING

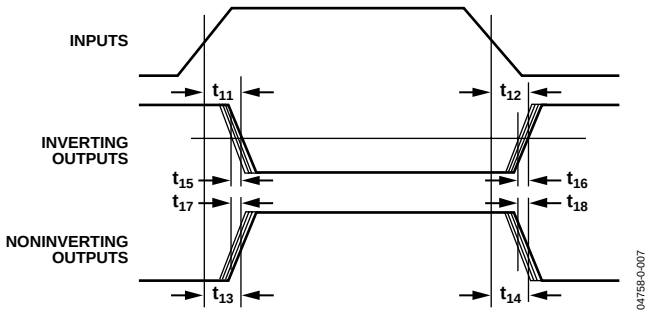

Figure 7. Inverting and Complementary Level Shifter Timing

Table 4.

Parameter	Conditions	Min	Typ	Max	Unit
LEVEL SHIFTER SECTION	T_A min to T_A max				
Output Rise, Fall Times, tr, tf					
DO1–DO8, DO9T–DO11T, DO9C–DO11C	C_L = 40 pF		20	30	ns
DO1–DO8	C_L = 300 pF		130	150	ns
Propagation Delay times, t_{11}, t_{12}, t_{13}, t_{14}					
DO1–DO8, DO9T–DO11T, DO9C–DO11C	C_L = 40 pF		23	50	ns
DO1–DO8	C_L = 300 pF		60	80	ns
Propagation Delay Skew, t_{15}, t_{16}	C_L = 40 pF				
DO1–DO8				2	ns
Propagation Delay Skew, t_{15}, t_{16}, t_{17}, t_{18}	C_L = 40 pF				
DO1–DO8 to DO9T–DO11T and DO9C–DO11C			4		ns

LEVEL SHIFTING EDGE DETECTOR TIMING CHARACTERISTICS

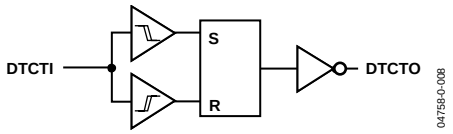

Figure 8. Level Shifting Edge Detector Timing Characteristics

LEVEL SHIFTING EDGE DETECTOR TIMING

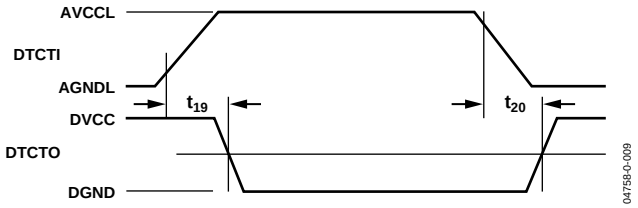

Figure 9. Level Shifting Edge Detector Timing

Table 5.

Parameter	Conditions	Min	Typ	Max	Unit
LEVEL SHIFTING EDGE DECTECTOR	C_L = 10 pF				
Input Low Voltage, V_{IL}				AGND + 1.5	V
Input High Voltage, V_{IH}		AVCC − 1.5			V
Input Rising Edge Threshold Voltage, V_{TH} LH			AGND + 3		V
Input Falling Edge Threshold Voltage, V_{TH} HL			AVCC − 3		V
Output High Voltage, V_{OH}		DVCC − 0.5	DVCC − 0.25		V
Output Low Voltage, V_{OL}			0.25	0.5	V
Input Current High State, I_{IH}			1.2	2.5	µA
Input Current, I_{IL}		−2.5	−1.2		µA
Input Rising Edge Propagation Delay Time, t_{19}			15.5		ns
Input Falling Edge Propagation Delay Time, t_{20}			16.5		ns
t_{20} Variation with Temperature, Δt_{20}	T_A = 25°C to 85°C		2		ns
Output Rise, Fall Time, t_r			6		ns

APPLICATIONS

The ADSY8401 is designed as part of a *DecDriver*® based LCD driver platform. The level shifters provide an interface between the image processor and a timing loop, operating at 3.3 V, and the LCD with high voltage timing input levels. The edge detecting level shifter provides an interface between the LCD monitor output at high voltage and a timing loop such as the AD8389 at 3.3 V. Low offset buffers, AMP and MUX, are capable of driving high capacitive loads such as VCOM and NRS without additional buffering. The high current buffer BFR is capable of 100 mA output current, providing high slew rates into large capacitive loads, which are often required for the precharge input, NRS of LCDs.

AMP CHANNEL

The AMP channel is a low offset unity gain buffer designed to drive a wide range of capacitive loads with a clean settling response. In LCD panel applications, it is most frequently used as a VCOM buffer.

MUX CHANNEL

The MUX channel is a 2-input, buffered analog multiplexer. The overall performance of its buffered output is very similar to that of the AMP channel. It is ideally suited for driving a wide range of capacitive loads, from very small up to several nF.

DRIVING NRS

Analog voltage switching capability is provided by the MUX channel. To achieve rapid settling while driving the capacitive NRS input, the output of the MUX is buffered by the high current drive BFR channel.

BFR CHANNEL

The BFR channel comprises a high output current buffer. It can be used to increase the output drive capability of either the AMP or MUX channels. The BFR channel is most often used in series with the MUX channel output to realize a high current drive NRS switch.

GROUNDED OUTPUT MODE

In certain designs it is desirable to pull the amplifier and buffer outputs to near ground during power-down. When the voltage on the GSW pin is tied to DGND, the AMPO, MUXO, and BFRO outputs are pulled to near AGND. When the GSW input is left unconnected or tied to DVCC, all outputs operate normally. The level shifters are not affected by the GSW input.

DRIVING VCOM

The AMP channel comprises a low offset, unity gain buffer. It can be used to drive a large capacitive load, such as VCOM, directly with low overshoot. In certain systems, it might be desirable for a single ADSY8401 to drive the VCOM inputs of more than one LCD panel. In such cases, the MUX channel can be used to drive VCOM directly. The MUX's switching function is not used, and its output is tied directly to VCOM without the use of the BFR channel. Offset errors and pulse response are the same as that of the AMP channel.

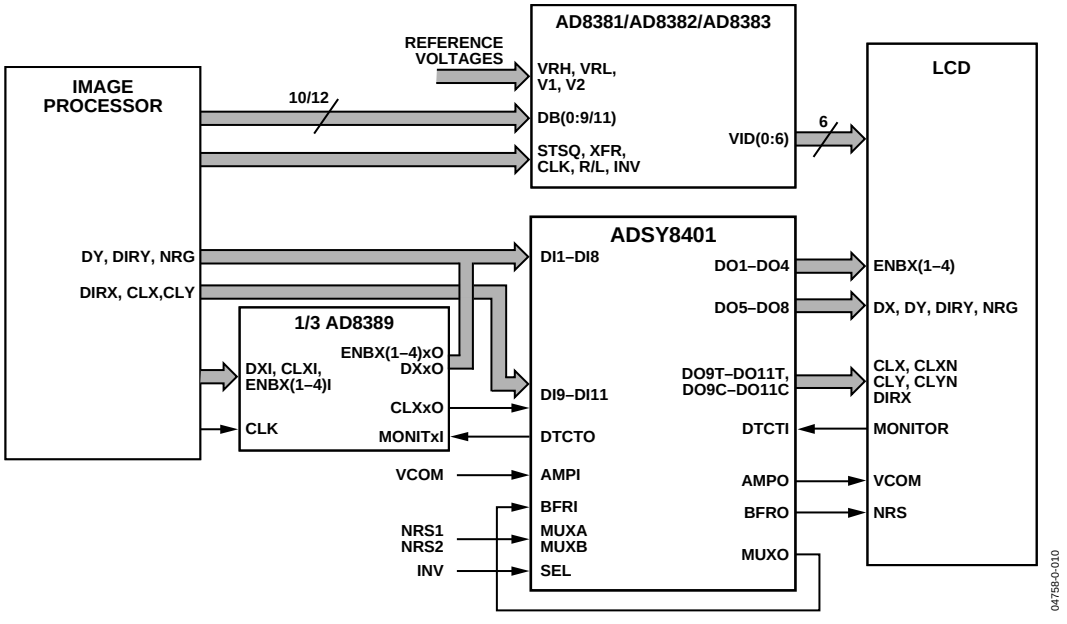

Figure 10. Typical Application—One ADSY8401 per Color

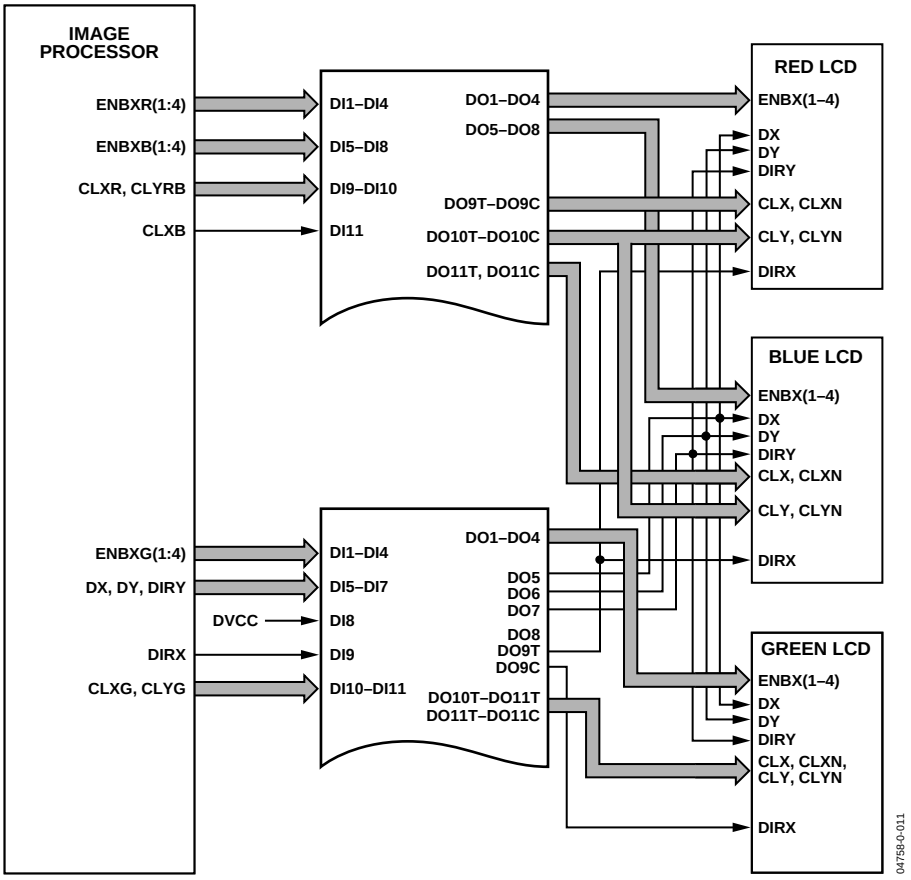

Figure 11. Typical Application—Two ADSY8401 per System, Level Shifters

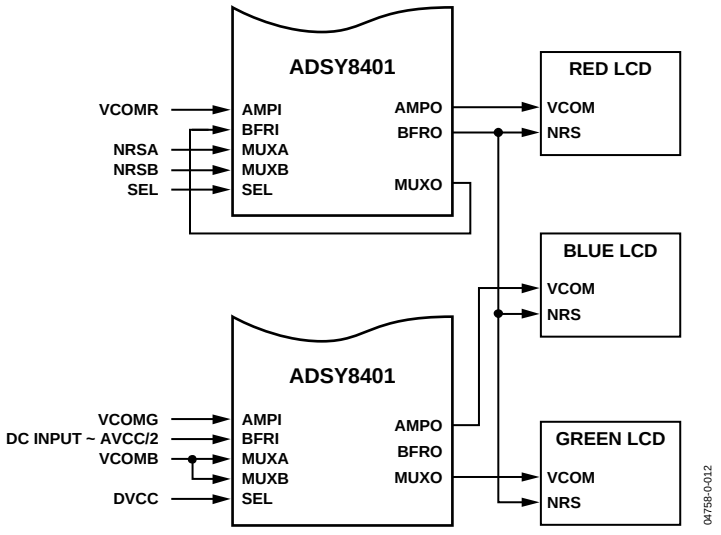

Figure 12. Typical Application—Two ADSY8401 per System, Amplifiers

PCB DESIGN FOR OPTIMIZED THERMAL PERFORMANCE

The total maximum power dissipation of the ADSY8401 is partly load-dependent. In a typical 60 Hz XGA system, the total maximum power dissipation is ≈ 1 W. The ADSY8401 package is designed to provide superior thermal characteristics, partly through the exposed die paddle on the bottom surface of the package. To take full advantage of this feature, the exposed paddle must be in direct thermal contact with the PCB, which then serves as a heat sink.

A thermally effective PCB must incorporate a thermal pad and a thermal via structure. The thermal pad provides a solderable contact surface on the top surface of the PCB. The thermal via structure provides a thermal path to the inner and bottom layers of the PCB to remove heat.

Thermal Pad Design

To minimize thermal performance degradation of production PCBs, the contact area between the thermal pad and the PCB should be maximized. Therefore, the size of the thermal pad on the top PCB layer should match the exposed paddle. The second thermal pad of the same size should be placed on the bottom side of the PCB. At least one thermal pad should be in direct thermal contact with an external plane such as AVCC or GND.

Thermal Via Structure Design

Effective heat transfer from the top to the inner and bottom layers of the PCB requires thermal vias incorporated into the thermal pad design. Thermal performance increases logarithmically with the number of vias. Near optimum thermal performance of production PCBs is attained only when tightly spaced thermal vias are placed on the full extent of the thermal pad.

Table 6. Recommended Land Pattern Dimensions

Land Pattern	Dimensions
Top and Bottom Layers	
Pad size	0.5 mm × 0.25 mm
Pad pitch	0.5 mm
Thermal pad size	5.25 mm × 5.25 mm
Thermal via structure	0.25 mm diameter vias on 0.5 mm grid

Thermal Pad and Thermal Via Connections

Thermal pads are connected to the AGND or AVCC plane. The thermal pad on the solder side is connected to a plane. The use of thermal spokes is not recommended when connecting the thermal pads or via structure to the plane.

Solder Masking

To minimize the formation of solder voids due to solder flowing into the via holes (solder wicking), the via diameter should be small. Solder masking of the via holes on the top layer of the PCB plugs the via holes, inhibiting solder flow into the holes. To optimize the thermal pad coverage, the solder mask diameter should be no more than 0.1 mm larger than the via diameter.

Table 7. Recommended Solder Mask Dimensions

Solder Mask	Dimensions
Top layer	
Pads	Set by customer's PCB design rules
Thermal vias	0.25 mm diameter circular mask centered on the vias
Bottom layer	Set by customer's PCB design rules

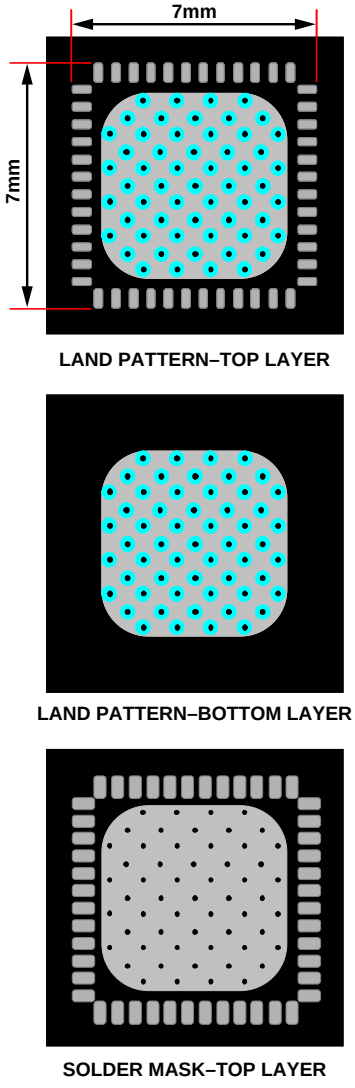

Figure 13. PCB Layers

POWER SUPPLY SEQUENCING

As indicated in the Absolute Maximum Ratings section, the voltage at any input pin cannot exceed its supply voltage by more than 0.5 V. To ensure compliance with the absolute maximum ratings, power-up and power-down sequencing might be required.

During power-up, initial application of nonzero voltages to any of the input pins must be delayed until the supply voltage ramps up to at least the highest maximum operational input voltage.

During power-down, the voltage at any input pin must reach zero during a period not exceeding the hold-up time of the power supply.

Failure to comply with the absolute maximum ratings may result in functional failure or damage to the internal ESD diodes. Damaged ESD diodes can cause temporary parametric failures, which can result in image artifacts. Damaged ESD diodes cannot provide full ESD protection, reducing reliability.

Power-on sequence:

1. Apply power to supplies.
2. Apply inputs.

Power-off sequence:

1. Remove signal from inputs.
2. Remove power from supplies.

Power-Off Sequencing Using the GSW Pin

In certain designs it is desirable to pull the amplifier, buffer, and level shifter outputs to near ground during power-down.

Power-off sequence with GSW:

1. Apply low to the GSW pin.
2. Apply high to all level shifter input pins.
3. Pull the MUXA, MUXB, AMPI, and BFRI inputs to AGND.
4. Remove AVCC.
5. Remove DVCC.

LAYOUT CONSIDERATIONS

The ADSY8401 is a mixed-signal, high speed, high accuracy device. To fully realize its specifications, it is essential to use a properly designed printed circuit board.

Layout and Grounding

The analog outputs and the digital inputs of the ADSY8401 are on opposite sides of the package. Keep these sections separated to minimize crosstalk and coupling of digital inputs into the analog outputs.

All signal trace lengths should be made as short and direct as possible to prevent signal degradation due to parasitic effects. Note that a digital signal should not cross or be routed near analog signals.

It is imperative to provide a solid analog ground plane under and around the ADSY8401. All ground pins of the part should be connected directly to this ground plane with no extra signal path length. This includes AGND, AGNDL, and DGND. The return traces for any of the signals should be routed close to the ground pin for that section to prevent stray signals from coupling into other ground pins.

Power Supply Bypassing

All power supply pins of the ADSY8401 must be properly bypassed to the analog ground plane for optimum performance.

TOTAL POWER DISSIPATION

The total power dissipation of the ADSY8401 has three components:

- Quiescent power dissipation when all digital inputs are low.
- Dynamic power dissipation due to the capacitance of the LCD (typical C_L = 200 pF for all the NRG control inputs, C_L = 40 pF for all other control inputs).
- Average power dissipation due to the toggling inputs.

When DI1–DI11 are at digital low, the quiescent power dissipation of the ADSY8401 is 576 mW. When DI1–DI11 are at digital high, the quiescent power dissipation is 771 mW.

The typical dynamic power dissipation of each of the three ADSY8401, due to the capacitance of the LCD, is 155 mW in a typical 60 Hz XGA system, shown in Figure 10. It is 304 mW and 153 mW, respectively, for the two ADSY8401s in the 60 Hz XGA system shown in Figure 11.

The average power dissipation of each of the three ADSY8401 due to DI1–DI11 toggling is 23 mW in the system shown in Figure 10. It is 32 mW and 22 mW, respectively, for the two ADSY8401 in the system shown in Figure 11.

The total power dissipation of each of the three ADSY8401 in the XGA system, shown in Figure 10, is 754 mW.

The total power dissipation of the two ADSY8401s in the XGA system, shown in Figure 12, is 912 mW and 751 mW, respectively.

OUTLINE DIMENSIONS

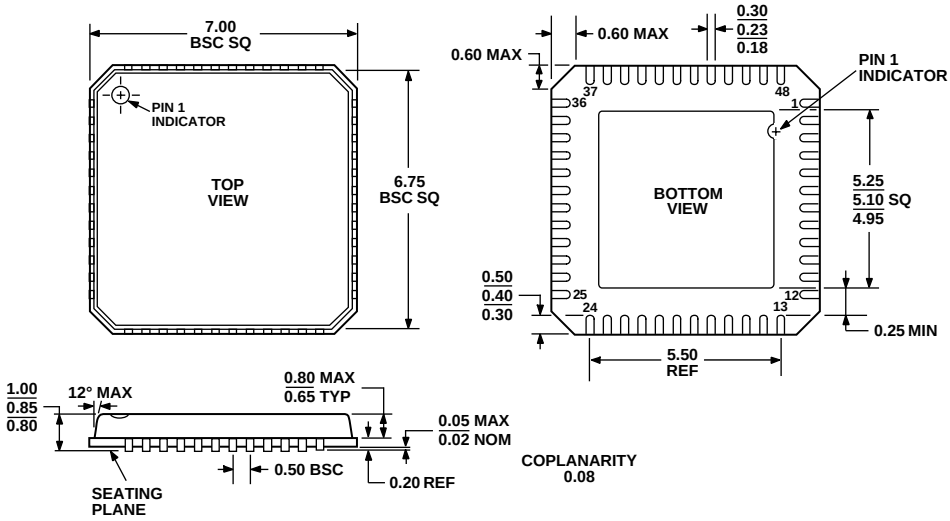

Figure 14. 48-Lead Lead Frame Chip Scale Package [LFCSP]
(CP-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADSYS8401JPCZ[1]	0°C to 85°C	Lead Frame Chip Scale Package	CP-48

[1] Z = Pb-free part.

NOTES

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