Programmable Dual-Axis Inclinometer/Accelerometer

Preliminary Technical Data

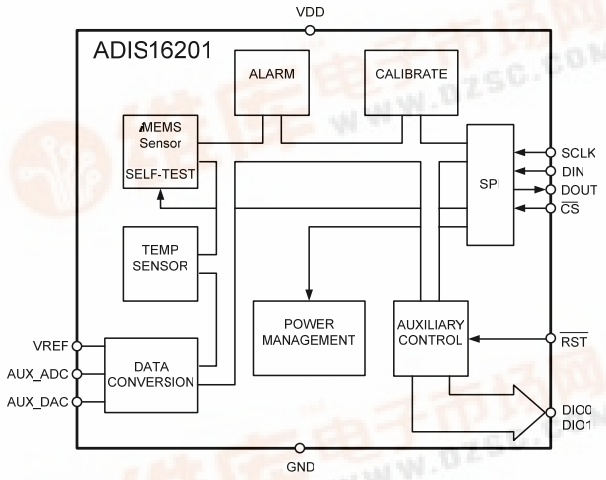
ADIS16201

FEATURES

Dual-axis inclinometer/accelerometer measurements
12/14-bit digital inclination/acceleration sensor outputs
±1.7 *g* accelerometer measurement range
±90° inclinometer measurement range
12-bit digital temperature sensor output
Digitally controlled sensitivity and bias calibration
Digitally controlled sample rate
Digitally controlled frequency response
Dual alarm settings with rate/threshold limits
Auxiliary digital I/O
Digitally activated self-test
Digitally activated low power mode
SPI® compatible serial interface
Auxiliary 12 bit ADC input and DAC output
Single-supply operation – 3.0 to 3.6V
3500 *g* powered shock survivability

APPLICATIONS

Platform stabilization and leveling
Tilt Sensing, Inclinometers
Motion / Position measurement
Monitor/Alarm Devices (Security, Medical, Safety)



FUNCTIONAL BLOCK DIAGRAM

GENERAL DESCRIPTION

The ADIS16201 is a complete, dual-axis acceleration and inclination angle measurement system available in a single compact package enabled by ADI's *i*Sensor™ integration. By enhancing ADI's *i*MEMS® sensor technology with an embedded signal processing solution, the ADIS16201 provides factory calibrated and tunable digital sensor data in a convenient format that can be accessed using a simple SPI serial interface. The SPI interface provides access to measurements of the following parameters: dual-axis linear acceleration, dual-axis linear inclination angle, temperature, power supply and one auxiliary analog input. Easy access to calibrated digital sensor data provides developers with a system-ready device, reducing development time, cost and program risk.

Unique characteristics of the end system can be easily accommodated via several built-in features, including an auto-zero recalibration via a single register command, as well as configurable sample rate and frequency response.

The ADIS16201 also offers a comprehensive set of features which can be used to further reduce the hardware complexity of system designs. These integrated features include a configurable alarm function, auxiliary 12-bit ADC, auxiliary 12-bit DAC, configurable digital I/O port, and a digital self test function. The ADIS16201 offers two different power management features that can be enabled via the SPI port: a programmable duty cycle sleep mode for systems that do not require continuous operation and a low power mode for systems that can trade reduced sample rates for more efficient power operation.

The ADIS16201 is available in a 9.2mm x 9.2mm x 4mm laminate based Land Grid Array (LGA) package with a temperature range of -40°C to +125°C.

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REVISION HISTORY

5/05—Revision PrA

10/05 —Revision PrB

SPECIFICATIONS

T_A = −40°C to 125°C, V_{DD} = 3.3 V, tilt = 0°, unless otherwise noted.

Table 1

Parameter	Conditions	Min	Typ	Max	Unit
INCLINOMETER	Each axis				
Input Range	Operable to ~±90 degree		±70		degree
Accuracy	0° to +30° , 25°C, max filter		±0.25		degree
	±30° to ±60° , 25°C, max filter		±0.50		degree
Initial Sensitivity	@ 25°C	TBD	10	TBD	LSB/degree
Sensitivity Over Temperature			40		ppm/°C
Initial Bias	@ 25°C	TBD	2048	TBD	LSB
Bias Over Temperature			40		ppm/°C
ACCELEROMETER	Each axis				
Input Range[1]	@25°C	±1.7			g
Nonlinearity[1]	% of full scale		±0.5	±2.5	%
Alignment Error	X sensor to Y sensor		±0.1		degree
Cross Axis Sensitivity[1]			±2	±5	%
Initial Sensitivity	@25°C	TBD	2.16	TBD	LSB/mg
Sensitivity Over Temperature			40		ppm/°C
Initial Bias	@25°C	TBD	8192	TBD	LSB
Bias Over Temperature			50		ppm/°C
ACCELEROMETER NOISE PERFORMANCE					
Output Noise	@25°C, no averaging		21.5		LSB rms
Noise Density	@25°C, no averaging		0.36		LSB/√Hz rms
ACCELEROMETER FREQUENCY RESPONSE					
Sensor Bandwidth			2250		Hz
Sensor Resonant Frequency			5.5		kHz
ACCELEROMETER SELF-TEST STATE[2]					
Output Change When Active		372	708	1040	LSB
TEMPERATURE SENSOR					
Output at 25°C			1278		LSB
Scale Factor			−2.129		LSB/°C
ADC Input					
Resolution			12		Bits
Integral Non-Linearity			±0.5		LSB
Differential Non-Linearity			±0.5		LSB
Offset Error			±1		LSB
Gain Error			±1		LSB
Input Range		0		2.5	Volts
Input Capacitance	During acquisition		20		pF

Parameter	Conditions	Min	Typ	Max	Unit
DAC OUTPUT	5 kΩ//100 pF to GND				
Resolution			12		Bit
Relative Accuracy	For Codes 101 to 3994		2		LSB
Differential Nonlinearity			1		LSB
Offset Error			5		mV
Gain Error			0.5		%
Output Range			0 to 2.5		V
Output Impedance			10		Ω
Output Settling Time			10		µs
LOGIC INPUTS					
Input High Voltage, V_{INH}		2.0			V
Input Low Voltage, V_{INL}				0.4	V
Input Current, I_{IN}			1	10	µA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS					
Output High Voltage (V_{OH})	I_{SOURCE} = 1.6 mA	VDD – 0.4			V
Output Low Voltage (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Sleep TIMER					
Timeout Period[3]		0.5		128	sec
FLASH MEMORY					
Endurance[4]		20,000			Cycles
Data Retention[5]	T_J = 55°C	20			Years
CONVERSION RATE					
Minimum Conversion Time			153		us
Maximum Conversion Time			605		ms
MaximumThroughput Rate			6554		SPS
Minimum Throughput Rate			1.65		SPS
POWER SUPPLY					
Operating Voltage Range VDD		3.0	3.3	3.6	V
Power Supply Current Normal Operation	Conversion time ≥ 1.0ms		12	TBD	mA
Power Supply Current High Performance Mode	Conversion time <1.0ms		38	TBD	mA
Power Supply Current Sleep Mode			500	TBD	µA
Turn-On Time			275		ms

[1] Guaranteed by *i*MEMs packaged part testing.

[2] Self-test response changes as the square of VDD.

[3] Guaranteed by Design.

[4] Endurance is qualified as per JEDEC Std. 22 Method A117 and measured at -40°C, +25°C, +85°C and +125°C.

[5] Retention lifetime equivalent at junction temperature (Tj) 55°C as per JEDEC Std. 22 Method A117. Retention lifetime will derate with junction temperature.

TIMING SPECIFICATIONS

T_A = −40°C to 125°C, V_{DD} = 3.3 V, tilt = 0°, unless otherwise noted.

Table 2

Parameter	Description	Min[1]	Typ	Max	Unit
f_{SCLK}		0.01		3.48	MHz
$t_{DATARATE}$	Chip Select Period, Higher Performance Mode	60			µs
$t_{DATARATE}$	Chip Select Period, Power Efficient Mode	100			µs
t_{cs}	Chip Select to Clock Edge	48.8			ns
t_{SL}	SCLK Low Pulse Width		TBD		ns
t_{SH}	SCLK High Pulse Width		TBD		ns
t_{DAV}	Data Output Valid after SCLK Edge			25	ns
t_{DSU}	Data Input Setup Time Before SCLK Rising Edge	24.4			ns
t_{DHD}	Data Input Hold Time After SCLK Rising Edge	48.8			ns
t_{DF}	Data Output Fall Time		5	12.5	ns min
t_{DR}	Data Output Rise Time		5	12.5	ns min
t_{SR}	SCLK Rise Time		5	12.5	ns min
t_{SF}	SCLK Fall Time		5	12.5	ns max
t_{SFS}	/CS High after SCLK Edge	0			us typ

[1] Guaranteed by design. Typical specifications are not tested or guaranteed.

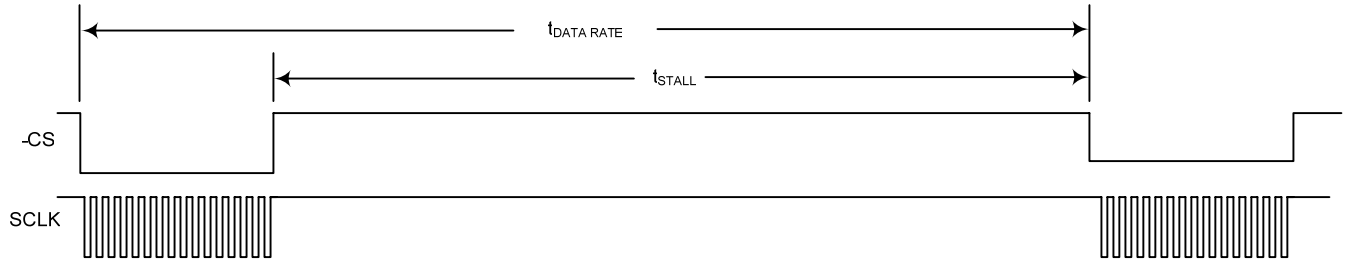

Figure 1 - SPI CHIP SELECT TIMING

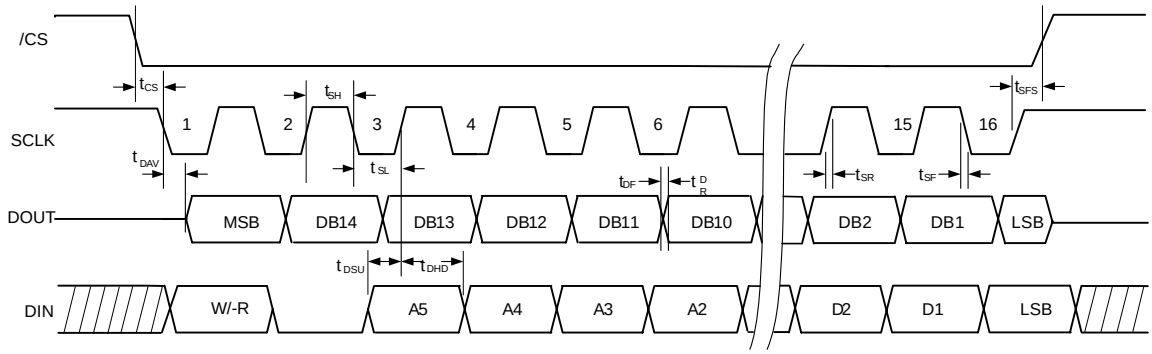

Figure 2 - SPI TIMING

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Acceleration (Any Axis, Unpowered)	3500 *g*
Acceleration (Any Axis, Powered)	3500 *g*
VDD to COM	–0.3 V to +7.0 V
Digital Input/Output Voltage to COM	–0.3 V to +5.5 V
Analog Inputs to COM	–0.3 to VDD + 0.3 V
Analog Inputs to COM	–0.3 to VDD + 0.3 V
Operating Temperature Range	–40°C to +125°C
Storage Temperature	–65°C to +150°C

Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

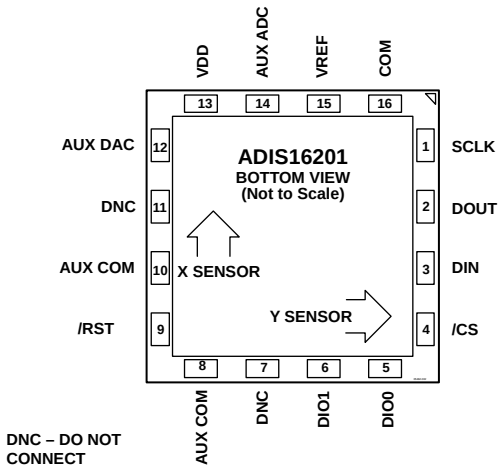

Figure 3 - Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
13	VDD	S	+3.3 V Power Supply.
16	COM	S	Common. Reference point for all circuitry in the ADIS16201.
12	AUX DAC	O	Auxiliary DAC Analog Voltage Output.
14	AUX ADC	I	Auxiliary ADC Analog Input Voltage.
15	VREF	O	Precision Reference Output.
1	SCLK	I	Serial Clock. SCLK provides the serial clock for accessing data from the part and writing serial data to the control registers.
3	DIN	I	Data In. Data to be written to the control registers is provided on this input and is clocked in on the rising edge of the SCLK.
2	DOUT	O	Data Out. The data on this pin represents data being read from the control registers and is clocked on the falling edge of the SCLK.
4	$\overline{CS}$	I	Chip Select. Active low. This input frames the serial data transfer.
9	$\overline{RST}$	I	Reset. Active low. This input resets the embedded microcontroller to a known state.
5, 6	DIO0–DIO1	I/O	Multifunction Digital I/O pin.
7, 11	DNC	NA	Do Not Connect.
8, 10	AUX COM	S	Auxiliary Grounds. Connected to GND for proper operation.

THEORY OF OPERATION

The ADIS16201 is a complete dual-axis digital inclinometer/accelerometer that uses Analog Devices' surface-micromachining process and embedded signal processing to make a functionally complete and low cost dual axis sensor.

The ADIS16201 is based upon a dual–axis micro-machined sensor element that develops independent analog signals representative of the acceleration levels applied to the part. The acceleration signals, along with the power supply voltage, an internal temperature signal and the auxiliary analog input signal are all sampled sequentially by an on-board precision ADC. These five signals are then processed and latched into output registers accessible to the user via the SPI.

In addition, the acceleration signals are further processed to produce inclination angle data for both axes. The inclination angle data represents the tilt away from the "ideal" plane that is normal to the earth's gravitational force. This calculation assumes that no force outside of the earth's gravitational force is acting on the device.

ACCELEROMETER OPERATION

The acceleration sensor used in the ADIS16201 is a surface-machined, polysilicon structure built on top of a silicon wafer. Polysilicon springs suspend the structure over the surface of the wafer and provide a resistance against acceleration forces. Deflection of the structure is measured using a differential capacitor that consists of independent fixed plates and plates attached to the moving mass. The fixed plates are driven by a set of square waves that are 180° out-of-phase from one another. Acceleration will deflect the beam and unbalance the differential capacitor, resulting in an output square wave whose amplitude is proportional to acceleration. Phase sensitive demodulation techniques are then used to rectify the signal and determine the direction of the acceleration. The output of the demodulator is amplified, digitized, and further processed within the digital domain to remove any process variations and sensitivities to supply variations.

INCLINOMETER OPERATION

The ADIS16201 inclination angle output data is linear with respect to degrees of inclination. As the tilt angle increases, the accelerometer sensitivity reduces and eventually hits zero at the boundary condition of 90° inclination angle. In fact, this behavior can be described by using a simple sinusoidal function. This can be seen in Figure 4(a) where both the ideal inclination and acceleration output data are plotted over a span of 0° to +90° inclination. A closer examination of the plots within Figure 4(b) reveals an increase in quantization error as the inclination approaches +90°.

Since the inclination output is developed using a linear approximation of the acceleration data, the quantization error observed within the inclination output will grow as the inclination angle approaches 90°. It is suggested that the user limit the usable full scale range of the inclination outputs based upon the resolution required of the end target. Figure 5 provides a convenient guideline for use in determining the appropriate dynamic range vs. accuracy trade-off in each system design. The quantization error behavior described is symmetrical about the 0° point and should be applied equally to both positive and negative inclination angles

TEMPERATURE SENSOR

The TEMP_OUT control register allows the end user to monitor the internal temperature of the ADIS16201 to an accuracy of +/- 3°C. The output data is presented in a straight binary format with a nominal 25°C die temperature correlating to 1278 LSB read through the TEMP_OUT output data register. The sensitivity of -2.13LSB/°C allows for a resolution of less than 0.5°C in the temperature reading within the output data register.

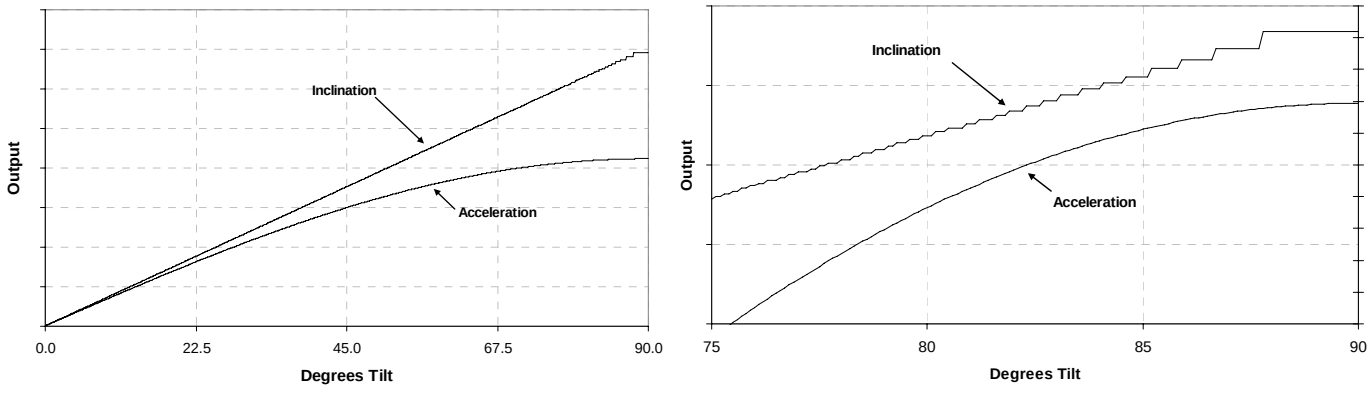

Figure 4 – Acceleration and Inclination Angle Behavior versus Tilt Angle

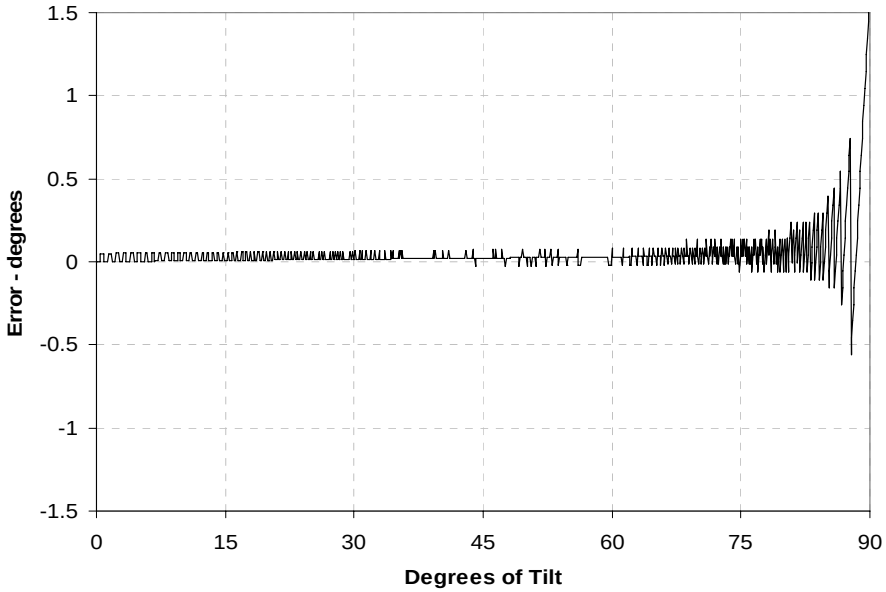

Figure 5 – Inclination Quantization Error

BASIC OPERATION

The ADIS16201 was designed for simple integration into industrial system designs, requiring only two things for acquisition of calibrated sensor data: a +3.3V power supply and a 4-wire, industry standard serial peripheral interface (SPI). All of the input/output functions on the ADIS16201 are facilitated by registers which can be accessed using the SPI interface. Each of these registers have been assigned a unique address and data format that has been tailored for their specific function.The SPI port operates in a full duplex mode; data is clocked out of the DOUT pin at the same time command/address data is being clocked in through the DIN pin. For more information on basic SPI port operation, see the Applications Section.

DATA OUTPUT REGISTER ACCESS

For the most basic operation of the ADIS16201, output data registers require only read commands for accessing calibrated sensor data, along with the temperature, power supply and auxiliary analog input channel data. Each read command requires two full 16-bit cycles. The first cycle is for transmitting the register address, and the second cycle is for reading of the data.

Table 5 displays these two cycles and their appropriate bit maps. The appropriate sequencing for each SPI signal (CS, SLCK, DIN and DOUT) during a read command can be found in Figure 6.

The data output register configuration is broken down into three different functions: new data ready bit (ND), alarm indicator (EA) and data bits (D0-D13). The ND bit is used to determine if a particular register has been updated since the last read command. As each register is updated, the data ready bit, referred to as ND in Table 5, is set to a "1" logic level. When a register is read, this bit is set to a "0" logic level. The alarm function provides users with a simple method for checking conditions and can be used to simplify system-level processing requirements.

The two acceleration output data registers are 14-bits in length and are formatted as two's complement binary numbers. The rest of the data output registers are 12 bits in length, leaving D12 and D13 as "don't care" bits. The output format for each of these registers, along with their addresses, can be found in Table 6. Each register function has two different addresses. The first address is for the upper byte, which contains the most significant bits (D8-D13), ND and EA data. The second address is for the lower byte, which contains the 8 least significant bits (D0-D7).

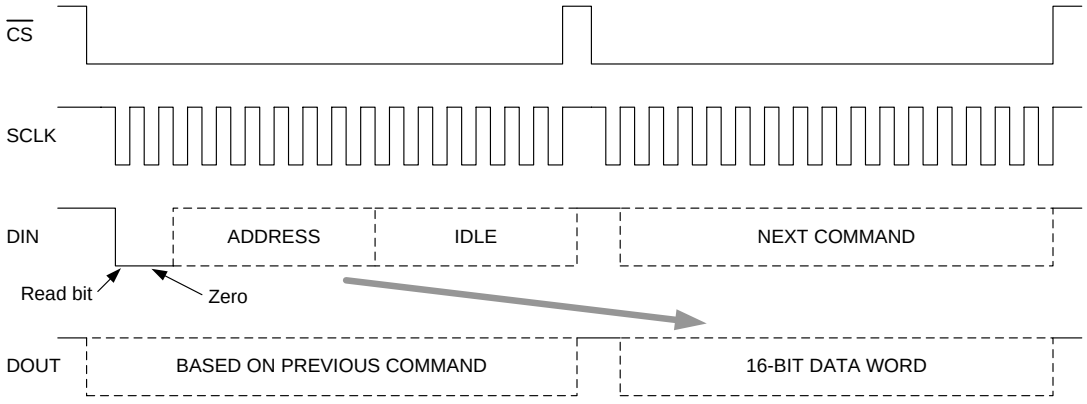

Figure 6 – Data Output Register Read Command Sequence

Table 5 – Data Output Register Read Command Bit Map

DIN	W/R	0	A5	A4	A3	A2	A1	A0	x	x	x	x	x	x	x	x

DOUT	ND	EA	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	Upper Byte								Lower Byte							

Table 6 – Data Output Register Information

Name	Function	Addresses	Resolution (bits)	Data Format	Scale Factor (per LSB)	Output Code Examples
SUPPLY_OUT	Power Supply Data	03h, 02h	12	Binary	1.22mV	3.3V = 2703 LSB 0V = 0 LSB
XACCL_OUT	X-Axis Acceleration Data	05h, 04h	14	2's Compliment	0.462mg	±1g = 8192 ± 2162 LSB 0g = 8192 LSB
YACCL_OUT	Y-Axis Acceleration Data	07h, 06h	14	2's Compliment	0.462mg	±1g = 8192 ± 2162 LSB 0g = 8192 LSB
AUX_ADC	Auxiliary Analog Input Data	09h, 08h	12	Binary	0.61mV	2.5V = 4095 LSB 0V = 0 LSB
TEMP_OUT	Sensor Temperature Data	0Bh, 0Ah	12	Binary	-0.47°C	0°C = 1331 LSB 25°C = 1278 LSB
XINCL_OUT	X-Axis Inclination Data	0Dh, 0Ch	12	2's Compliment	0.1°	±90° = 2048 ±900 LSB 0° = 2048 LSB
YINCL_OUT	Y-Axis Inclination Data	0Fh, 0Eh	12	2's Compliment	0.1°	±90° = 2048 ±900 LSB 0° = 2048 LSB

PROGRAMMING AND CONTROL

CONTROL REGISTER OVERVIEW

The previous section described the most basic operation of the ADIS16201. For added system flexibility and programmability, the following sections describe additional Control of the ADIS16201 sensor, as provided for through the use of twenty eight digital control registers accessible via the SPI interface. A high level listing of these registers is given within Table 7. The functionality of each of these control registers is expanded upon in the following sections, providing for the full clarification of each of the control registers behavior. Available control modes for the device include selectable sample rates for the reading of the seven output vectors, selectable data averaging at the output registers, alarm settings, control of the on-board 12 bit auxiliary DAC, handling of the two general purpose I/O lines, facilitating of the sleep mode, enabling the self-test mode, as well as other miscellaneous control functions.

The conversion process is continually repeated, providing for the continuous update of the seven output registers. DATA READY flag bits common to all seven output registers allow the completion of the conversion process to be tracked via the SPI. As an alternative, the digital I/O lines can be configured through software control to create a DATA READY hardware function which in turn can signal the completion of the conversion process.

Dual alarms function are provided for within the ADIS16201 sensor with either of the alarms being able to monitor any one of the seven output registers independent of the other alarm. The alarms can be configured to monitor for excursions above or below fixed thresholds or for rates of change beyond predefined limits. The alarm conditions can be actively monitored through the SPI. In addition, the user can configure the digital I/O lines through software control to create an ALARM function that allows for monitoring of the alarm conditions through hardware.

The seven output signals noted above are all independently calibrated at the factory providing for a high degree of accuracy. In addition, the user has access to independent OFFSET and SCALE factors for each the two acceleration output vectors and the two inclination output vectors. This allows independent modification of any one or all of these four registers on an automatic basis prior to the values being read via the SPI. In turn, field level calibrations can be implemented within the sensor itself through the use of these OFFSET and SCALE variables. System level commands provided for within the sensor include the automatic zeroing of the four outputs through the use of a single NULL command via the SPI. In addition, the original factory calibration settings can be recovered at any point through the use of a simple factory reset command.

CONTROL REGISTER ACCESS

The control registers within the ADIS16201 are based upon a 16 bit / 2 byte format, and are accessed via the SPI. The SPI operates in full duplex mode with the data clocked out of the Data Out pin at the same time data is being clocked in through the Data In pin. All commands written to the ASIS16201 can be categorized as either Write commands or Read commands. All Write commands are self contained and take place within a single cycle; each Read command requires two cycles to complete. The first cycle is for transmitting the register address, and the second cycle is for reading of the data. During this second cycle, within which the Data Out line becomes active, the Data In line can be used to receive the next sequential command. This allows for the 'overlapping' of the commands. For more information on basic SPI port operation, see the Applications Section.

The READ and WRITE commands are identifiable through the Most Significant Bit (MSB), B15, of the received data. A "1" written to B15 indicates a Write command while a "0" indicates a Read command. Bits B13 through B8 contain the address of the control register that is being written to or read from. The remaining 8 bits of the Write command contain the data that is being written into the part whereas the remaining 8 bits of the Read command contain 'don't care' levels. Given that the data within the Write command is 8 bits in length, the 8 bit data format is the default byte size. A Write command operates on a single cycle as defined by the chip select, and shown in Figure 7. The Read command operates on a 2 chip select cycle basis as seen in the previous section, Figure 6. The 6 bit address range allows for the addressing of the full 64 byte address space on a byte-wise basis as detailed in Table 5, 6, 7 and 8. Data written into the device is performed on a byte-wise basis with the address of each byte being explicitly called out in the write command. Conversely, data being read from the device consists of two back-to-back 8 byte variables being sent out with the first byte out corresponding to the upper address (odd number address) and the second byte relating to the next lower address space (even number address). For example, a data read of address 03h would result in the data from address 03h being fed out followed by data from address 02h. Likewise, a data read of address 02h will result in the same data stream being output from the device

The ADIS16201 is a FLASH based device with the non-volatile functional registers implemented as FLASH registers. The

endurance limitation of 20,000 writes should be taken into account when considering the implementation of the device into the end target. The "Non-Volatile" column called out within Table 7 is helpful in discerning which control register writes must be counted against the Endurance limit, along with the expected update rate. When writing to a non-volatile register, the user needs to assure that the power supply remains within limits for a minimum of 200 msec after the write is initiated. This will assure a successful write of the non-volatile data.

Table 7. Control Regsiter Mapping

Register Name	Type	Non-Volatile	Address	Bytes	Function
			00h-01h	2	Reserved
SUPPLY_OUT	R		02h	2	Power Supply output data.
XACCL_OUT	R		04h	2	X-Axis Acceleration output data.
YACCL_OUT	R		06h	2	Y-Axis Acceleration output data.
AUX_ADC	R		08h	2	Auxiliary ADC Data
TEMP_OUT	R		0Ah	2	Temperature output data
XINCL_OUT	R		0Ch	2	X-Axis Inclination output data.
YINCL_OUT	R		0Eh	2	Y-Axis Inclination output data.
XACCL_ OFF	R/W	X	10h	2	X-Axis Acceleration Null Factor.
YACCL_ OFF	R/W	X	12h	2	Y-Axis Acceleration Null Factor.
XACCL_ SCALE	R/W	X	14h	2	X-Axis Acceleration Scale Factor.
YACCL_ SCALE	R/W	X	16h	2	Y-Axis Acceleration Scale Factor.
XINCL_OFF	R/W	X	18h	2	X-Axis Inclination Null Factor.
YINCL_ OFF	R/W	X	1Ah	2	Y-Axis Inclination Null Factor.
XINCL_SCALE	R/W	X	1Ch	2	X-Axis Inclination Scale Factor.
YINCL_ SCALE	R/W	X	1Eh	2	Y-Axis Inclination Scale Factor.
ALM_MAG1	R/W	X	20h	2	Alarm 1 Amplitude Threshold.
ALM_MAG2	R/W	X	22h	2	Alarm 2 Amplitude Threshold.
ALM_SMPL1	R/W	X	24h	2	Alarm 1 Sample Period.
ALM_SMPL2	R/W	X	26h	2	Alarm 2 Sample Period.
ALM_CTRL	R/W	X	28h	2	Alarm Source Control Register
			2Ah-2Fh	6	Reserved
AUX_DAC	R/W		30h	2	Auxiliary DAC Data.
GPIO_CTRL	R/W		32h	2	Auxiliary Digital I/O Control Register.
MSC_CTRL	R/W		34h	2	Miscellaneous Control Register.
SMPL_PRD	R/W	X	36h	2	ADC Sample Period Control.
AVG_CNT	R/W	X	38h	2	Defines number of samples used by moving average filter.
PWR_MDE	R/W		3Ah	2	Counter used to determine length of Power-Down mode.
STATUS	R		3Ch	2	System Status Register.
COMMAND	W		3Eh	2	System Command Register.

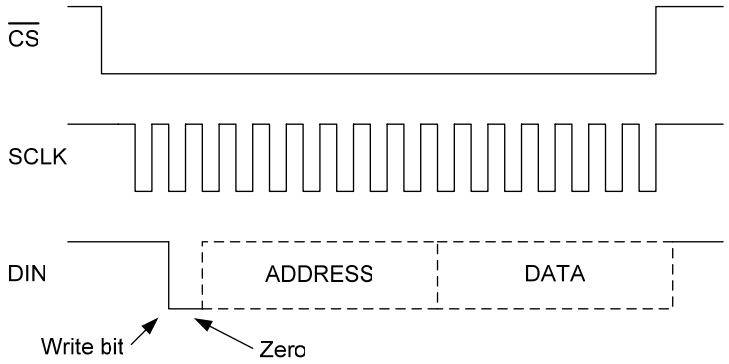

Figure 7 – Control Register Write Command Sequence of SPI Signals

Table 8 – Data Output Register Write Command Bit Map

DIN	W/R	0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
	Upper Byte								Lower Byte							

CONTROL REGISTER DETAILS

CALIBRATION

The ADIS16201 outputs are pre-calibrated at the factory, providing a high degree of accuracy and simpler system implementation. In addition, for system or field updates, the device has eight control registers associated with calibration updates of the acceleration and inclination output data, as defined in Table 9 below. Each of the registers has a read/write capability and is 16 bits/2bytes in length. All calibration registers contain 12 bit data with the exception of the Inclination Offset registers which contain 9 bit data. All data values are aligned to the LSB. The OFFSET registers all utilize the 2's complement format allowing for both positive and negative offsets. All SCALE registers utilize the straight binary format.

The data within these eight calibration registers is utilized in offsetting and scaling of the output data registers according to:

$$Output = A * (x + C)$$

where x represents the raw data prior to calibration, C is the offset, A is the scalar, and *Output* represents the Output Data register where the resultant data is stored. Each of the X and Y axis acceleration output data registers as well as the X and Y axis inclination output data registers is associated with an independent OFFSET and SCALE register for a total of four OFFSET registers and a total of four SCALE registers.

One of the primary functions of the various OFFSET and SCALE registers is to allow for the field level calibration of the ADIS16201 sensor. In particular, the OFFSET control registers allow the end user to reset to 0deg / 0mg reference point for the device. This is particularly important when considering the stack up of the tolerances in mounting the ADIS16201 to a Printed Circuit Board (PCB), the PCB to an enclosure, the enclosure mounted to the chassis of a piece of equipment, etc…. The end result is that the ADIS16201 mechanical reference may be offset several degrees from that of the end equipment mechanical reference resulting in serious offsets in the inclination and acceleration data output registers. Loading of the OFFSET registers with correction data can eliminate such errors.

A global command has been implemented within the ADIS16201 to simplify the loading of the OFFSETs. Once the end piece of equipment is leveled to its desired reference point a NULL command can be sent to the ADIS16201 via the COMMAND control register which will zero the two acceleration and the two inclination output data registers through the automatic loading of the four OFFSET registers with the inverse of the data presently located within the corresponding four output data registers (within range limits). Consequently, on the next reading of the seven output data registers the two acceleration and two inclination output data registers should be reset to mid-scale (neglecting noise and repeatability limitations). It is suggested that when the NULL command is to be implemented that the AVG_CNT control register be set to 08h in order to maximize the filtering and reduce the effects of noise in determining the values to be loaded into the OFFSET control registers. Then again, the user may prefer to manually load each of the eight calibration registers via the SPI in order to calibrate the end system. This could be applicable when it is planned to adjust the SCALE factors thus requiring an external stimulus to excite the ADIS16201.

Table 9. Calibration Register Definitions

XACCL_OFF

	MSB							LSB
(11h)	X	X	x	x	XANB	XANA	XAN9	XAN8
(10h)	XAN7	XAN6	XAN5	XAN4	XAN3	XAN2	XAN1	XAN0

XANB-XAN0	Offset factor for X-Axis Acceleration Output. A 12 bit two's complement format number added directly to data prior to Scale Factor multiplication. **The register is set to 0 upon initial power-up** resulting in an effective zero offset. Offset factor can be varied from -2048 to +2047. Resolution equals 0.462mg/LSB for a maximum offset of +/-0.945g assuming the use of a nominal SCALE factor. Last written value is non-volatile allowing for data recovery upon reset. Read/Write capability.

YACCL_OFF

	MSB							LSB
(13h)	X	X	x	x	YANB	YANA	YAN9	YAN8
(12h)	YAN7	YAN6	YAN5	YAN4	YAN3	YAN2	YAN1	YAN0

YANB-YAN0o	Offset factor for Y-Axis Acceleration Output. A 12 bit two's complement format number added directly to data prior to Scale Factor multiplication. **The register is set to 0 upon initial power-up** resulting in an effective zero offset. Offset factor can be varied from -2048 to +2047. Resolution equals 0.462mg/LSB for a maximum offset of +/-0.945g assuming the use of a nominal SCALE factor. Last written value is non-volatile allowing for data recovery upon reset. Read/Write capability.

XACCL_SCALE

MSB LSB

(15h)	x	x	x	x	XASB	XASA	XAS9	XAS8
(14h)	XAS7	XAS6	XAS5	XAS4	XAS3	XAS2	XAS1	XAS0

XASB-XAS0	Scale factor for X-Axis Acceleration Output. **The 12 bit register is set to 2048 upon initial power-up resulting in a unity gain scalar**. Can be varied from 0 to 4095 correlating to scale factor of 0 to 2 respectively with 0.05% resolution. Last written value is non-volatile allowing for data recovery upon reset. The full scale range limits will vary according to this scale factor. Read/Write capability.

YACCL_SCALE

MSB LSB

(17h)	x	x	x	x	YASB	YASA	YAS9	YAS8
(16h)	YAS7	YAS6	YAS5	YAS4	YAS3	YAS2	YAS1	YAS0

YASB-YAS0	Scale factor for Y-Axis Acceleration Output. **The 12 bit register is set to 2048 upon initial power-up resulting in a unity gain scalar**. Can be varied from 0 to 4095 correlating to scale factor of 0 to 2 respectively with 0.05% resolution. Last written value is non-volatile allowing for data recovery upon reset. The full scale range limits will vary according to this scale factor. Read/Write capability.

XINCL_OFF

MSB LSB

(19h)	x	x	x	x	x	X	X	XIN8
(18h)	XIN7	XIN6	XIN5	XIN4	XIN3	XIN2	XIN1	XIN0

XIN8-XIN0	Offset factor for X-Axis Inclination Output. A 9 bit two's complement format number added directly to data prior to Scale Factor multiplication. **The register is set to 0 upon initial power-up** resulting in an effective zero offset. Offset factor can be varied from -256 to +255. Resolution equals 0.1deg/LSB for a maximum offset of +/-25.5deg assuming the use of a nominal SCALE factor. Last written value is non-volatile allowing for data recovery upon reset. The full scale range limits of +/- 90.0deg for the output data register will be shifted according to this offset factor. Read/Write capability.

YINCL_OFF

MSB LSB

(1Bh)	x	x	x	x	x	X	X	YIN8
(1Ah)	YIN7	YIN6	YIN5	YIN4	YIN3	YIN2	YIN1	YIN0

YIN8- YIN0	Offset factor for Y-Axis Inclination Output. A 9 bit two's complement format number added directly to data prior to Scale Factor multiplication. **The register is set to 0 upon initial power-up** resulting in an effective zero offset. Offset factor can be varied from -256 to +255. Resolution equals 0.1deg/LSB for a maximum offset of +/-25.5deg assuming the use of a nominal SCALE factor. Last written value is non-volatile allowing for data recovery upon reset. The full scale range limits of +/- 90.0deg for the output data register will be shifted according to this offset factor. Read/Write capability.

XINCL_SCALE

MSB LSB

(1Dh)	x	x	x	x	XISB	XISA	XIS9	XIS8
(1Ch)	XIS7	XIS6	XIS5	XIS4	XIS3	XIS2	XIS1	XIS0

XISB-XIS0	Scale factor for X-Axis Inclination Output. **The 12 bit register is set to 2048 upon initial power-up resulting in a unity gain scalar**. Can be varied from 0 to 4095 correlating to scale factor of 0 to 2 respectively with 0.05% resolution. Last written value is non-volatile allowing for data recovery upon reset. The full scale range limits will vary according to this scale factor. Read/Write capability.

YINCL_SCALE

MSB LSB

(1Fh)	x	x	x	x	YISB	YISA	YIS9	YIS8
(1Eh)	YIS7	YIS6	YIS5	YIS4	YIS3	YIS2	YIS1	YIS0

YISB-YIS0	Scale factor for Y-Axis Inclination Output. **The 12 bit register is set to 2048 upon initial power-up resulting in a unity gain scalar**. Can be varied from 0 to 4095 correlating to scale factor of 0 to 2 respectively with 0.05% resolution. Last written value is non-volatile allowing for data recovery upon reset. The full scale range limits

	will vary according to this scale factor. Read/Write capability.

ALARM PROGRAMMING

The ADIS16201 contains two independent alarm functions which are referred to as Alarm1 and Alarm 2. The control registers relating to these two alarm functions are defined in Table 10 below. The Alarm 1 function is managed by the ALM_MAG1 and ALM_SMPL1 control registers, and the Alarm 2 function is managed by the ALM_MAG2 and ALM_SMPL2 control registers. Both the Alarm 1 and Alarm 2 functions share the ALM_CNTRL register. The discussion that follows references the Alarm 1 functionality only, for simplicity.

The 16 bit ALM_CNTRL register serves three distinct roles in controlling the Alarm 1 function. First it is used to enable the overall Alarm 1 function and select the output data variable that is to be monitored for the alarm condition. Second it is used to select whether the Alarm 1 function is to based upon a predefined Threshold (THR) level or a predefined Rate-Of-Change (ROC) slope. Last the ALM_CNTRL register can be used in setting up one of the two General Purpose Input/Output lines (GPIO) to serve as a hardware output that indicates when an alarm condition has occurred. The enabling of the alarm hardware function as well as the control of the actual I/O line to place the alarm function on as well as the polarity of the active alarm signal is controlled through this register. Note the hardware output indicator when enabled serves both the Alarm 1 and Alarm 2 functions and cannot be used to differentiate between one alarm condition or the other. It is simply used to indicate that an alarm is active and that the user should poll the device via the SPI to discern which alarm is the source of the alarm condition (see STATUS control register definition).

With the ALM_CTRL, MSC_CTRL and GPIO_CTRL control registers all being able to influence the same GPIO pins a priority level must be established for conflicting assignments of the two GPIO pins. This priority level is defined as: MSC_CTRL has precedence over ALM_CTRL which has precedence over GPIO_CTRL.

The ALM_MAG1 control register used in controlling the Alarm 1 function has two roles. The first is to store the value with which the output data variable will be compared against to discern if an alarm condition exists or not. The second is to identify whether the alarm should be active for excursions above or below the alarm limit. For a "1" in the GT1 bit of the ALM_MAG1 control register the alarm will be active for excursions extending above a given limit. For a "0" in the GT1 bit the alarm will be active for excursions dropping below the given limit. The comparison value contained within the ALM_MAG1 control register is located within the lower 14 bits. The format utilized for this 14 bit value should match that of the output data register that is being monitored for the alarm condition. For instance, if the YINCL_OUT output data register is being monitored by Alarm 1 then the 14 bit value within the ALM_MAG1 control register will take on a 2's complement format with each LSB equating to nominal 0.1deg (assumes unity SCALE and zero OFFSET factors). The ALM_MAG value is compared against the instantaneous value of the parameter being monitored and not the filtered output data.

When the THR function is enabled the output data variable is compared against the ALM_MAG1 level in a one for one manner. When the ROC function is enabled the comparison of the output data variable is against the ALM_MAG1 level averaged over the number of samples as identified in the ALM_SMPL1 control register. This acts to create a comparison of (Δ units / Δ time) or the derivative of the output data variable against a predefined slope.

The versatility built into the alarm function is intended to allow for an end user to adapt to any one of a number of different applications. For example, in the case of monitoring a 2's complement variable the 'GT1' bit within the ALM_MAG1 control register can allow for the detection of negative excursions below a fixed level. In addition, the Alarm 1 and the Alarm 2 functions can be set to monitor the same variable which allows for the end user to discern if an output variable remains within a predefined window. Other options include the ROC function which can be used in the monitoring of high frequency shock levels in the acceleration outputs or slowly changing outputs in the inclination level over a period of a minute or more. With the addition of the alarm hardware functionality the ADIS16201 can be left to run independently of the main processor and only interrupt the system when an alarm condition occurs. Conversely, the alarm condition can be monitored through the routine polling of any one of the seven data output registers

Table 10. ALARM Register Definitions

ALM_MAG1

(21h)
(20h)

MSB LSB

GT1	X	M1D	M1C	M1B	M1A	M19	M18
M17	M16	M15	M14	M13	M12	M11	M10

Alarm Magnitude 1 register is non-volatile. **Reset to 0 @ initial power-up**. Read/Write capability.	
BIT	DESCRIPTION
GT1	"Greater Than" active alarm bit; 1 – Alarm active for output 'Greater Than' Alarm Magnitude 1 register setting. 0 – Alarm active for output 'Less Than' Alarm Magnitude 1 register setting.
M1D – M10	Alarm 1 Magnitude Threshold. 14 Bits are provided for the setting of the threshold. The number can be either straight binary or 2's complement depending upon the format of the output variable that the alarm threshold is being compared against.

ALM_MAG2

(23h)
(22h)

MSB LSB

GT2	x	M2D	M2C	M2B	M2A	M29	M28
M27	M26	M25	M24	M23	M22	M21	M20

Alarm Magnitude 2 register is non-volatile. **Reset to 0 @ initial power-up**. Read/Write capability.	
BIT	DESCRIPTION
GT2	"Greater Than" active alarm bit; 1 – Alarm active for output 'Greater Than' Alarm Magnitude 2register setting. 0 – Alarm active for output 'Less Than' Alarm Magnitude 2 register setting.
M2D – M20	Alarm 2 Magnitude Threshold. 14 Bits are provided for the setting of the threshold. The number can be either straight binary or 2's complement depending upon the format of the output variable that the alarm threshold is being compared against.

ALM_SMPL1

(25h)
(24h)

MSB LSB

x	X	x	x	X	X	x	X
T17	T16	T15	T14	T13	T12	T11	T10

T17- T10	Alarm 1 Sample Period. This binary value represents the number of samples that an Output Variable is monitored over when performing Rate-of-Change alarm monitoring. The Rate-of-Change alarm function averages the change in the output variable over the specified number of samples and compares this change directly to the values specified in the Alarm Magnitude 1 register. Last written value is stored in non-volatile memory allowing for data recovery upon reset. **Reset to 0 @ initial power-up**. Read/Write capability.

ALM_SMPL2

(27h)
(26h)

MSB LSB

x	X	x	x	X	X	x	x
T27	T26	T25	T24	T23	T22	T21	T20

T27- T20	Alarm 2 Sample Period. This binary value represents the number of samples that an Output Variable is monitored over when performing Rate-of-Change alarm monitoring. The Rate-of-Change alarm function averages the change in the output variable over the specified number of samples and compares this change directly to the values specified in the Alarm Magnitude 2 register. Last written value is stored in non-volatile memory allowing for data recovery upon reset. **Reset to 0's @ initial power-up**. Read/Write capability.

ALM_CTRL

(29h)
(28h)

MSB LSB

ROC2	A2S_2	A2S_1	A2S_0	ROC1	A1S_2	A1S_1	A1S_0
x	X	x	x	X	AOE	AOP	AOL

Alarm Magnitude 1 register is non-volatile. **Reset to 0 @ initial power-up**. Read/Write capability.	
BIT	DESCRIPTION
ROC1, ROC2	Rate-of-Change (ROC) Enable for ALM1 and ALM2; 1 - ROC is active, 0 – Fixed Threshold is active.
A1S_2, A1S_1, A1S_0, or A2S_2, A2S_1, A2S_0	Alarm 1 and Alarm 2 Source Selects. Represents a 3 digit binary address enabling and selecting the output variable which is the source of the Alarm. 0,0,0 – Alarm Disabled 0,0,1 – Alarm Source: Power Supply Output Vector 0,1,0 – Alarm Source: X-Acceleration Output Vector 0,1,1 – Alarm Source: Y-Acceleration Output Vector 1,0,0 – Alarm Source: Auxiliary ADC Output Vector 1,0,1 – Alarm Source: Temperature Sensor Output Vector 1,1,0 – Alarm Source: X-Inclination Output Vector 1,1,1 – Alarm Source: Y-Inclination Output Vector
AOE	Alarm Output Enable; 1 – AO enabled, 0 - AO disabled
AOP	Alarm Output Polarity; 1 – active high, 0 – active low
AOL	Alarm Output Line Select; 1– DIO1, 0 – DIO0

SAMPLE PERIOD CONTROL

The seven output data variables within the ADIS16201 are sampled and updated at a rate based upon the SMPL_PRD control register. The sample period can be precisely controlled over more than a three decade range through the use of a time base with two settings and a 7 bit binary count. The use of a time base that varies with a ratio of 1:31 allows for a more optimum resolution in the sample period over the three and one half decade span in sample rate than a straight binary counter would allow for. This is reflected in Figure 8 where the frequency is presented on a logarithmic scale. The choice of the two setting time base acts to make the sample period setting a bit more linear versus the logarithmic frequency scale.

Note that the sample period given is defined as the cumulative time required to sample, process and update all seven data output variables. The seven data are sampled as a group and in unison with one another. Whatever update rate selected for one signal then all seven output data variables will updated at the same rate whether they are monitored via the SPI or not.

For a sample period setting of less than 1.224uS (SMPL_RATE <= 0x07), the overall power dissipation in the part rises by approximately 300% due to the faster sampling speed required of the ADC.

Table 11. Sample Period Control Register Definition

SMPL_ PRD

	MSB							LSB
(37h)	x	x	x	x	x	x	X	x
(36h)	TMBS	SP6	SP5	SP4	SP3	SP2	SP1	SP0

ADC Sample Period Control Register. The data within this register is non-volatile allowing for data recovery upon reset. **The initial value is set to '0Ah' upon initial power-up allowing for a sample period of 1.68mS.** Read/Write capability.	
TMBS	ADC Time Base Control. The MSB, TMBS, sets the time base of the acquisition system to 152.6uS when SR7 = 0 versus 4.73mS when SR7 = 1.
SP6-SP0	ADC Sample Period Count. The lower seven bits, SP6-SP0, represent a binary count which when added to one and then multiplied by the time base results in the combined sample period of the ADC ("Combined" sample period being the period required to sample and update all seven data outputs). The overall sample period can be varied from 152.6uSec to 19.53mS in 152.6uSec increments for TMBS=0 and from 4.73mS to 605mS in 4.73mS increments for TMBS=1. This equates to the sample rate varying from 4080SPS to 31.9SPS for TMBS=0 and from 131.6SPS to 1.028SPS for TMBS=1.

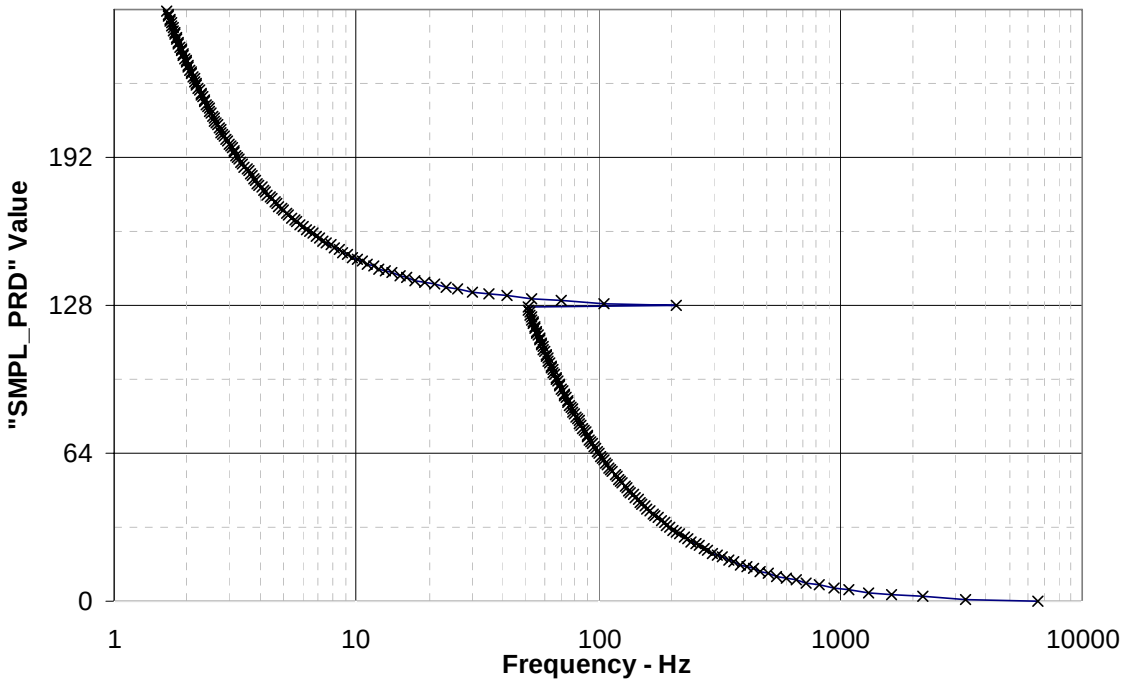

Figure 8. Sample Frequency versus "SMPL_PRD" Values

FILTERING CONTROL

The ADIS16201 has the ability to perform basic filtering on the seven output data variables through the AVG_CNT control register. The filtering performed is that of a low-pass moving average filter with the size of the data being averaged (number of filter taps) determined through the AVG_CNT control register. The filtering applied through the AVG_CNT control register is applied to all seven data output variables concurrently and thus one output variable cannot be filtered differently than another.

The number of taps (N) within the moving average filter is calculated as:

$$N = 2^{AVG\_CNT}$$

where *AVG_CNT* is shown as a decimal value. With AVG_CNT set to 00h N is reduced to 1 which effectively disables the moving average filter altogether. At the other extreme is when AVG_CNT is set to its maximum setting of 08h and N increases to 255 thus effectively reducing the apparent bandwidth by 255. Note that the contribution from each tap is set to 1/(N) thus allowing for unity gain in the filter response. The frequency response of the moving average filter is given as:

$$H(f) = \frac{\sin(\pi * N * f * t_s)}{N \sin(\pi * f * t_s)}$$

The more taps, the more zeros, thus the steeper the slope of the roll-off. Caution must be used with this filter mechanism since the amplitudes of the sideband peaks within the stopband are not reduced with an increasing number of taps thus potentially allowing for high-frequency components to leak through. Sample frequency response plots for the moving average filter utilizing various numbers of taps are detailed within Figure 9 below.

Table 12. Average Count Control Register Definition

AVG_CNT

	MSB							LSB
(39h)	x	x	x	X	X	x	x	X
(38h)	x	x	x	X	AC3	AC2	AC1	AC0

AC3-AC0	The Average Count Control Register. The binary value represented by AC3-AC0 is used to determine the number of output data samples (number of taps) that are averaged within the moving average filter. The

	binary data value represented by AC3-AC0 is limited to a value ranging from 0 to 8. **The register is set to all 0's upon initial power-up resulting in an effective disabling of the moving average filter.** Last written value is non-volatile allowing for data recovery upon reset. Read/Write capability.

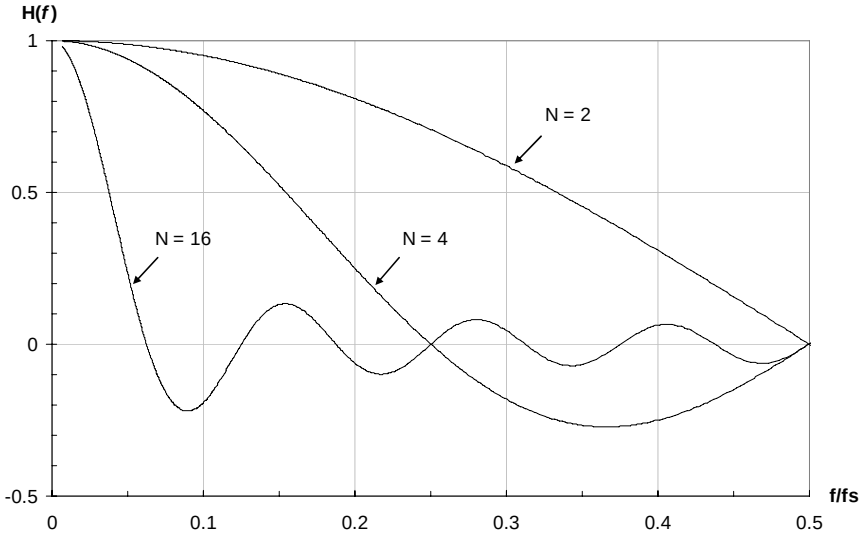

Figure 9. Sample Frequency Response versus Number of Taps

POWER-DOWN CONTROL

The ADIS16201 has the ability to be put into a power-down mode for varying amounts of time based upon the PWR_MDE control register. The amount of time specified by the PWR_MDE control register is equal to the binary count of the eight bit control word multiplied by 0.5 Sec. Thus for the binary count varying from 0 to 255 the power down period will be varied from 0 to 127.5 Sec. The PWR_MDE register is volatile and will be set to 0 upon both initial power up and subsequent wake-ups from the power down period. By setting the PWR_MDE control register to a non-zero state the ADIS16201 will automatically power down once the next sample period is completed and the seven data output registers are updated.

Note that the once the ADIS16201 is placed into the power down mode it can only return to normal operation by timing out or by reset via the /RST hardware control line. Once awake the seven data output registers can be scanned to determine what the state of the output registers were prior to powering down. Once the data is recovered the device can be powered down again by simply writing a non-zero value to the PWR_MDE control register and starting the process all over.

Recovery time for the ADIS16201 from the power down period is equal to TBD mSec. This recovery time is implemented within the device in order to allow for recovery of the ADC prior to performing the next data conversion. Note that the ND data bit within the seven data output control registers is cleared when the ADIS16201 is powered down. Likewise, the New Data Hardware I/O line is placed into an inactive state prior to being powered down. The DAC is placed into a power-down mode as well which results in the DAC output dropping to 0V during the power down period. All control register settings are retained while powered down with the exception of the PWR_MDE control register which is reset to zero prior to power down.

Table 13. Power Down Mode Control Register Definition

PWR_MDE

	MSB							LSB
(3Bh)	x	x	x	X	X	x	x	X
(3Ah)	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

PM7-PM0	The Power Down Mode Register. The power down period is determined by multiplying the binary value represented by PM7-PM0 times the constant 0.5 Sec. This results in a variable power-down period of 0.5 Sec to 127.5 Sec with 0.5 Sec resolution in the setting. A setting of 0 disables the power down mode whereas any non-zero entry will place the device in the power down mode at the next update of the data output registers. **The power down register is volatile and is set to all 0's upon initial power-up as well as recovery from the power down mode.** Read/Write capability.

STATUS FEEDBACK

The STATUS control register within the ADIS16201 is utilized in determining the present state of the device. The ability to monitor the device becomes necessary when and if the ADIS16201 has registered an alarm or error condition as indicated by the EA bit within the seven data output control registers. The 16 bit STATUS register is broken into two bytes. The three lower bits of the lower data byte are used to indicate which error condition exists whereas the two lower bits of the upper data byte are utilized in indicating which alarm condition exists.

Once the EA bits are set within the seven data output registers they can only be cleared by the removal of the error or alarm condition and the subsequent reading of the STATUS control register.

Table 14. Status Register Definition

STATUS

	MSB							LSB
(3Dh)	x	x	X	X	x	X	AM2	AM1
(3Ch)	x	x	X	X	ER3	ER2	ER1	ER0

The Status Control Register. Error or Alarm flags are set to indicate various error or alarm conditions within the device. Simultaneous setting of multiple flags is a possibility. All flags are cleared upon the reading of the STATUS register. The flags will be reset on a continuing basis as long as the error or alarm conditions persist. **All 0's upon reset**. Read mode only.	
BIT	DESCRIPTION
ER0	Power Supply Below 2.975V: 1 – error condition, 0 – normal mode.
ER1	Power Supply Above 3.625V: 1 – error condition, 0 – normal mode.
ER2	Control Register Update Failed: 1 – error condition, 0 – normal mode.
ER3	SPI Communications Failure 1 – error condition, 0 – normal mode
AM1	Alarm 1 Status; 1 - Alarm Active, 0 - Alarm Inactive.

AM2	Alarm 2 Status; 1 - Alarm Active, 0 - Alarm Inactive.

COMMAND CONTROL

The COMMAND control register is utilized in sending global commands to the ADIS16201 device. There are four separate commands that act as global commands in the controlling of the ADIS16201 operation. Any one of the four above commands can be implemented by simply writing a "1" to the corresponding bit location. The COMMAND control register has write-only capability and is consequently volatile.

First is the NULL command which is discussed in detail within the *Calibration Registers* section. Its purpose is to automatically load the four OFFSET registers in order to zero the two acceleration and two inclination data output registers. It is suggested that when the NULL command is to be implemented that the AVG_CNT control register be set to 08h in order to maximize the filtering and reduce the effects of noise in determining the values to be loaded into the OFFSET control registers. The second global command is the FACTORY RESET command which is utilized in the resetting of the four SCALE and four OFFSET registers to their ideal values of 800h and 000h respectively through the use of a single command. The third global command implemented within the COMMAND control register is the DAC LATCH command which as further discussed within the *Auxiliary DAC* section is utilized in latching of the data held within the AUX_DAC control register into the Auxiliary DAC itself. The fourth and final global command implemented within the COMMAND control register is the SOFTWARE RESET which is utilized in resetting the ADIS16201 through the SPI.

Table 15. Command Register Definition

COMMAND

	MSB							LSB
(3Fh)	X	x	X	x	x	X	x	x
(3Eh)	CMD7	x	X	x	X	CMD 2	CMD 1	CMD 0

System Command Register. Write mode only.	
BIT	DESCRIPTION
CMD0	NULL Command. Loads the X/Y Inclination OFFSET as well as the X/Y Acceleration OFFSET registers in order to zero out the Inclination and Acceleration outputs. Useful as a single command to simultaneously zero both inclination and acceleration outputs.
CMD1	FACTORY RESET Command. Allows user to reset all four system level OFFSET registers and all four system level SCALE registers to the nominal settings of 000h and 800h respectively upon receipt of command. Data within the Moving Average filters will likewise be reset.
CMD2	Auxiliary DAC LATCH Command. This command acts to latch the AUX_DAC control register data into the Auxiliary DAC upon receipt of the command. This allows for sequential loading of the upper and lower AUX_DAC data bytes via the SPI without having the Auxiliary DAC transition into unwanted intermediate states based upon the individual AUX_DAC data bytes. Once the two bytes of AUX_DAC have been loaded then the DAC LATCH command can be initiated in order to latch the data into the Auxiliary DAC itself.
CMD7	SOFTWARE RESET Command. Allows for resetting of the device via the SPI.

MISCELLANEOUS CONTROL REGISTER

The MISC_CTRL control register within the ADIS16201 provides control of two miscellaneous functions. First is the Data Ready Hardware I/O function. The second is the Self-Test function. The bits to control these two functions are detailed within Table 16 as listed below.

The operation of the Data Ready hardware I/O function is very similar to the Alarm hardware I/O function that is controlled through the ALM_CTRL control register. In this case, the MISC_CNTRL register can be used in setting up one of the two GPIO pins to serve as the hardware output pin that indicates when the sampling, conversion and processing of the seven data output variables has been completed. The enabling of the Data Ready hardware function as well as the control of the actual I/O line to place the Data Ready function on and the polarity of the active Data Ready signal is controlled through this control register. The Data Ready hardware I/O pin is reset to an inactive state whenever any one of the seven data output variables has been read via the SPI. Upon completion of the next sample/conversion/processing cycle the Data Ready hardware I/O line will be reasserted.

With the MSC_CTRL, ALM_CTRL and GPIO_CTRL control registers all being able to influence the same GPIO pins a priority level must be established for conflicting assignments of the two GPIO pins. This priority level is defined as: MSC_CTRL has precedence over ALM_CTRL which has precedence over GPIO_CTRL.

The Self-Test enable bit allows the end user to place the ADIS16201 into a diagnostics mode for the purposes of verifying the MEMs sensor operation. When this bit is set high an electrostatic force is generated internal to the MEMs sensor. The resulting movement within the sensor allows the end user to test if the accelerometer is functional. Typical change in the output will be 328mg (corresponding to 708 LSB). Once the Self-Test enable bit is returned to a low state the normal operation is resumed.

Table 16. Miscellaneous Control Register Definition

MSC_CTRL

	MSB							LSB
(35h)	x	x	x	x	X	x	X	ST
(34h)	x	x	x	x	X	DRE	DRP	DRL

The 16 bit Miscellaneous Control register is used in the controlling of the Self-Test and Data-Ready hardware functions. This includes turning on and off of the Self-test function as well as enabling and configuring the Data-Ready function. For the Data-Ready function the written values are non-volatile allowing for data recovery upon reset. **The Self-Test data is volatile and is set to 0's upon reset.** Read/Write capability.	
BIT	DESCRIPTION
DRE	Data-Ready Enable; 1 – DR enabled, 0 - DR disabled
DRP	Data-Ready Polarity; 1 – active high, 0 - active low
DRL	Data-Ready Line Select; 1– DIO1, 0 – DIO0
ST	Self-Test Enable; 1 – ST enabled, 0 – ST disabled

PERIPHERALS

AUXILIARY ADC FUNCTION

The auxiliary ADC function integrates a standard 12 bit ADC into the ADIS16201 to allow for the monitoring of miscellaneous functions within the end-users target system. The output of the ADC can be monitored through the AUX_ADC control register as defined in Table 6. The ADC consists of a 12-bit successive approximation converter. The output data is presented in straight binary format with the full scale range extending from 0V to VREF. A high precision, low drift, factory calibrated 2.5V reference is provided on-chip.

Figure 10 shows the equivalent circuit of the analog input structure of the ADC. The capacitor C1 is typically 4pF and can be attributed to pin capacitance. The two diodes provide ESD protection for the analog input. Care must be taken to ensure that the analog input signals never exceed the supply rails by more than 300mV. This would cause these diodes to become forward biased and start conducting up to 10mA without causing irreversible damage to the part. The resistor is a lumped component made up of the ON resistance of the switches. The value of this resistance is typically about 100Ω. The capacitor C2 represents the ADC sampling capacitor with a capacitance of 16pF typically.

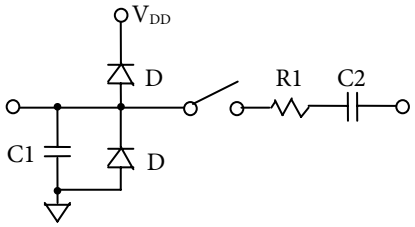

Figure 10. Equivalent Analog Input Circuit
Conversion Phase: Switch Open
Track Phase: Switch Closed

For AC applications, removing high-frequency components from the analog input signal is recommended by the use of an RC low-pass filter on the relevant analog input pins. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances will significantly affect the AC performance of the ADC. This may necessitate the use of an input buffer amplifier. When no input amplifier is used to drive the analog input, the source impedance should be limited to values lower than 1 kΩ. The maximum source impedance will depend on the amount of total harmonic distortion (THD) that can be tolerated.

AUXILIARY DAC FUNCTION

The auxiliary DAC function integrates a standard 12 bit DAC into the ADIS16201 with the DAC output buffered and fed off-chip to allow for the control of miscellaneous functions within the end-users target application. Data is downloaded through the writing of two adjacent data bytes as defined below in Table 9. In order to prevent the DAC from transitioning through inadvertent states as one data byte is downloaded and then the next data byte is downloaded, a single command is used to simultaneously latch both data bytes into the DAC after they have been initially written into the AUX_DAC control register. This command is implemented by writing a '1' to bit 2 of the COMMAND control register which once received will result in the DAC output transitioning to the desired state.

The DAC output spans the range between 0V and 2.5V. The DAC output buffer features a true rail-to-rail output stage implementation. This means that, unloaded, the output is capable of swinging of less than 5mV of ground. Moreover, the DAC's linearity performance (when driving a 5k resistive load to ground) is good through the full transfer function except for codes 0 to 100. Linearity degradation near ground is caused by saturation of the output amplifier. As the output is forced to sink more current, the nonlinear region at the bottom of the transfer function becomes larger. With larger current demands, this can significantly limit output voltage swing.

Table 17. Auxiliary DAC Control Register Definition

AUX_DAC

	MSB							LSB
(31h)	X	X	X	x	DAB	DAA	DA9	DA8
(30h)	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

DAB-DA0	Auxiliary DAC Digital Data. A 12 bit binary format number with zero representing 0 Volt and 0x0FFFh representing 2.5V. Read/Write capability. **The data within this register is volatile and is set to 0's upon reset.** Read/Write capability.

GENERAL PURPOSE I/O CONTROL

As previously noted the ADIS16201 provides two General Purpose bi-directional I/O pins (GPIO) which are available to the end user for control of auxiliary circuits within the target application. All I/O pins are 5V tolerant which means that the GPIOs support an input voltage of 5V. All GPIO pins have an internal pull up resistor (of about 100kOhm) and their drive capability is 1.6mA. The direction as well as the logic level can be controlled for these GPIO pins through the GPIO_CTRL control register as defined in Table 18.

These same GPIO pins are also controllable through the ALM_CTRL and MSC_CTRL control registers. The priority that these three control registers take in controlling the two GPIO pins follows as: MSC_CTRL has precedence over ALM_CTRL which has precedence over GPIO_CTRL.

Table 18. General Purpose I/O Control Register Definition

GPIO_CTRL

	MSB						LSB	
(33h)	X	x	X	X	X	x	DAT1	DAT0
(32h)	X	x	X	X	X	x	DIR1	DIR0

Auxiliary Digital I/O Control Register. **The data within this register is volatile and is set to 0's upon reset**. Read/Write capability.	
DIRx	Used to control data direction for General Purpose Input/Output (GPIO) signal pins DIO0 and DIO1. 0 – Input, 1 – Output.
DATx	Used to set the data levels for General Purpose Input/Output (GPIO) signal pins DIO0 and DIO1. 0 – Low, 1 – High.

APPLICATIONS

SERIAL PERIPHERAL INTERFACE

The ADIS16201 integrates a hardware Serial Peripheral Interface (SPI) on-chip. SPI is an industry standard synchronous serial interface that allows data to be synchronously transmitted and received simultaneously, i.e., full duplex up to a maximum bit rate of 3.48Mbs. The SPI Port is configured for Slave operation and consists of four pins, namely:

DOUT

The Data Out pin (DOUT) is an output pin used to transmit data out of the ADIS16201. The data is transmitted in a 16 bit / 2 byte format, MSB first.

DIN

The Data In pin (DIN) is an input pin that is used for the reception of data from the Master. The data is received in a 16 bit / 2 byte format with the W/-R control bit and address contained in the first data byte and the data contained within the second data byte, MSB first.

SCLK

The Serial Clock pin (SCLK) is used to synchronize the data being transmitted and received through the SCLK period. Therefore a 16 bit / 2 byte word is transmitted/received after sixteen SCLK periods. The SCLK pin is configured as an input.

/CS

In the ADIS16201 a transfer is initiated by the assertion of the Chip Select pin (/CS) which is an active low signal. The SPI port will then transmit and receive data in 16 bit blocks until the transfer is concluded by de-assertion of /CS.

The control registers within the ADIS16201 are based upon a 16 bit / 2 data byte format. Data is loaded in from the DIN pin of the ADIS16201 on the rising edge of SCLK. This requires 16 serial clocks for every data transfer framed by the /CS line going low and then returning high. The part operates in full duplex mode with the data clocked out of the DOUT pin likewise on the rising edge of the SCLK. For each Read command received the corresponding output data will clocked out of the DOUT pin during the following cycle as defined by the /CS line.

OUTPUT RESPONSE

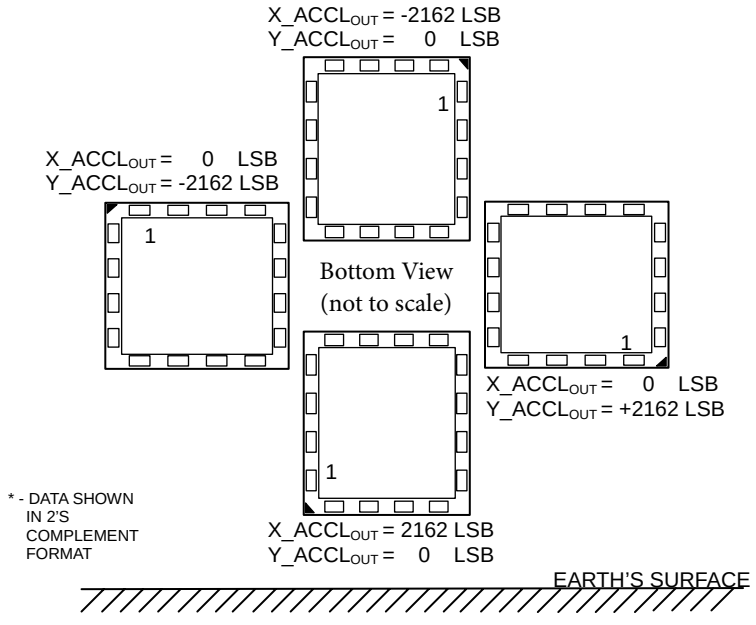

Figure 11. Output Response vs. Orientation

HARDWARE CONSIDERATIONS

The ADIS16201 can be operated from a single 3.3V (3.0V to 3.6V) power supply. This supply should be treated as an analog supply which should be kept relatively free of digital noise. Even though decoupling capacitors exist within the module on the VDD supply it is suggested that the supply line be decoupled externally through the use of a 10uF and 0.1uF capacitor combination. As per standard design practice, be sure the smaller capacitors are placed close to the VDD pin with trace lengths as short as possible. In some cases, particularly where noise is present at the 140KHz internal demodulator frequency of the sensor (or any harmonic thereof), noise on the supply may cause interference on the ADIS16201 output. If additional decoupling is needed, ferrite beads may be inserted in the supply line of the ADIS16201. Connect the ground terminal of each of these capacitors directly to the underlying ground plane. Finally, it should also be noted that all analog and digital grounds be referenced to the same system ground reference point.

GROUNDING AND BOARD LAYOUT RECOMENDATIONS

As with all high resolution data converters, special attention must be paid to grounding and PC board layout of ADIS16201 based designs in order to achieve optimum performance from the ADC and DAC.

Understanding that the ADIS16201 will typically connect to both analog and digital circuits, the user must tie the separate ground planes together very close to the ADIS16201. In systems where analog and digital ground planes are connected together somewhere else (at the system power supply for example), they cannot be tied together at the ADIS16201 since a ground loop would result. In systems with only one ground plane, ensure that the digital and analog components are physically separated onto separate halves of the board such that digital return currents do not flow near analog circuitry and vice versa. The ADIS16201 can then be placed between the digital and analog sections.

In all of these scenarios, and in more complicated real-life situations, keep in mind that the flow of the current from the supplies and back to ground. Make sure the return paths for all currents are as close as possible to the paths the currents took to reach their destinations. Whenever possible, avoid large discontinuities in the ground plane as they force return signals to travel a longer path. And of course, make all connections to the ground plane directly, with little or no trace separating the pin from its via to ground.

If the user plans to connect any high speed logic signals (rise/fall times <5nS) to either of the ADIS16201 digital I/O pins, add a series resistor to each line to keep the rise and fall times longer than 5ns at the ADIS16201 digital I/O pins. A values of 100Ω or 200Ω is usually sufficient to prevent high speed signals from coupling capacitively into the ADIS16201 and affecting the accuracy of the ADC conversions.

BANDGAP REFERENCE

The ADIS16201 provides an on-chip bandgap reference of 2.5V, which is utilized by the on-board ADC and DAC. This internal reference also appears on the V_{REF} pin. This reference can be connected to external circuits in the system. An external buffer would be required because of the low drive capability of the VREF output.

POWER-ON RESET OPERATION

An internal POR (Power-on Reset) is implemented internal to the ADSI16201. For V_{DD} below 2.35V, the internal POR will hold the ADIS16201 in reset. As V_{DD} rises above 2.35V, An internal timer will time out for typically TBD before the part is released from reset. The user must ensure that the power supply has reached a stable 3.0V minimum level by this time. Likewise on power-down, the internal POR will hold the ADIS16201in reset until V_{DD} has dropped below 2.35V. Figure 12 illustrates the operation of the internal POR in detail.

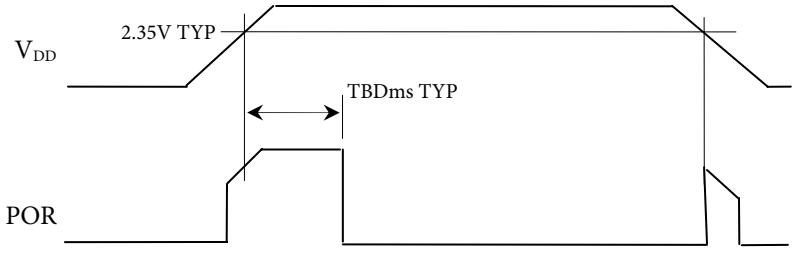

Figure 12. Internal Power-on-Rest Operation

OUTLINE DIMENSIONS

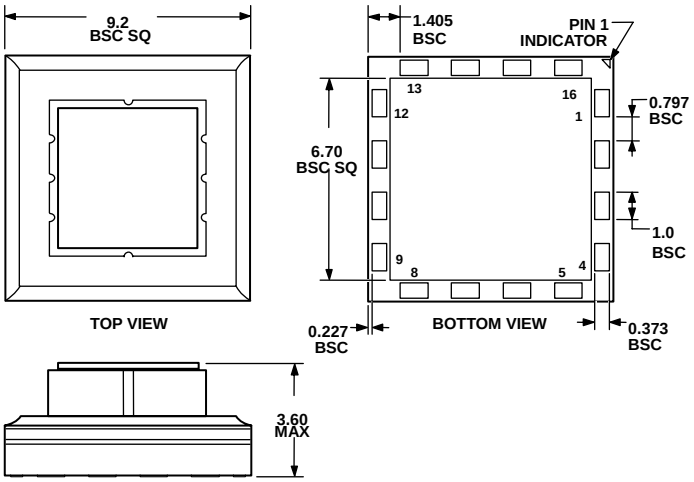

Figure 13. 16-Terminal Land Grid Array [LGA]
(CC-16-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADIS16201CCCZ	–40°C to +125°C	16-Terminal Land Grid Array (LGA)	CC-16-1
ADIS16201/PCB		Evaluation Board	

NOTES

PR05462-0-10/05(PrB)