ANALOG DEVICES

0.5 Ω CMOS 1.65 V TO 3.6 V Dual SPDT/2:1 MUX

ADG836

FEATURES

0.5 Ω typical on resistance
0.8 Ω maximum on resistance at 125°C
1.65 V to 3.6 V operation
Automotive temperature range: –40°C to +125°C
High current carrying capability: 300 mA continuous
Rail-to-rail switching operation
Fast-switching times <20 ns
Typical power consumption (<0.1 μW)

APPLICATIONS

Cellular phones
PDAs
MP3 players
Power routing
Battery-powered systems
PCMCIA cards
Modems
Audio and video signal routing
Communication systems

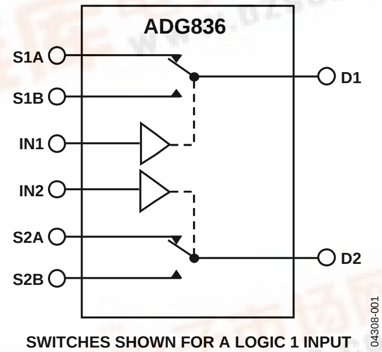

Figure 1.

GENERAL DESCRIPTION

The ADG836 is a low voltage CMOS device containing two independently selectable single-pole, double-throw (SPDT) switches. This device offers ultralow on resistance of less than 0.8 Ω over the full temperature range. The ADG836 is fully specified for 3.3 V, 2.5 V, and 1.8 V supply operation.

Each switch conducts equally well in both directions when on, and has an input signal range that extends to the supplies. The ADG836 exhibits break-before-make switching action.

The ADG836 is available in a 10-lead MSOP and a 3 mm × 3 mm 12-lead LFCSP.

PRODUCT HIGHLIGHTS

1. <0.8 Ω over full temperature range of −40°C to +125°C.
2. Single 1.65 V to 3.6 V operation.
3. Compatible with 1.8 V CMOS logic.
4. High current handling capability (300 mA continuous current at 3.3 V).
5. Low THD + N (0.02% typ).
6. 3 mm × 3 mm LFCSP package and 10-lead MSOP package.

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REVISION HISTORY

4/05—Rev. 0 to Rev. A

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Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 3.6 V, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	Temperature[1] +25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	0.5			Ω typ	V_{DD} = 2.7 V, V_S = 0 V to V_{DD}, I_S = 100 mA;
	0.65	0.75	0.8	Ω max	Figure 19
On Resistance Match	0.04			Ω typ	V_{DD} = 2.7 V, V_S = 0.65 V, I_S = 100 mA
Between Channels (ΔR_{ON})		0.075	0.08	Ω max	
On Resistance Flatness ($R_{FLAT (ON)}$)	0.1			Ω typ	V_{DD} = 2.7 V, V_S = 0 V to V_{DD}
		0.15	0.16	Ω max	I_S = 100 mA
LEAKAGE CURRENTS					V_{DD} = 3.6 V
Source Off Leakage I_S (OFF)	±0.2			nA typ	V_S = 0.6 V/3.3 V, V_D = 3.3 V/0.6 V; Figure 20
Channel On Leakage I_D, I_S (ON)	±0.2			nA typ	V_S = V_D = 0.6 V or 3.3 V; Figure 21
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current					
I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	
C_{IN}, Digital Input Capacitance	4			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}	21			ns typ	R_L = 50 Ω, C_L = 35 pF
	26	28	29	ns max	V_S = 1.5 V/0 V; Figure 22
t_{OFF}	4			ns typ	R_L = 50 Ω, C_L = 35 pF
	7	8	9	ns max	V_S = 1.5 V; Figure 22
Break-Before-Make Time Delay	17			ns typ	R_L = 50 Ω, C_L = 35 pF
(t_{BBM})			5	ns min	V_{S1} = V_{S2} = 1.5 V; Figure 23
Charge Injection	40			pC typ	V_S = 1.5 V, R_S = 0 Ω, C_L = 1 nF; Figure 24
Off Isolation	−67			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 25
Channel-to-Channel Crosstalk	−90			dB typ	S1A–S2A/S1B–S2B, R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 28
	−67			dB typ	S1A–S1B/S2A–S2B, R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 27
Total Harmonic Distortion (THD + N)	0.02			%	R_L = 32 Ω, f = 20 Hz to 20 kHz, V_S = 2 V p-p
Insertion Loss	−0.05			dB typ	R_L = 50 Ω, C_L = 5 pF; Figure 26
−3 dB Bandwidth	57			MHz typ	R_L = 50 Ω, C_L = 5 pF; Figure 26
C_S (OFF)	25			pF typ	
C_D, C_S (ON)	75			pF typ	
POWER REQUIREMENTS					V_{DD} = 3.6 V
I_{DD}	0.003			μA typ	Digital inputs = 0 V or 3.6 V
		1	4	μA max	

[1] Temperature range for Y version is −40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

V_{DD} = 2.5 V ± 0.2 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	Temperature[1] +25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	0.65			Ω typ	V_{DD} = 2.3 V, V_S = 0 V to V_{DD}, I_S = 100 mA;
	0.72	0.8	0.88	Ω max	Figure 19
On Resistance Match Between	0.04			Ω typ	V_{DD} = 2.3 V, V_S = 0.7 V, I_S = 100 mA
Channels (ΔR_{ON})		0.08	0.085	Ω max	
On Resistance Flatness ($R_{FLAT (ON)}$)	0.16			Ω typ	V_{DD} = 2.3 V, V_S = 0 V to V_{DD}, I_S = 100 mA
		0.23	0.24	Ω max	
LEAKAGE CURRENTS					V_{DD} = 2.7 V
Source Off Leakage I_S (OFF)	±0.2			nA typ	V_S = 0.6 V/2.4 V, V_D = 2.4 V/0.6 V; Figure 20
Channel On Leakage I_D, I_S (ON)	±0.2			nA typ	V_S = V_D = 0.6 V or 2.4 V; Figure 21
DIGITAL INPUTS					
Input High Voltage, V_{INH}			1.7	V min	
Input Low Voltage, V_{INL}			0.7	V max	
Input Current					
I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	
C_{IN}, Digital Input Capacitance	4			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}	23			ns typ	R_L = 50 Ω, C_L = 35 pF
	29	30	31	ns max	V_S = 1.5 V/0 V; Figure 22
t_{OFF}	5			ns typ	R_L = 50 Ω, C_L = 35 pF
	7	8	9	ns max	V_S = 1.5 V; Figure 22
Break-before-Make Time Delay (t_{BBM})	17			ns typ	R_L = 50 Ω, C_L = 35 pF
			5	ns min	V_{S1} = V_{S2} = 1.5 V; Figure 23
Charge Injection	30			pC typ	V_S = 1.25 V, R_S = 0 Ω, C_L = 1 nF; Figure 24
Off Isolation	−67			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 25
Channel-to-Channel Crosstalk	−90			dB typ	S1A−S2A/S1B−S2B,
					R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 28
	−67			dB typ	S1A−S1B/S2A−S2B,
					R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 27
Total Harmonic Distortion (THD + N)	0.022			%	R_L = 32 Ω, f = 20 Hz to 20 kHz, V_S = 1.5 V p-p
Insertion Loss	−0.06			dB typ	R_L = 50 Ω, C_L = 5 pF; Figure 26
−3 dB Bandwidth	57			MHz typ	R_L = 50 Ω, C_L = 5 pF; Figure 26
C_S (OFF)	25			pF typ	
C_D, C_S (ON)	75			pF typ	
POWER REQUIREMENTS					V_{DD} = 2.7 V
I_{DD}	0.003			μA typ	Digital inputs = 0 V or 2.7 V
		1	4	μA max	

[1] Temperature range for Y version is −40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

V_{DD} = 1.65 V ± 1.95 V, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	Temperature[1] +25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	1			Ω typ	V_{DD} = 1.8 V, V_S = 0 V to V_{DD}, I_S = 100 mA;
	1.4	2.2	2.2	Ω max	Figure 19
	2	4	4	Ω max	V_{DD} = 1.65 V, V_S = 0 V to V_{DD}, I_S = 100 mA; Figure 19
On Resistance Match Between Channels (ΔR_{ON})	0.1			Ω typ	V_{DD} = 1.65 V, V_S = 0.7 V, I_S = 100 mA
LEAKAGE CURRENTS					V_{DD} = 1.95 V
Source Off Leakage I_S (OFF)	±0.2			nA typ	V_S = 0.6 V/1.65 V, V_D = 1.65 V/0.6 V; Figure 20
Channel On Leakage I_D, I_S (ON)	±0.2			nA typ	V_S = V_D = 0.6 V or 1.65 V; Figure 21
DIGITAL INPUTS					
Input High Voltage, V_{INH}			0.65 V_{DD}	V min	
Input Low Voltage, V_{INL}			0.35 V_{DD}	V max	
Input Current					
I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	
C_{IN}, Digital Input Capacitance	4			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}	28			ns typ	R_L = 50 Ω, C_L = 35 pF
	37	38	39	ns max	V_S = 1.5 V/0 V; Figure 22
t_{OFF}	7			ns typ	R_L = 50 Ω, C_L = 35 pF
	9	10	11	ns max	V_S = 1.5 V; Figure 22
Break-Before-Make Time Delay (t_{BBM})	21			ns typ	R_L = 50 Ω, C_L = 35 pF
			5	ns min	V_{S1} = V_{S2} = 1 V; Figure 23
Charge Injection	20			pC typ	V_S = 1 V, R_S = 0 V, C_L = 1 nF; Figure 24
Off Isolation	−67			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 25
Channel-to-Channel Crosstalk	−90			dB typ	S1A–S2A/S1B–S2B; R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 28
	−67			dB typ	S1A–S1B/S2A–S2B; R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; Figure 27
Total Harmonic Distortion, THD	0.14			%	R_L = 32 Ω, f = 20 Hz to 20 kHz, V_S = 1.2 V p-p
Insertion Loss	−0.08			dB typ	R_L = 50 Ω, C_L = 5 pF; Figure 26
−3 dB Bandwidth	57			MHz typ	R_L = 50 Ω, C_L = 5 pF; Figure 26
C_S (OFF)	25			pF typ	
C_D, C_S (ON)	75			pF typ	
POWER REQUIREMENTS					V_{DD} = 1.95 V
I_{DD}	0.003			μA typ	Digital inputs = 0 V or 1.95 V
		1.0	4	μA max	

[1] Temperature range for Y version is −40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to GND	−0.3 V to +4.6 V
Analog Inputs[1]	−0.3 V to V_{DD} + 0.3 V
Digital Inputs[1]	−0.3 V to 4.6 V or 10 mA, whichever occurs first
Peak Current, S or D	
3.3 V Operation	500 mA
2.5 V Operation	460 mA
1.8 V Operation	420 mA (pulsed at 1ms, 10% duty cycle max)
Continuous Current, S or D	
3.3 V Operation	300 mA
2.5 V Operation	275 mA
1.8 V Operation	250 mA
Operating Temperature Range	
Automotive (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
MSOP Package	
θ_{JA} Thermal Impedance	206°C/W
θ_{JC} Thermal Impedance	44°C/W
LFCSP Package	
θ_{JA} Thermal Impedance (3-Layer Board)	61.1°C/W
IR Reflow, Peak Temperature <20 sec	235°C

[1] Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

Table 5. Truth Table

Logic	Switch A	Switch B
0	Off	On
1	On	Off

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

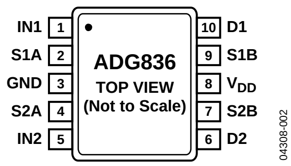


Figure 2. 10-Lead MSOP (RM-10)

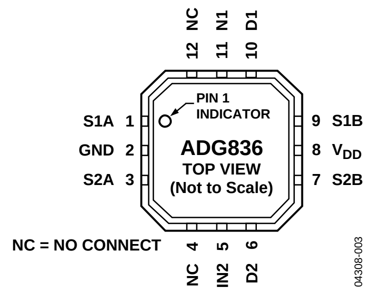


Figure 3. 12-Lead LFCSP (CP-12)

Table 6. Terminology

V_{DD}	Most positive power supply potential.
I_{DD}	Positive supply current.
GND	Ground (0 V) reference.
S	Source terminal. May be an input or output.
D	Drain terminal. May be an input or output.
IN	Logic control input.
V_D (V_S)	Analog voltage on terminals D, S.
R_{ON}	Ohmic resistance between D and S.
$R_{FLAT (ON)}$	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.
ΔR_{ON}	On resistance match between any two channels.
I_S (OFF)	Source leakage current with the switch off.
I_D (OFF)	Drain leakage current with the switch off.
I_D, I_S (ON)	Channel leakage current with the switch on.
V_{INL}	Maximum input voltage for Logic 0.
V_{INH}	Minimum input voltage for Logic 1.
I_{INL} (I_{INH})	Input current of the digital input.
C_S (OFF)	Off switch source capacitance. Measured with reference to ground.
C_D (OFF)	Off switch drain capacitance. Measured with reference to ground.
C_D, C_S (ON)	On switch capacitance. Measured with reference to ground.
C_{IN}	Digital input capacitance.
t_{ON}	Delay time between the 50% and the 90% points of the digital input and switch on condition.
t_{OFF}	Delay time between the 50% and the 90% points of the digital input and switch off condition.
t_{BBM}	On or off time measured between the 80% points of both switches when switching from one to another.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during on-off switching.
Off Isolation	A measure of unwanted signal coupling through an off switch.
Crosstalk	A measure of unwanted signal, which is coupled through from one channel to another, as a result of parasitic capacitance.
−3 dB Bandwidth	The frequency at which the output is attenuated by 3 dB.
On Response	The frequency response of the on switch.
Insertion Loss	The loss due to the on resistance of the switch.
THD + N	The ratio of the harmonics amplitude plus noise of a signal to the fundamental.

TYPICAL PERFORMANCE CHARACTERISTICS

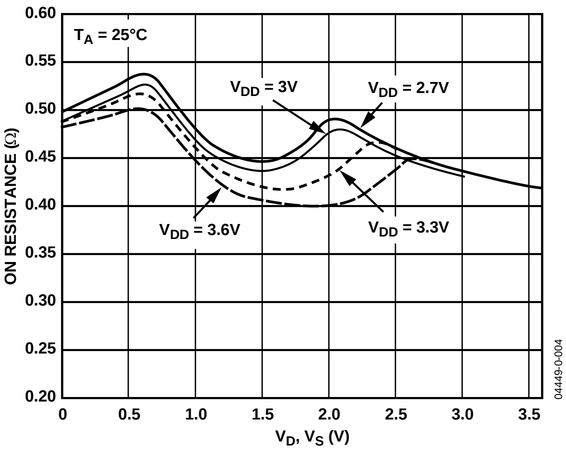


Figure 4. On Resistance vs. V_D (V_S) V_{DD} = 2.7 to 3.6 V

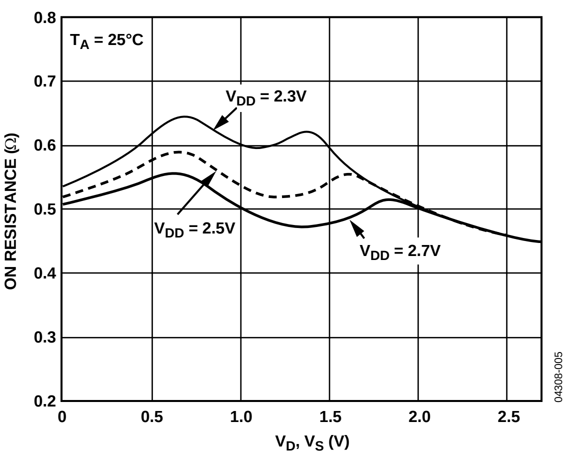


Figure 5. On Resistance vs. V_D (V_S) V_{DD} = 2.5 V to 0.2 V

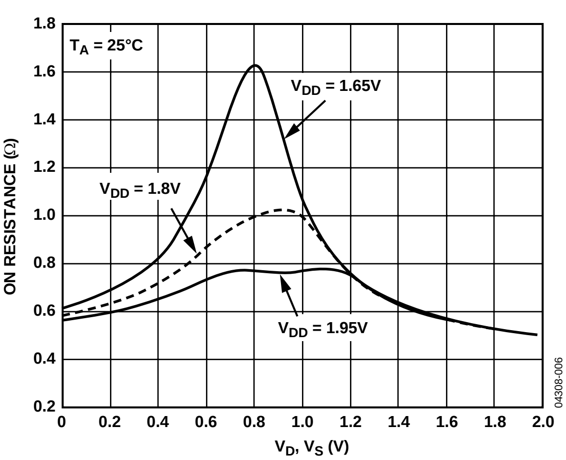


Figure 6. On Resistance vs. V_D (V_S) V_{DD} = 1.8 ± 3.6

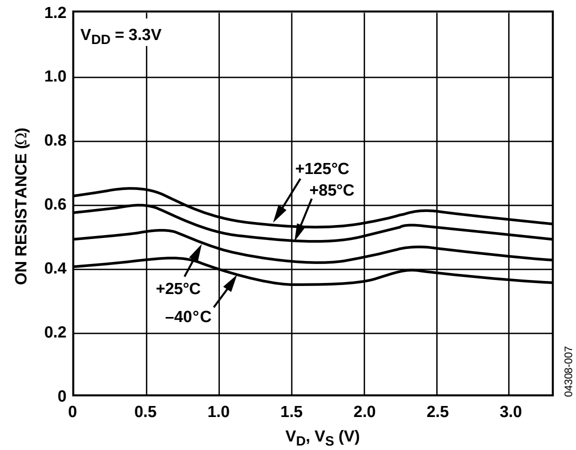


Figure 7. On Resistance vs. V_D (V_S) for Different Temperature, 3.3 V

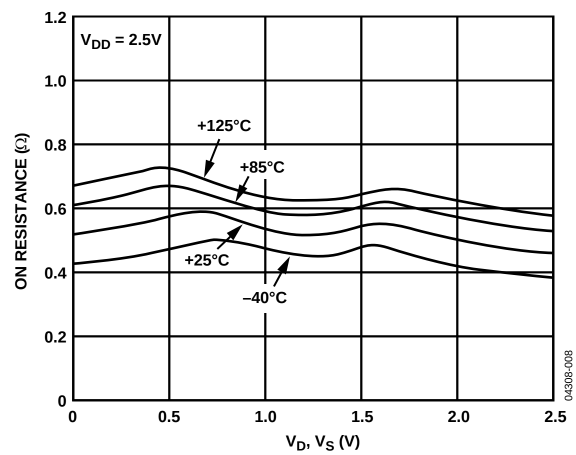


Figure 8. On Resistance vs. V_D (V_S) for Different Temperature, 2.5 V

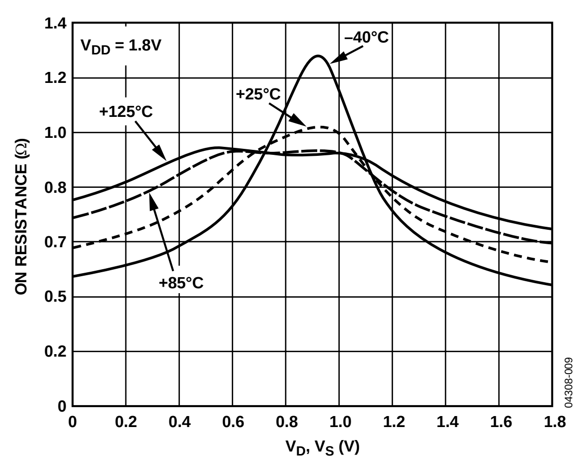


Figure 9. On Resistance vs. V_D (V_S) for Different Temperature, 1.8 V

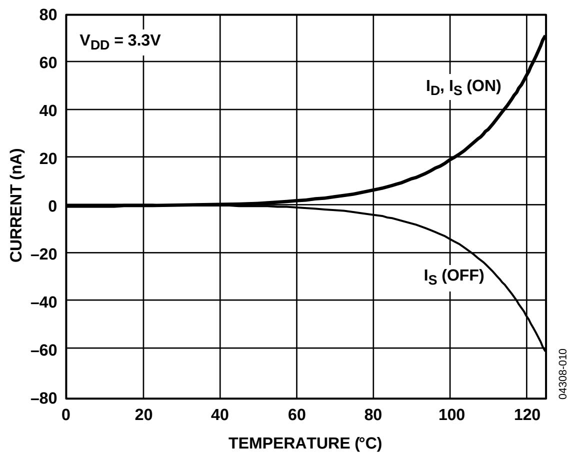


Figure 10. Leakage Current vs. Temperature, 3.3 V

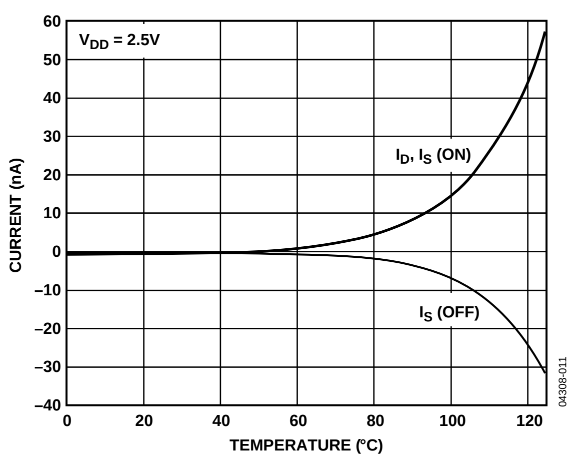


Figure 11. Leakage Current vs. Temperature, 2.5 V

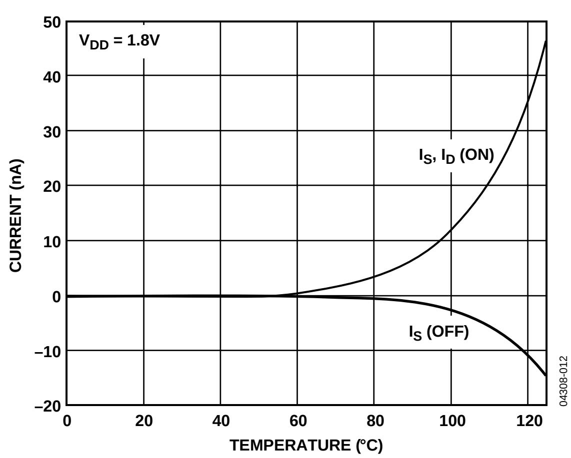


Figure 12. Leakage Current vs. Temperature, 1.8 V

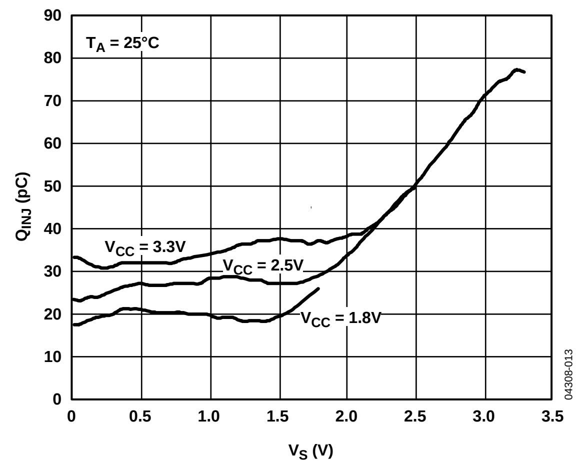


Figure 13. Charge Injection vs. Source Voltage

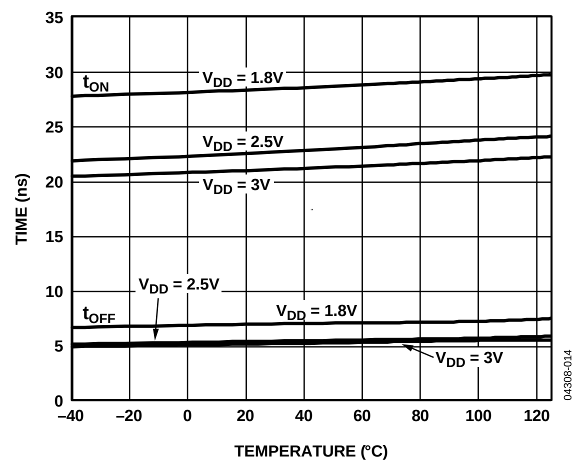


Figure 14. t_{on}/t_{off} Times vs. Temperature

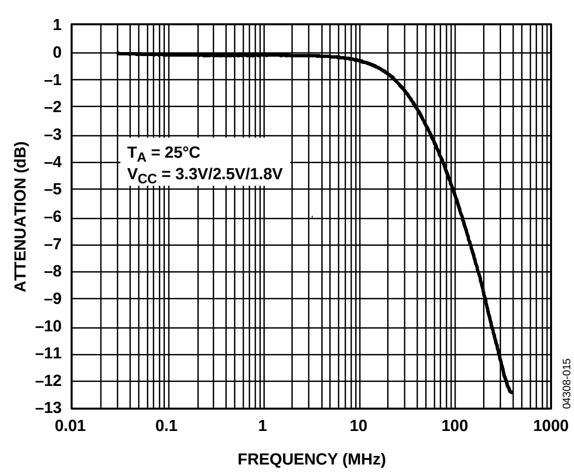


Figure 15. Bandwidth

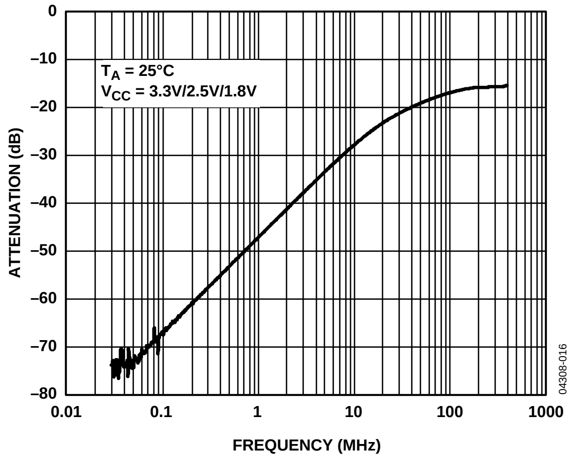


Figure 16. Off Isolation vs. Frequency

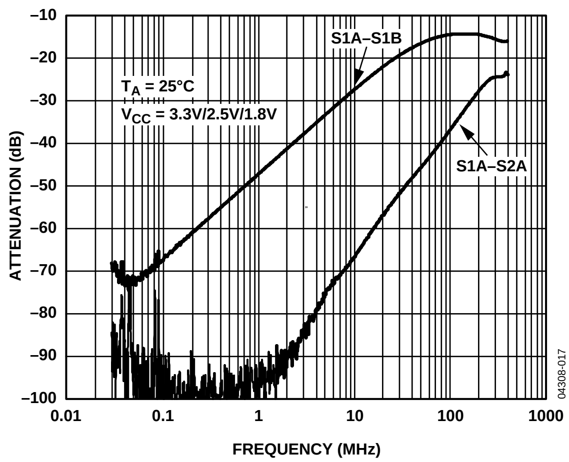


Figure 17. Crosstalk vs. Frequency

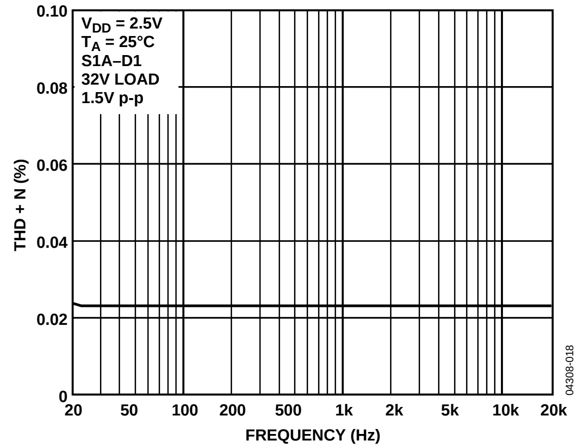


Figure 18. Total Harmonic Distortion + Noise

TEST CIRCUITS

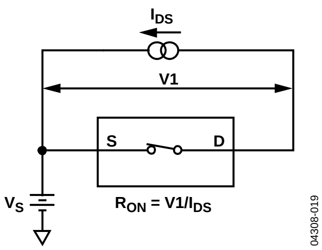


Figure 19. On Resistance

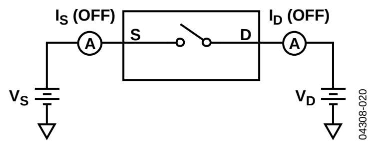


Figure 20. Off Leakage

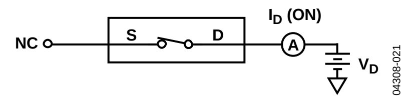


Figure 21. On Leakage

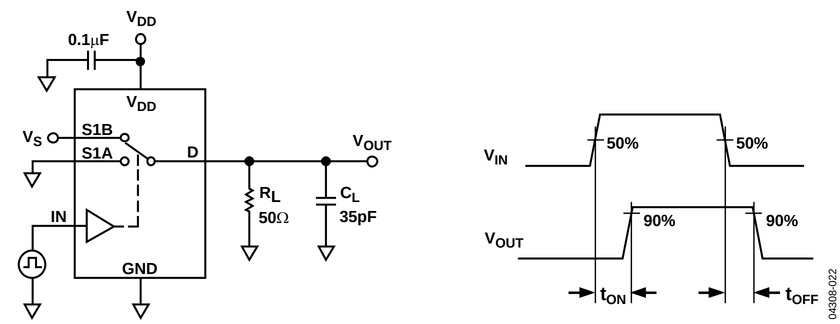


Figure 22. Switching Times, t_{ON}, t_{OFF}

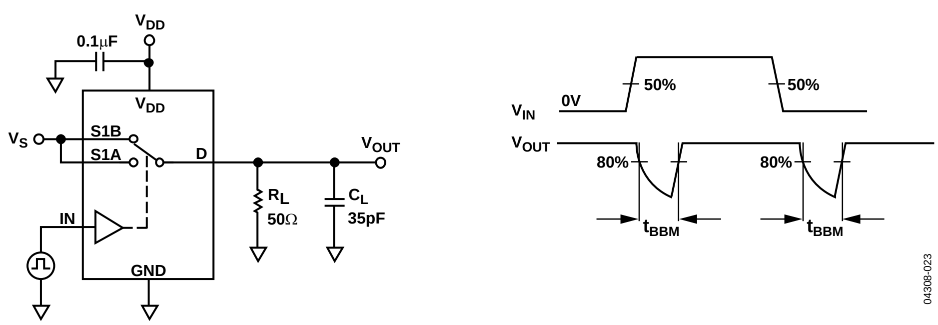


Figure 23. Break-Before-Make Time Delay, t_{BBM}

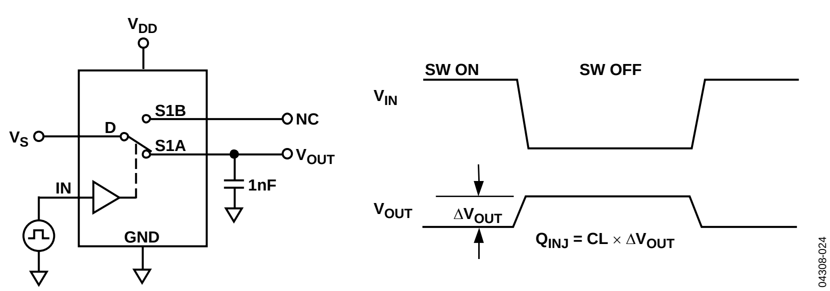
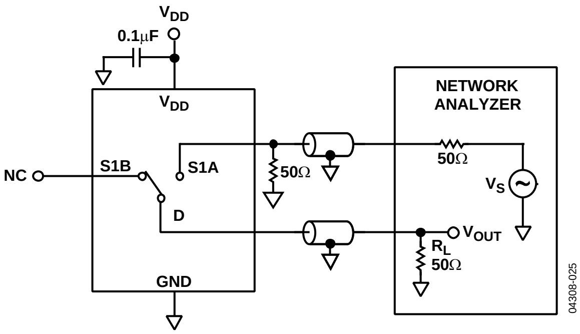
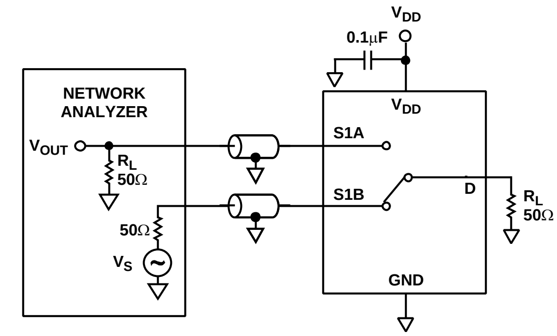


Figure 24. Charge Injection



$$\text{OFF ISOLATION} = 20\ \text{LOG}\ \frac{V_{OUT}}{VS}$$

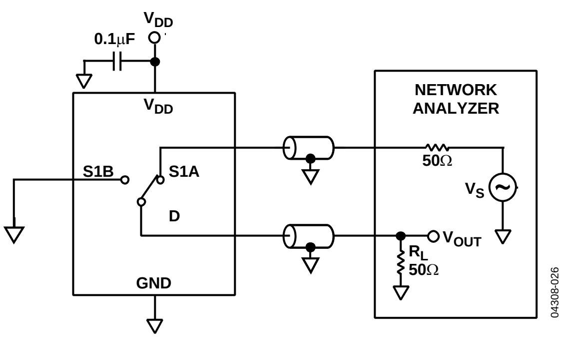
Figure 25. Off Isolation



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20\ \text{LOG}\ \frac{V_{OUT}}{VS}$$

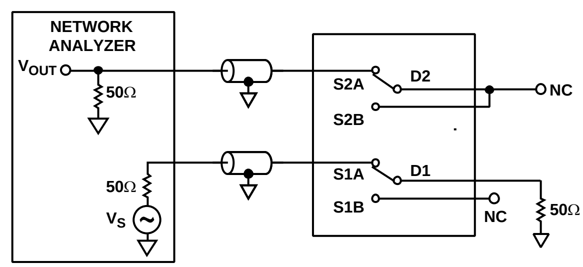
04308-027

Figure 27. Channel-to-Channel Crosstalk (S1A–S1B)



$$\text{INSERTION LOSS} = 20\ \text{LOG}\ \frac{V_{OUT}\ \text{WITH SWITCH}}{V_{OUT}\ \text{WITHOUT SWITCH}}$$

Figure 26. Bandwidth

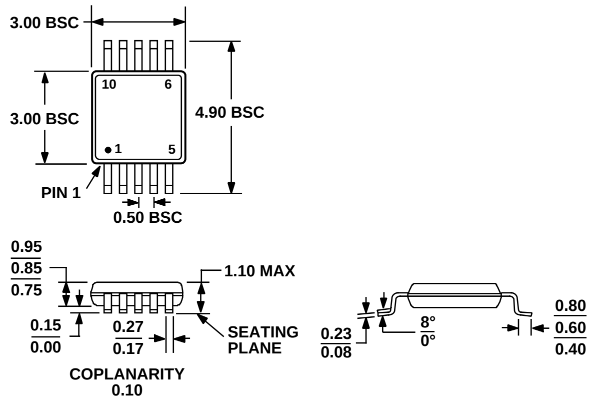


$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20\ \text{LOG}\ \frac{V_{OUT}}{VS}$$

04308-028

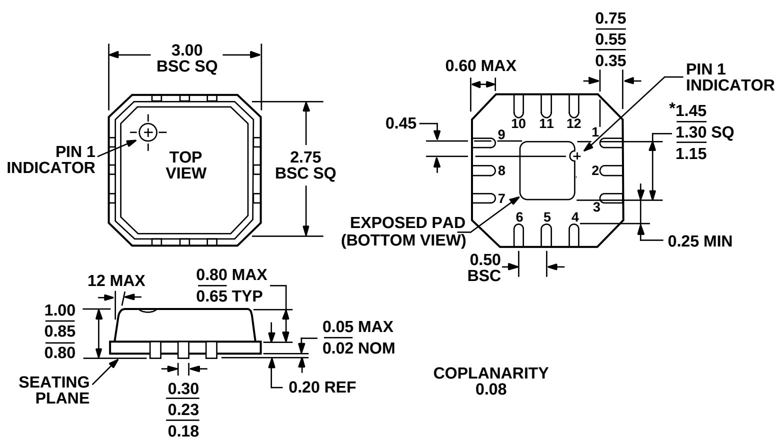
Figure 28. Channel-to-Channel Crosstalk (S1A–S2A)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 29. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters



*COMPLIANT TO JEDEC STANDARDS MO-220-VEED-1
EXCEPT FOR EXPOSED PAD DIMENSION.

Figure 30. 12-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
3 x 3 mm Body, Very Thin Quad
(CP-12-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding[1]
ADG836YRM	–40°C to +125°C	Mini Small Outline Package (MSOP)	RM-10	S9A
ADG836YRM-REEL	–40°C to +125°C	Mini Small Outline Package (MSOP)	RM-10	S9A
ADG836YRM-REEL7	–40°C to +125°C	Mini Small Outline Package (MSOP)	RM-10	S9A
ADG836YRMZ[2]	–40°C to +125°C	Mini Small Outline Package (MSOP)	RM-10	S05
ADG836YRMZ-REEL[2]	–40°C to +125°C	Mini Small Outline Package (MSOP)	RM-10	S05
ADG836YRMZ-REEL7[2]	–40°C to +125°C	Mini Small Outline Package (MSOP)	RM-10	S05
ADG836YCP-REEL	–40°C to +125°C	Lead Frame Chip Scale Package (LFCSP_VQ)	CP-12-1	S9A
ADG836YCP-REEL7	–40°C to +125°C	Lead Frame Chip Scale Package (LFCSP_VQ)	CP-12-1	S9A

[1] Branding on this package is limited to three characters due to space constraints.
[2] Z = Pb-free part.

NOTES

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C04308-0-4/05(A)