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High Performance ISM Band FSK/GFSK Transceiver IC

Preliminary Technical Data

ADF7025

FEATURES

Low power, Zero- IF RF transceiver
Frequency bands:
  431 MHz to 480 MHz
  862 MHz to 956 MHz
Data rates supported:
  1.35 kbps to 384kbps, FSK/GFSK
2.3 V to 3.6 V power supply
Programmable output power:
  −16 dBm to +13 dBm in 0.3 dBm steps
Receiver sensitivity:
  −102.4 dBm at 64 kbps, FSK
  −100.6 dBm at 172.8kbps, FSK
  −96.3 dBm at 345.6 kbps, FSK
Low power consumption:
  19 mA in receive mode
  28 mA in transmit mode (10 dBm output)
On-chip VCO and fractional-N PLL
On-chip 7-bit ADC and temperature sensor
Digital RSSI
Integrated TRx switch
Leakage current <1 µA in power-down mode

APPLICATIONS

Wireless audio/video
Remote control/security systems
Wireless metering
Keyless entry
Home automation

FUNCTIONAL BLOCK DIAGRAM

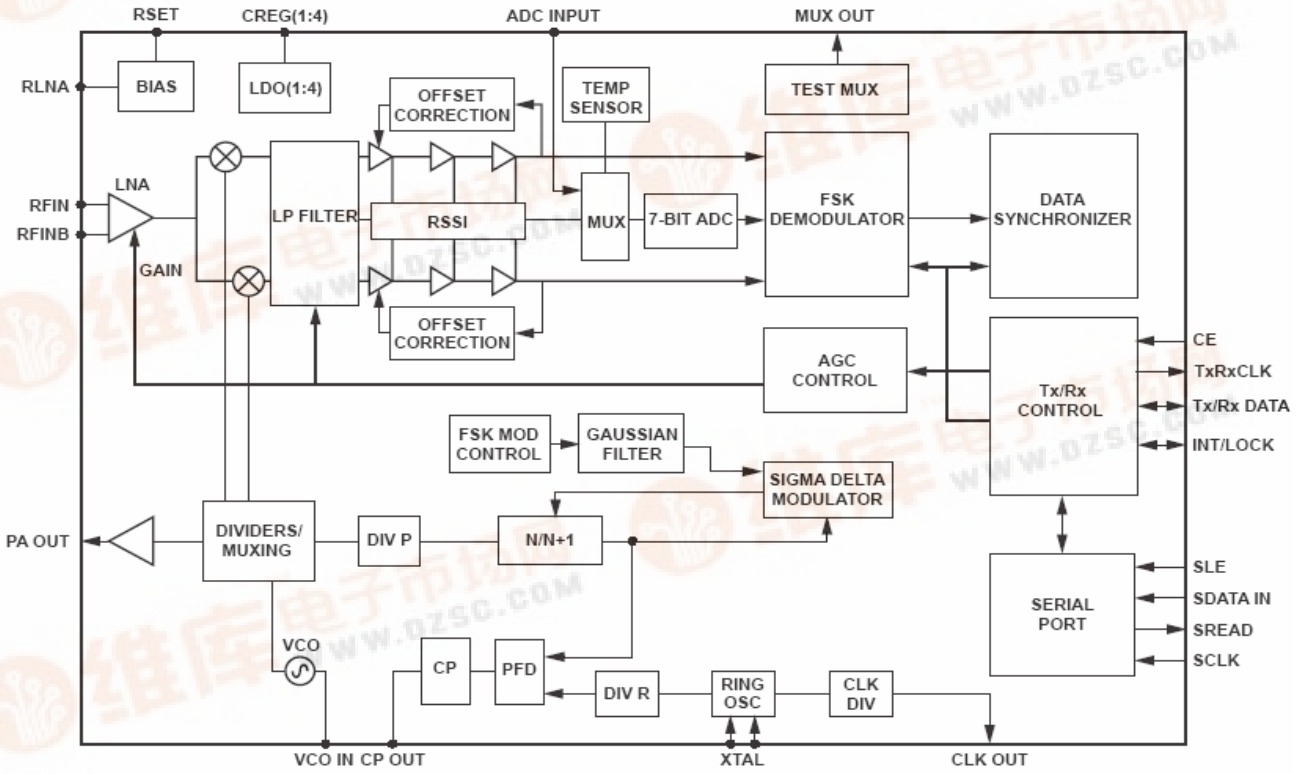

Figure 1.

Rev. PrD

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REVISION HISTORY

Revision PrD: Preliminary Version

GENERAL DESCRIPTION

The ADF7025 is a low power, highly integrated FSK/GFSK transceiver. It is designed for operation in the license–free ISM bands of 433MHz and 868MHz in Europe and 915MHz in North America. The ADF7025 is intended for applications operating under the European ETSI EN300-220 or the North American FCC (Part 15) regulatory standards. The ADF7025 is intended for wideband, high data rate applications with deviation frequencies from 150 kHz to 500 kHz and data rates from 9.6kbps to 384kbps. A complete transceiver can be built using a small number of external discrete components, making the ADF7025 very suitable for price-sensitive and area-sensitive applications.

The transmit section contains a VCO and low noise fractional-N PLL with output resolution of <1 ppm. The VCO operates at twice the fundamental frequency to reduce spurious emissions and frequency pulling problems.

The transmitter output power is programmable in 0.3 dB steps from −16 dBm to +13 dBm. The transceiver RF frequency, channel spacing, and modulation are programmable using a simple 3-wire interface. The device operates with a power supply range of 2.3 V to 3.6 V and can be powered down when not in use.

A zero-IF architecture is used in the receiver, minimizing power consumption and the external component count and avoiding the need for image rejection. The baseband filter has programmable bandwidths of ±300 kHz, ±450 kHz and ±600 kHz. A high pass pole at 80 kHz eliminates the problem of DC offsets that is characteristic of zero-IF architectures.

The ADF7025 supports a wide variety of programmable features including Rx linearity, sensitivity, and filter bandwidth, allowing the user to trade off receiver sensitivity and selectivity against current consumption, depending on the application.

An on-chip ADC provides readback of an integrated temperature sensor, an external analog input, the battery voltage, or the RSSI signal, which provides savings on an ADC in some applications. The temperature sensor is accurate to ±5°C over the full operating temperature range of −40°C to +8°C.

SPECIFICATIONS

V_{DD} = 2.3 V to 3.6 V, GND = 0 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical specifications are at V_{DD} = 3 V, T_A = 25°C. All measurements are performed using the EVAL-ADF7025DB1 using PN9 data sequence, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions
RF CHARACTERISTICS					
Frequency Ranges	862		956	MHz	
Frequency Ranges (Divide-by-2 Mode)	431		478	MHz	
Phase Frequency Detector Frequency	RF/256		20	MHz	
TRANSMISSION PARAMETERS					
Data Rate					
FSK/GFSK	9.6		384	kbps	
FSK/GFSK Frequency Deviation	150		311.89	kHz	PFD = 10 MHz
	150		796	kHz	PFD = 20 MHz
Deviation Frequency Resolution	220			Hz	PFD = 3.625 MHz
Gaussian Filter BT		0.5			
Transmit Power[1]	−20		+13	dBm	V_{DD} = 3.0 V, T_A = 25°C
Transmit Power Variation vs. Temp.		±1		dB	From −40°C to +85°C
Transmit Power Variation vs. VDD		±1		dB	From 2.3 V to 3.6 V at 915 MHz, T_A = 25°C
Transmit Power Flatness		±1		dB	From 902 MHz to 928 MHz, 3 V, T_A = 25°C
Programmable Step Size					
−20 dBm to +13 dBm		0.3125		dB	
Spurious Emissions during PLL Settling			TBD	dBm	
Integer Boundary		−55		dBc	50 kHz loop BW
Reference		−65		dBc	
Harmonics					
Second Harmonic		−27	−18	dBc	Unfiltered conductive
Third Harmonic		−21	−18	dBc	
All Other Harmonics			−35	dBc	
VCO Frequency Pulling		TBD		kHz rms	DR = 9.6 kbps
Optimum PA Load Impedance		39 + j61		Ω	FRF = 915 MHz
		48 + j54		Ω	FRF = 868 MHz
		54 + j94		Ω	FRF = 433 MHz
RECEIVER PARAMETERS					
FSK/GFSK Input Sensitivity					At BER = 1E − 3, FRF = 915 MHz, LNA and PA matched separately[2]
Sensitivity at 115.2 kbps		−102.6		dBm	FDEV = 200 kHz, LPF B/W = ±300kHz
Sensitivity at 172.8 kbps		−100.6		dBm	FDEV = 200 kHz, LPF B/W = ±450kHz
Sensitivity at 345.6 kbps		−96.3		dBm	FDEV = 300 kHz, LPF B/W = ±600kHz
Baseband Filter Bandwidths					Programmable
		±300		kHz	
		±450		kHz	
		±600		kHz	
LNA and Mixer, Input IP3					
Enhanced Linearity Mode		TBD		dBm	Pin = −20 dBm, 2 CW interferers
Low Current Mode		TBD		dBm	FRF = 915 MHz, f1 = FRF + 3 MHz
High Sensitivity Mode		TBD		dBm	F2 = FRF + 6 MHz, maximum gain
Rx Spurious Emissions[3]			TBD	dBm	<1 GHz at antenna input
			TBD	dBm	>1 GHz at antenna input
CHANNEL FILTERING					
Adjacent Channel Rejection (Offset = ±1 × IF Filter BW Setting)		TBD		dB	

Parameter	Min	Typ	Max	Unit	Test Conditions
Second Adjacent Channel Rejection (Offset = ±2 × IF Filter BW Setting)		TBD		dB	
Third Adjacent Channel Rejection (Offset = ±3 × IF Filter BW Setting)		TBD		dB	
Image Channel Rejection		TBD		dB	
CO-CHANNEL REJECTION		TBD		dB	
Wide-Band Interference Rejection		70		dB	Swept from 100 MHz to 2 GHz, measured as channel rejection
BLOCKING:					Desired signal 3 dB above the input sensitivity level, CW interferer power level increased until BER = 10^{-2}
+/- 1MHz		TBD		dB	
+/- 5MHz		TBD		dB	
+/- 10MHz		TBD		dB	
+/- 10MHz (High Linearity Mode)		TBD		dB	
Saturation (Maximum Input Level)		12		dBm	FSK mode, BER = 10^{-3}
LNA Input Impedance		24 – j60		Ω	FRF = 915 MHz, RFIN to GND
		26 – j63		Ω	FRF = 868 MHz
		71 – j128		Ω	FRF = 433 MHz
RSSI					
Range at Input		−100 to −36		dBm	
Linearity		±2		dB	
Absolute Accuracy		±3		dB	
Response Time		150		µs	
PHASE-LOCKED LOOP					
VCO Gain		65		MHz/V	902 MHz to 928 MHz band, VCO adjust = 0, VCO_BIAS_SETTING = 8
		130		MHz/V	860 MHz to 870 MHz band, VCO adjust = 0
		65		MHz/V	433 MHz, VCO adjust = 0
Phase Noise (In-Band)		−89		dBc/Hz	PA = 0 dBm, V_{DD} = 3.0 V, PFD = 10 MHz, FRF = 915 MHz, VCO_BIAS_SETTING = 8
Phase Noise (Out-of-Band)		−110		dBc/Hz	1 MHz offset
Residual FM		128		Hz	From 200 Hz to 20 kHz, FRF = 868MHz
PLL Settling Time		40		µs	Measured for a 10 MHz frequency step to within 5 ppm accuracy, PFD = 20 MHz, LBW = 50kHz
REFERENCE INPUT					
Crystal Reference	3.625		24	MHz	
External Oscillator	3.625		24	MHz	
Load Capacitance		33		pF	
Crystal Start-Up Time		1.0		ms	Using 33 pF load capacitors
Input Level				CMOS levels	
TIMING INFORMATION					
Chip Enabled to Regulator Ready			TBD	µs	C_{REG} = 100 nF
Crystal Oscillator Startup Time		1		ms	With 19.2 MHz XTAL
Tx to Rx Turnaround Time		150 µs + (5 × T_{BIT})			Time to synchronized data, includes AGC settling.
LOGIC INPUTS					
Input High Voltage, V_{INH}	0.7 × V_{DD}			V	
Input Low Voltage, V_{INL}			0.2 × V_{DD}	V	
Input Current, I_{INH}/I_{INL}			±1	µA	
Input Capacitance, C_{IN}			10	pF	

Parameter	Min	Typ	Max	Unit	Test Conditions
Control Clock Input			50	MHz	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	DV_{DD} – 0.4			V	I_{OH} = 500 µA
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 500 µA
CLK_{OUT} Rise/Fall			5	ns	
CLK_{OUT} Load			10	pF	
TEMPERATURE RANGE—T_A	−40		+85	°C	
POWER SUPPLIES					
Voltage Supply					
V_{DD}	2.3		3.6	V	All V_{DD} pins must be tied together
Transmit Current Consumption					FRF = 915 MHz, V_{DD} = 3.0 V, PA is matched in to 50 Ω
−20 dBm		14.6		mA	
−10 dBm		15.8		mA	
0 dBm		19.3		mA	
10 dBm		28		mA	
Receive Current Consumption					
Low Current Mode		19		mA	
High Sensitivity Mode		21		mA	
Power-Down Mode					
Low Power Sleep Mode		0.1	1	µA	

[1] Measured as maximum unmodulated power. Output power varies with both supply and temperature.
[2] Sensitivity for combined matching network case is typically 2 dB less than separate matching networks.
[3] Follow the matching and layout guidelines to achieve the relevant FCC/ETSI specifications.

TIMING CHARACTERISTICS

V_{DD} = 3 V ± 10%; VGND = 0 V, T_A = 25°C, unless otherwise noted.
Guaranteed by design, but not production tested.

Table 2.

Parameter	Limit at T_{MIN} to T_{MAX}	Unit	Test Conditions/Comments
t_1	<10	ns	SDATA to SCLK Setup Time
t_2	<10	ns	SDATA to SCLK Hold Time
t_3	<25	ns	SCLK High Duration
t_4	<25	ns	SCLK Low Duration
t_5	<10	ns	SCLK to SLE Setup Time
t_6	<20	ns	SLE Pulse Width
t_7	<TBD	ns	SLE to SCLK Setup Time, Readback
t_8	<TBD	ns	SCLK to SREAD Data Valid, Readback
t_9	<TBD	ns	SREAD Hold Time after SCLK, Readback
t_{10}	<TBD	ns	SCLK to SLE Disable Time, Readback

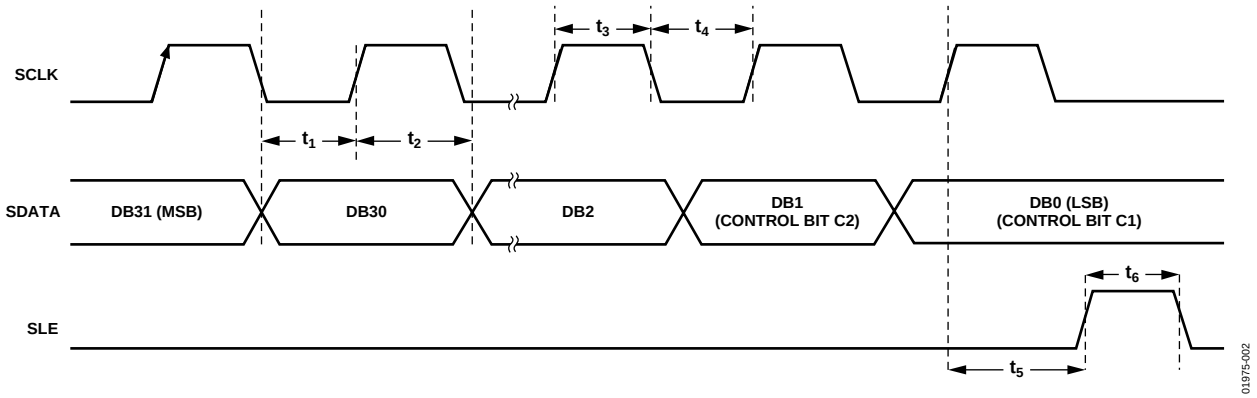

Figure 2. Serial Interface Timing Diagram

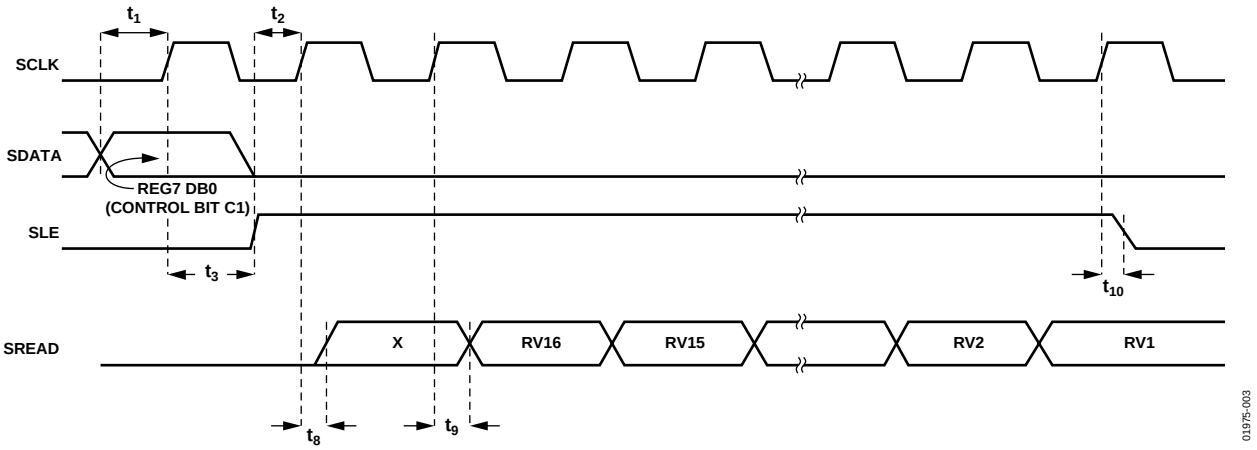

Figure 3. Readback Timing Diagram

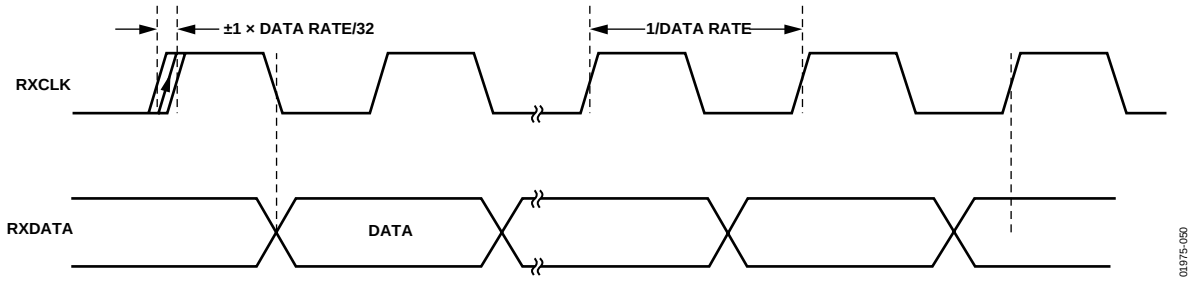

Figure 4. RxData/RxCLK Timing Diagram

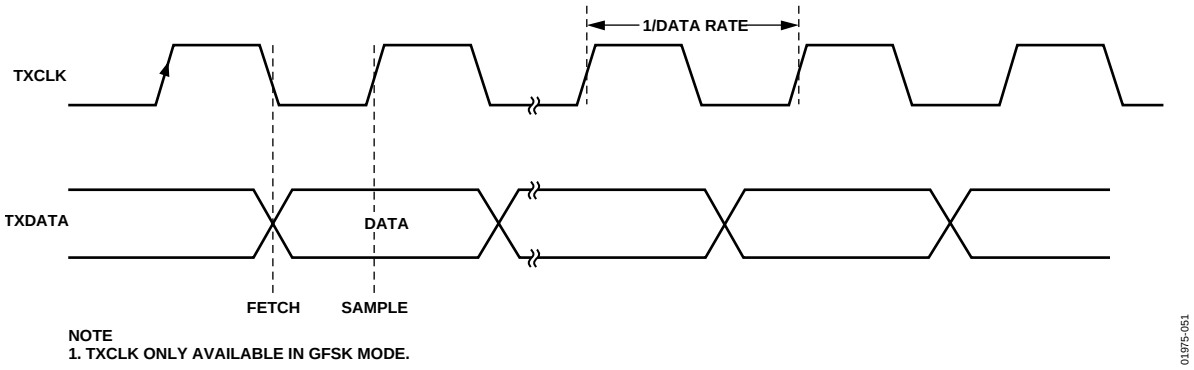

Figure 5. TxData/TxCLK Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND[1]	−0.3 V to +5 V
Analog I/O Voltage to GND	−0.3 V to AV_{DD} + 0.3 V
Digital I/O Voltage to GND	−0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	125°C
MLF θ_{JA} Thermal Impedance	TBD°C/W
Lead Temperature Soldering	
Vapor Phase (60 s)	235°C
Infrared (15 s)	240°C

[1] GND = CPGND = RFGND = DGND = AGND = 0 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high-performance RF integrated circuit with an ESD rating of <2 kV and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

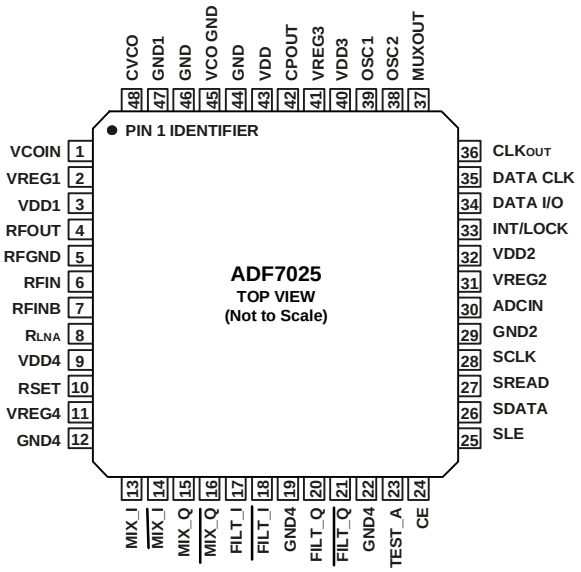

Figure 6. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	VCOIN	The tuning voltage on this pin determines the output frequency of the voltage controlled oscillator (VCO). The higher the tuning voltage, the higher the output frequency.
2	VREG1	Regulator Voltage for PA Block. A 100 nF in parallel with a 5.1 pF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
3	VDD1	Voltage Supply for PA Block. Decoupling capacitors of 0.1 µF and 10pF should be placed as close as possible to this pin. All VDD pins should be tied together.
4	RFOUT	The modulated signal is available at this pin. Output power levels are from −20 dBm to +13 dBm. The output should be impedance matched to the desired load using suitable components. See the Transmitter section.
5	RFGND	Ground for Output Stage of Transmitter.
6	RFIN	LNA Input for Receiver Section. Input matching is required between the antenna and the differential LNA input to ensure maximum power transfer. See the LNA/PA Matching section.
7	RFINB	Complementary LNA Input. See the LNA/PA Matching section.
8	R_{LNA}	External bias resistor for LNA. Optimum resistor is 1.1 kΩ with 5% tolerance.
9	VDD4	Voltage supply for LNA/MIXER block. This pin should be decoupled to ground with a 10 nF capacitor.
10	RSET	External Resistor to Set Charge Pump Current and Some Internal Bias Currents. Use 3.6 kΩ with 5% tolerance.
11	VREG4	Regulator Voltage for LNA/MIXER block. A 100 nF capacitor should be placed between this pin and GND for regulator stability and noise rejection.
12	GND4	Ground for LNA/MIXER block.
13–18	MIX/FILT	Signal Chain Test Pins. These pins are high impedance under normal conditions and should be left unconnected.
19, 22	GND4	Ground for LNA/MIXER block.
20, 21, 23	FILT/TEST_A	Signal Chain Test Pins. These pins are high impedance under normal conditions and should be left unconnected.
24	CE	Chip Enable. Bringing CE low puts the ADF7025 into complete power-down. Register values are lost when CE is low, and the part must be reprogrammed once CE is brought high.
25	SLE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches. A latch is selected using the control bits.

Pin No.	Mnemonic	Function
26	SDATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs as the control bits. This pin is a high impedance CMOS input.
27	SREAD	Serial Data Output. This pin is used to feed readback data from the ADF7025 to the microcontroller. The SCLK input is used to clock each readback bit (ADC readback) from the SREAD pin.
28	SCLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This pin is a digital CMOS input.
29	GND2	Ground for Digital Section.
30	ADCIN	Analog-to-Digital Converter Input. The internal 7-bit ADC can be accessed through this pin. Full scale is 0 to 1.9 V. Readback is made using the SREAD pin.
31	VREG2	Regulator Voltage for Digital Block. A 100 nF in parallel with a 5.1 pF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
32	VDD2	Voltage Supply for Digital Block. A decoupling capacitor of 10 nF should be placed as close as possible to this pin.
33	INT/LOCK	Bidirectional Pin. In output mode (INTerrupt mode), the ADF7025 asserts the INT/ LOCK pin when it has found a match for the preamble sequence. In input mode (lock mode), the microcontroller can be used to lock the demodulator threshold when a valid preamble has been detected. Once the threshold is locked, NRZ data can be reliably received. In this mode, a demod lock can be asserted with minimum delay.
34	DATA I/O	Transmit Data Input/Received Data Output. This is a digital pin and normal CMOS levels apply.
35	DATA CLK	In receive mode, the pin outputs the synchronized data clock. The positive clock edge is matched to the center of the received data. In GFSK transmit mode, the pin outputs an accurate clock to latch the data from the microcontroller into the transmit section at the exact required data rate. See the Gaussian Frequency Shift Keying (GFSK) section.
36	CLKOUT	A Divided-Down Version of the Crystal Reference with Output Driver. The digital clock output can be used to drive several other CMOS inputs such as a microcontroller clock. The output has a 50:50 mark-space ratio.
37	MUXOUT	This pin provides the Lock_Detect signal, which is used to determine if the PLL is locked to the correct frequency. Other signals include Regulator_Ready, which is an indicator of the status of the serial interface regulator.
38	OSC2	The reference crystal should be connected between this pin and OSC1. A TCXO reference can be used by driving this pin with CMOS levels and disabling the crystal oscillator.
39	OSC1	The reference crystal should be connected between this pin and OSC2.
40	VDD3	Voltage Supply for the Charge Pump and PLL Dividers. This pin should be decoupled to ground with a 0.01 µF capacitor.
41	VREG3	Regulator Voltage for Charge Pump and PLL Dividers. A 100 nF in parallel with a 5.1 pF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
42	CPOUT	Charge Pump Output. This output generates current pulses that are integrated in the loop filter. The integrated current changes the control voltage on the input to the VCO.
43	VDD	Voltage Supply for VCO Tank Circuit. This pin should be decoupled to ground with a 0.01 µF capacitor.
44–47	GND	Grounds for VCO Block.
48	CVCO	A 22 nF capacitor should be placed between this pin and VREG1 to reduce VCO noise.

Typical Performance Characteristics

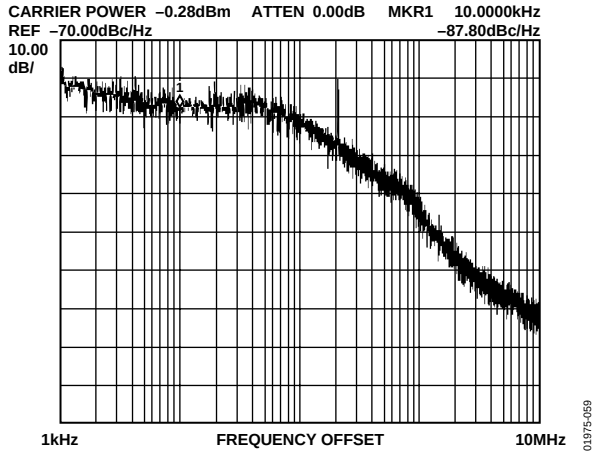

Figure 7. Phase Noise Response at 868.3MHz, VDD = 3.0 V, ICP = 1.5 mA

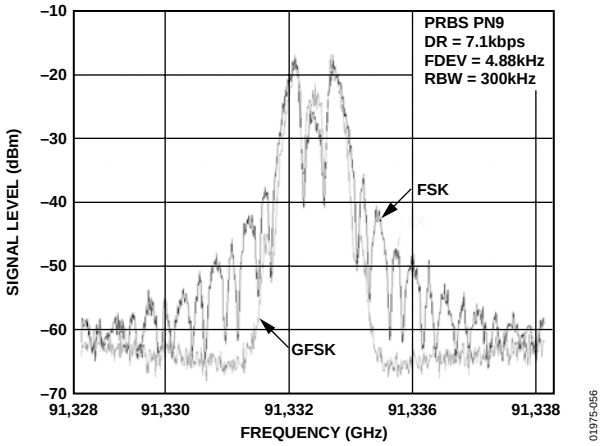

Figure 8. Output Spectrum in FSK and GFSK Modulation

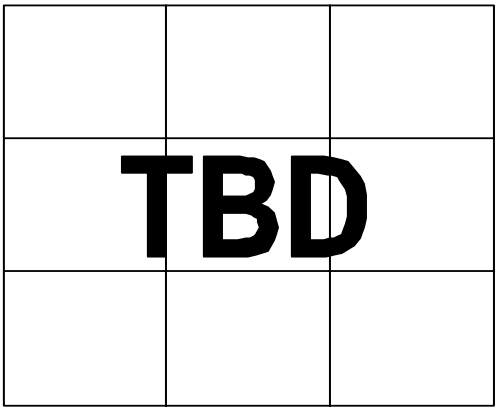

Figure 9.

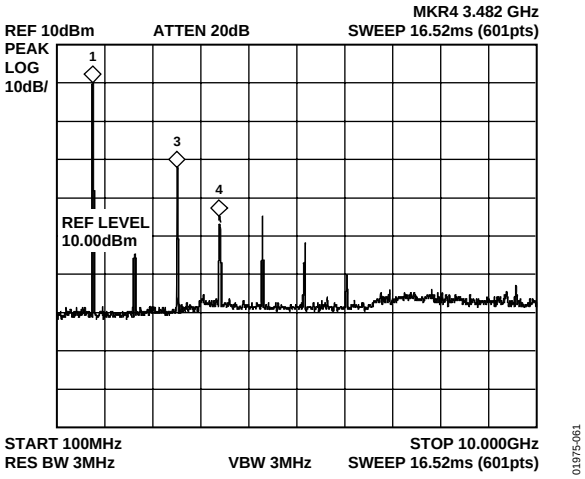

Figure 10. Harmonic Response, RF_{OUT} Matched to 50 Ω, No Filter

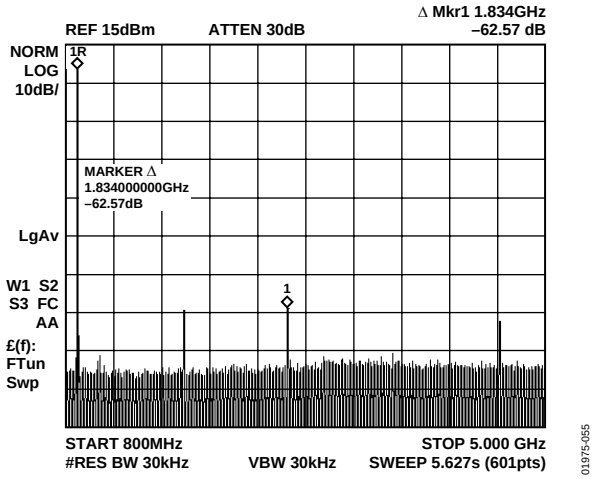

Figure 11. Harmonic Response, Murata Dielectric Filter

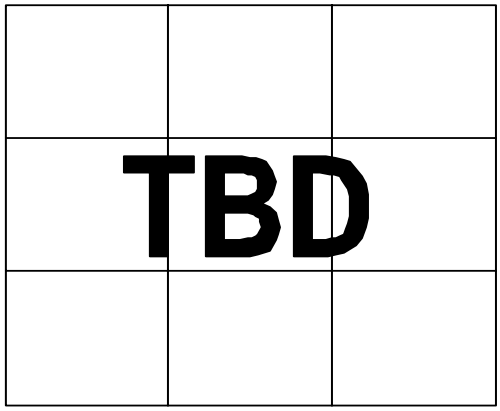

Figure 12.

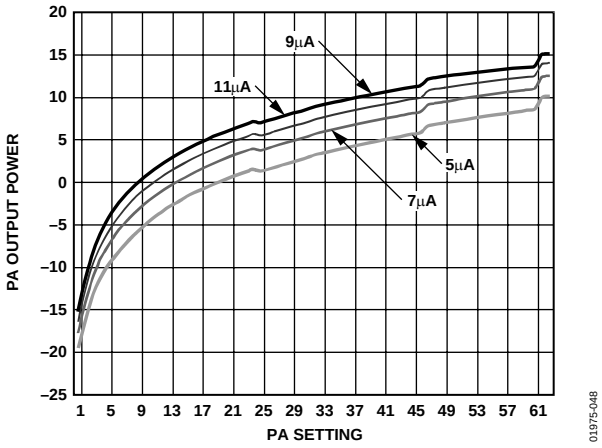

Figure 13. PA Output Power vs. Setting

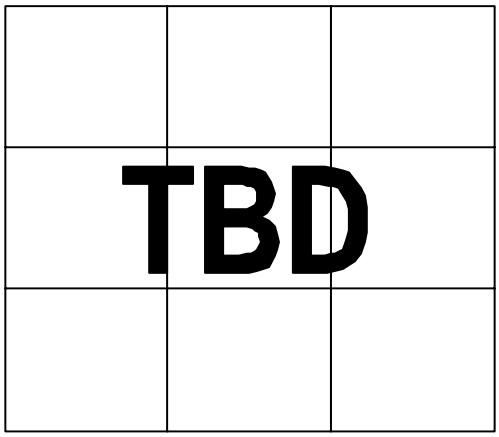

Figure 16. Sensitivity vs. VDD and Temperature

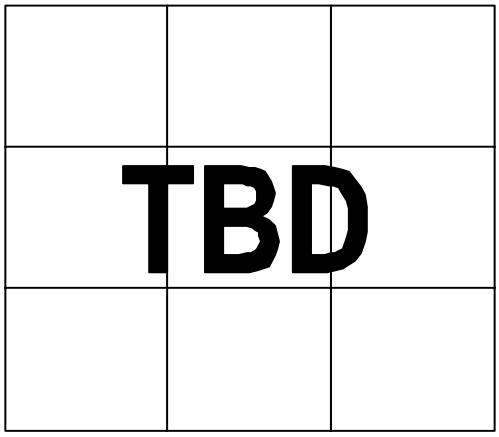

Figure 14. Wideband Interference Rejection.

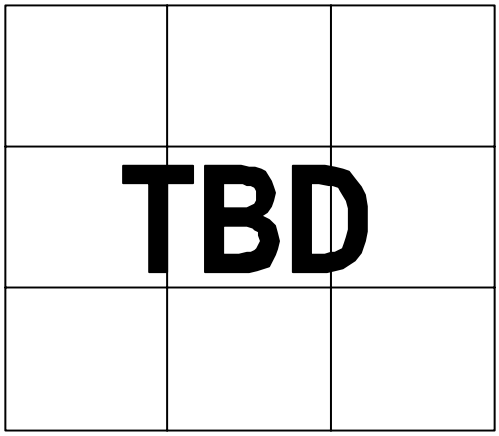

Figure 17. BER vs. Data-Rate (Combined Matching Network)

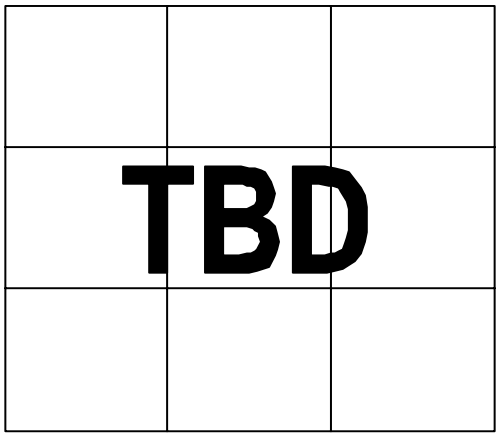

Figure 15. Interference Rejection Close-In, Showing Co-Channel

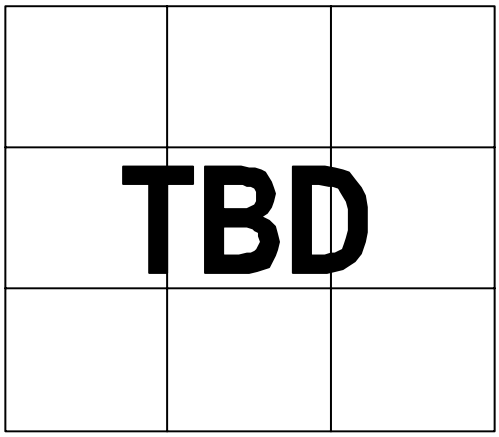

Figure 18.

FREQUENCY SYNTHESIZER

REFERENCE INPUT SECTION

The on-board crystal oscillator circuitry (Figure 19) can use an inexpensive quartz crystal as the PLL reference. The oscillator circuit is enabled by setting R1_DB12 high. It is enabled by default on power-up and is disabled by bringing CE low. Errors in the crystal can be corrected by adjusting the fractional-N value (see the N Counter section). A single-ended reference (TCXO, CXO) can also be used. The CMOS levels should be applied to OSC2 with R1_DB12 set low.

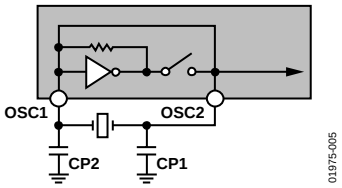

Figure 19. Oscillator Circuit on the ADF7025

Two parallel resonant capacitors are required for oscillation at the correct frequency; their values are dependent on the crystal specification. They should be chosen so that the series value of capacitance added to the PCB track capacitance adds up to the load capacitance of the crystal, usually 20 pF. Track capacitance values vary from 2 pF to 5 pF, depending on board layout. Where possible, choose capacitors that have a very low temperature coefficient to ensure stable frequency operation over all conditions.

CLKOUT Divider and Buffer

The CLKOUT circuit takes the reference clock signal from the oscillator section, shown in Figure 19, and supplies a divided-down 50:50 mark-space signal to the CLKOUT pin. An even divide from 2 to 30 is available. This divide number is set in R1_DB(8:11). On power-up, the CLKOUT defaults to divide-by-8.

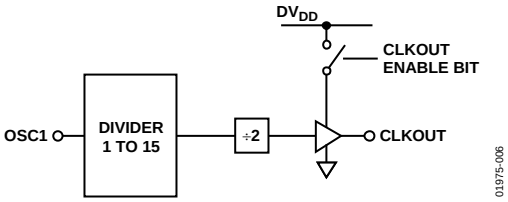

Figure 20. CLK_{OUT} Stage

To disable CLKOUT, set the divide number to 0. The output buffer can drive up to a 20 pF load with a 10% rise time at 4.8 MHz. Faster edges can result in some spurious feedthrough to the output. A small series resistor (50 Ω) can be used to slow the clock edges to reduce these spurs at F_{CLK}.

R Counter

The 3-bit R counter divides the reference input frequency by an integer from 1 to 7. The divided-down signal is presented as the reference clock to the phase frequency detector (PFD). The divide ratio is set in Register 1. Maximizing the PFD frequency reduces the N value. This reduces the noise multiplied at a rate of 20 log(N) to the output, as well as reducing occurrences of spurious components. The R Register defaults to R = 1 on power-up:

$$PFD\ [\text{Hz}] = XTAL/R$$

MUXOUT and Lock Detect

The MUXOUT pin allows the user to access various digital points in the ADF7025. The state of MUXOUT is controlled by Bits R0_DB(29:31).

Regulator Ready

REGULATOR READY is the default setting on MUXOUT after the transceiver has been powered up. The power-up time of the regulator is typically 50 µs. Because the serial interface is powered from the regulator, the regulator must be at its nominal voltage before the ADF7025 can be programmed. The status of the regulator can be monitored at MUXOUT. When the REGULATOR READY signal on MUXOUT is high, programming of the ADF7025 can begin.

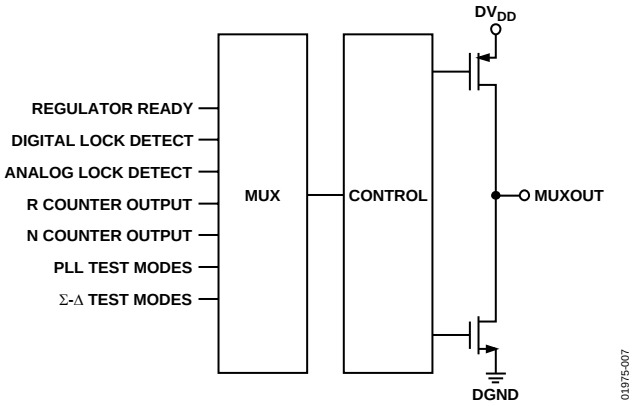

Figure 21. MUXOUT Circuit

Digital Lock Detect

Digital lock detect is active high. The lock detect circuit is located at the PFD. When the phase error on five consecutive cycles is less than 15 ns, lock detect is set high. Lock detect remains high until 25 ns phase error is detected at the PFD. Because no external components are needed for digital lock detect, it is more widely used than analog lock detect.

Analog Lock Detect

This N-channel open-drain lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When a lock has been detected, this output is high with narrow low-going pulses.

Voltage Regulators

The ADF7025 contains four regulators to supply stable voltages to the part. The nominal regulator voltage is 2.3 V. Each regulator should have a 100 nF capacitor connected between VREG and GND. When CE is high, the regulators and other associated circuitry are powered on, drawing a total supply current of 2 mA. Bringing the chip-enable pin low disables the regulators, reduces the supply current to less than 1 μA, and erases all values held in the registers. The serial interface operates off a regulator supply; therefore, to write to the part, the user must have CE high and the regulator voltage must be stabilized. Regulator status (VREG4) can be monitored using the regulator ready signal from MUXOUT.

Loop Filter

The loop filter integrates the current pulses from the charge pump to form a voltage that tunes the output of the VCO to the desired frequency. It also attenuates spurious levels generated by the PLL. A typical loop filter design is shown in Figure 22.

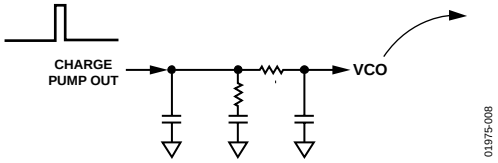

Figure 22. Typical Loop Filter Configuration

In FSK, the loop should be designed so that the loop bandwidth (LBW) is approximately five times the data rate. Widening the LBW excessively reduces the time spent jumping between frequencies, but can cause insufficient spurious attenuation.

Narrow-loop bandwidths can result in the loop taking long periods of time to attain lock. Careful design of the loop filter is critical to obtaining accurate FSK/GFSK modulation.

For GFSK, it is recommended that an LBW of 2.0 to 2.5 times the data rate be used to ensure that sufficient samples are taken of the input data while filtering system noise. The free design tool ADIsimPLL can be used to design loop filters for the ADF7025.

N Counter

The feedback divider in the ADF7025 PLL consists of an 8-bit integer counter and a 14-bit Σ-Δ fractional-N divider. The integer counter is the standard pulse-swallow type common in PLLs. This sets the minimum integer divide value to 31. The fractional divide value gives very fine resolution at the output, where the output frequency of the PLL is calculated as

$$F_{OUT} = \frac{XTAL}{R} \times \left(Integer\text{-}N + \frac{Fractional\text{ - }N}{2^{15}}\right)$$

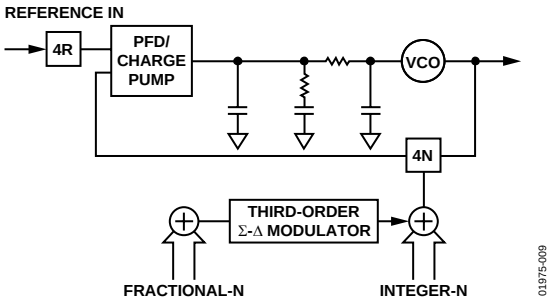

Figure 23. Fractional-N PLL

The combination of the integer-N (maximum = 255) and the fractional-N (maximum = 16383/16384) give a maximum N divider of 255 + 1. Therefore, the minimum usable PFD is

PDF_{MIN} [Hz] = *Maximum Required Output Frequency*/(255 + 1)

For example, when operating in the European 868 MHz to 870 MHz band, PFD_{MIN} equals 3.4 MHz.

Voltage Controlled Oscillator (VCO)

To minimize spurious emissions, the on-chip VCO operates from 1732 MHz to 1856 MHz. The VCO signal is then divided by 2 to give the required frequency for the transmitter and the required LO frequency for the receiver.

The VCO should be re-centered, depending on the required frequency of operation, by programming the VCO adjust bits R1_DB(20:21).

The VCO is enabled as part of the PLL by the PLL-enable bit, R0_DB28.

A further frequency divide-by-2 is included to allow operation in the lower 431 MHz to 478 MHz bands. To enable operation in these bands, R1_DB13 should be set to 1. The VCO needs an external 22 nF between the VCO and the regulator to reduce internal noise.

431-478MHz Operation

For operation in the 431 to 478 MHz band then the frequency divide by 2 has to be enabled. This is enabled by R1_DB13. As this divide is external to the synthesizer loop the feedback divider number (N+F) should programmed to a value twice the desired RF output frequency.

VCO Bias Current

VCO bias current can be adjusted using Bits R1_DB19 to R1_DB16. To ensure VCO oscillation, the minimum bias current setting under all conditions is 0x8.

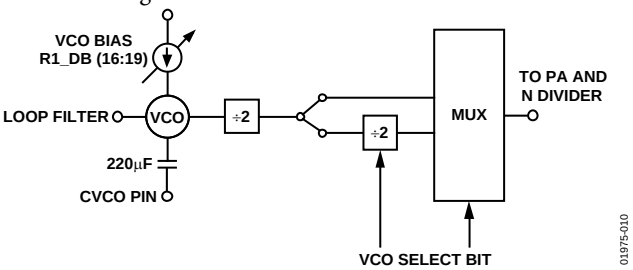

Figure 24. Voltage Controlled Oscillator (VCO)

CHOOSING CHANNELS FOR BEST SYSTEM PERFORMANCE

The fractional-N PLL allows the selection of any channel within 868 MHz to 928 MHz (and 433MHz using divide-by-2) to a resolution of <100 Hz. This also facilitates frequency hopping systems.

Careful selection of the RF transmit channels must be made to achieve best spurious performance. The architecture of fractional-N results in some level of the nearest integer channel moving through the loop to the RF output. These "beat-note" spurs are not attenuated by the loop, if the desired RF channel and the nearest integer channel are separated by a frequency of less than the LBW.

The occurrence of beat-note spurs is rare, because the integer frequencies are at multiples of the reference, which is typically >10 MHz.

Beat-note spurs can be significantly reduced in amplitude by avoiding very small or very large values in the fractional register, using the frequency doubler. By having a channel 1 MHz away from an integer frequency, a 100 kHz loop filter can reduce the level to less than−45 dBc.

TRANSMITTER

RF OUTPUT STAGE

The PA of the ADF7025 is based on a single-ended, controlled current, open-drain amplifier that has been designed to deliver up to 13 dBm into a 50 Ω load at a maximum frequency of 928 MHz.

The PA output current and, consequently, the output power are programmable over a wide range. The PA configuration in FSK/GFSK modulation modes is shown in Figure 25. In FSK/GFSK modulation mode, the output power is independent of the state of the DATA_IO pin. The output power can be adjusted as follows:

- FSK/GFSK: The output power is set using bits R2_DB(9:14).

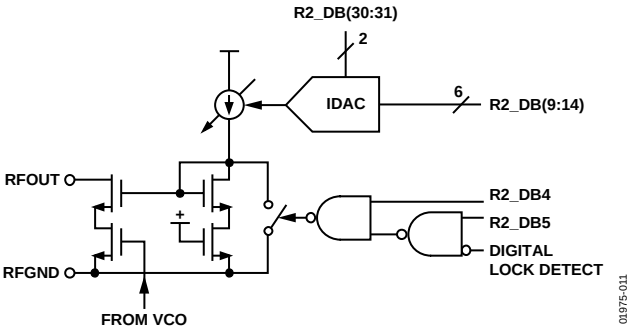

Figure 25. PA Configuration in FSK/GFSK Mode

The PA is equipped with overvoltage protection, which makes it robust in severe mismatch conditions. Depending on the application, one can design a matching network for the PA to exhibit optimum efficiency at the desired radiated output power level for a wide range of different antennas, such as loop or monopole antennas. See the LNA/PA Matching section for details.

PA Bias Currents and Mute PA until Lock Bit

Control Bits R2_DB(30:31) facilitate an adjustment of the PA bias current to further extend the output power control range, if necessary. If this feature is not required, the default value of 7 μA is recommended. The output stage is powered down by resetting Bit R2_DB4.

MODULATION SCHEMES

Frequency Shift Keying (FSK)

Frequency shift keying is implemented by setting the N value for the center frequency and then toggling this with the TxData line. The deviation from the center frequency is set using Bits R2_DB(15:23). The deviation from the center frequency in Hz is

$$FSK_{DEVIATION}\ [\text{Hz}] = \frac{PFD \times Modulation\ Number}{2^{14}}$$

where *Modulation Number* is a number from 1 to 511 (R2_DB(15:23)) .

Select FSK using Bits R2_DB(6:8).

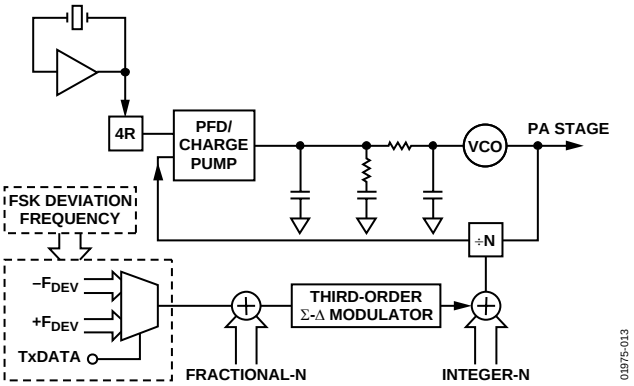

Figure 26. FSK Implementation

Gaussian Frequency Shift Keying (GFSK)

Gaussian frequency shift keying reduces the bandwidth occupied by the transmitted spectrum by digitally prefiltering the TxData. A TxCLK output line is provided from the ADF7025 for synchronization of TxData from the micro-controller. The TxCLK line can be connected to the clock input of a shift register that clocks data to the transmitter at the exact data rate.

Setting Up the ADF7025 for GFSK

To set up the frequency deviation, set the PFD and the mod control bits:

$$GFSK_{DEVIATION}\ [\text{Hz}] = \frac{PFD \times 2^{m}}{2^{12}}$$

where *m* is GFSK_MOD_CONTROL set using R2_DB(24:26).

To set up the GFSK data rate:

$$DR\,[\text{bps}] = \frac{PFD}{DIVIDER_FACTOR \times INDEX_COUNTER}$$

RECEIVER SECTION

RF FRONT END

The ADF7025 is based on a fully integrated, zero-IF receiver architecture. The zero-IF architecture minimizes power consumption and the external component count while avoiding the need for image rejection.

Figure 27 shows the structure of the receiver front end. The numerous programming options allow users to trade off sensitivity, linearity, and current consumption against each other in the way best suitable for their applications. To achieve a high level of resilience against spurious reception, the LNA features a differential input. Switch SW2 shorts the LNA input when transmit mode is selected (R0_DB27 = 0). This feature facilitates the design of a combined LNA/PA matching network, avoiding the need for an external Rx/Tx switch. See the LNA/PA Matching section for details on the design of the matching network.

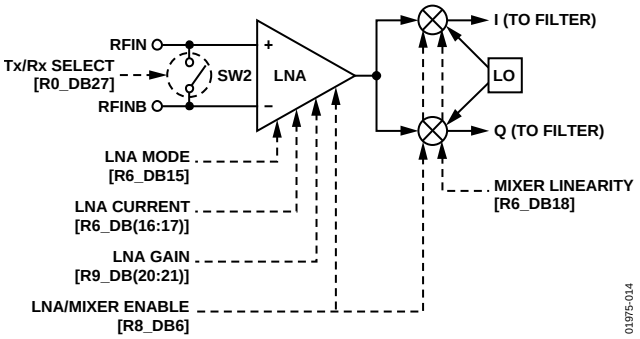

Figure 27. ADF7025 RF Front End

The LNA is followed by a quadrature down conversion mixer, which converts the RF signal direct to baseband. The output frequency of the synthesizer must be programmed to the value equal to the center frequency of the received channel.

The LNA has two basic operating modes: high gain/low noise mode and low gain/low power mode. To switch between these two modes, use the LNA_mode bit, R6_DB15. The mixer is also configurable between a low current and an enhanced linearity mode using the mixer_linearity bit, R6_DB18.

Based on the specific sensitivity and linearity requirements of the application, it is recommended to adjust control bits LNA_mode (R6_DB15) and mixer_linearity (R6_DB18) as outlined in Table 5.

The gain of the LNA is configured by the LNA_gain field, R9_DB(20:21), and can be set by either the user or the Automatic Gain Control (AGC) logic.

Filter Settings/Calibration

Out-of-band interference is rejected by means of a fifth-order low-pass filter (LPF). The bandwidth of the filter can be programmed between ±300kHz, 450kHz and ±600kHz by means of Control Bits R1_DB(22:23), and should be chosen as a compromise between interference rejection and attenuation of the desired signal.

To compensate for manufacturing tolerances, the LPF should be calibrated once after power-up. The LPF calibration logic requires that the LPF divider in Bits R6_DB(20:28) be set dependent on the crystal frequency. Once initiated by setting Bit R6_DB19, the calibration is performed automatically without any user intervention. The calibration time is 200 µs, during which the ADF7025 should not be accessed. It is important not to initiate the calibration cycle before the crystal oscillator has fully settled. If the AGC loop is disabled, the gain of LPF can be set to three levels using the filter_gain field, R9_DB(20:21). The filter gain is adjusted automatically, if the AGC loop is enabled.

Table 5. LNA/Mixer Modes

Receiver Mode	LNA Mode (R6_DB15)	LNA Gain Value R9_DB(21:20)	Mixer Linearity (R6_DB18)	Sensitivity (DR = 100 kbps, f_{DEV} = 200 kHz)	Rx Current Consumption (mA)	Input IP3 (dBm)
High Sensitivity Mode (default)	0	30	0	TBD	TBD	TBD
RxMode2	1	10	0	TBD	TBD	TBD
Low Current Mode	1	3	0	TBD	TBD	TBD
Enhanced Linearity Mode	1	3	1	TBD	TBD	TBD
RxMode5	1	10	1	TBD	TBD	TBD
RxMode6	0	30	1	TBD	TBD	TBD

RSSI/AGC SECTION

The RSSI is implemented as a successive compression log amp following the base-band channel filtering. The log amp achieves ±3 dB log linearity. It also doubles as a limiter to convert the signal-to-digital levels for the FSK demodulator. Offset correction is achieved using a switched capacitor integrator in feedback around the log amp. This uses the BB offset clock divide. The RSSI level is converted for user readback and digitally controlled AGC by an 80-level (7-bit) flash ADC. This level can be converted to input power in dBm.

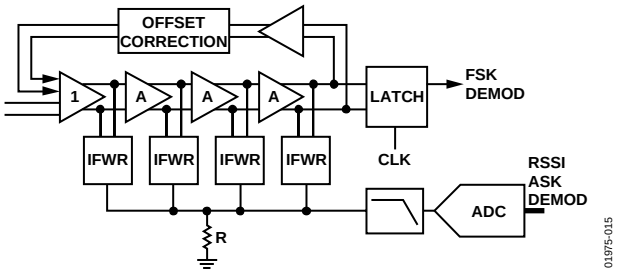

Figure 28. RSSI Block Diagram

RSSI Thresholds

When the RSSI is above AGC_HIGH_THRESHOLD, the gain is reduced. When the RSSI is below AGC_LOW_THRESHOLD, the gain is increased. A delay (AGC_DELAY) is programmed to allow for settling of the loop. The user programs the two threshold values (recommended defaults, 27 and 76) and the delay (default, 10). The default AGC setup values should be adequate for most applications. The threshold values must be chosen to be more than 30 apart for the AGC to operate correctly.

Offset Correction Clock

In Register 3, the user should set the BB offset clock divide bits R3_DB(4:5) to give an offset clock between 1 MHz and 2 MHz, where:

$$BBOS_CLK\ [\text{Hz}] = XTAL/(BBOS_CLK_DIVIDE)$$

BBOS_CLK_DIVIDE can be set to 4, 8, or 16.

AGC Information

In Register 9, the user should select automatic gain control by selecting auto in R9_DB18 and auto in R9_DB19. The user should then program AGC low threshold R9_DB(4:10) and AGC high threshold R9_DB(11:17). The recommended/default values for the low and high thresholds are 27 and 76, respectively. In the AGC2 register the user should program the AGC delay to be long enough to allow the loop to settle. The recommended value is 10.

RSSI Formula (Converting to dBm)

$$Input_Power\ [\text{dBm}] = -98\text{dBm} + (Readback_Code + Gain_Mode_Correction) \times 0.5$$

where:

Readback_Code is given by Bits RV7 to RV1 in the readback register (see Readback Format section).

Gain_Mode_Correction is given by the values in Table 6.

LNA gain and filter gain (LG2/LG1, FG2/FG1) are also obtained from the readback register.

Table 6. Gain Mode Correction

LNA Gain (LG2, LG1)	Filter Gain (FG2, FG1)	Gain Mode Correction
H (11)	H (10)	0
M (10)	H (10)	17
M (10)	M (01)	53
M (10)	L (00)	65
L (01)	L (00)	90
EL (00)	L (00)	113

These numbers are for an un-modulated tone. For a modulated signal the RSSI value will generally be about 1dB less. An additional factor should be introduced for this. An additional factor should also be introduced to account for losses in the front-end matching network/antenna.

FSK DEMODULATORS ON THE ADF7025

The two FSK demodulators on the ADF7025 are

- FSK correlator/demodulator
- Linear demodulator

Select these using the demod select bits, R4_DB(4:5).

FSK CORRELATOR/DEMODULATOR

The quadrature outputs of the IF filter are first limited and then fed to a pair of digital frequency correlators that perform bandpass filtering of the binary FSK frequencies at (IF + F_{DEV}) and (IF − F_{DEV}). Data is recovered by comparing the output levels from each of the two correlators. The performance of this frequency discriminator approximates that of a matched filter detector, which is known to provide optimum detection in the presence of AWGN.

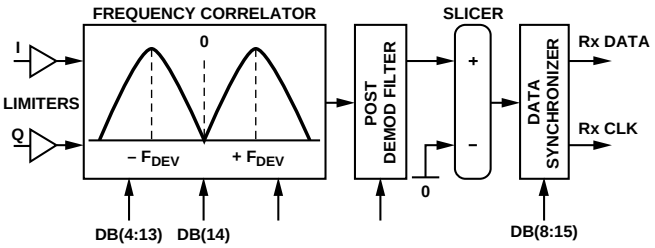

Figure 29. FSK Correlator/Demodulator Block Diagram

Postdemodulator Filter

A second-order, digital low-pass filter removes excess noise from the demodulated bit stream at the output of the discriminator. The bandwidth of this postdemodulator filter is programmable and must be optimized for the user's data rate. If the bandwidth is set too narrow, performance is degraded due to intersymbol interference (ISI). If the bandwidth is set too wide, excess noise degrades the receiver's performance. Typically, the 3 dB bandwidth of this filter is set at approximately 0.75 times the user's data rate, using Bits R4_DB(6:15).

Bit Slicer

The received data is recovered by threshold detecting the output of the postdemodulator low-pass filter. In the correlator/demodulator, the binary output signal levels of the frequency discriminator are always centered on zero. Therefore, the slicer threshold level can be fixed at zero and the demodulator performance is independent of the run-length constraints of the transmit data bit stream. This results in robust data recovery, which does not suffer from the classic baseline wander problems that exist in the more traditional FSK demodulators.

Data Synchronizer

An oversampled digital PLL is used to resynchronize the received bit stream to a local clock. The oversampled clock rate of the PLL (CDR_CLK) must be set at 32 times the data rate. See the notes for the Register 3—Receiver Clock Register section for a definition of how to program. The clock recovery PLL can accommodate frequency errors of up to ±2%.

FSK Correlator Register Settings

To enable the FSK correlator/demodulator, Bits R4_DB(5:4) should be set to [01]. To achieve best performance, the bandwidth of the FSK correlator must be optimized for the specific deviation frequency that is used by the FSK transmitter.

The discriminator BW is controlled in Register 6 by R6_DB(4:13) and is defined as

$$Discriminator_BW = DEMOD_CLK / (4 \times \text{Fdev})$$

where:

DEMOD_CLK is as defined in the Register 3—Receiver Clock Register section, Note 2.

Fdev is the deviation from the carrier frequency in FSK/GFSK modulation.

Postdemodulator Bandwidth Register Settings

The 3 dB bandwidth of the postdemodulator filter is controlled by Bits R4_ DB(6:15) and is given by

$$Post_Demod_BWSetting = \frac{2^{10} \times 2\pi \times F_{CUTOFF}}{DEMOD_CLK}$$

where F_{CUTOFF} is the target 3 dB bandwidth in Hz of the postdemodulator filter. This should typically be set to 0.75 times the data rate (DR).

Some sample settings for the FSK correlator/demodulator are

$DEMOD_CLK = 11.0592\text{MHz}$
$DR = 200$ kbps
$F_{DEV} = 300$ kHz

Therefore,

$F_{CUTOFF} = 0.75 \times 200 \times 10^3$ Hz
$Post_Demod_BW = 2^{11}\ \pi\ 150\times 10^3$ Hz/(11.0592MHz)
$Post_Demod_BW = Round(87.266) = 87$

and

$Discriminator_BW = (11.0592\text{ MHz})/(4 \times 300 \times 10^3) = 9.21$
$= 9$ (rounded to nearest integer)

Table 7. Register Settings

Setting Name	Register Address	Value
Post_Demod_BW	R4_DB(6:15)	0x09
Discriminator BW	R6_DB(4:13)	0x58

LINEAR FSK DEMODULATOR

A block diagram of the linear FSK demodulator is shown in Figure 30.

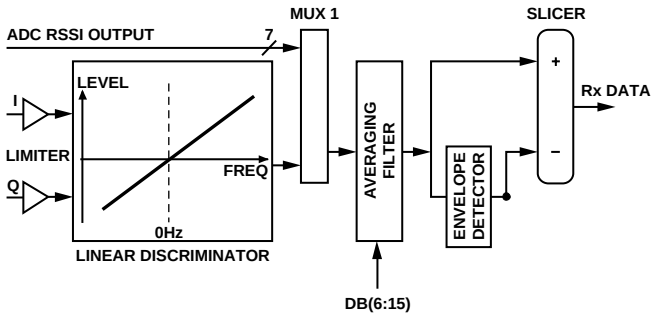

Figure 30. Block Diagram of Linear FSK Demodulator

This method of frequency demodulation is useful when very short preamble length is required.

A digital frequency discriminator provides an output signal that is linearly proportional to the frequency of the limiter outputs. The discriminator output is then filtered and averaged using a combined averaging filter and envelope detector. The demodulated FSK data is recovered by threshold-detecting the output of the averaging filter, as shown in Figure 30. In this mode, the slicer output shown in Figure 30 is routed to the data synchronizer PLL for clock synchronization. To enable the linear FSK demodulator, set Bits R4_DB(4:5) to [00].

The 3 dB bandwidth of the postdemodulation filter is set in the same way as the FSK correlator/demodulator, which is set in R4_DB(6:15) and is defined as

$$Post_Demod_BW_Setting = \frac{2^{10} \times 2\pi \times F_{CUTOFF}}{DEMOD_CLK}$$

where:

F_{CUTOFF} is the target 3 dB bandwidth in Hz of the postdemodulator filter.
DEMOD_CLK is as defined in the Register 3—Receiver Clock Register section, Note 2.

AUTOMATIC SYNC WORD RECOGNITION

The ADF7025 also supports automatic detection of the sync or ID fields. To activate this mode, the sync (or ID) word must be preprogrammed into the ADF7025. In receive mode, this preprogrammed word is compared to the received bit stream and, when a valid match is identified, the external pin INT/LOCK is asserted by the ADF7025.

This feature can be used to alert the microprocessor that a valid channel has been detected. It relaxes the computational requirements of the microprocessor and reduces the overall power consumption. The INT/LOCK is automatically de-asserted again after nine data clock cycles.

The automatic sync/ID word detection feature is enabled by selecting demod mode 2 or 3 in the demodulator setup register. Do this by setting R4_DB(25:23) = [010] or [011]. Bits R5_DB(4:5) are used to set the length of the sync/ID word, which can be either 12, 16, 20, or 24 bits long. The transmitter must transmit the MSB of the sync byte first and the LSB last to ensure proper alignment in the receiver sync byte detection hardware.

For systems using FEC, an error tolerance parameter can also be programmed that accepts a valid match when up to three bits of the word are incorrect. The error tolerance value is assigned in R5_DB(6:7).

APPLICATIONS SECTION

LNA/PA MATCHING

The ADF7025 exhibits optimum performance in terms of sensitivity, transmit power, and current consumption only if its RF input and output ports are properly matched to the antenna impedance. For cost-sensitive applications, the ADF7025 is equipped with an internal Rx/Tx switch, which facilitates the use of a simple combined passive PA/LNA matching network. Alternatively, an external Rx/Tx switch such as the Analog Devices ADG919 can be used, which yields a slightly improved receiver sensitivity and lower transmitter power consumption.

External Rx/Tx Switch

Figure 31 shows a configuration using an external Rx/Tx switch. This configuration allows an independent optimization of the matching and filter network in the transmit and receive path, and is, therefore, more flexible and less difficult to design than the configuration using the internal Rx/Tx switch. The PA is biased through inductor L1, while C1 blocks dc current. Both elements, L1 and C1, also form the matching network, which transforms the source impedance into the optimum PA load impedance, Z_{OPT}_PA.

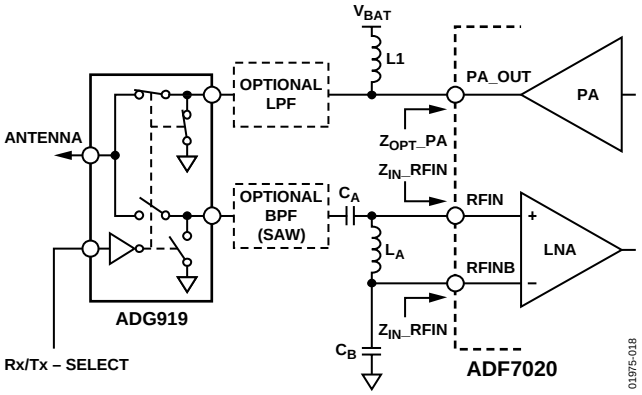

Figure 31. ADF7025 with External Rx/Tx Switch

Z_{OPT}_PA depends on various factors such as the required output power, the frequency range, the supply voltage range, and the temperature range. Selecting an appropriate Z_{OPT}_PA helps to minimize the Tx current consumption in the application. This datasheet contains a number of Z_{OPT}_PA values for representative conditions. Under certain conditions, however, it is recommended to obtain a suitable Z_{OPT}_PA value by means of a load-pull measurement.

Due to the differential LNA input, the LNA matching network must be designed to provide both a single-ended to differential conversion and a complex conjugate impedance match. The network with the lowest component count that can satisfy these requirements is the configuration shown in Figure 31, which consists of two capacitors and one inductor. A first-order implementation of the matching network can be obtained by understanding the arrangement as two L-type matching networks in a back-to-back configuration. Due to the asymmetry of the network with respect to ground, a compromise between the input reflection coefficient and the maximum differential signal swing at the LNA input must be established. The use of appropriate CAD software is strongly recommended for this optimization.

Depending on the antenna configuration, the user might need a harmonic filter at the PA output to satisfy the spurious emission requirement of the applicable government regulations. The harmonic filter can be implemented in various ways, such as a discrete LC-filter. Dielectric low-pass filter components such as the LFL18924MTC1A052 (for operation in the 915 MHz band), or LFL18869MTC2A160 (for operation in the 868 MHz band), both by Murata Mfg. Co., Ltd., represent an attractive alternative to discrete designs. The immunity of the ADF7025 to strong out-of-band interference can be improved by adding a band-pass filter in the Rx path. Apart from discrete designs, SAW or dielectric filter components such as the SAFCH869MAM0T00B0S, SAFCH915MAL0N00B0S, DCFB2869MLEJAA-TT1, or DCFB3915MLDJAA-TT1, all by Murata Mfg. Co., Ltd., are well suited for this purpose.

Internal Rx/Tx Switch

Figure 32 shows the ADF7025 in a configuration where the internal Rx/Tx switch is used with a combined LNA/PA matching network. Depending on the application, the slight performance degradation caused by the internal Rx/Tx switch might be acceptable, allowing the user to take advantage of the cost-saving potential of this solution. The design of the combined matching network must compensate for the reactance presented by the networks in the Tx and the Rx paths, taking the state of the Rx/Tx switch into consideration.

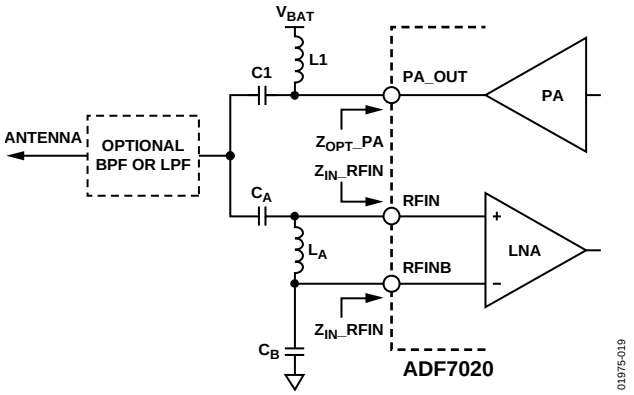

Figure 32. ADF7025 with Internal Rx/Tx Switch

The procedure typically requires several iterations until an acceptable compromise has been reached. The successful implementation of a combined LNA/PA matching network for the ADF7025 is critically dependent on the availability of an accurate electrical model for the PC board. In this context, the

use of a suitable CAD package is strongly recommended. To avoid this effort, the reference design provided for the ADF7025 RF module can be used. Gerber files are available on request.

As with the external Rx/Tx switch, an additional LPF or BPF might be required to suppress harmonics in the transmit spectrum or to improve the resilience of the receiver against out-of-band interferers.

TRANSMIT PROTOCOL AND CODING CONSIDERATIONS

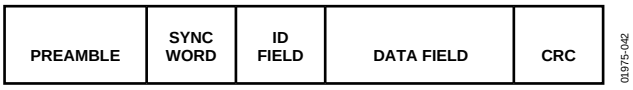

Figure 33. Typical Format of a Transmit Protocol

A dc-free preamble pattern is recommended for FSK/GFSK demodulation. The recommended preamble pattern is a dc-free pattern such as a 10101010… pattern. Preamble patterns with longer run-length constraints such as 11001100…. can also be used. However, this results in a longer synchronization time of the received bit stream in the receiver.

Manchester coding can be used for the entire transmit protocol. However, the remaining fields that follow the preamble header do not have to use dc-free coding. For these fields, the ADF7025 can accommodate coding schemes with a run-length of up to 6 bits without any performance degradation.

If longer run-length coding must be supported, the ADF7025 has several other features that can be activated. These involve a range of programmable options that allow the envelope detector output to be frozen after preamble acquisition.

DEVICE PROGRAMMING AFTER INITIAL POWER-UP

Table 8 lists the minimum number of writes needed to set up the ADF7025 in either Tx or Rx mode after CE is brought high. Additional registers can also be written to tailor the part to a particular application, such as setting up sync byte detection. When going from Tx to Rx or vice versa, the user needs to write only to the N Register to alter the LO by 200 kHz and to toggle the Tx/Rx bit.

Table 8. Minimum Register Writes Required for Tx/Rx Setup

Mode	Registers				
Tx	Reg 0	Reg 1	Reg 2		
Rx (G/FSK)	Reg 0	Reg 1	Reg 2	Reg 4	Reg 6
Tx <-> Rx	Reg 0				

Figure 36 and Figure 37 show the recommended programming sequence and associated timing for power-up from standby mode.

INTERFACING TO MICROCONTROLLER/DSP

Low level device drivers are available for interfacing to the ADF7025, the ADI ADuC84X microcontroller parts, or the Blackfin BF53X DSPs using the hardware connections shown in Figure and Figure 35.

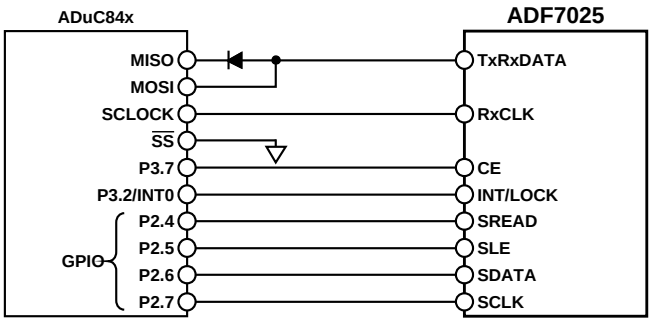

Figure 34. ADuC84X to ADF7025 Connection Diagram

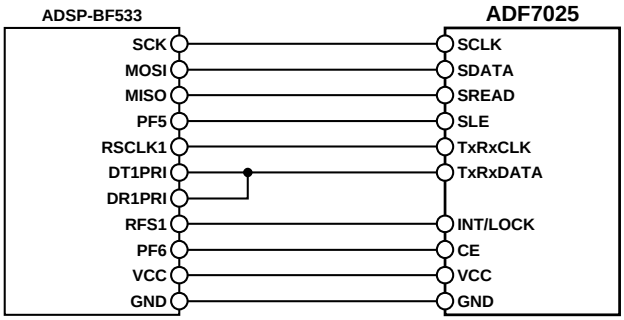

Figure 35. BF533 to ADF7025 Connection Diagram

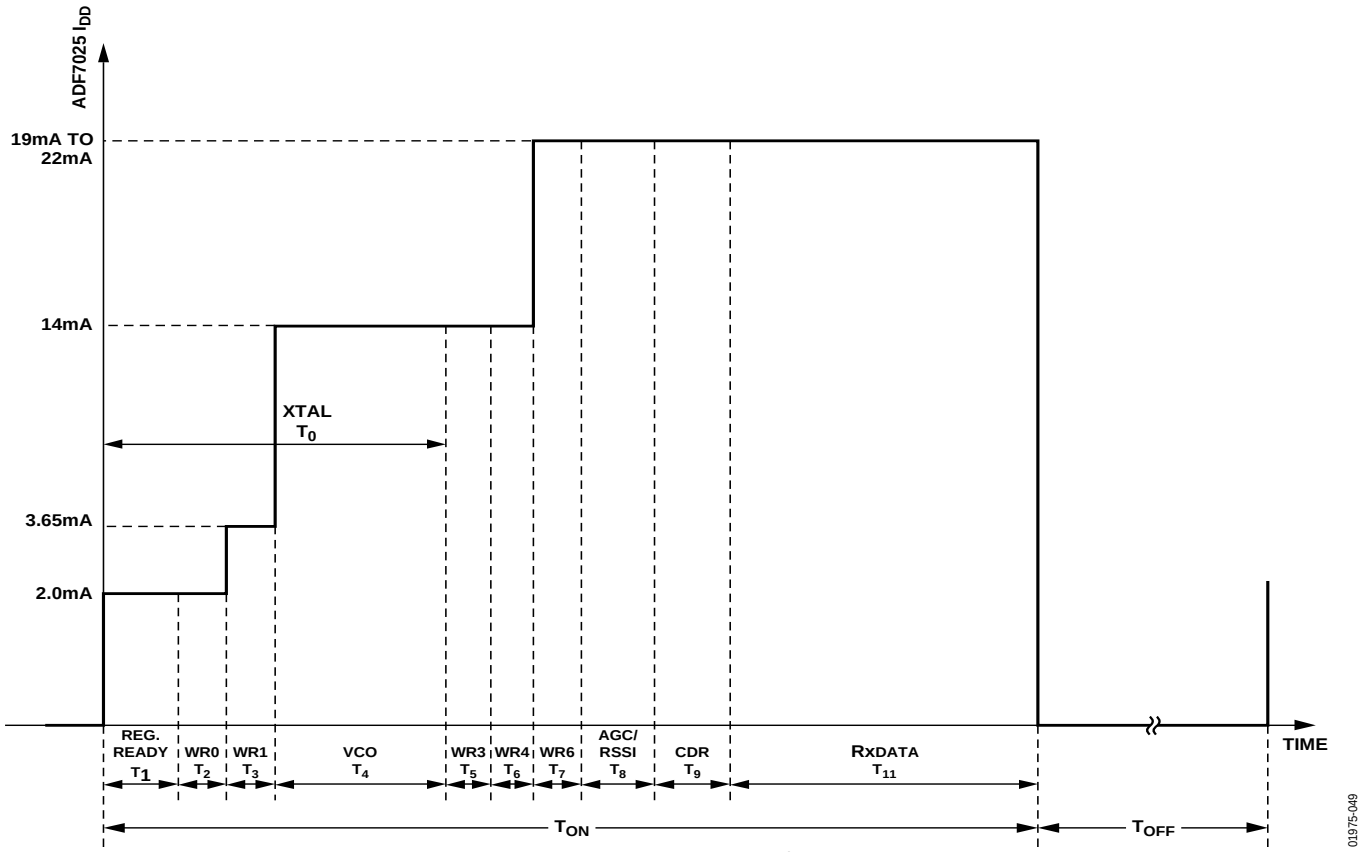

Figure 36. Rx Programming Sequence and Timing Diagram

Table 9: Power Up Sequence description

Parameter	Value	Description/Notes	Signal to Monitor
T0	2 ms	XTAL starts power-up after CE is brought high. This typically depends on the XTAL type and the load capacitance specified.	CLKOUT
T1	10 µs	Time for regulator to power up. The serial interface can be written to after this time.	Muxout
T2/T3/T5 /T6/T7	32 x 1/SPI_CLK	Time to write to a single register. Maximum SPI_CLK is 25 MHz.	
T4	1 ms	The VCO can power-up in parallel with the Xtal. This depends on the CVCO cpacitance value used. A value of 22 nF is recommended as a trade-off between phase noise performance and power-up time.	CVCO pin
T8	150 µs	This depends on the number of gain changes the AGC loop needs to cycle through and AGC settings programmed. This is described in more detail in the AGC Information and Timing Section.	Analog RSSI on TEST_A Pin
T9	5 x Bit_Period	This is the time for the clock and data recovery circuit to settle. This typically requires 5 bit transitions to acquire sync and is usually covered by the preamble.	
T11	Packet Length	Number of bits in payload by the bit period	

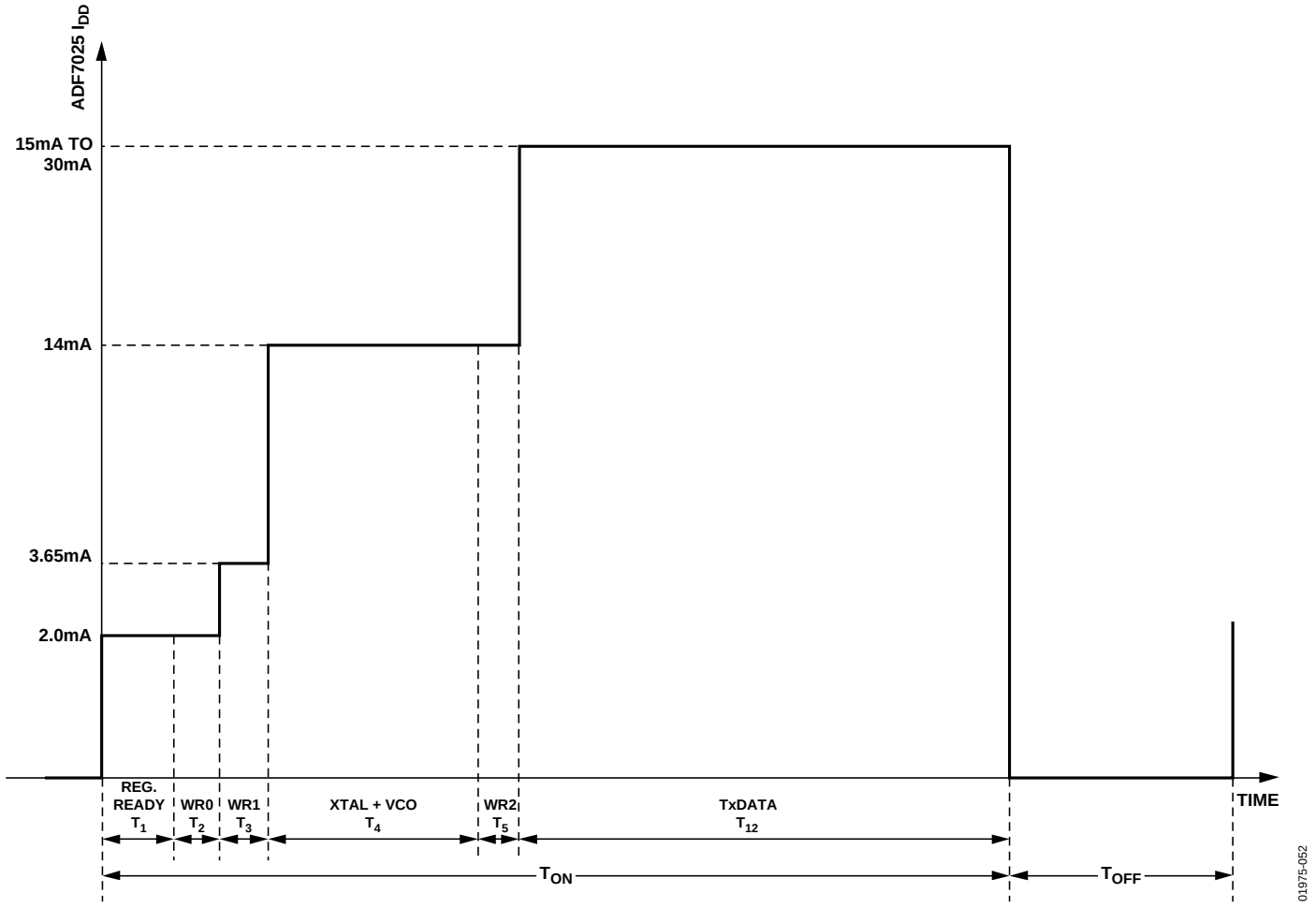

Figure 37. Tx Programming Sequence and Timing Diagram

SERIAL INTERFACE

The serial interface allows the user to program the eleven 32-bit registers using a 3-wire interface (SCLK, SDATA, and SLE). It consists of a level shifter, 32-bit shift register and eleven latches. Signals should be CMOS compatible. The serial interface is powered by the regulator, and, therefore, is inactive when CE is low.

Data is clocked into the register, MSB first, on the rising edge of each clock (SCLK). Data is transferred to one of eleven latches on the rising edge of SLE. The destination latch is determined by the value of the four control bits (C4 to C1). These are the bottom four LSBs, DB3 to DB0, as shown in the timing diagram in 3. Data can also be read back on the SREAD pin.

READBACK FORMAT

The readback operation is initiated by writing a valid control word to the readback register and setting the readback-enable bit (R7_DB8 = 1). The readback can begin after the control word has been latched with the SLE signal. SLE must be kept high while the data is being read out. Each active edge at the SCLK pin clocks the readback word out successively at the SREAD pin, as shown in Figure 38, starting with the MSB first. The data appearing at the first clock cycle following the latch operation must be ignored.

RSSI Readback

The RSSI readback operation yields valid results in Rx mode. The format of the readback word is shown in Figure 38. It is comprised of the RSSI level information (Bits RV1 to RV7), the current filter gain (FG1, FG2), and the current LNA gain (LG1, LG2) setting. The filter and LNA gain are coded in accordance with the definitions in Register 9. The input power can be calculated from the RSSI readback value as outlined in the RSSI/AGC Section.

Battery Voltage ADCIN/Temperature Sensor Readback

The battery voltage is measured at Pin VDD4. The readback information is contained in Bits RV1 to RV7. This also applies for the readback of the voltage at the ADCIN pin and the temperature sensor. From the readback information, the battery or ADCIN voltage can be determined using

$$V_{BATTERY} = (Battery_Voltage_Readback)/21.1$$
$$V_{ADCIN} = (ADCIN_Voltage_Readback)/42.1$$

Silicon Revision Readback

The silicon revision readback word is valid without setting any other registers, especially directly after power-up. The silicon revision word is coded with four quartets in BCD format. The product code (PC) is coded with two quartets extending from Bits RV9 to RV16. The revision code (RV) is coded with 1 quartets extending from Bits RV1 to RV8. The product code should read back as PC = 0x25. The current revision code should read as RC = 0x08.

Filter Calibration Readback

The filter calibration readback word is contained in Bits RV1 to RV8, and is for diagnostic purposes only. Using the automatic filter calibration function, accessible through Register 6, is recommended. Before filter calibration is initiated decimal 32 should be readback.

READBACK MODE	READBACK VALUE															
	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RSSI READBACK	X	X	X	X	X	LG2	LG1	FG2	FG1	RV7	RV6	RV5	RV4	RV3	RV2	RV1
BATTERY VOLTAGE/ADCIN/ TEMP. SENSOR READBACK	X	X	X	X	X	X	X	X	X	RV7	RV6	RV5	RV4	RV3	RV2	RV1
SILICON REVISION	RV16	RV15	RV14	RV13	RV12	RV11	RV10	RV9	RV8	RV7	RV6	RV5	RV4	RV3	RV2	RV1
FILTER CAL READBACK	0	0	0	0	0	0	0	0	RV8	RV7	RV6	RV5	RV4	RV3	RV2	RV1

Figure 38. Readback Value Table

REGISTER 0—N REGISTER

MUXOUT			PLL ENABLE	Tx/Rx	8-BIT INTEGER-N								15-BIT FRACTIONAL-N															ADDRESS BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
M3	M2	M1	PLE1	TR1	N8	N7	N6	N5	N4	N3	N2	N1	M15	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C4 (0)	C3 (0)	C2 (0)	C1 (0)

TR1	TRANSMIT/ RECEIVE
0	TRANSMIT
1	RECEIVE

PLE1	PLL ENABLE
0	PLL OFF
1	PLL ON

M3	M2	M1	MUXOUT
0	0	0	REGULATOR READY (DEFAULT)
0	0	1	R DIVIDER OUTPUT
0	1	0	N DIVIDER OUTPUT
0	1	1	DIGITAL LOCK DETECT
1	0	0	ANALOG LOCK DETECT
1	0	1	THREE-STATE
1	1	0	PLL TEST MODES
1	1	1	Σ-Δ TEST MODES

M15	M14	M13	...	M3	M2	M1	FRACTIONAL DIVIDE RATIO
0	0	0	...	0	0	0	0
0	0	0	...	0	0	1	1
0	0	0	...	0	1	0	2
.	.	.	...	.	.	.	.
.	.	.	...	.	.	.	.
.	.	.	...	.	.	.	.
1	1	1	...	1	0	0	32764
1	1	1	...	1	0	1	32765
1	1	1	...	1	1	0	32766
1	1	1	...	1	1	1	32767

N8	N7	N6	N5	N4	N3	N2	N1	N COUNTER DIVIDE RATIO
0	0	0	1	1	1	1	1	31
0	0	1	0	0	0	0	0	32
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	0	1	253
1	1	1	1	1	1	1	0	254
1	1	1	1	1	1	1	1	255

01975-026

Figure 39.

Notes

1. The Tx/Rx bit (R0_DB27) configures the part in Tx or Rx mode and also controls the state of the internal Tx/Rx switch.

2. $$F_{OUT} = \frac{XTAL}{R} \times (Integer\text{-}N + \frac{Fractional\text{-}N}{2^{15}})$$.

3. If operating in 433 MHz band, with VCO Band bit set, you should program the desired frequency F_{out} to be twice the desired operating frequency, due to removal of divide-by-2 stage in feedback path.

REGISTER 1—OSCILLATOR/FILTER REGISTER

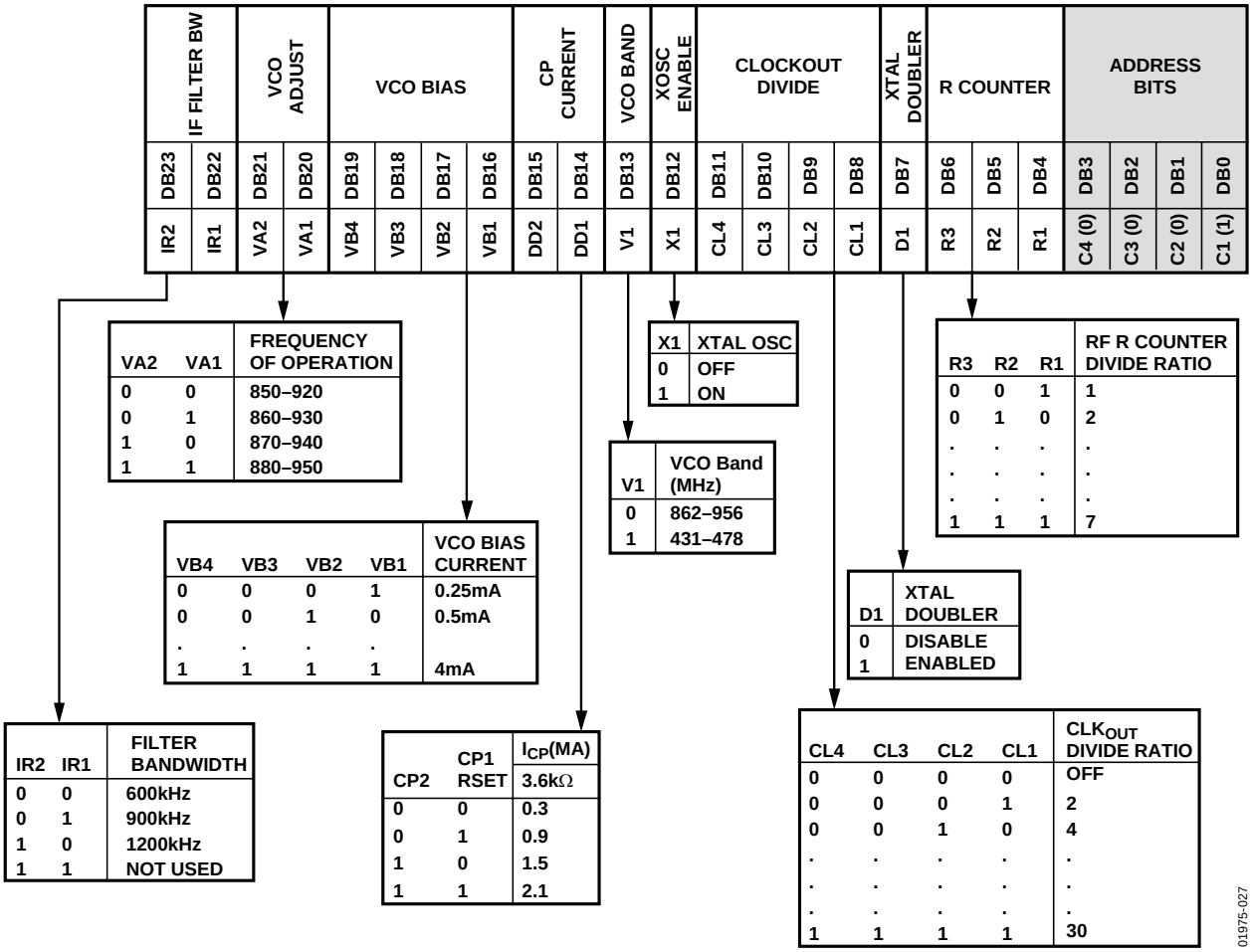

Figure 40.

Notes

1. Set the VCO adjust bits (R1_DB(20:21) to 0 for normal operation.
2. VCO bias setting should be 0xA. All VCO gain numbers are specified for this setting.

REGISTER 2—TRANSMIT MODULATION REGISTER (FSK MODE)

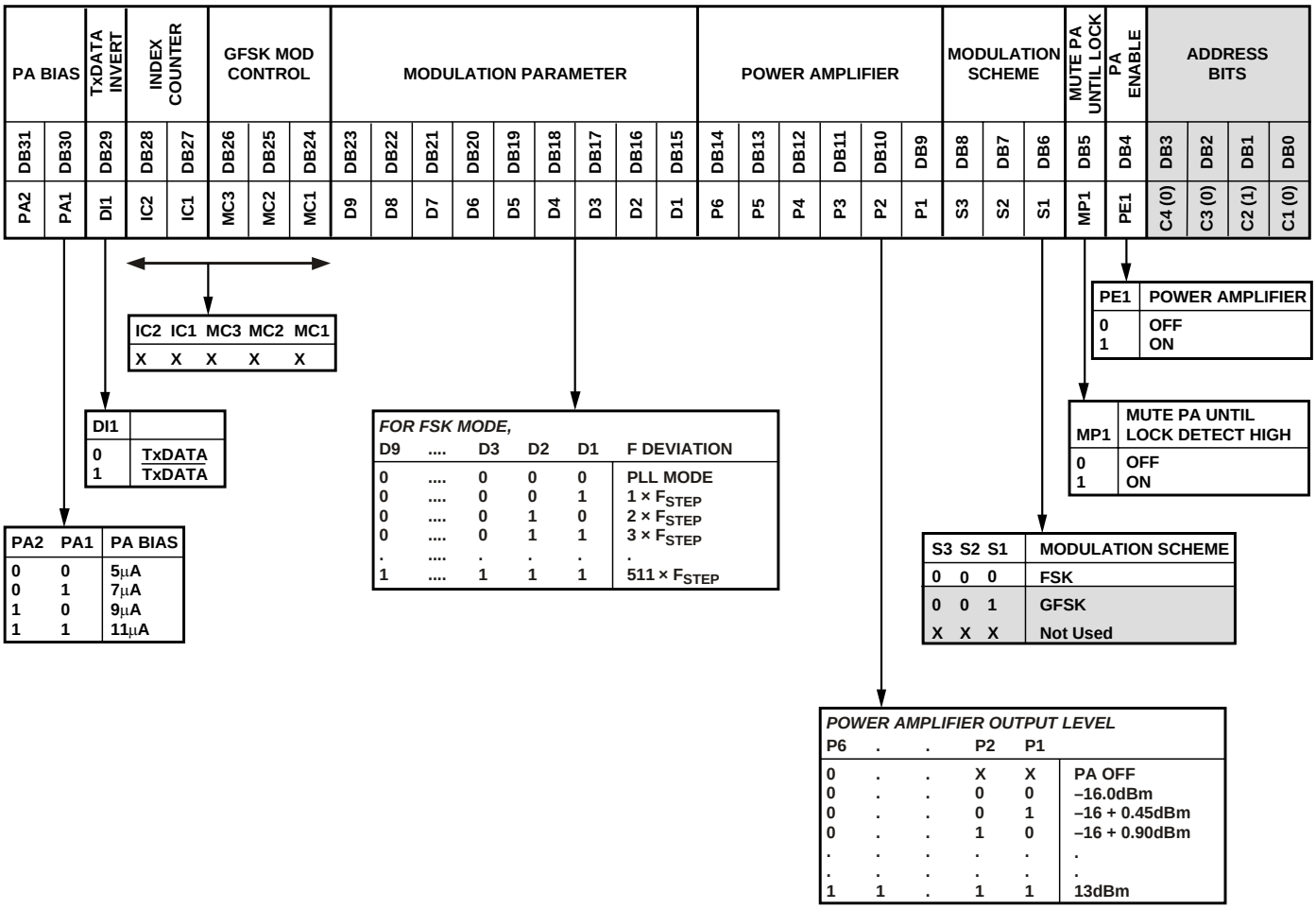

Figure 41.

Notes

1. $F_{STEP} = PDF/12^{14}$.
2. When operating in the 431-478 MHz band: $F_{STEP} = PDF/12^{15}$.
3. PA Bias default = 9 µA.

REGISTER 2—TRANSMIT MODULATION REGISTER (GFSK MODE)

PA BIAS		TxDATA INVERT	INDEX COUNTER		GFSK MOD CONTROL			MODULATION PARAMETER									POWER AMPLIFIER						MODULATION SCHEME			MUTE PA UNTIL LOCK	PA ENABLE	ADDRESS BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
PA2	PA1	DI1	IC2	IC1	MC3	MC2	MC1	D9	D8	D7	D6	D5	D4	D3	D2	D1	P6	P5	P4	P3	P2	P1	S3	S2	S1	MP1	PE1	C4 (0)	C3 (0)	C2 (1)	C1 (0)

DI1	
0	TxDATA
1	$\overline{\text{TxDATA}}$

D7	...	D3	D2	D1	DIVIDER_FACTOR
0	...	0	0	0	INVALID
0	...	0	0	1	1
0	...	0	1	0	2
0	...	0	1	1	3
.	...	.	.	.	.
1	...	1	1	1	127

PE1	POWER AMPLIFIER
0	OFF
1	ON

MP1	MUTE PA UNTIL LOCK DETECT HIGH
0	OFF
1	ON

PA2	PA1	PA BIAS
0	0	5μA
0	1	7μA
1	0	9μA
1	1	11μA

D9	D8	GAUSSIAN – OOK MODE
0	0	NORMAL MODE
0	1	OUTPUT BUFFER ON
1	0	BLEED CURRENT ON
1	1	BLEED/BUFFER ON

S3	S2	S1	MODULATION SCHEME
0	0	0	FSK
0	0	1	GFSK
X	X	X	Not Used

IC2	IC1	INDEX_COUNTER
0	0	16
0	1	32
1	0	64
1	1	128

MC3	MC2	MC1	GFSK_MOD_CONTROL
0	0	0	0
0	0	1	1
.	.	.	.
1	1	1	7

POWER AMPLIFIER OUTPUT LEVEL

P6	.	.	P2	P1	
0	.	.	X	X	PA OFF
0	.	.	0	0	–16.0dBm
0	.	.	0	1	–16 + 0.45dBm
0	.	.	1	0	–16 + 0.90dBm
.	.	.	.	.	.
.	.	.	.	.	.
1	1	.	1	1	13dBm

01975-030

Figure 42.

Notes

1. $GFSK_DEVIATION = (2^{GFSK_MOD_CONTROL} \times PFD)/2^{12}$.
2. When operating in the 431-478 MHz band: $GFSK_DEVIATION = (2^{GFSK_MOD_CONTROL} \times PFD)/2^{13}$.
3. $Data\text{-}Rate = PFD/(INDEX_COUNTER \times DIVIDER_FACTOR)$.
4. PA Bias default = 9 μA.

REGISTER 3—RECEIVER CLOCK REGISTER

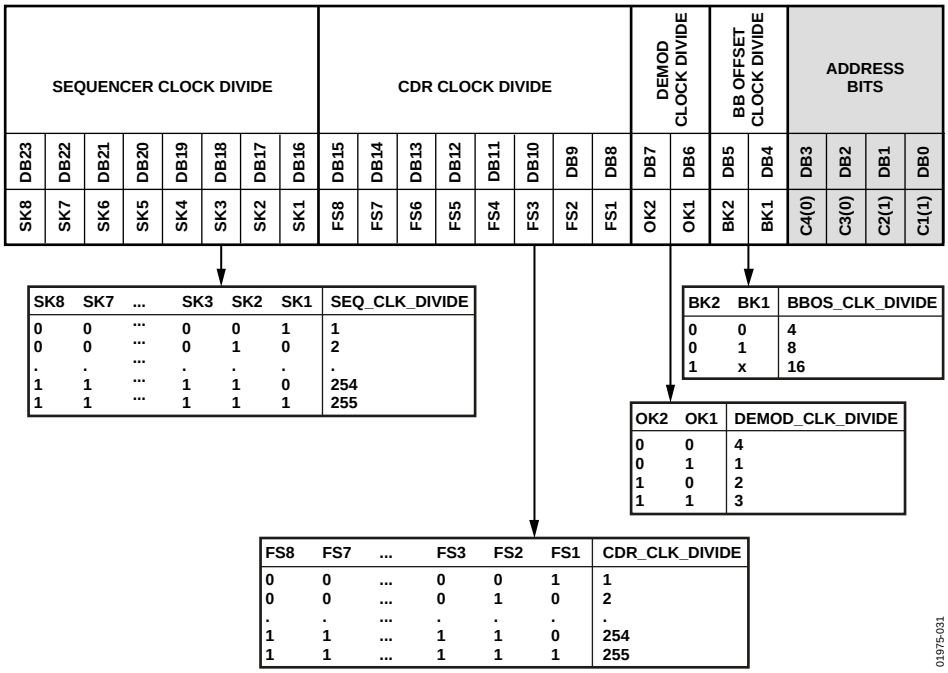

Figure 43.

Notes

1. Baseband offset clock frequency (BBOS_CLK) must be greater than 1 MHz and less than 2 MHz, where:

$$BBOS_CLK = \frac{XTAL}{BBOS_CLK_DIVIDE}$$

2. The demodulator clock (DEMOD_CLK) must be < 12 MHz, where:

$$DEMOD_CLK = \frac{XTAL}{DEMOD_CLK_DIVIDE}$$

3. Data/clock recovery frequency (CDR_CLK) should be within 2% of (32 × data rate), where:

$$CDR_CLK = \frac{DEMOD_CLK}{CDR_CLK_DIVIDE}$$

Note that this might affect your choice of XTAL, depending on the desired data rate.

4. The sequencer clock (SEQ_CLK) supplies the clock to the digital receive block. It should be close to 100 kHz.

$$SEQ_CLK = \frac{XTAL}{SEQ_CLK_DIVIDE}$$

REGISTER 4—DEMODULATOR SETUP REGISTER

						DEMOD LOCK/ SYNC WORD MATCH		DEMODULATOR LOCK SETTING								POSTDEMODULATOR BW										DEMOD SELECT		ADDRESS BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
						LM2	LM1	DL8	DL7	DL6	DL5	DL4	DL3	DL2	DL1	DW10	DW9	DW8	DW7	DW6	DW5	DW4	DW3	DW2	DW1	DS2	DS1	C4(0)	C3(1)	C2(0)	C1(0)

DS2	DS1	DEMODULATOR TYPE
0	0	LINEAR DEMODULATOR
0	1	CORRELATOR/DEMODULATOR
1	0	INVALID
1	1	INVALID

DEMOD MODE	LM2	LM1	DL8	DEMOD LOCK/SYNC WORD MATCH	INT/LOCK PIN
0	0	0	0	SERIAL PORT CONTROL – FREE RUNNING	–
1	0	0	1	SERIAL PORT CONTROL – LOCK THRESHOLD	–
2	0	1	0	SYNC WORD DETECT – FREE RUNNING	OUTPUT
3	0	1	1	SYNC WORD DETECT – LOCK THRESHOLD	OUTPUT
4	1	0	X	INTERRUPT/LOCK PIN LOCKS THRESHOLD	INPUT
5	1	1	DL8	DEMOD LOCKED AFTER DL8–DL1 BITS	–

MODE5 ONLY

DL8	DL7	...	DL3	DL2	DL1	LOCK_THRESHOLD_TIMEOUT
0	0	...	0	0	0	0
0	0	...	0	0	1	1
0	0	...	0	1	0	2
.	.	...	.	.	.	.
1	1	...	1	1	0	254
1	1	...	1	1	1	255

Figure 44.

Notes

1. Demodulator Modes 1, 3, 4, and 5 are modes that can be activated to allow the ADF7025 to demodulate data-encoding schemes that have run-length constraints greater than 7.

2. $Post_Demod_BW = 2^{11}\ \pi\ F_{CUTOFF}/DEMOD_CLK$,

   where the cutoff frequency (F_{CUTOFF}) of the postdemodulator filter should typically be 0.75 times the data-rate.

3. For Mode 5, the *timeout delay to lock threshold* = (*LOCK_THRESHOLD_SETTING*)/*SEQ_CLK*, where *SEQ_CLK* is defined in the Register 3—Receiver Clock Register section.

REGISTER 5—SYNC BYTE REGISTER

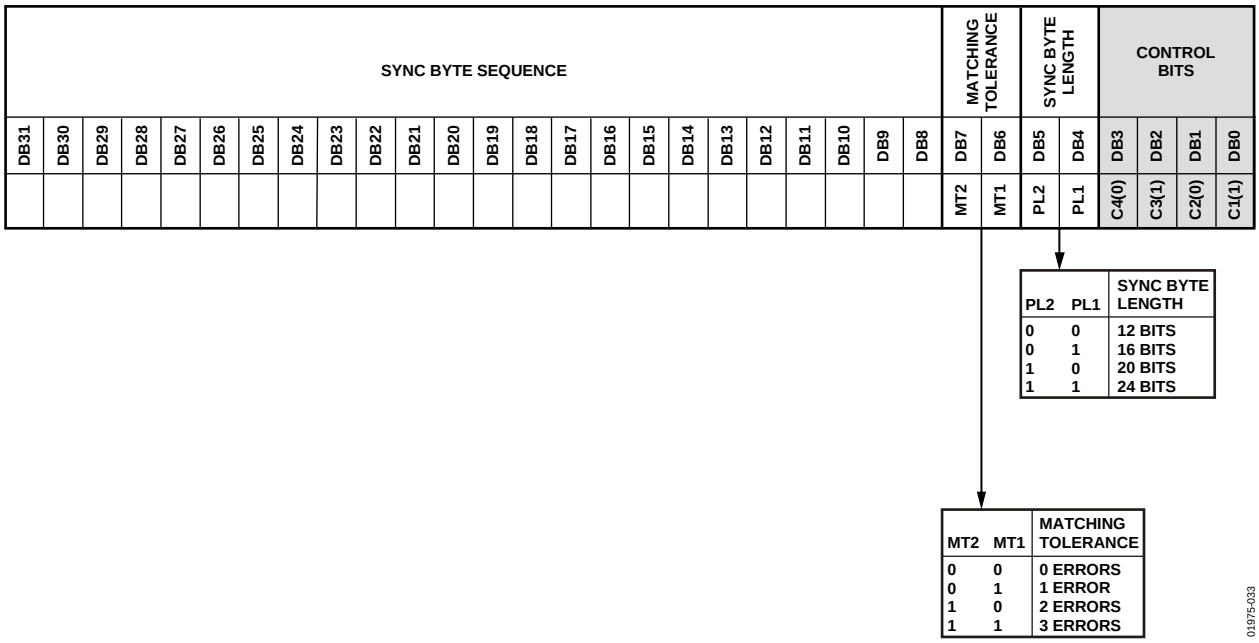

Figure 45.

Notes

1. Sync byte detect is enabled by programming Bits R4_DB(25:23) to [010] or [011].
2. This register allows a 24-bit sync byte sequence to be stored internally. If the sync byte detect mode is selected, then the INT/LOCK pin goes high when the sync byte has been detected in Rx mode. Once the sync word detect signal has gone high, it goes low again after nine data bits.
3. The transmitter must transmit the MSB of the sync byte first and the LSB last to ensure proper alignment in the receiver sync byte detection hardware.
4. Choose a sync byte pattern that has good autocorrelation properties.

REGISTER 6—CORRELATOR/DEMODULATOR REGISTER

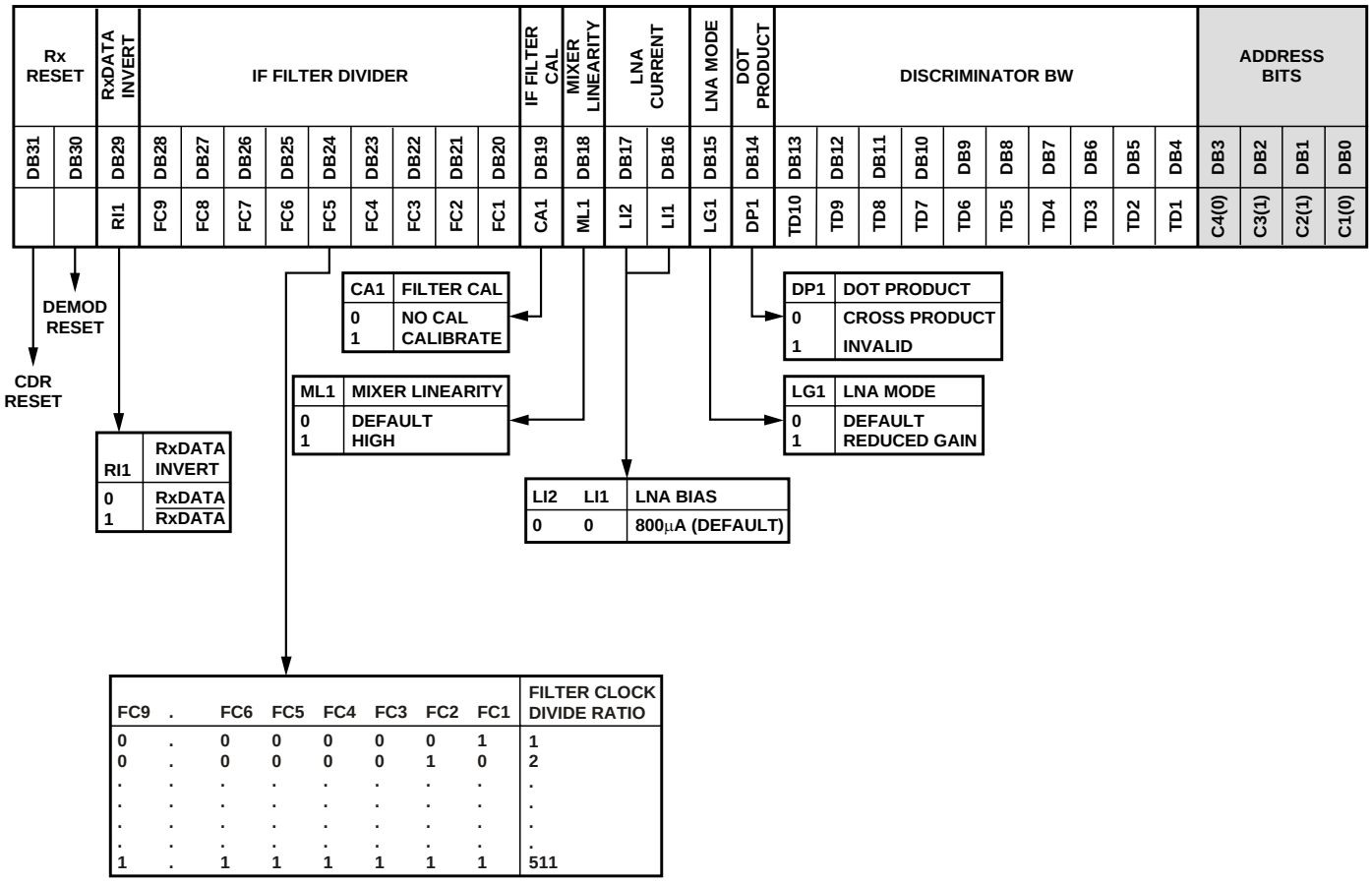

Figure 46.

Notes

1. See the FSK Correlator/Demodulator section for an example of how to determine register settings.
2. Non-adherence to correlator programming guidelines results in poorer sensitivity.
3. The filter clock is used to calibrate the LP filter. The filter clock divide ratio should be adjusted so that the frequency is 50 kHz. The formula is XTAL/FILTER_CLOCK_DIVIDE.
4. The filter should be calibrated only when the crystal oscillator is settled. The filter calibration is initiated every time Bit R6_DB19 is set high.
5. *Discriminator_BW* = (*DEMOD_CLK* × *4*DEVIATION_Freq)*. See the FSK Correlator/Demodulator section. *Maximum value* = 600.
6. When LNA Mode = 1 (reduced gain mode), this prevents the Rx from selecting the highest LNA gain setting. This might be used when linearity is a concern. See Table 5 for details of the different Rx modes.

REGISTER 7—READBACK SETUP REGISTER

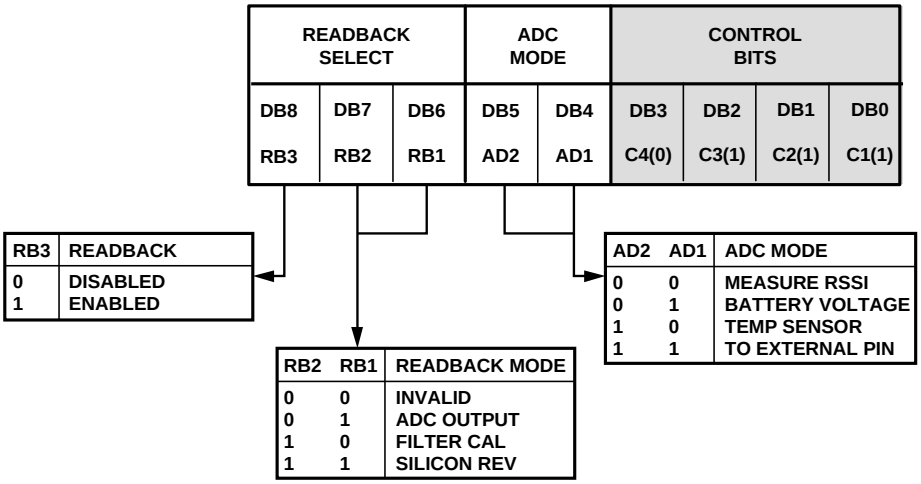

Figure 47.

Notes

1. Readback of the measured RSSI value is valid only in Rx mode. Readback of the battery voltage, the temperature sensor, and the voltage at the external pin is not available in Rx mode, if AGC is enabled.
2. Readback of the ADC value is valid in Tx mode only if the log amp/RSSI has not been disabled through the power-down bits R8_DB10. The log amp/RSSI section is active by default upon enabling Tx mode.
3. See the Readback Format section for more information.

REGISTER 8—POWER-DOWN TEST REGISTER

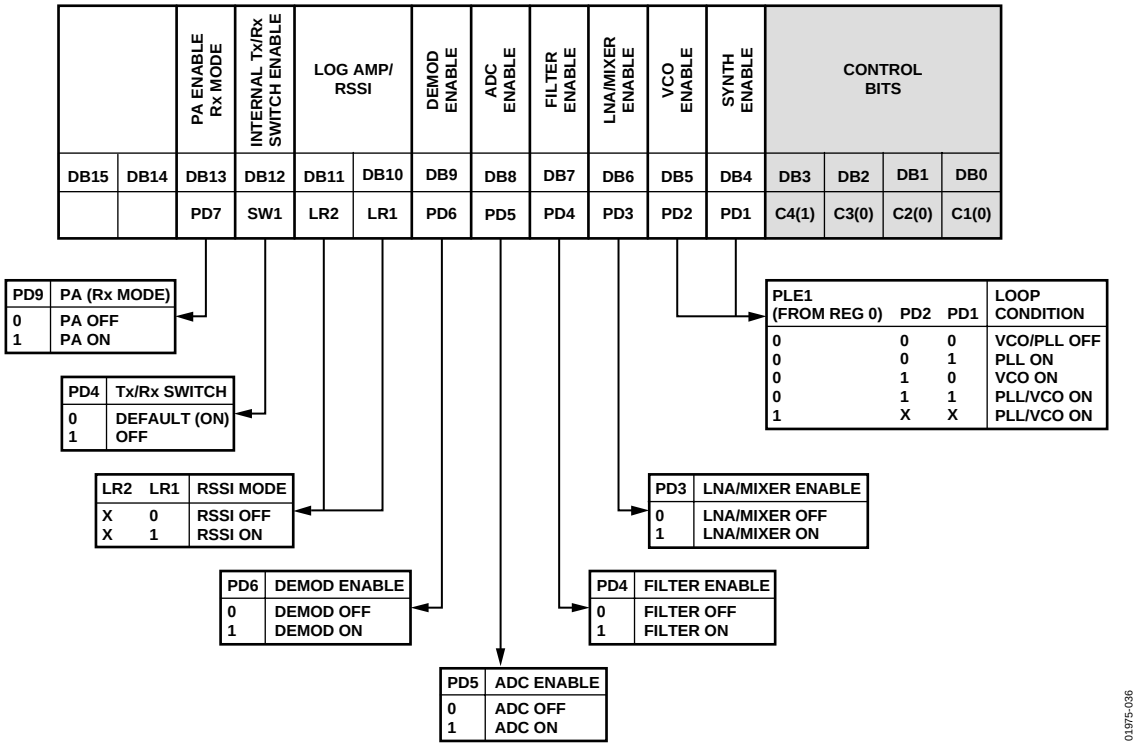

Figure 48.

Notes

1. For a combined LNA/PA matching network, Bit R8_DB12 should always be set to 0. This is the power-up default condition.
2. It is not necessary to write to this register under normal operating conditions.

REGISTER 9—AGC REGISTER

					DIGITAL TEST IQ		FILTER CURRENT	FILTER GAIN		LNA GAIN		GAIN CONTROL	AGC SEARCH	AGC HIGH THRESHOLD							AGC LOW THRESHOLD							ADDRESS BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
							FI1	FG2	FG1	LG2	LG1	GC1	GS1	GH7	GH6	GH5	GH4	GH3	GH2	GH1	GL7	GL6	GL5	GL4	GL3	GL2	GL1	C4(1)	C3(0)	C2(0)	C1(1)

FI1	FILTER CURRENT
0	LOW
1	HIGH

FG2	FG1	FILTER GAIN
0	0	8
0	1	24
1	0	72
1	1	INVALID

GS1	AGC SEARCH
0	AUTO AGC
1	HOLD SETTING

GC1	GAIN CONTROL
0	AUTO
1	USER

GL7	GL6	GL5	GL4	GL3	GL2	GL1	AGC LOW THRESHOLD
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
0	0	0	0	1	0	0	4
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	1	1	1	1	0	1	61
1	1	1	1	1	1	0	62
1	1	1	1	1	1	1	63

LG2	LG1	LNA GAIN
0	0	<1
0	1	3
1	0	10
1	1	30

GH7	GH6	GH5	GH4	GH3	GH2	GH1	RSSI LEVEL CODE
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
0	0	0	0	1	0	0	4
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	0	0	1	1	1	0	78
1	0	0	1	1	1	1	79
1	0	1	0	0	0	0	80

01975-037

Figure 49.

Notes

1. Default AGC_LOW_THRESHOLD = 30, default AGC_HIGH_THRESHOLD = 70. See the RSSI/AGC Section for details.
2. AGC high and low settings must be more than 30 apart to ensure correct operation.
3. LNA gain of 30 is available only if LNA mode, R6_DB15, is set to zero.

REGISTER 10—AGC 2 REGISTER

			SELECT I/Q	I/Q PHASE ADJUST				RESERVED	SELECT I/Q	UP/DOWN	I/Q GAIN ADJUST					AGC DELAY				LEAK FACTOR				PEAK RESPONSE				ADDRESS BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
			SIQ2	PH4	PH3	PH2	PH1	R1	SIQ1	UD1	GC5	GC4	GC3	GC2	GC1	DH4	DH3	DH2	DH1	GL7	GL6	GL5	GL4	PR4	PR3	PR2	PR1	C4 (1)	C3 (0)	C2 (1)	C1 (0)

SIQ2	SELECT IQ
0	PHASE TO I CHANNEL
1	PHASE TO Q CHANNEL

SIQ2	SELECT IQ
0	GAIN TO I CHANNEL
1	GAIN TO Q CHANNEL

DEFAULT = 10

DEFAULT = 10

DEFAULT = 2

01975-038

Figure 50.

Notes

1. This register is not used under normal operating conditions.
2. If adjusting AGC Delay or Leak Factor, clear Bits DB31 to DB16.

OUTLINE DIMENSIONS

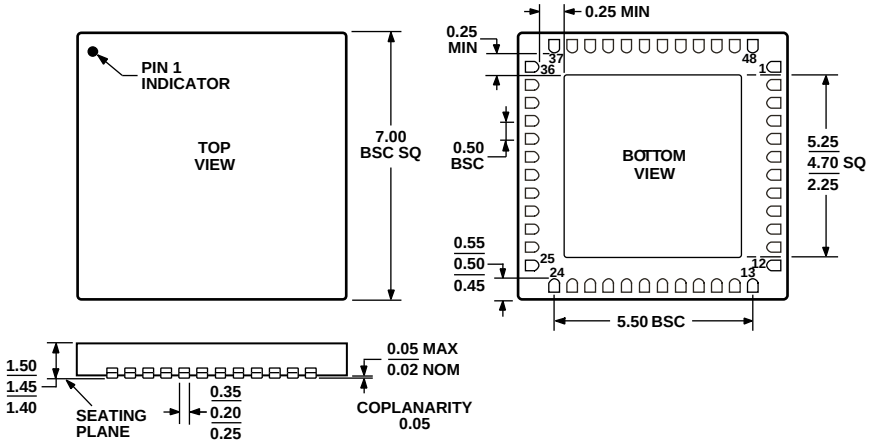

Figure 51. 48-Lead Lead Frame Chip Scale Package [MQ_LFCSP]
(CP-48-2)
7 mm × 7 mm Body, Thick Quad
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADF7025BCP	–40°C to +85°C	48-Lead Lead Frame Chip Scale Package [MQ_LFCSP]	CP-48-2

NOTES

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