4-Channel 500 MSPS DDS with 10-Bit DACs

AD9959

FEATURES

- 4 synchronized DDS channels @ 500 MSPS
- Independent frequency/phase/amplitude control between channels
- Matched latencies for frequency/phase/amplitude changes
- Excellent channel-to-channel isolation (>65 dB)
- Linear frequency/phase/amplitude sweeping capability
- Up to 16 levels of frequency/phase/amplitude modulation (pin-selectable)
- 4 integrated 10-bit D/A converters (DACs)
- Individually programmable DAC full-scale currents
- 32-bit frequency tuning resolution
- 14-bit phase offset resolution
- 10-bit output amplitude scaling resolution
- Serial I/O Port (SPI) with enhanced data throughput
- Software-/hardware-controlled power-down
- Dual supply operation (1.8 V DDS core/3.3 V serial I/O)
- Multiple device synchronization
- Selectable 4× to 20× REF_CLK multiplier (PLL)
- Selectable REF_CLK crystal oscillator
- 56-pin LFCSP package

APPLICATIONS

- Agile local oscillator
- Phased array radar/sonar
- Instrumentation
- Synchronized clocking
- RF source for AOTF

FUNCTIONAL BLOCK DIAGRAM

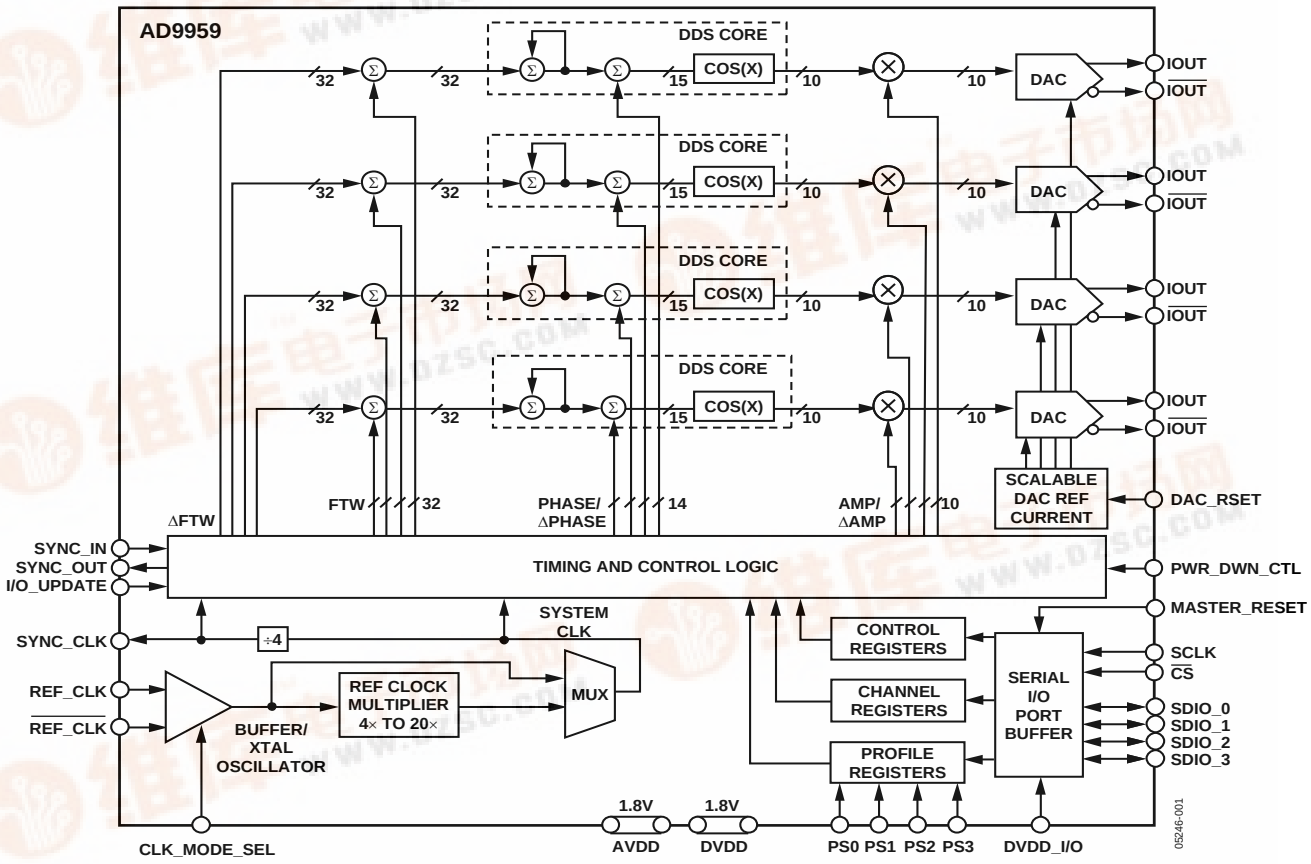

Figure 1.

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REVISION HISTORY

7/05—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9959 consists of four DDS cores that provide independent frequency, phase, and amplitude control on each channel. This flexibility can be used to correct imbalances between signals due to analog processing such as filtering, amplification, or PCB layout-related mismatches. Since all channels share a common system clock, they are inherently synchronized. Synchronization of multiple devices is supported.

The AD9959 can perform up to a 16-level modulation of frequency, phase, or amplitude (FSK, PSK, ASK). Modulation is performed by applying data to the profile pins. In addition, the AD9959 also supports linear sweep of frequency, phase, or amplitude for applications such as radar and instrumentation.

The AD9959 serial I/O port offers multiple configurations to provide significant flexibility. The serial I/O port offers an SPI-compatible mode of operation that is virtually identical to the SPI operation found in earlier Analog Devices' DDS products. Flexibility is provided by four data pins (SDIO_0:3) that allow four programmable modes of serial I/O operation.

The AD9959 uses advanced DDS technology that provides low power dissipation with high performance. The device incorporates four integrated high speed 10-bit DACs with excellent wideband and narrowband SFDR. Each channel has a dedicated 32-bit frequency tuning word, 14-bits of phase offset, and a 10-bit output scale multiplier.

The DAC outputs are supply referenced and must be terminated into AVDD by a resistor or an AVDD center-tapped transformer. Each DAC has its own programmable reference to enable different full-scale currents for each channel.

The DDS acts as a high resolution frequency divider with the REF_CLK as the input and the DAC providing the output. The REF_CLK input source is common to all channels and can be driven directly or used in combination with an integrated REF_CLK multiplier (PLL) up to a maximum of 500 MSPS. The PLL multiplication factor is programmable from 4 to 20, in integer steps. The REF_CLK input also features an oscillator circuit to support an external crystal as the REF_CLK source. The crystal must be between 20 MHz and 30 MHz. The crystal can be used in combination with the REF_CLK multiplier.

The AD9959 comes in a space-saving 56-lead LFCSP package. The DDS core (AVDD and DVDD pins) is powered by a 1.8 V supply. The digital I/O interface (SPI) operates at 3.3 V and requires the pin labeled DVDD_I/O (Pin 49) be connected to 3.3 V.

The AD9959 operates over the industrial temperature range of −40°C to +85°C.

SPECIFICATIONS

AVDD and DVDD = 1.8 V ± 5%; DVDD_I/O = 3.3 V ± 5%; R_{SET} = 1.91 kΩ; external reference clock frequency = 500 MSPS (REF_CLK multiplier bypassed), unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REF CLOCK INPUT CHARACTERISTICS					See Figure 33 and Figure 34
Frequency Range					
REF_CLK Multiplier Bypassed	1		500	MHz	
REF_CLK Multiplier Enabled	10		125	MHz	
Internal VCO Output Frequency Range VCO Gain Bit Set High[1]	255		500	MHz	
Internal VCO Output Frequency Range VCO Gain Bit Set Low	100		160	MHz	
Crystal REF_CLK Source Range	20		30	MHz	
Input Power Sensitivity	−5		+3	dBm	Measured at the pin (single-ended)
Input Voltage Bias Level		1.15		V	
Input Capacitance		2		pF	
Input Impedance		1500		Ω	
Duty Cycle w/REF_CLK Multiplier Bypassed	45		55	%	
Duty Cycle w/REF_CLK Multiplier Enabled	35		65	%	
CLK Mode Select (Pin 24) Logic 1 Voltage	1.25		1.8	V	1.8 V digital input logic
CLK Mode Select (Pin 24) Logic 0 Voltage			0.5	V	1.8 V digital input logic
DAC OUTPUT CHARACTERISTICS					Must be referenced to AVDD
Resolution			10	Bits	
Full-Scale Output Current	1.25		10	mA	
Gain Error	−10		+10	%FS	
Channel-to-Channel Output Amplitude Matching Error	−2.5		+2.5	%	
Output Current Offset		1	+25	μA	
Differential Nonlinearity		±0.5		LSB	
Integral Nonlinearity		±1.0		LSB	
Output Capacitance		3		pF	
Voltage Compliance Range	AVDD − 0.50		AVDD + 0.50	V	
Channel-to-Channel Isolation	65			dB	DAC supplies tied together (see Figure 21)
WIDEBAND SFDR					The frequency range for wideband SFDR is defined as dc to Nyquist
1 to 20 MHz Analog Out		−65		dBc	
20 to 60 MHz Analog Out		−62		dBc	
60 to 100 MHz Analog Out		−59		dBc	
100 to 150 MHz Analog Out		−56		dBc	
150 to 200 MHz Analog Out		−53		dBc	
NARROWBAND SFDR					
1.1 MHz Analog Out (±10 kHz)		−90		dBc	
1.1 MHz Analog Out (±50 kHz)		−88		dBc	
1.1 MHz Analog Out (±250 kHz)		−86		dBc	
1.1 MHz Analog Out (±1 MHz)		−85		dBc	
15.1 MHz Analog Out (±10 kHz)		−90		dBc	
15.1 MHz Analog Out (±50 kHz)		−87		dBc	
15.1 MHz Analog Out (±250 kHz)		−85		dBc	
15.1 MHz Analog Out (±1 MHz)		−83		dBc	
40.1 MHz Analog Out (±10 kHz)		−90		dBc	
40.1 MHz Analog Out (±50 kHz)		−87		dBc	
40.1 MHz Analog Out (±250 kHz)		−84		dBc	
40.1 MHz Analog Out (±1 MHz)		−82		dBc	
75.1 MHz Analog Out (±10 kHz)		−87		dBc	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
75.1 MHz Analog Out (±50 kHz)		−85		dBc	
75.1 MHz Analog Out (±250 kHz)		−83		dBc	
75.1 MHz Analog Out (±1 MHz)		−82		dBc	
100.3 MHz Analog Out (±10 kHz)		−87		dBc	
100.3 MHz Analog Out (±50 kHz)		−85		dBc	
100.3 MHz Analog Out (±250 kHz)		−83		dBc	
100.3 MHz Analog Out (±1 MHz)		−81		dBc	
200.3 MHz Analog Out (±10 kHz)		−87		dBc	
200.3 MHz Analog Out (±50 kHz)		−85		dBc	
200.3 MHz Analog Out (±250 kHz)		−83		dBc	
200.3 MHz Analog Out (±1 MHz)		−81		dBc	
PHASE NOISE CHARACTERISTICS					
Residual Phase Noise @ 15.1 MHz (f_{OUT})					
@ 1 kHz Offset		−150		dBc/Hz	
@ 10 kHz Offset		−159		dBc/Hz	
@ 100 kHz Offset		−165		dBc/Hz	
@ 1 MHz Offset		−165		dBc/Hz	
Residual Phase Noise @ 40.1 MHz (f_{OUT})					
@ 1 kHz Offset		−142		dBc/Hz	
@ 10 kHz Offset		−151		dBc/Hz	
@ 100 kHz Offset		−160		dBc/Hz	
@ 1 MHz Offset		−162		dBc/Hz	
Residual Phase Noise @ 75.1 MHz (f_{OUT})					
@ 1 kHz Offset		−135		dBc/Hz	
@ 10 kHz Offset		−146		dBc/Hz	
@ 100 kHz Offset		−154		dBc/Hz	
@ 1 MHz Offset		−157		dBc/Hz	
Residual Phase Noise @ 100.3 MHz (f_{OUT})					
@ 1 kHz Offset		−134		dBc/Hz	
@ 10 kHz Offset		−144		dBc/Hz	
@ 100 kHz Offset		−152		dBc/Hz	
@ 1 MHz Offset		−154		dBc/Hz	
Residual Phase Noise @ 15.1 MHz (f_{OUT}) w/REF_CLK Multiplier Enabled 5×					
@ 1 kHz Offset		−139		dBc/Hz	
@ 10 kHz Offset		−149		dBc/Hz	
@ 100 kHz Offset		−153		dBc/Hz	
@ 1 MHz Offset		−148		dBc/Hz	
Residual Phase Noise @ 40.1 MHz (f_{OUT}) w/REF_CLK Multiplier Enabled 5×					
@ 1 kHz Offset		−130		dBc/Hz	
@ 10 kHz Offset		−140		dBc/Hz	
@ 100 kHz Offset		−145		dBc/Hz	
@ 1 MHz Offset		−139		dBc/Hz	
Residual Phase Noise @ 75.1 MHz (f_{OUT}) w/REF_CLK Multiplier Enabled 5×					
@ 1 kHz Offset		−123		dBc/Hz	
@ 10 kHz Offset		−134		dBc/Hz	
@ 100 kHz Offset		−138		dBc/Hz	
@ 1 MHz Offset		−132		dBc/Hz	
Residual Phase Noise @ 100.3 MHz (f_{OUT}) w/REF_CLK Multiplier Enabled 5×					
@ 1 kHz Offset		−120		dBc/Hz	
@ 10 kHz Offset		−130		dBc/Hz	
@ 100 kHz Offset		−135		dBc/Hz	
@ 1 MHz Offset		−129		dBc/Hz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Residual Phase Noise @ 15.1 MHz (f_{OUT}) w/REF_CLK Multiplier Enabled 20×					
@ 1 kHz Offset		–127		dBc/Hz	
@ 10 kHz Offset		–136		dBc/Hz	
@ 100 kHz Offset		–139		dBc/Hz	
@ 1 MHz Offset		–138		dBc/Hz	
Residual Phase Noise @ 40.1 MHz (f_{OUT}) w/REF_CLK Multiplier Enabled 20×					
@ 1 kHz Offset		–117		dBc/Hz	
@ 10 kHz Offset		–128		dBc/Hz	
@ 100 kHz Offset		–132		dBc/Hz	
@ 1 MHz Offset		–130		dBc/Hz	
Residual Phase Noise @ 75.1 MHz (f_{OUT}) w/REF_CLK Multiplier Enabled 20×					
@ 1 kHz Offset		–110		dBc/Hz	
@ 10 kHz Offset		–121		dBc/Hz	
@ 100 kHz Offset		–125		dBc/Hz	
@ 1 MHz Offset		–123		dBc/Hz	
Residual Phase Noise @ 100.3 MHz (f_{OUT}) w/REF_CLK Multiplier Enabled 20×					
@ 1 kHz Offset		–107		dBc/Hz	
@ 10 kHz Offset		–119		dBc/Hz	
@ 100 kHz Offset		–121		dBc/Hz	
@ 1 MHz Offset		–119		dBc/Hz	
SERIAL PORT TIMING CHARACTERISTICS					
Maximum Frequency Serial Clock (SCLK)			200	MHz	
Minimum SCLK Pulse Width Low (t_{PWL})	1.6			ns	
Minimum SCLK Pulse Width High (t_{PWH})	2.2			ns	
Minimum Data Set-Up Time (t_{DS})	2.2			ns	
Minimum Data Hold Time	0			ns	
Minimum CSB Set-Up Time (t_{PRE})	1.0			ns	
Minimum Data Valid Time for Read Operation	12			ns	
MISCELLANEOUS TIMING CHARACTERISTICS					
Master_Reset Minimum Pulse Width	1				Min pulse width = 1 Sync clock period
I/O_Update Minimum Pulse Width	1				Min pulse width = 1 Sync clock period
Minimum Set-Up Time (I/O_Update to SYNC_CLK)	4.8			ns	Rising edge to rising edge
Minimum Hold Time (I/O_Update to SYNC_CLK)	0			ns	Rising edge to rising edge
Minimum Set-Up Time (Profile Inputs to SYNC_CLK)	5.4			ns	
Minimum Hold Time (Profile Inputs to SYNC_CLK)	0			ns	
Minimum Set-Up Time (SDIO Inputs to SYNC_CLK)	2.5			ns	
Minimum Hold Time (SDIO Inputs to SYNC_CLK)	0			ns	
Propagation Time Between REF_CLK and SYNC_CLK	2.25	3.5	5.5	ns	
CMOS LOGIC INPUTS					
V_{IH}	2.0			V	
V_{IL}			0.8	V	
Logic 1 Current		3	12	µA	
Logic 0 Current		–12		µA	
Input Capacitance		2		pF	
CMOS LOGIC OUTPUTS (1 mA Load)					
V_{OH}	2.7			V	
V_{OL}			0.4	V	
POWER SUPPLY					
Total Power Dissipation—All Channels On, Single-Tone Mode		540	635	mW	Dominated by supply variation
Total Power Dissipation—All Channels On, w/Sweep Accumulator		580	680	mW	Dominated by supply variation
Total Power Dissipation—Full Power Down		13		mW	
IAVDD—All Channels On, Single Tone Mode		155	180	mA	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
IAVDD—All Channels On, Sweep Accumulator, REF_CLK Multiplier and 10-Bit Output Scalar Enabled		160	185	mA	
IDVDD—All Channels On, Single Tone Mode		105	125	mA	
IDVDD—All Channels On, Sweep Accumulator, REF_CLK Multiplier and 10-Bit Output Scalar Enabled		125	145	mA	
IDVDD_I/O			40	mA	IDVDD = read
IDVDD_I/O			30	mA	IDVDD = write
IAVDD Power-Down Mode		0.7		mA	
IDVDD Power-Down Mode		1.1		mA	
DATA LATENCY (PIPELINE DELAY) SINGLE TONE MODE[2, 3]					
Frequency, Phase, and Amplitude Words to DAC Output w/Matched Latency Enabled	29			Sys Clk	
Frequency Word to DAC Output w/Matched Latency Disabled	29			Sys Clk	
Phase Offset Word to DAC Output w/Matched Latency Disabled	25			Sys Clk	
Amplitude Word to DAC Output w/Matched Latency Disabled	17			Sys Clk	
DATA LATENCY (PIPELINE DELAY) MODULATION MODE[3, 4]					
Frequency Word to DAC Output	34			Sys Clk	
Phase Offset Word to DAC Output	29			Sys Clk	
Amplitude Word to DAC Output	21			Sys Clk	
DATA LATENCY (PIPELINE DELAY) LINEAR SWEEP MODE[3, 4]					
Frequency Rising/Falling Delta Tuning Word to DAC Output	41			Sys Clk	
Phase Offset Rising/Falling Delta Tuning Word to DAC Output	37			Sys Clk	
Amplitude Rising/Falling Delta Tuning Word to DAC Output	29			Sys Clk	

[1] For the VCO frequency range of 160 MHz to 255 MHz there is no guarantee of operation.
[2] Data latency is referenced to the I/O_UPDATE.
[3] Data latency is fixed.
[4] Data latency is referenced to a profile change.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Maximum Junction Temperature	150°C
DVDD_I/O (Pin 49)	4 V
AVDD, DVDD	2 V
Digital Input Voltage (DVDD_I/O = 3.3 V)	−0.7 V to +4 V
Digital Output Current	5 mA
Storage Temperature	−65°C to +150°C
Operating Temperature	−40°C to +85°C
Lead Temperature (10 sec Soldering)	300°C
θ_{JA}	21°C/W
θ_{JC}	2°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

EQUIVALENT INPUT AND OUTPUT CIRCUITS

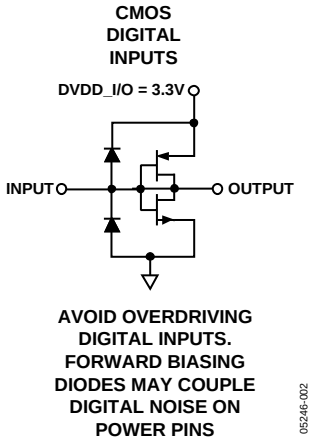


Figure 2.

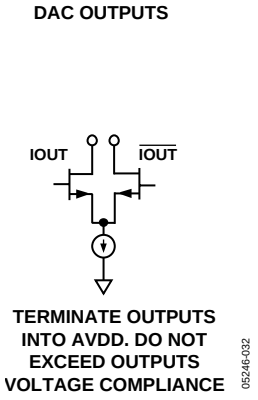


Figure 3.

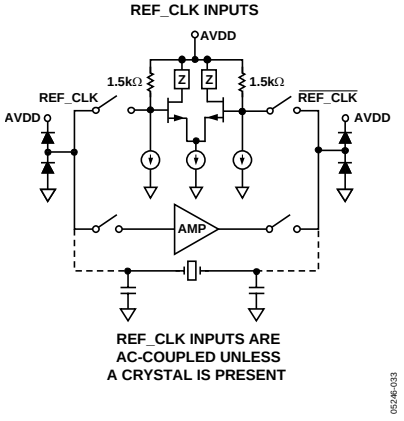


Figure 4.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

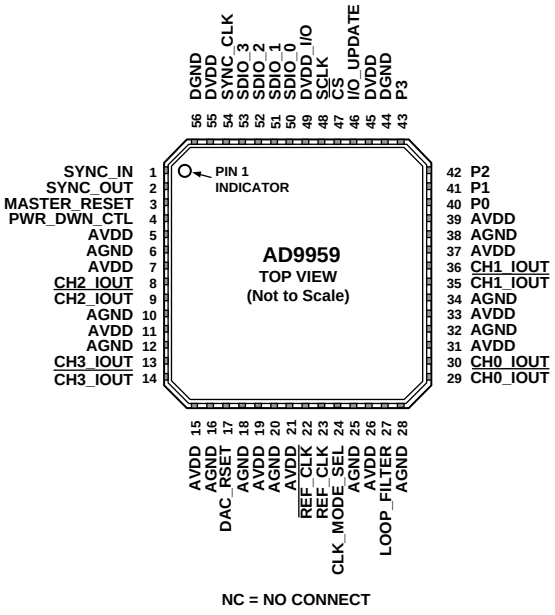


Figure 5. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	I/O	Description
1	SYNC_IN	I	Used to Synchronize Multiple AD9959s. Connects to the SYNC_OUT pin of the master AD9959 device.
2	SYNC_OUT	O	Used to Synchronize Multiple AD9959s. Connects to the SYNC_IN pin of the slave AD9959 devices.
3	MASTER_RESET	I	Active High Reset Pin. Asserting the MASTER_RESET pin forces the AD9959's internal registers to their default state, as described in the Register Map.
4	PWR_DWN_CTL	I	External Power-Down Control.
5, 7, 11, 15, 19, 21, 26, 31, 33, 37, 39	AVDD	I	Analog Power Supply Pins (1.8 V).
6, 10, 12, 16, 18, 20, 25, 28, 32, 34, 38	AGND	I	Analog Ground Pins.
45, 55	DVDD	I	Digital Power Supply Pins (1.8 V).
44, 56	DGND	I	Digital Power Ground Pins.
8	$\overline{\text{CH2\_IOUT}}$	O	True DAC Output. Terminates into AVDD.
9	CH2_IOUT	O	Complementary DAC Output. Terminates into AVDD.
13	$\overline{\text{CH3\_IOUT}}$	O	True DAC Output. Terminates into AVDD.
14	CH3_IOUT	O	Complementary DAC Output. Terminates into AVDD.
17	DAC_RSET	I	Establishes the Reference Current for all DACs. A 1.91 kΩ resistor (nominal) is connected from Pin 17 to AGND.
22	$\overline{\text{REF\_CLK}}$	I	Complementary Reference Clock/Oscillator Input. When the REF_CLK is operated in single-ended mode, this pin should be decoupled to AVDD or AGND with a 0.1 µF capacitor.
23	REF_CLK	I	Reference Clock/Oscillator Input. When the REF_CLK is operated in single-ended mode, this is the input. See Modes of Operation section for the reference clock configuration.

Pin No.	Mnemonic	I/O	Description
24	CLK_MODE_SEL	I	Control Pin for the Oscillator Section. CAUTION: Do not drive this pin beyond 1.8 V. When high (1.8 V), the oscillator section is enabled to accept a crystal as the REF_CLK source. When low, the oscillator section is bypassed.
27	LOOP_FILTER	I	Connects to the external zero compensation network of the PLL loop filter. Typically the network consists of a 0 Ω resistor in series with a 680 pF capacitor tied to AVDD.
29	$\overline{\text{CH0\_IOUT}}$	O	Complementary DAC Output. Terminates into AVDD.
30	CH0_IOUT	O	True DAC Output. Terminates into AVDD.
35	$\overline{\text{CH1\_IOUT}}$	O	Complementary DAC Output. Terminates into AVDD.
36	CH1_IOUT	O	True DAC Output. Terminates into AVDD.
40 to 43	P0 to P3	I	Data pins used for modulation (FSK, PSK, ASK), start/stop the sweep accumulators or used to ramp up/down the output amplitude. Any toggle of these data inputs is equivalent to an I/O_UPDATE. The data is synchronous to the SYNC_CLK (Pin 54). The data inputs must meet the set-up and hold time requirements of the SYNC_CLK. This guarantees a fixed pipeline delay of data to the DAC output; otherwise, a ±1 SYNC_CLK period of uncertainty occurs. The functionality of these pins is controlled by profile pin configuration (PPC) bits in Register FR1 <12:14>.
46	I/O_UPDATE	I	A rising edge transfers data from the serial I/O port buffer to active registers. I/O_UPDATE is synchronous to the SYNC_CLK (Pin 54). I/O_UPDATE must meet the set-up and hold time requirements to the. SYNC_CLK to guarantee a fixed pipeline delay of data to DAC output. If not, a ±1 SYNC_CLK period of uncertainty occurs. The minimum pulse width is one SYNC_CLK period.
47	$\overline{\text{CS}}$	I	Active low chip select allowing multiple devices to share a common I/O bus (SPI).
48	SCLK	I	Serial Data Clock for I/O Operations. Data bits are written on the rising edge of SCLK and read on the falling edge of SCLK.
49	DVDD_I/O	I	3.3 V Digital Power Supply for SPI Port and Digital I/O.
50	SDIO_0,	I/O	Data Pin SDIO_0 is dedicated to the Serial Port I/O only.
51 to 53	SDIO_1 to SDIO_3	I/O	Data Pins SDIO_1:3 can be used for the serial port I/O port or used to initiate a ramp up/down (RU/RD) of the DAC output amplitude.
54	SYNC_CLK	O	The SYNC_CLK runs at one-fourth the system clock rate. It can be disabled. I/O_UPDATE or data (Pins 40 to 43) is synchronous to the SYNC_CLK. To guarantee a fixed pipeline delay of data to DAC output, I/O_UPDATE or data (Pins 40 to 43) must meet the set-up and hold time requirements to the rising edge of SYNC_CLK. If not, a ±1 SYNC_CLK period of uncertainty occurs.

TYPICAL PERFORMANCE CHARACTERISTICS

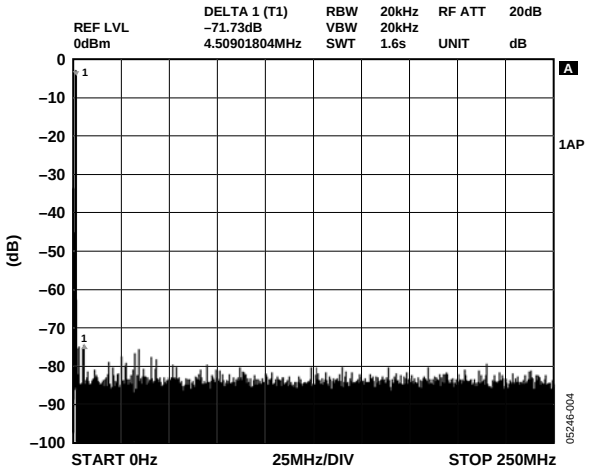


Figure 6. f_{OUT} = 1.1 MHz, f_{CLK} = 500 MSPS, Wideband SFDR

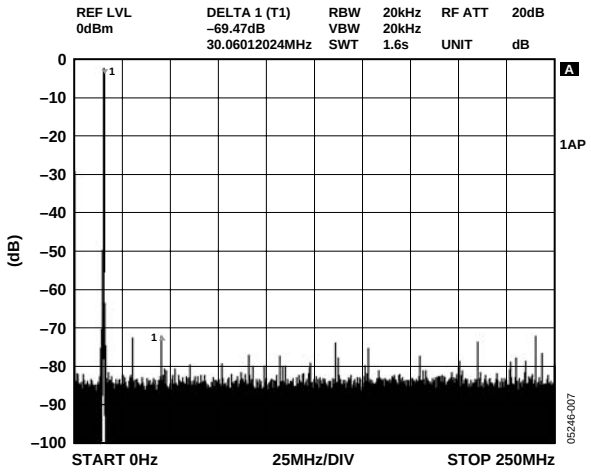


Figure 9. f_{OUT} = 15.1 MHz, f_{CLK} = 500 MSPS, Wideband SFDR

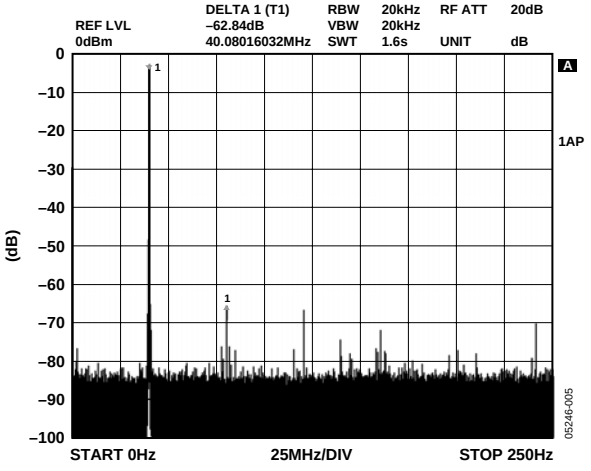


Figure 7. f_{OUT} = 40.1 MHz, f_{CLK} = 500 MSPS, Wideband SFDR

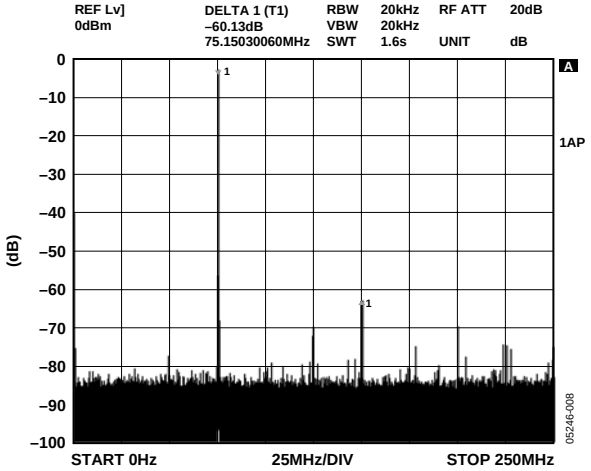


Figure 10. f_{OUT} = 75.1 MHz, f_{CLK} = 500 MSPS, Wideband SFDR

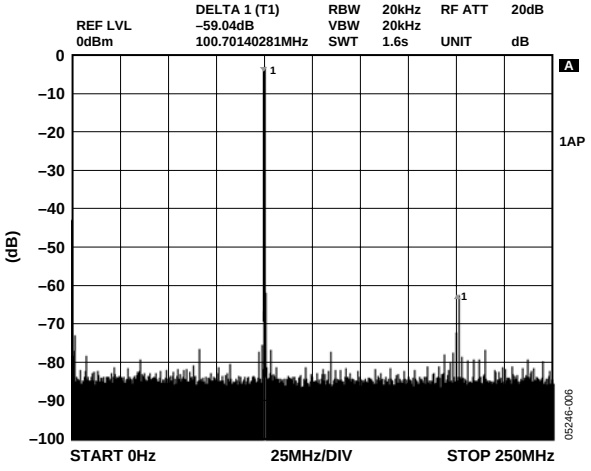


Figure 8. f_{OUT} = 100.3 MHz, f_{CLK} = 500 MSPS, Wideband SFDR

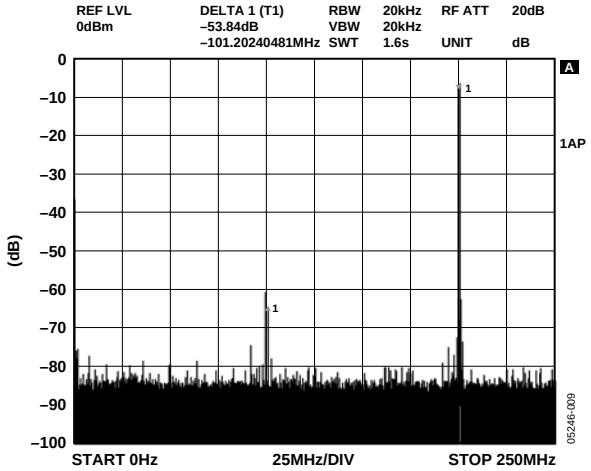


Figure 11. f_{OUT} = 200.3 MHz, f_{CLK} = 500 MSPS, Wideband SFDR

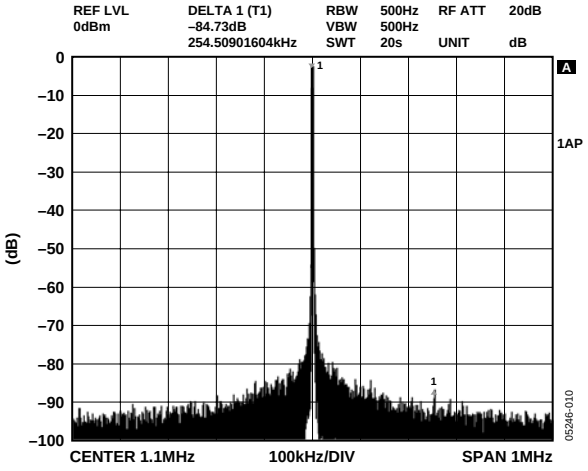


Figure 12. f_{OUT} = 1.1 MHz, f_{CLK} = 500 MSPS, NBSFDR, ±1 MHz

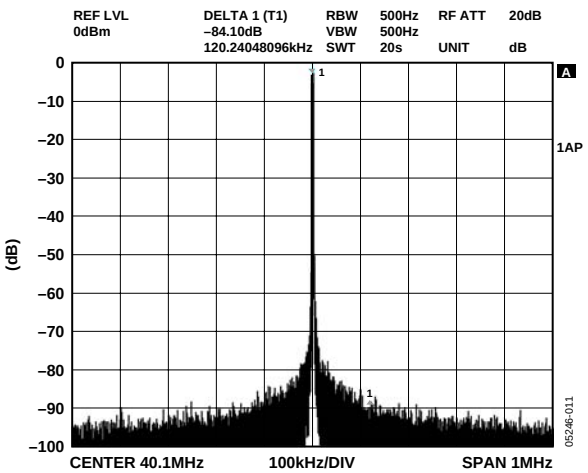


Figure 13. f_{OUT} = 40.1 MHz, f_{CLK} = 500 MSPS, NBSFDR, ±1 MHz

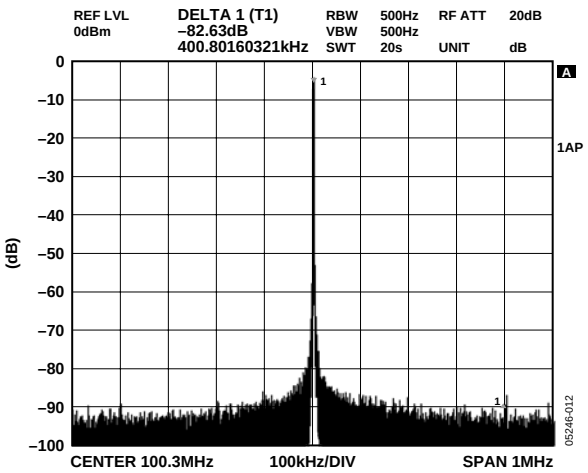


Figure 14. f_{OUT} = 100.3 MHz, f_{CLK} = 500 MSPS, NBSFDR, ±1 MHz

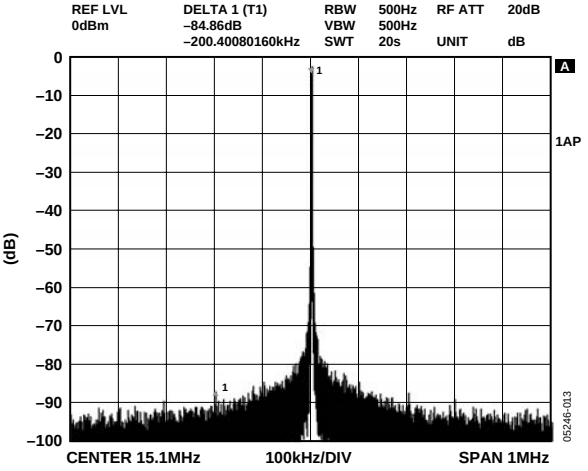


Figure 15. f_{OUT} = 15.1 MHz, f_{CLK} = 500 MSPS, NBSFDR, ±1 MHz

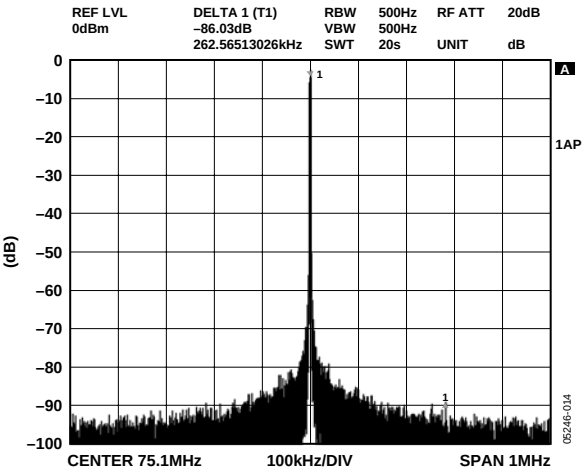


Figure 16. f_{OUT} = 75.1 MHz, f_{CLK} = 500 MSPS, NBSFDR, ±1 MHz

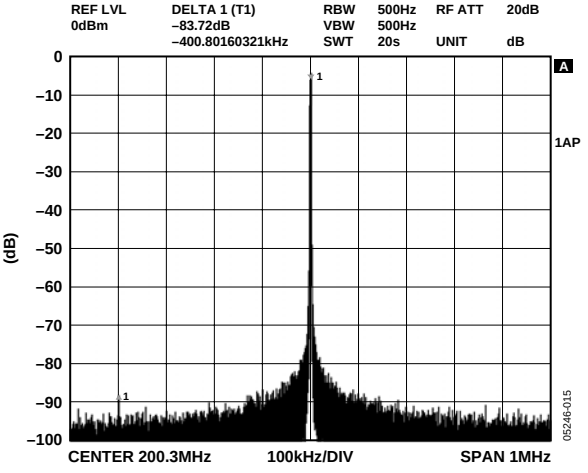


Figure 17. f_{OUT} = 200. 3MHz, f_{CLK} = 500 MSPS, NBSFDR, ±1 MHz

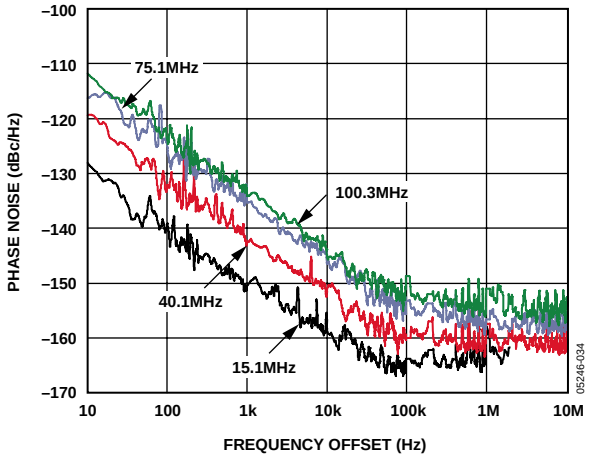


Figure 18. Residual Phase Noise (SSB) with f_{OUT} = 15.1 MHz, 40.1 MHz, 75.1 MHz, 100.3 MHz, f_{CLK} = 500 MHz with REF_CLK Multiplier Bypassed

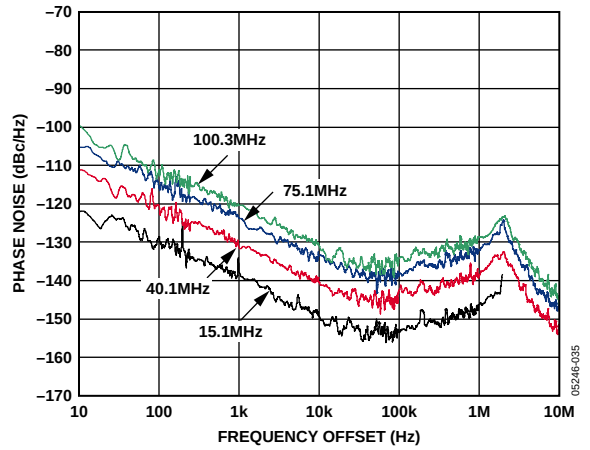


Figure 19. Residual Phase Noise (SSB) with f_{OUT} = 15.1 MHz, 40.1 MHz, 75.1 MHz, 100.3 MHz, f_{CLK} = 500 MHz with REF_CLK Multiplier = 5x

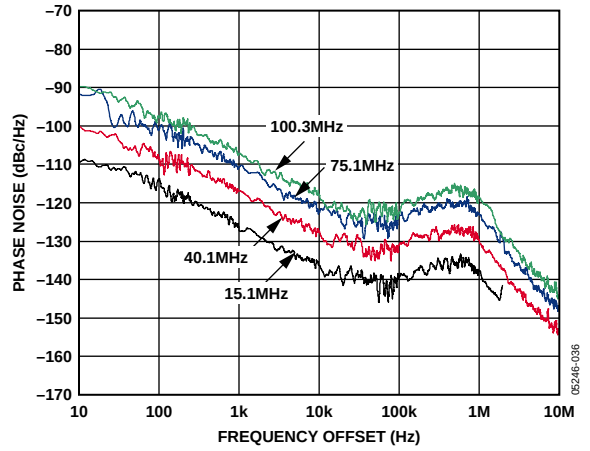


Figure 20. Residual Phase Noise(SSB) with f_{OUT} = 15.1 MHz, 40.1 MHz, 75.1 MHz,100.3 MHz, f_{CLK} = 500 MHz with REF_CLK Multiplier = 20×

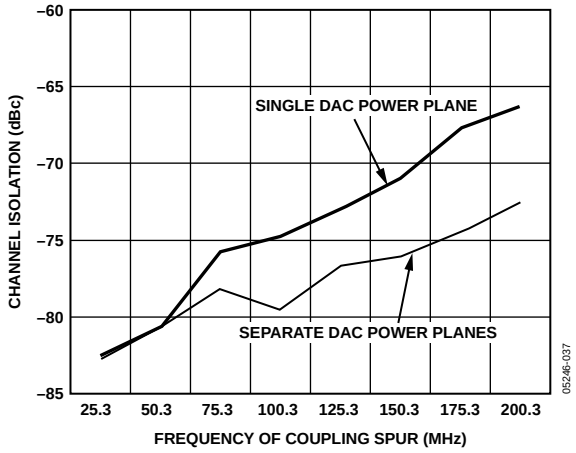


Figure 21. Channel Isolation at 500 MSPS Operation. Conditions are Channel of Interest Fixed at 110.3 MHz, the Other Channels Are Frequency Swept

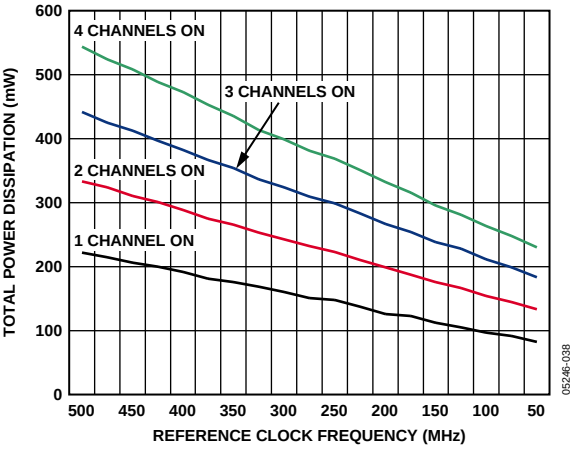


Figure 22. Reference Clock Frequency vs. Power Dissipation vs. Channel(s) Power On/Off

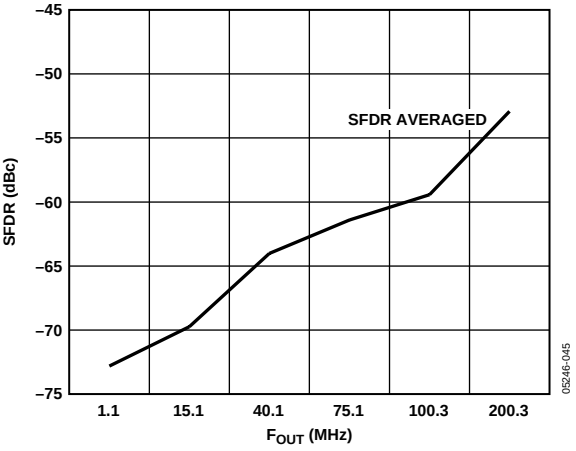


Figure 23. Averaged Channel SFDR vs. f_{OUT}

APPLICATION CIRCUITS

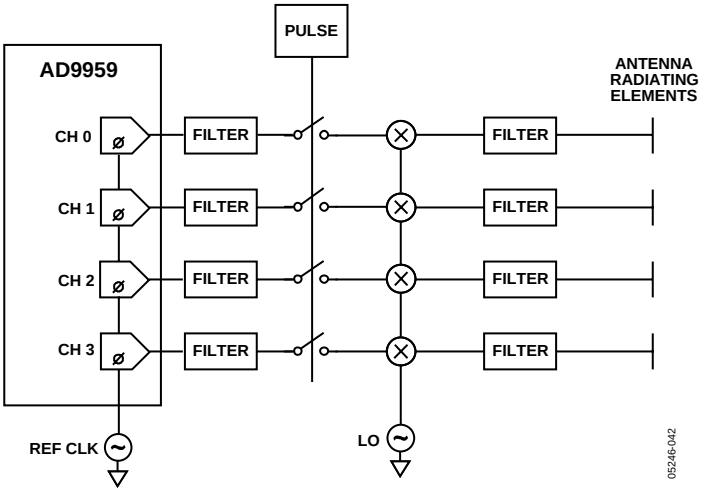


Figure 24. Phase Array Radar Using Precision Frequency/Phase Control from DDS in FMCW or Pulsed Radar Applications. DDS Provides Either Continuous Wave or Frequency Sweep.

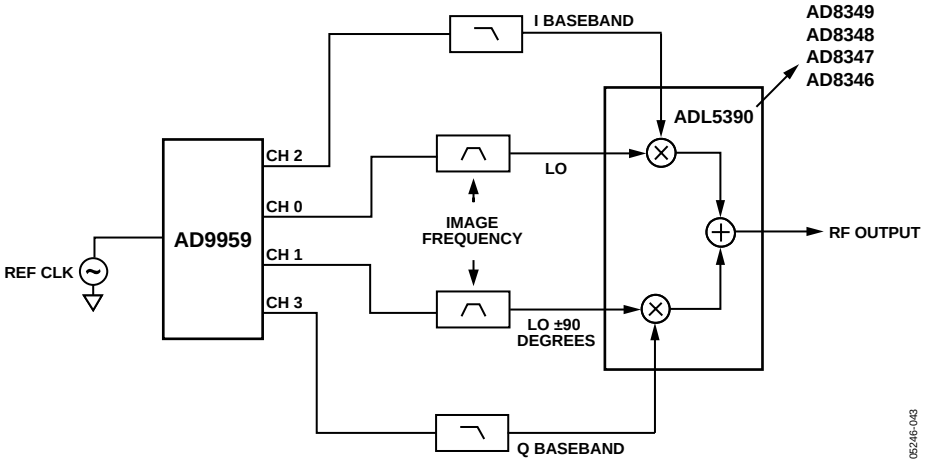


Figure 25. Single-Sideband-Suppressed Carry-Up Conversion

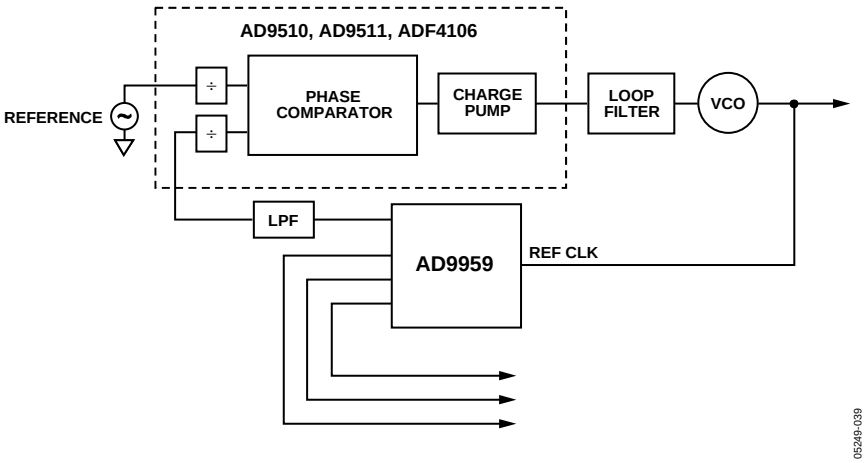


Figure 26. DDS in PLL Locking to Reference Offering Distribution with Fine Frequency and Delay Adjust Tuning

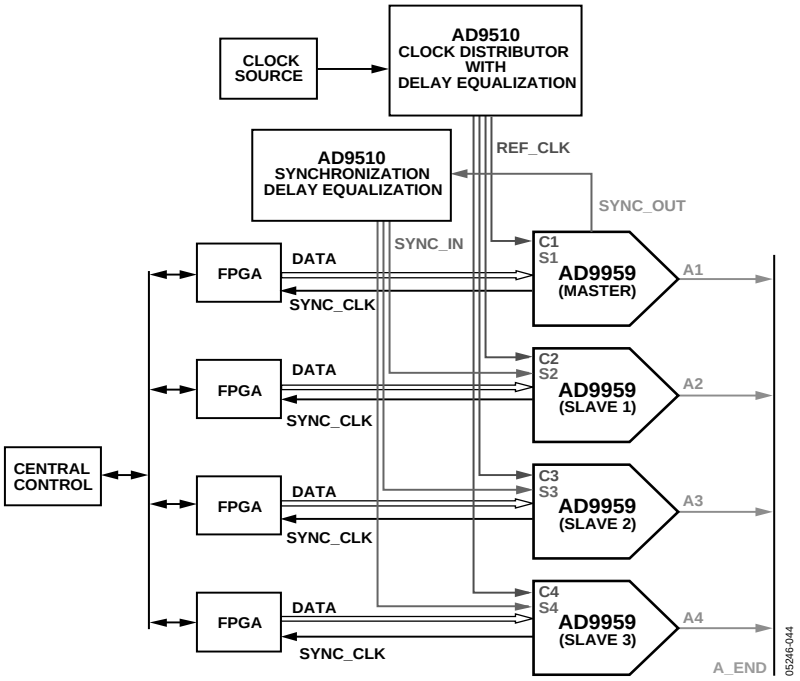


Figure 27. Synchronizing Multiple Devices to Increase Channel Capacity Using the AD9510 as a Clock Distributor for the Reference and SYNC Clock

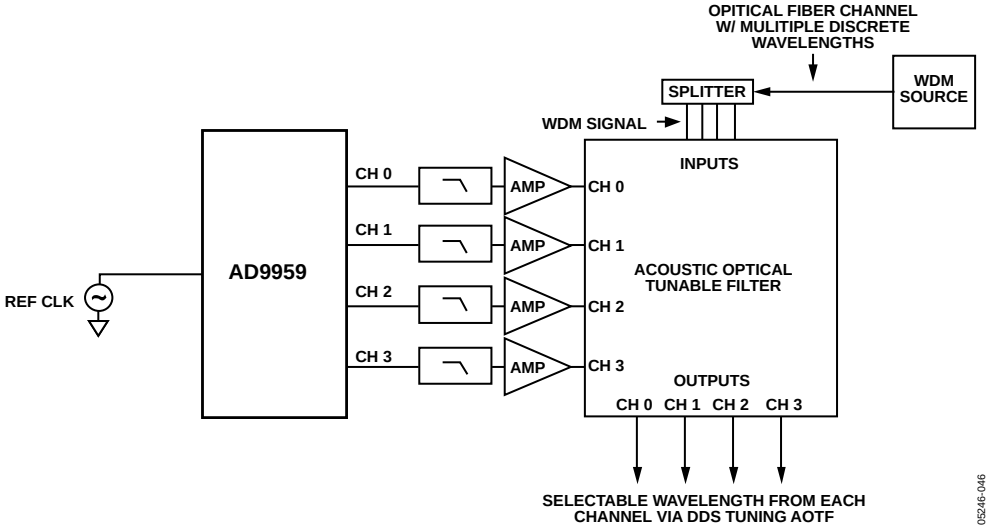


Figure 28. DDS Providing Stimulus for Acoustic Optical Tunable Filter

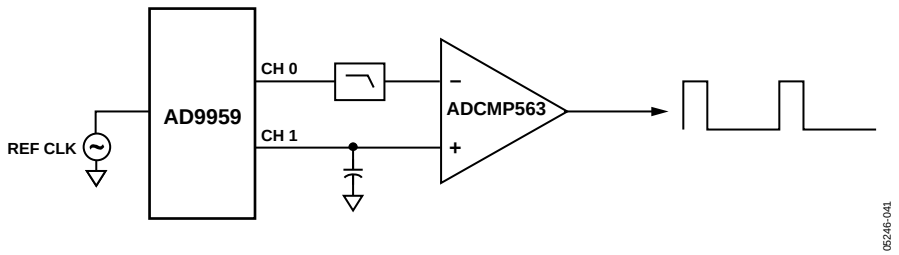


Figure 29. Agile Clock Source with Duty Cycle Control Using the Phase Offset Value in DDS to Change the DC Voltage to Comparator

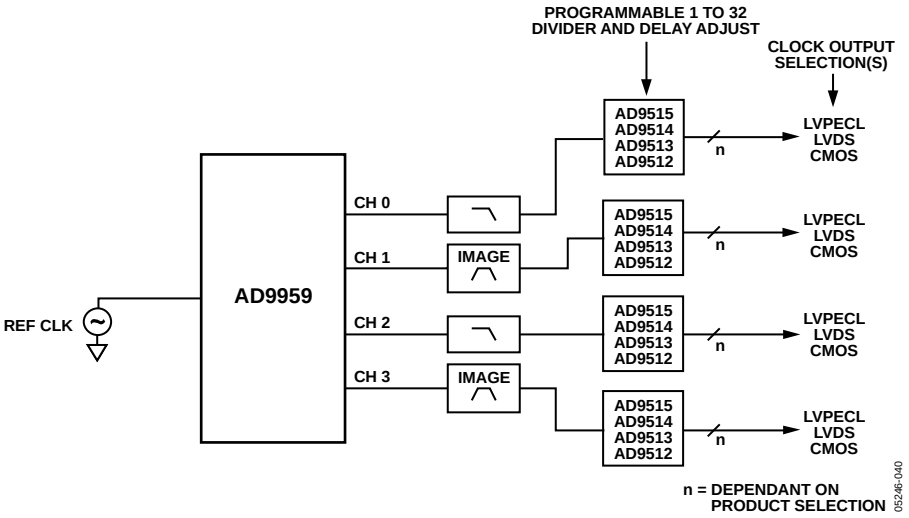


Figure 30. Clock Generation Circuit Using the AD951x Series of Clock Distribution Chips

THEORY OF OPERATION

DDS CORE

The AD9959 has four DDS cores each consisting of a 32-bit phase accumulator and phase-to-amplitude converter. Together, these digital blocks generate a digital sine wave when the phase accumulator is clocked and the phase increment value (frequency tuning word) is greater than 0. The phase-to-amplitude converter simultaneously translates phase information to amplitude information by a COS (θ) operation.

The output frequency (f_O) of each DDS channel is a function of the rollover rate of each phase accumulator. The exact relationship is given in the following equation:

$$f_O = \frac{(FTW)(f_S)}{2^{32}} \; with \; 0 \le FTW \le 2^{31}$$

where:
f_S = the system clock rate
FTW = the frequency tuning word
2^{32} represents the phase accumulator's capacity.

Since all four channels share a common system clock, they are inherently synchronized.

The DDS core architecture also supports the capability to phase offset the output signal. This is performed by the channel phase offset word (CPOW). The CPOW is a 14-bit register that stores a phase offset value. This value is added to the output of the phase accumulator to offset the current phase of the output signal. Each channel has its own phase offset word register. This feature can be used for placing all channels in a known phase relationship relative to one another. The exact value of phase offset is given by the following equation:

$$\Phi = \left(\frac{POW}{2^{14}} \right) \times 360°$$

D/A CONVERTER

The AD9959 incorporates four, 10-bit current output DACs. The DAC converts a digital code (amplitude) into a discrete analog quantity. The DAC's current outputs can be modeled as a current source with high output impedance (typically 100 kΩ). Unlike many DACs, these current outputs require termination into AVDD via a resistor or a center-tapped transformer for expected current flow.

Each DAC has complementary outputs that provide a combined full-scale output current (I_{OUT} + I_{OUTB}). The outputs always sink current and their sum equals the full-scale current at any point in time. The full-scale current is controlled by means of an external resistor (R_{SET}) and the scalable DAC current control bits discussed in the Modes of Operation section. The resistor R_{SET} is connected between the DAC_RSET pin and analog ground (AGND). The full-scale current is inversely proportional to the resistor value as follows:

$$R_{SET} = \frac{18.91}{I_{OUT}}$$

The maximum full-scale output current of the combined DAC outputs is 15 mA, but limiting the output to 10 mA provides optimal spurious-free dynamic range (SFDR) performance. The DAC output voltage compliance range is AVDD + 0.5 V to AVDD − 0.5 V. Voltages developed beyond this range can cause excessive harmonic distortion. Proper attention should be paid to the load termination to keep the output voltage within its compliance range. Exceeding this range could potentially damage the DAC output circuitry.

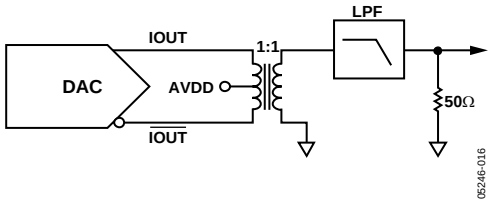


Figure 31. Typical DAC Output Termination Configuration

MODES OF OPERATION

There are many combinations of modes (for example, single-tone, modulation, linear sweep) that the AD9959 can perform simultaneously. However, some modes require multiple data pins, which can impose limitations. The following guidelines can help determine if a specific combination of modes can be performed simultaneously by the AD9959.

CHANNEL CONSTRAINT GUIDELINES

1. Single tone generation, 2-level modulation, and linear sweep modes can be enabled on any channel and in any combination at the same time.
2. Any one or two channels in any combination can perform 4-level modulation. The remaining channels can perform single-tone generation.
3. Any channel can perform 8-level modulation. The three remaining channels can be in single-tone mode.
4. Any channel can perform 16-level direct modulation. The three remaining channels can be in single-tone mode.
5. The RU/RD function can be used on all four channels in single-tone generation mode. See the Output Amplitude Control Mode section for the RU/RD function.
6. When profile Pins P2 and P3 are used for RU/RD, any two channels can perform 2-level modulation with RU/RD or any two channels can perform linear frequency or phase sweep with RU/RD. The other two channels can be in single-tone generation mode.
7. When profile Pin P3 is used for RU/RD, any channel can be used in 8-level modulation with RU/RD. The other three channels can be in single-tone generation mode.
8. When SDIO_1:3 pins are used for RU/RD, any one or two channels, any three channels, or all four channels can perform 2-level modulation with RU/RD. Any channels not in the 2-level modulation can be in single-tone generation mode.
9. When the SDIO_1:3 pins are used for RU/RD, any one or two channels can perform 4-level modulation with RU/RD. Any channels not in 4-level modulation can be in single-tone generation mode.
10. When the SDIO_1:3 pins are used for RU/RD, any channel can perform 16-level modulation with RU/RD. The other three channels can be in single-tone generation mode.
11. Amplitude modulation, linear amplitude sweep modes, and the RU/RD function cannot operate simultaneously, but frequency and phase modulation can operate simultaneously as the RU/RD function.

POWER SUPPLIES

The AVDD and DVDD supply pins provide power to the DDS core and supporting analog circuitry. These pins connect to a 1.8 V nominal power supply.

The DVDD_I/O pin connects to a 3.3 V nominal power supply. All digital inputs are 3.3 V logic except for the CLK_MODE_SEL input. The CLK_MODE_SEL (Pin 24) is an analog input and should be operated by 1.8 V logic.

SINGLE-TONE MODE

Single-tone mode is the default mode of operation after a master reset signal. In this mode, all four DDS channels share a common address location for the frequency tuning word (Register 0x04) and phase offset word address location (Register 0x05). Channel enable bits are provided in combination with these shared addresses. As a result, the frequency tuning word and/or phase offset word can be independently programmed between channels (see the following Step 1 through Step 5). The channel enable bits do not require an I/O update to enable or disable a channel.

See the Register Map section for a description of the channel enable bits in the channel select register or CSR (Register 0x00). The channel enable bits are enabled or disabled immediately after the CSR's data byte is written.

Address sharing enables channels to be written simultaneously, if desired. The default state enables all channel enable bits. Therefore, the frequency tuning word and/or phase offset word will be common to all channels, but written only once through the serial I/O port.

The following steps present a basic protocol to program a different frequency tuning word and/or phase offset word for each channel using the channel enable bits.

1. Power-up DUT and issue a master reset. A master reset places the part in single-tone mode and single-bit mode for serial programming operations (refer to the Serial I/O Modes of Operation section). Frequency tuning words and phase offset words default to 0 at this point.
2. Enable only one channel enable bit (Register 0x00) and disable the other channel enable bits.
3. Using the serial I/O port, program the desired frequency tuning word (Register 0x04) and/or the phase offset word (Register 0x05) for the enabled channel.
4. Repeat Step 2 and Step 3 for each channel.
5. Send an I/O update signal. After an I/O update, all channels should output their programmed frequency and/or phase offset value.

Single-Tone Mode—Matched Pipeline Delay

In single-tone mode, the AD9959 offers matched pipeline delay to the DAC input for all frequency, phase, and amplitude changes. This avoids having to deal with different pipeline delays between the three input ports for such applications. The feature is enabled by asserting the match pipeline delay bit found in the channel function register (CSR) (Register 0x03). This feature is available in single-tone mode only.

REFERENCE CLOCK MODES

The AD9959 supports multiple reference clock configurations to generate the internal system clock. As an alterative to clocking the part directly with a high frequency clock source, the system clock may be generated using the internal, PLL-based reference clock multiplier. An on-chip oscillator circuit is also available for providing a low frequency reference signal by connecting a crystal to the clock input pins. Enabling these features allows the part to operate with a low frequency clock source and still provide a high update rate for the DDS and DAC. However, using the clock multiplier changes the output phase noise characteristics. For best phase noise performance, a clean, stable clock with a high slew is required. Refer to Figure 19 and Figure 20.

Enabling the PLL allows multiplication of the reference clock frequency from 4× to 20×, in integer steps. The PLL multiplication value is represented by a 5-bit multiplier value. These bits are located in the Function Register 1 (FR1), bits <22:18>. Refer to the Register Map.

When FR1 <22:18> is programmed with values ranging from 4 to 20 (decimal), the clock multiplier is enabled. The integer value in the register represents the multiplication factor. The system clock rate with the clock multiplier enabled is equal to the reference clock rate multiplied by the multiplication factor. If FR1 <22:18> is programmed with a value less than 4 or greater than 20, the clock multiplier is disabled and the multiplication factor is effectively 1.

Whenever the PLL clock multiplier is enabled or the multiplication value is changed, time should be allowed to lock the PLL (typically 1ms).

Note that the output frequency of the PLL is restricted to a frequency range of 100 MHz to 500 MHz. However, there is a VCO gain bit that must be used appropriately. The VCO gain bit defines two ranges (low/high) of frequency output. The VCO gain bit defaults to low (see Specifications for details).

The charge pump current in the PLL defaults to 75 μA. This setting typically produces the best phase noise characteristics. Increasing the charge pump current may degrade phase noise, but it decreases the lock time and changes the loop bandwidth.

Enabling the on-chip oscillator for crystal operation is performed by driving the CLK_MODE_SEL (Pin 24) to logic high (1.8 V logic). With the on-chip oscillator enabled, connection of an external crystal to the REF_CLK and REF_CLKB inputs is made, producing a low frequency reference clock. The crystal's frequency must be in the range of 20 MHz to 30 MHz.

Table 4 summarizes the clock modes of operation. See the Specifications table for more details.

Table 4.

CLK_MODE_SEL Pin (24)	FR1<22:18> PLL bits = M	Oscillator Enabled	System Clock ($f_{SYS\ CLK}$)	Min/Max Freq. Range (MHz)
High = 1.8 V logic	4 ≤ M ≤ 20	Yes	$f_{SYS\ CLK} = f_{OSC} \times M$	100 < f_{SYSCLK} < 500
High = 1.8 V logic	M < 4 or M > 20	Yes	$f_{SYS\ CLK} = F_{OSC}$	20 < f_{SYSCLK} < 30
Low	4 ≤ M ≤ 20	No	$f_{SYS\ CLK} = F_{REF\ CLK} \times M$	100 < f_{SYSCLK} < 500
Low	M < 4 or M > 20	No	$f_{SYS\ CLK} = F_{REF\ CLK}$	0 < $f_{SYS\ CLK}$ < 500

Reference Clock Input Circuitry

The reference clock input circuitry has two modes of operation controlled by the logic state of Pin 24 (clock mode select). The first mode (logic low) configures as an input buffer. In this mode, the reference clock must be ac-coupled to the input due to internal dc biasing. This mode supports either differential or single-ended configurations. If single-ended mode is chosen, the complementary reference clock input (Pin 23) should be decoupled to AVDD or AGND via a 0.1 μF capacitor. Figure 32 to Figure 34 exemplify typical reference clock configurations for the AD9959.

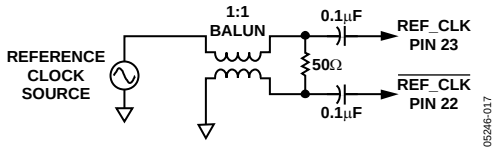


Figure 32.

The reference clock inputs can also support an LVPECL or PECL driver as the reference clock source.

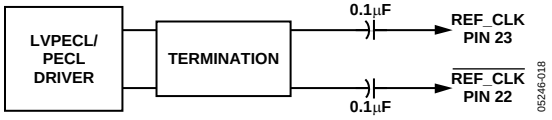


Figure 33.

The second mode of operation (Pin 24 = logic high = 1.8 V) provides an internal oscillator for crystal operation. In this mode, both clock inputs are dc-coupled via the crystal leads and bypassed. The range of crystal frequencies supported is from 20 MHz to 30 MHz. Figure 34 shows the configuration for using a crystal.

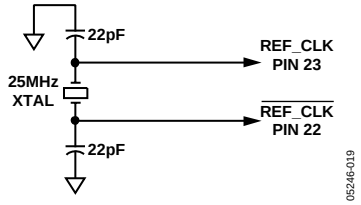


Figure 34.

SCALABLE DAC REFERENCE CURRENT CONTROL MODE

The R_{SET} is common to all four DACs. As a result, the full-scale currents are equal by default. The scalable DAC reference can be used to set each DAC's full-scale current independently from one another. This is accomplished by using the CFR register bits <9:8>. Table 5 shows how each DAC can be individually scaled for independent channel control. This provides for binary attenuation.

Table 5.

CFR <9:8>		LSB Current State
1	1	Full scale
0	1	Half scale
1	0	Quarter scale
0	0	Eighth scale

POWER-DOWN FUNCTIONS

The AD9959 supports an externally controlled power-down feature and the more common software programmable power-down bits found in previous Analog Devices' DDS products.

The software control power down allows the input clock circuitry, DAC, and the digital logic (for each separate channel) to be individually powered down via unique control bits (CFR <7:6>). These bits are not active when the externally controlled power-down pin (PWR_DWN_CTL) is high. When the PWR_DWN_CTL input pin is high, the AD9959 enters a power-down mode based on the FR1 <6> bit. When the PWR_DWN_CTL input pin is low, the external power-down control is inactive.

When the FR1 <6> bit is zero, and the PWR_DWN_CTL input pin is high, the AD9959 is put into a fast recovery power-down mode. In this mode, the digital logic and the DAC digital logic are powered down. The DAC bias circuitry, oscillator, and clock input circuitry is not powered down.

When the FR1 <6> bit is high and the PWR_DWN_CTL pin is high, the AD9959 is put into the full power-down mode. In this mode, all functions are powered down. This includes the DAC and PLL, which take a significant amount of time to power up. When the PLL is bypassed, the PLL is shut down to conserve power.

When the PWR_DWN_CTL input pin is high, the individual power down bits (CFR <7:6>) and (FR1 <7>) are invalid (don't care) and are unused. When the PWR_DWN_CTL input pin is low, the individual power down bits controls the power-down modes of operation.

Note that the power-down signals are all designed such that a Logic 1 indicates the low power mode and Logic 0 indicates the powered-up mode.

MODULATION MODE

The AD9959 can perform 2-/4-/8- or 16-level modulation of frequency, phase, or amplitude. Modulation is achieved by applying data to the profile pins. Each channel can be programmed separately, but the ability to modulate multiple channels simultaneously is constrained by the limited number of profile pins. For instance, 16-level modulation uses all four profile pins, which inhibits modulation for the remaining channels.

In addition, the AD9959 has the ability to ramp up or ramp down the output amplitude before, during, or after a modulation (FSK, PSK only) sequence. This is performed by using the 10-bit output scalar. If the RU/RD feature is desired, unused profile pins or unused SDIO_1:3 pins can be configured to initiate the operation. See the Output Amplitude Control Mode section for more details of the RU/RD feature.

In modulation mode, each channel has its own set of control bits to determine the type (frequency, phase, or amplitude) of modulation. Each channel has 16 profile registers for flexibility. Registers 0x0A through 0x18 are profile registers for modulation of frequency, phase, or amplitude. Registers 0x04, 0x05, and 0x06 are dedicated registers for frequency, phase, and amplitude, respectively. These registers contain the first frequency, phase offset, and amplitude word.

Frequency modulation has a 32-bit resolution, phase modulation is 14 bits, and amplitude is 10 bits. When modulating phase or amplitude, the word value must be MSB-aligned in the profile registers and the unused bits are don't care bits.

In modulation mode, AFP bits (CFR <23:22>) and level bits (FR1 <9:8>) are programmed to configure the modulation type and level. See Table 6 and Table 7 settings. Note that the linear sweep enable bit must be set to Logic 0 in direct modulation mode.

Table 6.

AFP CFR <23:22>		Linear Sweep Enable CFR <14>	Description
0	0	X	Modulation disabled
0	1	0	Amplitude modulation
1	0	0	Frequency modulation
1	1	0	Phase modulation

Table 7.

Modulation Level Bits FR1 <9:8>		Description
0	0	2-level modulation
0	1	4-level modulation
1	0	8-level modulation
1	1	16-level modulation

When modulating, the RU/RD function can be limited based on pins available for controlling the feature. SDIO pins are for RU/RD only, not modulation.

Table 8.

RU/RD Bits FR1 <11:10>		Description
0	0	RU/RD disabled.
0	1	Only profile Pin 2 and Pin 3 available for RU/RD operation.
1	0	Only profile Pin 3 available for RU/RD operation.
1	1	Only SDIO Pins 1, 2, and 3 available for RU/RD operation; this forces the serial I/O to be used only in1-bit mode.

If profile pins are used for RU/RD, Logic 0 is for ramp-up and Logic 1 is for ramp down.

Because of the number of available channels and limited data pins, it is necessary to assign the profile pins and/or SDIO_1:3 pins to a dedicated channel. This is controlled by the profile pin configuration or PPC bits (FR1 <14:12>). Each of the modulation descriptions to follow incorporates data pin assignments.

2-Level Modulation—No RU/RD

Modulation level bits are set to 00 (2-level). AFP bits are set to the desired modulation type. RU/RD bits and the linear sweep bit are disabled. Table 9 displays how the profile pins and channels are assigned.

Table 9.

Profile Pin Configuration(PPC) Bits FR1<14:12>			P0	P1	P2	P3	Description
x	x	x	CH0	CH1	CH2	CH3	2-level mode all channels No RU/RD

As shown in Table 9, only profile Pin P0 can be used to modulate Channel 0. If the P0 pin is Logic 0, Register 0 (Register 0x04) is chosen, if the P0 pin is Logic 1, Register 1 (Register 0x0A) is chosen.

4-Level Modulation—No RU/RD

Modulation level bits are set to 01 (4-level). AFP bits are set to the desired modulation type. RU/RD bits and the linear sweep bit are disabled. Note that the other two channels not being used should have their AFP bits set to 00 due to the lack of profile pins. The table below displays how the profile pins and channels are assigned to each other.

Table 10.

Profile Pin Config. (PPC) Bits FR1 <14:12>			P0	P1	P2	P3	Description
0	0	0	CH0	CH0	CH1	CH1	4-level modulation on CH0 and CH1, no RU/RD
0	0	1	CH0	CH0	CH2	CH2	4-level modulation on CH0 and CH2, no RU/RD
0	1	0	CH0	CH0	CH3	CH3	4-level modulation on CH0 and CH3, no RU/RD
0	1	1	CH1	CH1	CH2	CH2	4-level modulation on CH1 and CH2, no RU/RD
1	0	0	CH1	CH1	CH3	CH3	4-level modulation on CH1 and CH3, no RU/RD
1	0	1	CH2	CH2	CH3	CH3	4-level modulation on CH2 and CH3, no RU/RD

For the above condition, the profile register chosen is based on the two bit value presented to profile pins <P0:P1> or <P2:P3>.

For example, if PPC = 010 , <P1:P2>= 11, and <P2:P3>= 01, then the contents of Profile Register 3 of Channel 0 are presented to Channel 0's output and the contents of Profile Register 1 of Channel 3 are presented to Channel 3's output.

8-Level Modulation—No RU/RD

Modulation level bits are set to 10 (8-level). AFP bits are set to a non-zero value. RU/RD bits and the linear sweep bit are disabled. Note that the AFP bits of the three channels not being used must be set to 00. Table 11 shows the assignment of profile pins and channels.

Table 11.

Profile Pin Config. Bits FR1 <14:12>			P0	P1	P2	P3	Description
x	0	0	CH0	CH0	CH0	x	8-level modulation on CH0, no RU/RD
x	0	1	CH1	CH1	CH1	x	8-level modulation on CH1 no RU/RD
x	1	0	CH2	CH2	CH2	x	8-level modulation on CH2, no RU/RD
x	1	1	CH3	CH3	CH3	x	8-level modulation on CH3, no RU/RD

For this condition, the profile register (1 of 16) chosen is based on the 3-bit value presented to the profile <P0-P2> pins. For example, if PPC = X10 and <P0-P2> = 111, the contents of Profile Register 7 of Channel 0 are presented to Channel 0.

16-Level Modulation—No RU/RD

Modulation level bits are set to 11 (16-level). AFP bits are set to the desired modulation type. RU/RD bits and the linear sweep bit are disabled. The AFP bits of the three channels not being used must be set to 00. Table 12 displays how the profile pins and channels are assigned.

Table 12.

Profile Pin Config. (PPC) Bits FR1 <14:12>			P0	P1	P2	P3	Description
x	0	0	CH0	CH0	CH0	CH0	16-level modulation on CH0, no RU/RD
x	0	1	CH1	CH1	CH1	CH1	16-level modulation on CH1, no RU/RD
x	1	0	CH2	CH2	CH2	CH2	16-level modulation on CH2, no RU/RD
x	1	1	CH3	CH3	CH3	CH3	16-level modulation on CH3, no RU/RD

For the above conditions, the profile register chosen is based on the four bit value presented to profile <P0-P3> pins. For example, if PPC = X11 and <P0-P3>= 1110, the contents of Profile Register 14 of Channel 3 is presented to Channel 3.

2-Level Modulation Using Profile Pins for RU/RD

When the RU/RD bit = 01, Profile Pins P2 and P3 are available for RU/RD. Note that only a modulation level of two is available in this mode. See Table 13 for available pin assignments.

Table 13.

Profile Pin Config. Bits FR1 <14:12>			P0	P1	P2	P3	Description
0	0	0	CH0	CH1	CH0 RU/RD	CH1 RU/RD	2-level modulation w/RU/RD, CH0, CH1
0	0	1	CH0	CH2	CH0 RU/RD	CH2 RU/RD	2-level modulation w/RU/RD, CH0, CH2
0	1	0	CH0	CH3	CH0 RU/RD	CH3 RU/RD	2-level modulation w RU/RD, CH0, CH3
0	1	1	CH1	CH2	CH1 RU/RD	CH2 RU/RD	2-level modulation w/RU/RD , CH1, CH2
1	0	0	CH1	CH3	CH1 RU/RD	CH3 RU/RD	2-level modulation w/RU/RD, CH1, CH3
1	0	1	CH2	CH3	CH2 RU/RD	CH3 RU/RD	2-level modulation w/RU/RD, CH2, CH3

8-Level Modulation Using a Profile Pin for RU/RD

When the RU/RD bit = 10, Profile Pin P3 is available for RU/RD. Note that only a modulation level of eight is available. See Table 14 for available pin assignments.

Table 14.

Profile Pin Config. Bits FR1 <14:12>			P0	P1	P2	P3	Description
x	0	0	CH0	CH0	CH0	CH0 RU/RD	8-level modulation with RU/RD, Channel 0
x	0	1	CH1	CH1	CH1	CH1 RU/RD	8-level modulation with RU/RD, Channel 1
x	1	0	CH2	CH2	CH2	CH2 RU/RD	8-level modulation with RU/RD, Channel 2
x	1	1	CH3	CH3	CH3	CH3 RU/RD	8-level modulation with RU/RD, Channel 3

MODULATION USING SDIO PINS FOR RU/RD

For RU/RD bits = 11, SDIO Pins 1, 2, and 3 are available for RU/RD. In this mode, modulation levels of 2/4/16 are available. Note that the serial I/O port can only be used in 1-bit serial mode.

2-Level Modulation Using SDIO Pins for RU/RD

Table 15.

Profile Pin Config. Bits FR1 <14:12>			P0	P1	P2	P3
x	x	x	CH0	CH1	CH2	CH3

For the configuration above each profile pin is dedicated to a specific channel. In this case, the SDIO pins can be used for the RU/RD function, as described in Table 16.

Table 16.

SDIO Pins			
1	2	3	Description
0	0	0	Triggers the ramp-up function for Channel 0
0	0	1	Triggers the ramp-down function for Channel 0
0	1	0	Triggers the ramp-up function for Channel 1
0	1	1	Triggers the ramp-down function for Channel 1
1	0	0	Triggers the ramp-up function for Channel 2
1	0	1	Triggers the ramp-down function for Channel 2
1	1	0	Triggers the ramp-up function for Channel 3
1	1	1	Triggers the ramp-down function for Channel 3

4-Level Modulation Using SDIO Pins for RU/RD

For RU/RD = 11 (SDIO Pins 1 and 2 are available for RU/RD), the modulation level is set to four. See Table 17 for pin assignments, including SDIO pin assignments.

Table 17.

Profile Pin Config. Bits FR1 <14:12>			P0	P1	P2	P3	SDIO_1	SDIO_2	SDIO_3
0	0	0	CH0	CH0	CH1	CH1	CH0 RU/RD	CH1 RU/RD	NA
0	0	1	CH0	CH0	CH2	CH2	CH0 RU/RD	CH2 RU/RD	NA
0	1	0	CH0	CH0	CH3	CH3	CH0 RU/RD	CH3 RU/RD	NA
0	1	1	CH1	CH1	CH2	CH2	CH1 RU/RD	CH2 RU/RD	NA
1	0	0	CH1	CH1	CH3	CH3	CH1 RU/RD	CH3 RU/RD	NA
1	0	1	CH2	CH2	CH3	CH3	CH2 RU/RD	CH3 RU/RD	NA

For the configuration shown in Table 17, the profile register is chosen based on the two bit value presented to <P1:P2> or <P3:P4>.

For example, if PPC = 011, <P0:P1> = 11, and <P2:P3> = 01, the contents of Profile Register 3 of Channel 1 are presented to Channel 1's output and the contents of Profile Register 1 of Channel 2 are presented to Channel 2's output. SDIO Pins 1 and 2 provide the RU/RD function.

16-Level Modulation Using SDIO Pins for RU/RD

RU/RD = 11 (SDIO Pin 1 available for RU/RD) and the level is set to 16. See the pin assignment shown in Table 18.

Table 18.

Profile Pin Configuration FR1<14:12>			P0	P1	P2	P3	SDIO_1	SDIO_2	SDIO_3
x	0	0	CH0	CH0	CH0	CH0	CH0 RU/RD	NA	NA
x	0	1	CH1	CH1	CH1	CH1	CH1 RU/RD	NA	NA
x	1	0	CH2	CH2	CH2	CH2	CH2 RU/RD	NA	NA
x	1	1	CH3	CH3	CH3	CH3	CH3 RU/RD	NA	NA

For the configuration shown in Table 18, the profile register is chosen based on the four bit value presented to <P0:P3>. For example, if PPC = 1110 and <P0-P1> = 1101, then the contents of Profile Register 13 of Channel 2 is presented to Channel 2. The SDIO_1 pin provides the RU/RD function.

LINEAR SWEEP (SHAPED) MODULATION MODE

Linear sweep enables the user to sweep frequency, phase, or amplitude from a starting point (S0) to an endpoint (E0). The purpose of linear sweep modes is to provide better bandwidth containment compared to direct modulation by replacing greater instantaneous changes with more gradual, user-defined changes between S0 and E0.

In linear sweep mode, S0 is loaded into Profile Register 0 (Profile 0 is represented by one of the three Registers 0x04, 0x05, or 0x06 depending on the type of sweep) and E0 is always loaded into Profile Register 1 (Register 0x0A). If E0 is configured for frequency sweep, the resolution is 32-bits, phase sweep is 14 bits, and amplitude sweep is 10 bits. When sweeping phase or amplitude, the word value must be MSB-aligned in Profile 1 register. The unused bits are don't care bits

The profile pins are used to trigger and control the direction of the linear sweep for frequency, phase, and amplitude. All channels can be programmed separately for a linear sweep. In linear sweep mode, Profile Pin 0 is dedicated to Channel 0. Profile Pin 1 is dedicated to Channel 1, and so on.

The AD9959 has the ability to ramp up or ramp down (RU/RD) the output amplitude (using the 10-bit output scalar) before and after a linear sweep. If the RU/RD feature is desired, unused profile pins or unused SDIO_1:3 pins can be configured for the RU/RD operation.

To enable linear sweep mode for a particular channel, AFP bits (CFR <23:22>), modulation level bits (FR1 <9:8>), and the linear sweep enable bit (CFR <14>) are programmed.

The AFP bits determine the type of linear sweep to be performed. The modulation level bits must be set to 00 (2-level) for that specific channel (see Table 19 and Table 20)

Table 19.

AFP CFR <23:22>		Linear Sweep Enable CFR <14>	Description
0	0	1	N/A
0	1	1	Amplitude sweep
1	0	1	Frequency sweep
1	1	1	Phase sweep

Table 20.

Modulation Level Bits FR1 <9:8>		Description
0	0	2-level modulation
0	1	4-level modulation
1	0	8-level modulation
1	1	16-level modulation

Setting the Slope of the Linear Sweep

The slope of the linear sweep is set by the intermediate step size (delta-tuning word) between S0 and E0 and the time spent (sweep ramp rate word) at each step. The resolution of the delta-tuning word is 32 bits for frequency, 14 bits for phase, and 10 bits for amplitude. The resolution for the delta ramp rate word is 8 bits.

In linear sweep, each channel is assigned a rising delta tuning word (RDW, Register 0x08) and a rising sweep ramp rate word (RSRR, Register 0x07). These settings apply when sweeping up towards E0. The falling delta tuning word (FDW, Register 0x09) and falling sweep ramp rate (FSRR, Register 0x07) apply when sweeping down towards S0. The following graph displays a linear sweep up and then down using a profile pin. Note that the no-dwell bit is disabled; otherwise, the sweep accumulator returns to 0 upon reaching EO.

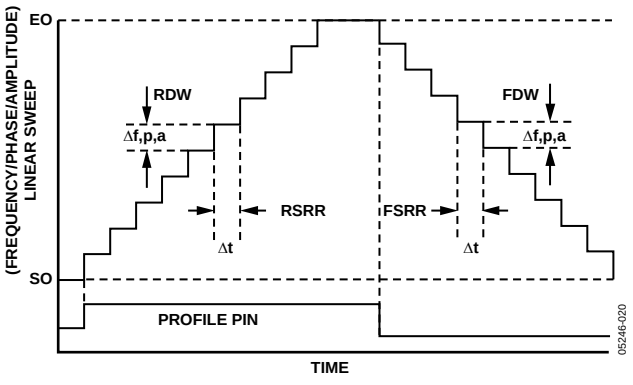


Figure 35.

For a piecemeal or a nonlinear transition between S0 and E0, the delta-tuning words and ramp rate words can be reprogrammed during the transition to produce the desired response.

The formulae for calculating the step size of RDW or FDW for delta frequency, delta phase, or delta amplitude are as follows:

$$\Delta f = \left(\frac{RDW}{2^{32}}\right) \times SYNC\_CLK \text{ (Hz)}$$

$$\Delta \Phi = \left(\frac{RDW}{2^{14}}\right) \times 360°$$

$$\Delta a = \left(\frac{RDW}{2^{10}}\right) \times 1024 \text{ (DAC full scale current)}$$

The formula for calculating delta time from RSRR or FSRR is

$$t = \left(\frac{RSRR}{2^{8}}\right) \times 1/SYNC\_CLK$$

At 500 MSPS operation (SYNC_CLK =125 MHz), the maximum time interval between steps is 1/125 MHz × 256 = 2.048 µs. The minimum time interval is (1/125 MHz) × 1 = 8.0 ns.

The sweep ramp rate block (timer) consists of a loadable 8-bit down counter that continuously counts down from the loaded value to 1. When the ramp rate timer equals 1, the proper ramp rate value is loaded and the counter begins counting down to 1 again. This load and count-down operation continues for as long as the timer is enabled. However, the count can be reloaded before reaching 1 by either of the following two methods:

1. Method one is by changing the profile pin. When the profile pin changes from Logic 0 to Logic 1, the rising sweep ramp rate register (RSRR) value is loaded into the ramp rate timer, which then proceeds to count down as normal. When the profile pin changes from Logic 1 to Logic 0, the falling sweep ramp rate register (FSRR) value is loaded into the ramp rate timer, which then proceeds to count down as normal.

2. Method two is by setting the CFR <14> bit and issuing an I/O update. If sweep is enabled and CFR <14> is set, the ramp rate timer loads the value determined by the profile pin. If the profile pin is high the ramp rate timer loads the RSRR; if the profile pin is low, the ramp rate timer loads FSRR.

Frequency Linear Sweep Example: AFP Bits =10

Modulation level bits = 00, sweep enable = 1, no-dwell bit = 0.

In linear sweep mode, when the profile pin transitions from low to high, the RDW is applied to the input of the sweep accumulator and the RSRR register is loaded into the sweep rate timer.

The RDW accumulates at the rate given by the ramp rate (RSRR) until the output is equal to the CTW1 register value. The sweep is then complete and the output is held constant in frequency.

When the profile pin transitions from high to low, the FDW is applied to the input of the sweep accumulator and the FSRR register is loaded into the sweep rate timer.

The FDW accumulates at the rate given by the ramp rate (FSRR) until the output is equal to the CTW0 register value. The sweep is then complete and the output is held constant in frequency.

See Figure 36 for the linear sweep block diagram. Figure 38 depicts a frequency sweep with no-dwell mode disabled. In this mode, the output follows the state of the profile pin. A phase or amplitude sweep works in the same manner.

LINEAR SWEEP—NO-DWELL MODE

If the linear sweep no-dwell bit is set (CFR <15>), the rising sweep is started in an identical manner to the dwell linear sweep mode. That is, upon detecting Logic 1 on the profile input pin, the rising sweep action is initiated. The word continues to sweep up at the rate set by the rising sweep ramp rate at the resolution set by the rising delta tuning word until it reaches the terminal value. Upon reaching the terminal value, the output immediately reverts back to the starting point and remains until Logic 1 is detected on the profile pin.

Figure 37 shows an example of the no-dwell mode. The points labeled "A" indicate where a rising edge is detected on the profile pin and the points labeled "B" indicate where the AD9959 has deter-mined that the output has reached E0 and reverts to S0. The falling ramp rate register and the falling delta word are unused in this mode.

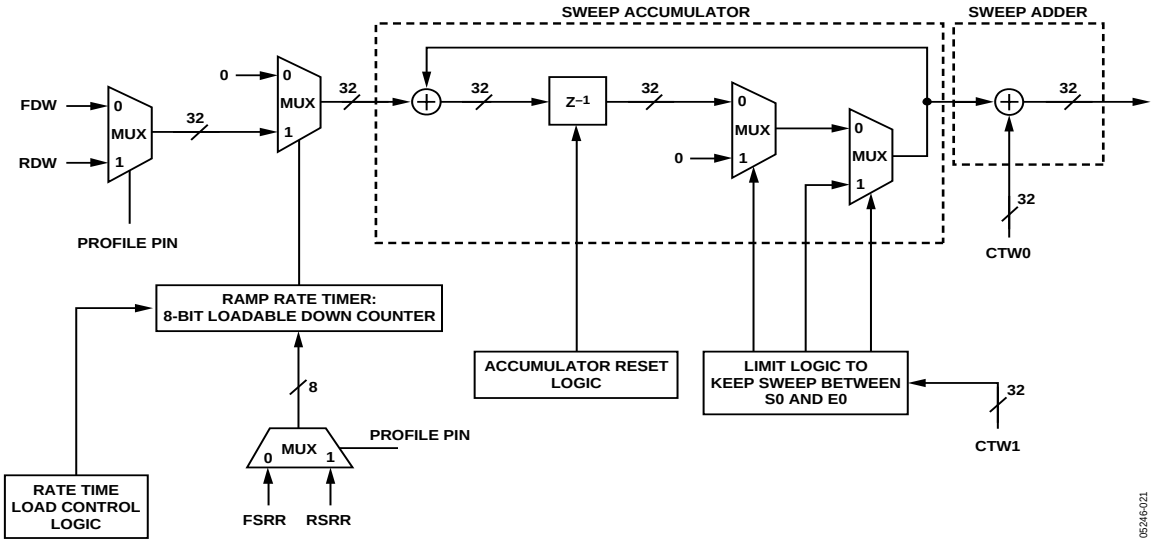


Figure 36. Linear Sweep Block Diagram

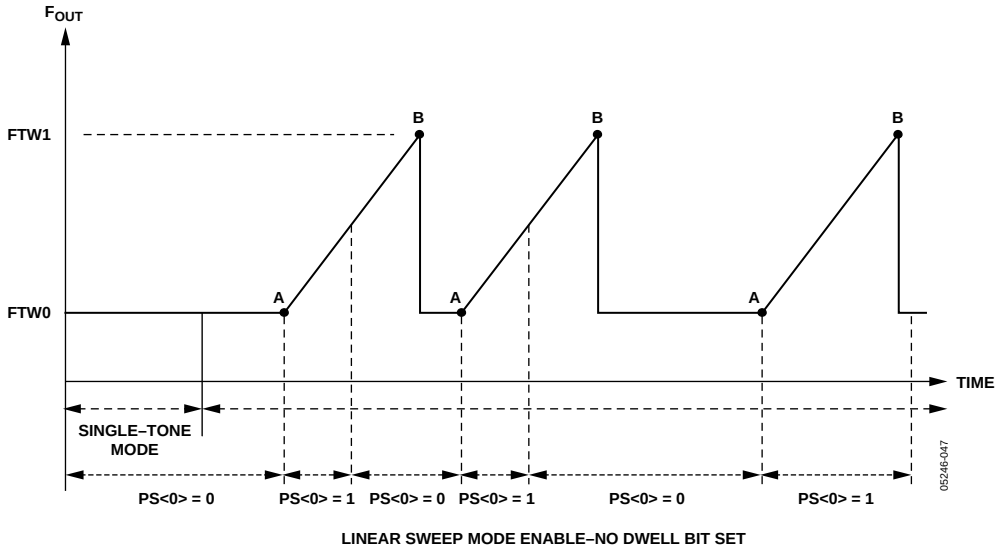


Figure 37.

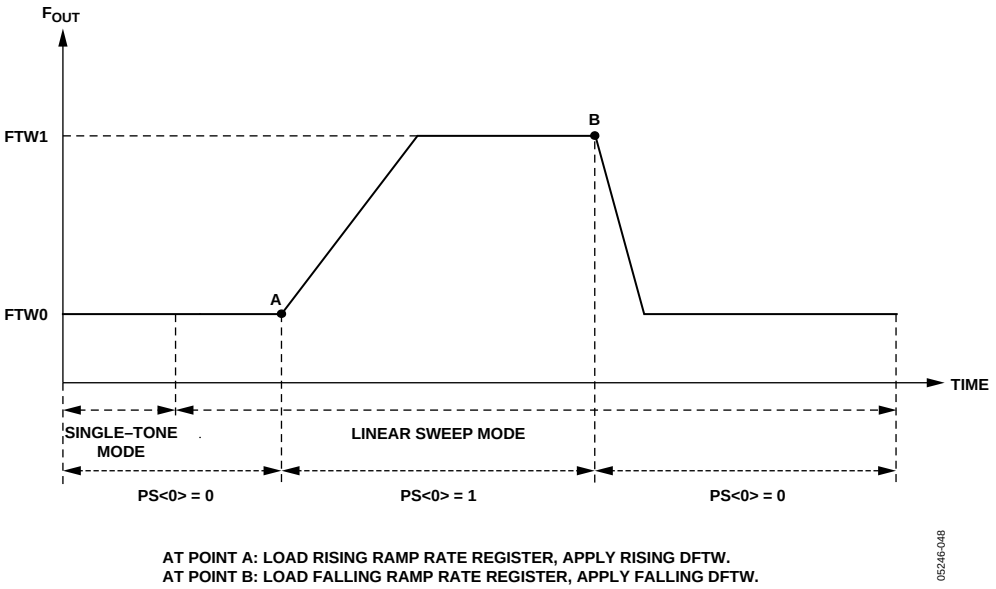


Figure 38. Linear Sweep with the No-Dwell Feature Disabled

SWEEP AND PHASE ACCUMULATOR CLEARING FUNCTIONS

The AD9959 allows two different clearing functions. The first is a continuous zeroing of the sweep logic and phase accumulator (clear and hold). The second is a clear and release or automatic zeroing function. CFR <4> is the automatic clear sweep accumulator bit and CFR <2> is the automatic clear phase accumulator bit. The continuous clear bits are located in CFR, where CFR <3> clears the sweep accumulator and CFR <1> clears the phase accumulator.

Continuous Clear Bits

The continuous clear bits are static control signals that, when active high, hold the respective accumulator at 0 while the bit is active. When the bit goes low, the respective accumulator is allowed to operate.

Clear and Release Bits

The auto clear sweep accumulator bit, when set, clears and releases the sweep accumulator upon an I/O update or a change in the profile input pins. The autoclear phase accumulator, when set, clears and releases the phase accumulator upon an I/O update or a change in the profile pins. The automatic clearing function is repeated for every subsequent I/O update or change in profile pins until the clear and release bits are reset via the serial port.

OUTPUT AMPLITUDE CONTROL MODE

The 10-bit scale factor (multiplier) controls the ramp-up and ramp-down (RU/RD) time of an on/off emission from the DAC. In burst transmissions of digital data, it reduces the adverse spectral impact of abrupt bursts of data. It can be bypassed by clearing the multiplier enable bit (ACR <12> = 0).

Automatic and manual RU/RD modes are supported. The automatic mode generates a zero-scale up to a full-scale (10-bits) linear ramp at a rate determined by the amplitude ramp rate control register. The start and direction of the ramp can be controlled by either the profile pins or the SDIO1:3 pins.

Manual mode allows the user to directly control the output amplitude by manually writing to the amplitude scale factor value in the amplitude control register (Register 0x06). Manual mode is enabled by setting Bits ACR <12> = 1 and ACR <11> = 0.

Automatic RU/RD Mode Operation

The automatic RU/RD mode is active when both Bits ACR <12> and ACR <11> are set. When automatic RU/RD is enabled, the scale factor is internally generated and applied to the multiplier input port for scaling the output. The scale factor is the output of a 10-bit counter that increments/decrements at a rate set by the 8-bit output ramp rate register. The scale factor increments if the external pin is high and decrements if the pin is low. The internally generated scale factor step size is controlled by the <15:14> bits in the ACR register. Table 21 describes the increment/decrement step size of the internally generated scale factor per the ACR <15:14> bits.

Table 21.

Autoscale Factor Step Size ASF <15:14> (Binary)	Increment/Decrement Size
00	1
01	2
10	4
11	8

A special feature of this mode is that the maximum output amplitude allowed is limited by the contents of the amplitude scale factor register (ASFR). This allows the user to ramp to a value less than full scale.

Ramp Rate Timer

The ramp rate timer is a loadable down counter that generates the clock signal to the 10-bit counter that generates the internal scale factor. The ramp rate timer is loaded with the value of the ASFR each time the counter reaches 1 (decimal). This load and count down operation continues for as long as the timer is enabled unless the timer is forced to load before reaching a count of 1.

If the load ARR timer bit ACR <10> is set, the ramp rate timer is loaded at an I/O update, a change in profile input, or on reaching a value of 1. The ramp timer can be loaded before reaching a count of 1 by three methods.

1. In the first method, the profile pin(s) or the SDIO_1:3 pins are changed. When the control signal changes state, the ACR value is loaded into the ramp rate timer, which then proceeds to count down as normal.
2. In the second method, the load ARR timer bit (ACR <10>) is set and an I/O update is issued.
3. The third method is by changing from inactive auto RU/RD mode to active auto RU/RD mode.

RU/RD Pin-to-Channel Assignment

1. When all four channels are in single-tone mode, the profile pins are used for RU/RD operation.
2. When both linear sweep and RU/RD modes are activated, the SDIO_1:3 pins are used for RU/RD operation.
3. In modulation mode, please refer to the Modulation Mode section for pin assignments.

Table 22.

Profile Pin	RU/RD Operation
P0	Ch 0
P1	Ch 1
P2	Ch 2
P3	Ch 3

Table 23.

LS and RU/RD Modes Enable Simultaneously	SDIO			Ramp-Up/Ramp-Down Control Signal Assignment
	1	2	3	
Enable for CH0	0	0	0	Ramp-up function for CH0
Enable for CH0	0	0	1	Ramp-down function for CH0
Enable for CH1	0	1	0	Ramp-up function for CH1
Enable for CH1	0	1	1	Ramp-down function for CH1
Enable for CH2	1	0	0	Ramp-up function for CH2
Enable for CH2	1	0	1	Ramp-down function for CH2
Enable for CH3	1	1	0	Ramp-up function for CH3
Enable for CH3	1	1	1	Ramp-down function for CH3

SYNCHRONIZING MULTIPLE AD9959 DEVICES

The AD9959 allows easy synchronization of multiple AD9959 devices. At power-up, the phase of SYNC_CLK can be offset between multiple devices. To correct for the offset and align the SYNC_CLK edges, there are three methods (one automatic mode and two manual modes) of synchronizing SYNC_CLKs. These modes force the internal state machines of multiple devices to a known state, which aligns SYNC_CLKs.

Any mismatch in REF_CLK phase between devices results in a corresponding phase mismatch on the SYNC_CLKs.

AUTOMATIC MODE SYNCHRONIZATION

In automatic mode, multiple part synchronization is achieved by connecting the SYNC_OUT pin on the master device to the SYNC_IN pin of the slave device(s). Devices are configured as master or slave through programming bits, accessible via the serial port.

A configuration for synchronizing multiple AD9959 devices in automatic mode is shown in the Application Circuits section. In this configuration, the AD9510 provides coincident REF_CLKs and SYNC_OUTs to all devices.

Operation

The first step is to program the master and slave devices for their respective roles. Enabling the master device is performed by writing its master enable bit (FR2 <6>) true. This causes the SYNC_OUT of the master device to output a pulse that has a pulse width equal to one system clock period and a frequency equal to one fourth of the system clock frequency. Enabling device(s) as slaves is performed by writing the slave enable bit (FR2 <7>) true.

In automatic synchronizing mode, the slave device(s) sample SYNC_OUT pulses from the master device and a comparison of all state machines is made by the autosynchronization circuitry. If the slave device(s) state machines are not identical to the master, the slave device(s) state machines are stalled for one system clock cycle. This procedure synchronizes the slave device(s) within three SYNC_CLK periods.

Delay Time Between SYNC_OUT and SYNC_IN

When the delay between SYNC_OUT and SYNC_IN exceeds one system clock period, phase offset bits (FR2 <1:0>) are used to compensate. The default state of these bits is 00, which implies that the SYNC_OUT of the master and the SYNC_IN of the slave have a propagation delay of less than one system clock period. If the propagation time is greater than one system clock period, the time should be measured and the appropriate offset programmed. Table 24 describes the delays required per system clock offset value.

Table 24.

System Clock Offset Value	SYNC_OUT/SYNC_IN Propagation Delay
00	0 ≤ delay ≤ 1
01	1 ≤ delay ≤ 2
10	2 ≤ delay ≤ 3
11	3 ≤ delay ≤ 4

Automatic Synchronization Status Bits

If a slave device falls out of sync, the sync status bit is set high. This bit can be read through the serial port bit (FR2 <5>). It is automatically cleared when read.

The synchronization routine continues to operate regardless of the state of the status bit. The status bit can be masked by writing Logic 1 to the synchronization status mask bit (FR2 <4>). If the status bit is masked, it is held low.

MANUAL SOFTWARE MODE SYNCHRONIZATION

The manual software mode is enabled by setting the manual synchronization bit (FR1 <0>) to Logic 1 in a device. In this mode, the I/O update that writes the Manual SW synchronization bit to Logic 0 stalls the state machine of the clock generator for one system clock cycle. Stalling the clock generation state machine by one cycle changes the phase relationship of SYNC_CLK between devices by one system clock period (90°).

Note that the user may have to repeat this process until the devices have their SYNC_CLK signals in phase. The SYNC_IN input may be left floating since it has an internal pull-up. The SYNC_OUT is not used.

The synchronization is complete when the master and slave(s) devices have their SYNC_CLK signals in phase.

MANUAL HARDWARE MODE SYNCHRONIZATION

Manual hardware mode is enabled by setting the manual SW synchronization bit (FR1 <1>) to Logic 1 in a device. In manual HW synchronization mode, the SYNC_CLK stalls by one system clock cycle each time a rising edge is detected on the SYNC_IN input. Stalling SYNC_CLK's state machine by one cycle changes the phase relationship of SYNC_CLK between devices by one system clock period (90°).

Note that the user may have to repeat the process until the devices have their SYNC_CLK signals in phase. The SYNC_IN input might be left floating since it has an internal pull-up. The SYNC_OUT is not used.

The synchronization is complete when the master and slave(s) devices have their SYNC_CLK signals in phase.

I/O_UPDATE, SYNC_CLK, AND SYSTEM CLOCK RELATIONSHIPS

I/O_UPDATE and SYNC_CLK are used together to transfer data from the serial I/O buffer to the active registers in the device. Data in the buffer is inactive.

SYNC_CLK is a rising edge active signal. It is derived from the system clock and a divide-by-4 frequency divider. The SYNC_CLK is externally provided, which can be used to synchronize external hardware to the AD9959's internal clocks.

I/O_UPDATE initiates the start of a buffer transfer. It can be sent synchronously or asynchronous relative to the SYNC_CLK. If the set-up time between these signals is met, then constant latency (pipeline) to the DAC output exists. For example, if repetitive changes to phase offset via the SPI port is desired, the latency of those changes to the DAC output is constant, otherwise a time uncertainty of one SYNC_CLK period will be present.

The I/O UPDATE is essentially over-sampled by the SYNC_CLK. Therefore, I/O_UPDATE must have a minimum pulse width greater than one SYNC_CLK period.

The timing diagram shown in Figure 39 depicts when data in the buffer is transferred to the active registers.

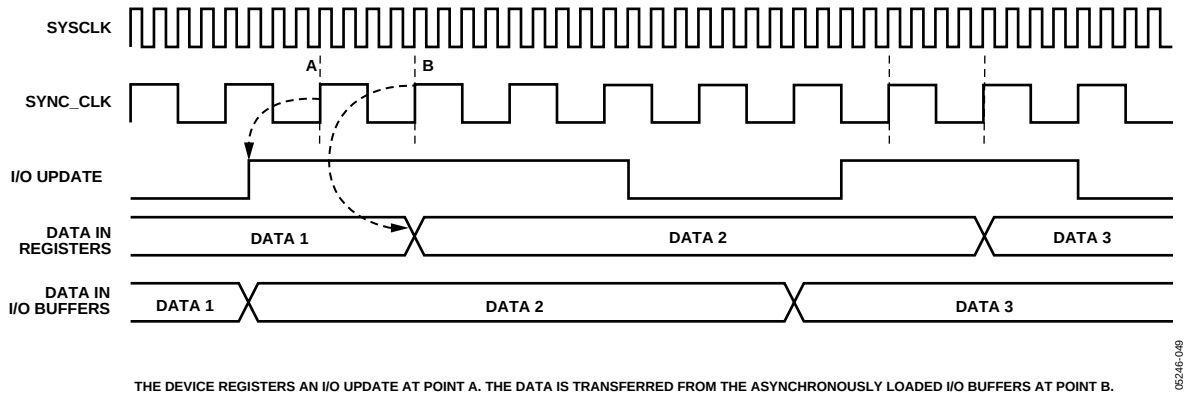


Figure 39.

SERIAL I/O PORT SECTION

OVERVIEW

The AD9959 serial I/O port offers multiple configurations to provide significant flexibility. The serial I/O port offers an SPI-compatible mode of operation that is virtually identical to the SPI operation found in earlier Analog Devices' DDS products. The flexibility is provided by four data (SDIO_0:3) pins that allow four programmable modes of serial I/O operation.

Three of the four data pins (SDIO_1:3) can be used for other functions than serial I/O port operation. These pins can also be used to initiate a ramp-up or ramp-down (RU/RD) of the 10-bit amplitude output scalar. In addition, one of these pins (SDIO_3) can also be used to provide the SYNC_I/O function that resynchronizes the serial I/O port controller if it is out of proper sequence.

The maximum speed of the serial I/O port SCLK is 200 MHz, but the four data (SDIO_0:3) pins can be used to further increase data throughput. The maximum data throughput using all SDIO_0:3 pins is 800 Mbps.

Note that all channels share Registers 0x03 to 0x18, which are shown in the Register Map section. This address sharing enables all four DDS channels to be written to simultaneously. For example, if a common frequency tuning word is desired for all four channels, it can be written once through the serial I/O port to all four channels. This is the default mode of operation (all channels enabled). To enable each channel to be independent, the four channel enable bits found in the channel select register (CSR) must be used.

There are effectively four sets or copies of addresses (0x03 to 0x18) that channel enable bits can access to provide channel independence. See the Control Register Descriptions section for further discussion of programming channels that are common to or independent from each other.

Serial operation of the AD9959 occurs at the register level, not the byte level. That is, the controller expects that all byte(s) contained in the register address will be accessed. The SYNC_I/O function can be used to abort an I/O operation, thereby allowing fewer than all bytes to be accessed. This feature can be used to program only a part of the addressed register. Note that only completed bytes are affected.

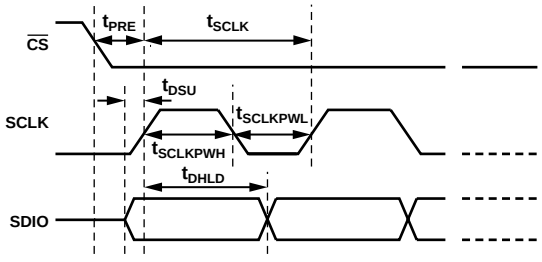
There are two phases to a serial communications cycle. Phase 1 is the instruction cycle, which writes the instruction byte into the AD9959. Each bit of the instruction byte is registered on each corresponding rising edge of SCLK. The instruction byte defines whether the upcoming data transfer is either a write or read operation. The instruction byte contains the serial address of the address register.

Phase 2 of the I/O cycle consists of the actual data transfer (write/read) between the serial port controller and the serial port buffer. The number of bytes transferred during this phase of the communication cycle is a function of the register being accessed. The actual number of additional SCLK rising edges required for the data transfer and instruction byte depends on the number of byte(s) in the register and the serial I/O mode of operation.

For example, when accessing Function Register 1 (FR1), which is three bytes wide, Phase 2 of the I/O cycle requires that three bytes be transferred. After transferring all data bytes per the instruction byte, the communication cycle is completed for that register.

At the completion of a communication cycle, the AD9959 serial port controller expects the next set of rising SCLK edges to be the instruction byte for the next communication cycle. All data written to the AD9959 is registered on the rising edge of SCLK. Data is read on the falling edge of SCLK. See Figure 36 and Figure 37.

Each set of communication cycles does not require an I/O_UPDATE to be issued. The I/O_UPDATE transfers data from the I/O port buffer to active registers. The I/O_UPDATE can be sent for each communication cycle or can be sent when all serial operations are complete. However, data is not active until an I/O_UPDATE is sent, with the exception of the channel enable bits in the Channel Select Register (CSR). These bits do not require an I/O_UPDATE to be enabled.



SYMBOL	DEFINITION	MIN
t_{PRE}	$\overline{CS}$ SETUP TIME	1.0ns
t_{SCK}	PERIOD OF SERIAL DATACLOCK	5.0ns
t_{DSU}	SERIAL DATA SETUP TIME	2.2ns
$t_{SCLKPWH}$	SERIAL DATA CLOCK PULSEWIDTH HIGH	2.2ns
$t_{SCLKPWL}$	SERIAL DATA CLOCK PULSEWIDTH LOW	1.6ns
t_{DHLD}	SERIAL DATA HOLD TIME	0ns

05246-023

Figure 40. Set-Up and Hold Timing for the Serial I/O Port

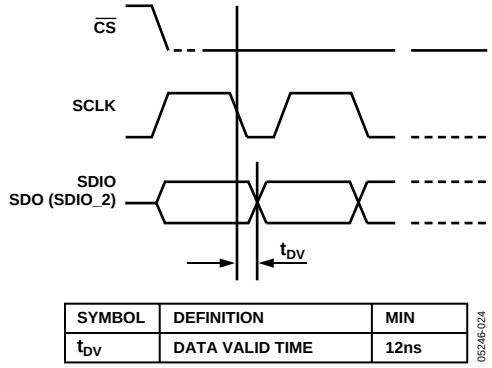


Figure 41. Timing Diagram for Data Read for Serial I/O Port

INSTRUCTION BYTE DESCRIPTION

The instruction byte contains the following information.

Table 25.

MSB	D6	D5	D4	D3	D2	D1	LSB
R/Wb	x[1]	x[1]	A4	A3	A2	A1	A0

[1] x = don't care bit.

Bit 7 of the instruction byte (R/Wb) determines whether a read or write data transfer occurs after the instruction byte write. A logic high indicates a read operation. Logic 0 indicates a write operation.

Bits 4 to 0 of the instruction byte determine which register is accessed during the data transfer portion of the communications cycle. The internal byte addresses are generated by the AD9959.

SERIAL I/O PORT PIN DESCRIPTION

Serial Data Clock (SCLK). The serial clock pin is used to synchronize data to and from the internal state machines of the AD9959. The maximum SCLK toggle frequency is 200 MHz.

Chip Select ($\overline{CS}$). The chip select pin allows more than one AD9959 device to be on the same set of serial communications lines. The chip select is an active low enable pin. Defined SDIO inputs go to a high impedance state when $\overline{CS}$ is high. If $\overline{CS}$ is driven high during any communications cycle, that cycle is suspended until $\overline{CS}$ is reactivated low. The $\overline{CS}$ pin can be tied low in systems that maintain control of SCLK.

Serial Data I/O (SDIO_0:3). Of the four SDIO pins, only the SDIO_0 pin is a dedicated SDIO pin. SDIO_1:3 can also be used to RU/RD the output amplitude. Bits <2:1> in the channel select register (CSR Register 0x00) control the configuration of these pins. See the Serial I/O Modes of Operation for more information.

SERIAL I/O PORT FUNCTION DESCRIPTION

Serial Data Out (SDO). The SDO function is available in single-bit (3-wire) mode only. In SDO mode, data is read from the SDIO_2 pin for protocols that use separate lines for transmitting and receiving data. (See Table 26 for pin configuration options) Bits <2:1> in the CSR register (Register 0x00) control the configuration of this pin. The SDO function is not available in 2-bit or 4-bit serial I/O modes.

SYNC_I/O. The SYNC_I/O function is available in 1-bit and 2-bit modes. SDIO_3 serves as the SYNC_I/O pin when this function is active. Bits <2:1> in the CSR register (Register 0x00) control the configuration of this pin. Otherwise the SYNC_I/O function is used to synchronize the I/O port state machines without affecting the addressable register contents. An active high input on the SYNC_I/O (SDIO_3) pin causes the current communication cycle to abort. After SDIO_3 returns low (Logic 0), another communication cycle can begin, starting with the instruction byte write. The SYNC_I/O function is not available in 4-bit serial I/O mode.

MSB/LSB TRANSFER DESCRIPTION

The AD9959 serial port can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. This functionality is controlled by CSR <0> in the channel select register (CSR). MSB first is the default mode. When CSR <0> is set high, the AD9959 serial port is in LSB first format. The instruction byte must be written in the format indicated by CSR <0>. That is, if the AD9959 is in LSB first mode, the instruction byte must be written from LSB to MSB. If the AD9959 is in MSB first mode (default), the instruction byte must be written from MSB to LSB.

Example Operation

To write the Function Register 1 (FR1) in MSB first format apply an instruction byte of MSB > 00000001 < LSB, starting with the MSB. From this instruction, the internal controller recognizes a write transfer of three bytes starting with the MSB, Bit <23>, in the FR1 address (Register 0x01). Bytes are written on each consecutive rising SCLK edge until Bit<0> is transferred. Once the last data bit is written, the I/O communication cycle is complete and the next byte is considered an instruction byte.

To write the Function Register 1 (FR1) in LSB first format, apply an instruction byte of MSB > 00000001 < LSB, starting with the LSB bit. From this instruction, the internal controller recognizes a write transfer of three bytes, starting with the LSB <0> in the FR1 address (0x01). Bytes are written on each consecutive rising SCLK edge until Bit <23> is transferred. Once the last data bit is written, the I/O communication cycle is complete and the next byte is considered an instruction byte

SERIAL I/O MODES OF OPERATION

The following are the four programmable modes of the serial I/O port operation:

1. Single-bit serial 2-wire mode (default mode).
2. Single-bit serial 3-wire mode.
3. 2-bit serial mode.
4. 4-bit serial mode (SYNC_I/O not available).

Table 26 displays the function of all six serial I/O interface pins, depending on the mode of serial I/O operation programmed.

Table 26. Serial I/O Port Pin Function vs. Serial I/O Mode

Pin Name	Single Bit, Serial 2-Wire Mode	Single Bit Serial 3-Wire Mode	2-Bit Serial Mode	4-Bit Serial Mode
SCLK	Serial Clock	Serial Clock	Serial Clock	Serial Clock
CSB	Chip Select	Chip Select	Chip Select	Chip Select
SDIO_0	Serial Data I/O	Serial Data In	Serial Data I/O	Serial Data I/O
SDIO_1	Not used for SDIO[1]	Not used for SDIO[1]	Serial Data I/O	Serial Data I/O
SDIO_2	Not used for SDIO[1]	Serial Data Out (SDO)	Not used for SDIO[1]	Serial Data I/O
SDIO_3	SYNC_I/O	SYNC_I/O	SYNC_I/O	Serial Data I/O

[1]In serial mode, these pins can be used for RU/RD operation.

The two bits CSR <2:1> in the channel select register set the serial I/O mode of operation are defined as follows:

CSR <2:1> = 00. Single bit serial mode (2-wire mode).

CSR <2:1> = 01. Single bit serial mode (3-wire mode).

CSR <2:1> = 10. 2-bit serial mode

CSR <2:1> = 11. 4-bit serial mode.

Single-Bit Serial (2- and 3-Wire) Modes

The single-bit serial mode interface allows read/write access to all registers that configure the AD9959. MSB first or LSB first transfer formats are supported. In addition, the single-bit serial mode interface port can be configured as either a single pin I/O, which allows a two-wire interface or two unidirectional pins for in/out, which enable a 3-wire interface. Single bit mode allows the use of the SYNC_I/O function.

In single-bit serial mode, 2-wire interface operation, the SDIO_0 pin is the single serial data I/O pin. In single-bit serial mode 3-wire interface operation, the SDIO_0 pin is the serial data input pin and the SDIO_2 pin is the output data pin. Regardless of the number of wires used in the interface, the SDIO_3 pin is configured as an input and operates as the SYNC_I/O pin in the single-bit serial mode and 2-bit serial mode. The SDIO_1 pin is unused in this mode. See Table 26.

2-Bit Serial Mode

The SPI port operation in 2-bit serial mode is identical to the SPI port operation in single-bit serial mode, except that two bits of data are registered on each rising edge of SCLK. Therefore, it only takes four clock cycles to transfer eight bits of information. The SDIO_0 pin contains the even numbered data bits using the notation D <7:0> and the SDIO_1 pin contains the odd numbered data bits. This even and odd numbered pin/data alignment is valid in both MSB and LSB first formats. See Figure 39.

4-Bit Serial Mode

The SPI port in 4-bit serial mode is identical to the SPI port in single bit serial mode, except that four bits of data are registered on each rising edge of SCLK. Therefore, it only takes two clock cycles to transfer eight bits of information. The SDIO_0 and SDIO_2 pins contain even numbered data bits using the notation D <7:0> and the SDIO_0 pin contains the LSB of the nibble. The SDIO_1 and SDIO_3 pins contain the odd numbered data bits and the SDIO_1 pin contains the LSB of the nibble to be accessed.

Note that when programming the device for 4-bit serial mode, it is important to keep the SDIO_3 pin at Logic 0 until the device is programmed out of the single bit serial mode. Failure to do so can result in the serial I/O port controller being out of sequence.

Figure 42 through Figure 44 represent write timing diagrams for each serial I/O modes available. Both MSB and LSB first modes are shown. LSB first bits are shown in parenthesis. The clock stall low/high feature shown is not required. It is used to show that data (SDIO) must have the proper setup time relative to the rising edge of SCLK.

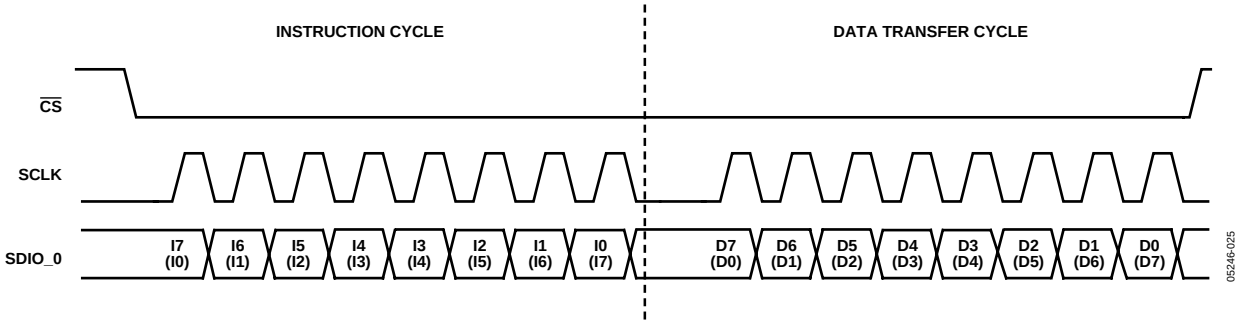


Figure 42. Single-Bit Serial Mode Write Timing—Clock Stall Low

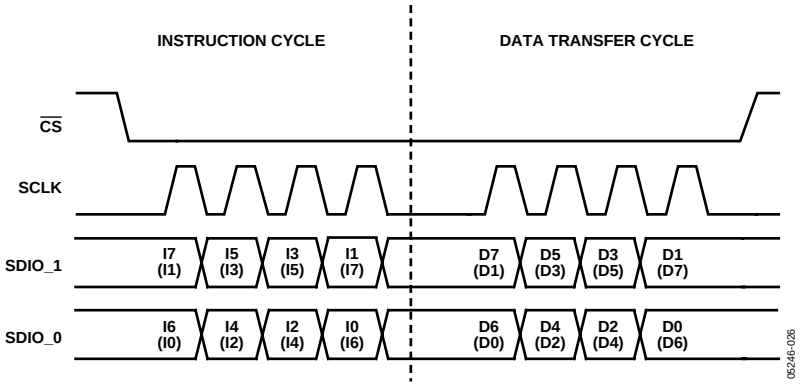


Figure 43. 2-Bit Serial Mode Write Timing—Clock Stall Low

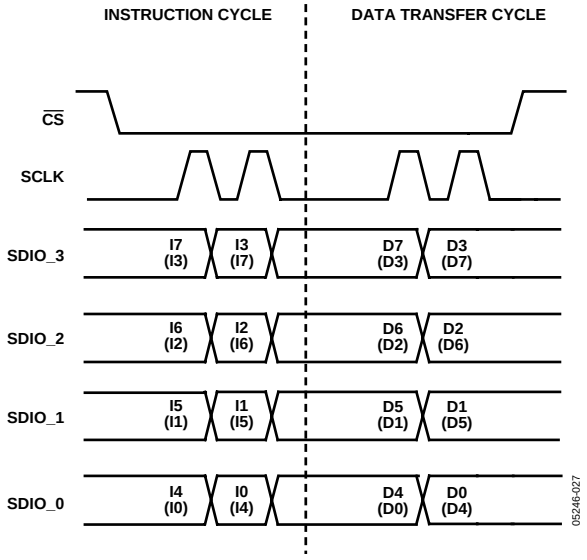


Figure 44. 4-Bit Serial Mode Write Timing—Clock Stall Low

Figure 45 through Figure 48 represent read timing diagrams for each serial I/O modes available. Both MSB and LSB first modes are shown. LSB first bits are shown in parenthesis. The clock stall low/high feature shown is not required. It is used to show that data (SDIO) must have the proper set-up time relative to the rising edge of SCLK for the instruction byte and the read data that follows the falling edge of SCLK.

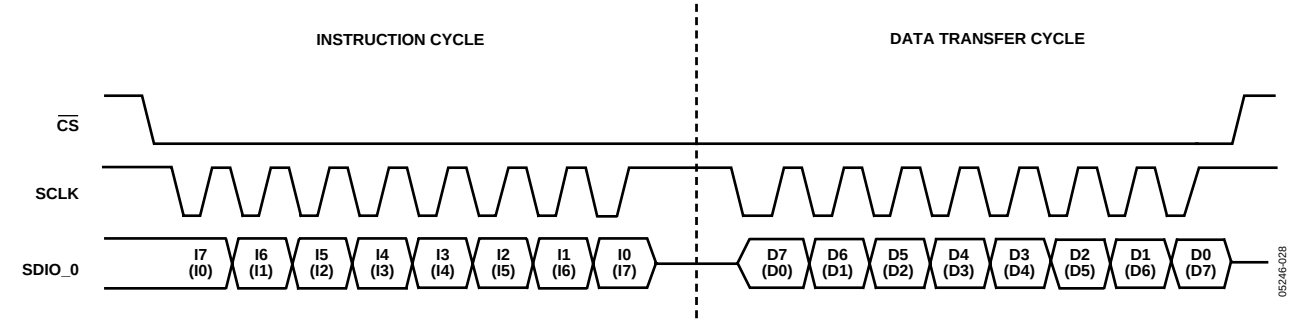


Figure 45. Single-Bit Serial Mode (2-Wire) Read Timing—Clock Stall High

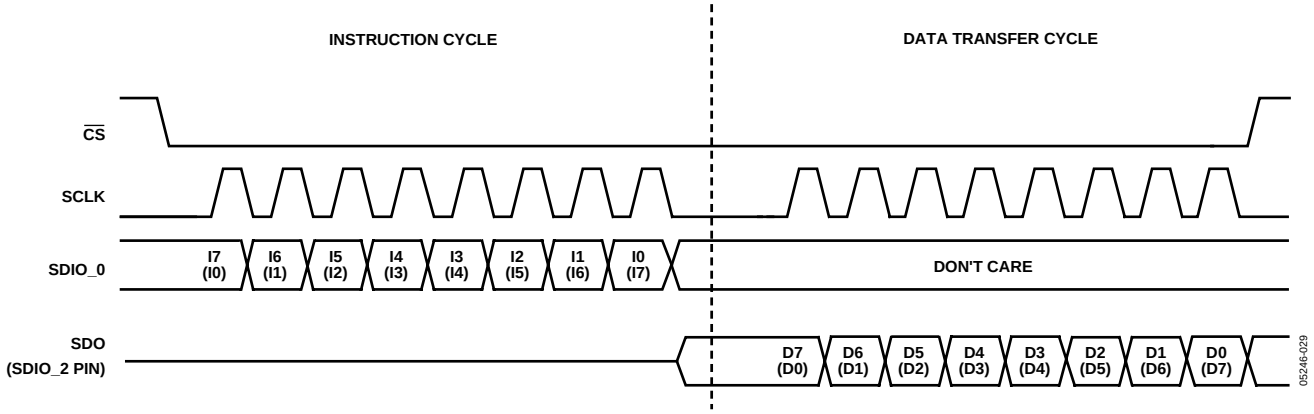


Figure 46. Single-Bit Serial Mode (3-Wire) Read Timing—Clock Stall Low

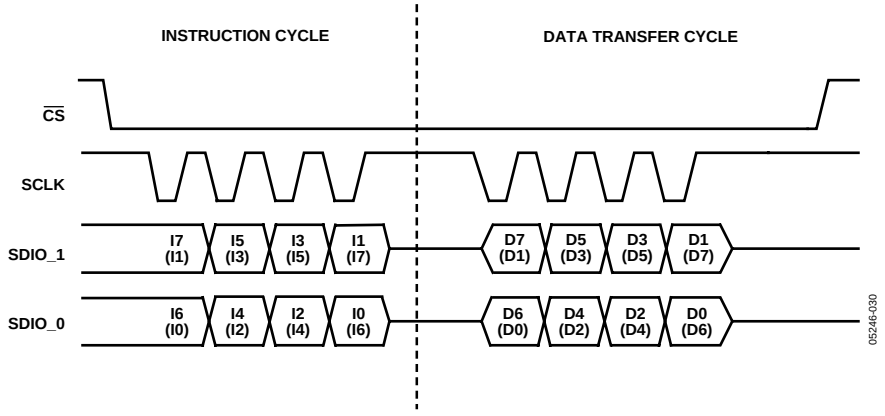


Figure 47. 2-Bit Serial Mode Read Timing—Clock Stall High

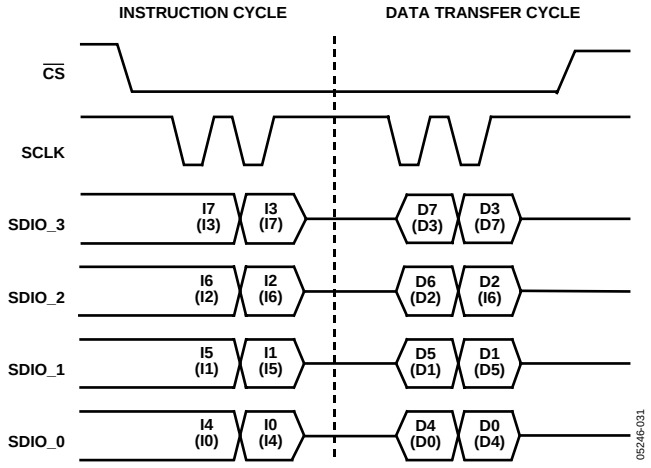


Figure 48. 4-Bit Serial Mode Read Timing—Clock Stall High

REGISTER MAPS

CONTROL REGISTER MAP

Table 27.

Register Name (Address)	Bit Range	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
Channel Select Register (CSR) (0x00)	<7:0>	Channel 3 enable[1]	Channel 2 enable[1]	Channel 1 enable[1]	Channel 0 enable[1]	Must be 0	Serial I/0 mode select <2:1>		LSB first	0xF0
Function Register 1 (FR1) (0x01)	<7:0>	Reference clock input power down	External power down mode	Sync clock disable	DAC reference power down	Open	Open	Manual hardware synchronization	Manual software synchronization	0x00
	<15:8>	Open	Profile pin configuration <14:12>			Ramp up/ramp down <11:10>		Modulation Level <9:8>		0x00
	<23:16>	VCO gain control	PLL divider ratio <22:18>					Charge pump control <17:16>		0x00
Function Register Two (FR2) (0x02)	<7:0>	Multidevice synchronization slave enable	Multidevice synchronization master enable	Multidevice synchronization status	Multidevice synchronization mask	Open <3:2>		System clock offset <1:0>		0x00
	<15:8>	All channels auto clear sweep accumulator	All channels clear sweep accumulator	All channels auto clear phase accumulator	All channels clear phase accumulator	Open <11:10>		Open <9:8>		0x00

[1] Channel enable bits do not require an I/O update to be activated. These bits are active immediately after the byte containing the bits is written. All other bits need an I/O update to become active. The four channel enable bits shown in the register map are used to enable/disable any combination of the four channels. The default for all four channels is enabled.

In the CSR register, if the user wants four different frequencies for all four DDS channels, the following protocol suffices.

1. Enable (Logic 1) the CH0 bit, which is only located in the channel select register and disable the other three channels (Logic 0).
2. Write the desired frequency tuning word for CH0, as described in Step 1, then disable the CH0 bit (Logic 0)
3. Enable the CH1 bit only, located in the channel select register, and disable the other three channels.
4. Write the desired frequency tuning word for CH1 above, then disable the CH1 bit.

CHANNEL REGISTER MAP

Table 28.

Register Name (Address)	Bit Range	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Default Value
Channel Function[1] (CFR) (0x03)	<7:0>	Digital power-down	DAC power down	Matched pipe delays active	Autoclear sweep accumulator	Clear sweep accumulator	Autoclear phase accumulator	Clear phase accumulator[2]	Sine wave output enable	0x02
	<15:8>	Linear sweep no-dwell	Linear sweep enable	Load SRR at I/O Update	Open	Open	Must be 0	DAC full-scale current control <9:8>		0x03
	<23:16>	Amplitude freq. phase select <23:22>		Open <21:16>						0x00
Channel Frequency Tuning Word 0 (CTW0) (0x04)	<7:0>	Frequency Tuning Word 0 <7:0>								0x00
	<15:8>	Frequency Tuning Word 0 <15:8>								
	<23:16>	Frequency Tuning Word 0 <23:16>								
	<31:24>	Frequency Tuning Word 0 <31:24>								
Channel Phase[1] Offset Word 0 (CPW0) (0x05)	<7:0>	Phase Offset Word 0								0x00
	<15:8>	Open <15:14>		Phase Offset Word 0 <13:8>						0x00
Amplitude Control (ACR) (0x06)	<7:0>	Amplitude scale factor								0x00
	<15:8>	Increment/decrement step size <15:14>		Open	Amplitude multiplier enable	Ramp-up/ ramp-down enable	Load ARR at I/O update	Amplitude scale factor <9:8>		0x00
	<23:16>	Amplitude ramp rate <23:16>								–
Linear Sweep Ramp Rate[1] (LSR) (0x07)	<7:0>	Linear sweep rising ramp rate (RSRR) <7:0>								–
	<15:8>	Linear sweep falling ramp rate (FSRR) <15:8>								–
LSR Rising Delta[1] (RDW) (0x08)	<7:0>	Rising delta word <7:0>								–
	<15:8>	Rising delta word <15:8>								–
	<23:16>	Rising delta word <23:16>								–
	<31:24>	Rising delta word <31:24>								–
LSR Falling Delta[1] (FDW) (0x09)	<7:0>	Falling delta word <7:0>								–
	<15:8>	Falling delta word <15:8>								–
	<23:16>	Falling delta word <23:16>								–
	<31:24>	Falling delta word <31:24>								–

[1] There are four sets of channel registers and profile registers, one per channel. This is not shown in the channel or profile register maps because the addresses of all channel registers and profile registers are the same for each channel. Therefore, the channel enable bits determine if the channel's channel registers and/or profile registers are written to or not.

[2] The clear accumulator bit is set to Logic 1 after a master reset. It self clears or is set to Logic 0 when an I/O update is asserted.

PROFILE REGISTER MAP

Table 29.

Register Name (address)	Bit Range	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Default Value
Channel Word 1 (CTW1) (0x0A)	<31:0>	Freq. tuning word <31:0> or phase word <31:18> or amplitude word <31:22>								–
Channel Word 2 (CTW2) (0x0B)	<31:0>	Freq. tuning word <31:0> or phase word <31:18> or amplitude word <31:22>								–
Channel Word 3 (CTW3) (0x0C)	<31:0>	Freq. tuning word <31:0> or phase word <31:18> or amplitude word <31:22>								–
Channel Word 3 (CTW4) (0x0D)	<31:0>	Freq. tuning word <31:0> or phase word <31:18> or amplitude word <31:22>								–
Channel Word 5 (CTW5) (0x0E)	<31:0>	Freq. tuning word <31:0> or phase word <31:18> or amplitude word <31:22>								–
Channel Word 6 (CTW6) (0x0F)	<31:0>	Freq. tuning word <31:0> or phase word <31:18> or amplitude word <31:22>								–
Channel Word 7 (CTW7) (0x10)	<31:0>	Freq. tuning word <31:0> or phase word <31:18> or amplitude word <31:22>								–
Channel Word 8 (CTW8) (0x11)	<31:0>	Freq. tuning word <31:0> or phase word <31:18> or amplitude word <31:22>								–
Channel Word 9 (CTW9) (0x12)	<31:0>	Freq. tuning word <31:0> or phase word <31:18> or amplitude word <31:22>								–
Channel Word 10 (CTW10) (0x13)	<31:0>	Freq. tuning word <31:0> or phase word <31:18> or amplitude word <31:22>								–
Channel Word 11 (CTW11) (0x14)	<31:0>	Freq. Tuning Word <31:0> or phase word <31:18> or amplitude word <31:22>								–
Channel Word 12 (CTW12) (0x15)	<31:0>	Freq. Tuning Word <31:0> or phase word <31:18> or amplitude word <31:22>								–
Channel Word 13 (CTW13) (0x16)	<31:0>	Freq. tuning word <31:0> or phase word <31:18> or amplitude word <31:22>								–
Channel Word 14 (CTW14) (0917)	<31:0>	Freq. tuning word <31:0> or phase word <31:18> or amplitude word <31:22>								–
Channel Word 15 (CTW15) (0x18)	<31:0>	Freq. tuning word <31:0> or phase word <31:18> or amplitude word <31:22>								–

CONTROL REGISTER DESCRIPTIONS

CHANNEL SELECT REGISTER (CSR)

The CSR register determines if channels are enabled or disabled by the status of the four channel enable bits. All four channels are enabled by their default state. The CSR register also determines which serial mode of operation is selected. In addition, the CSR register offers a choice of MSB first or LSB first format. The functionality of each bit is detailed in this section.

The CSR is comprised of one byte, located in Register 0x00.

CSR <0> LSB first.

CSR <0> = 0 (default), the serial interface accepts serial data in MSB first format. CSR <0> = 1, the serial interface accepts serial data in LSB first format.

CSR <2:1> Serial I/O mode select.

CSR <2:1> 00 = Single bit serial (2-wire mode).
01 = Single bit serial (3-wire mode).
10 = 2-bit serial mode.
11 = 4-bit serial mode.

See the Serial I/O Modes of Operation section for more details.

CSR <3> = must be set to 0.

CSR <7:4> channel enable bits.

CSR <7:4> bits are active immediately after being written. They do not require an I/O update to take effect.

There are four sets of channel registers and profile registers, one per channel. This is not shown in the channel or profile register map. The addresses of all channel registers and profile registers are the same for each channel. Therefore, the channel enable bits distinguish each channel's channel registers and profile registers values.

For example,

CSR <7:4> = 1001, only Channel 3 and Channel 0 receive commands from the channel registers and profile registers.

CSR <7:4> = 0010, only Channel 1 receives commands from the channel registers and profile registers.

Function Register 1 (FR1) Description

FR1 is comprised of three bytes located in Register 0x01. The FR1 is used to control the mode of operation of the chip. The functionality of each bit is detailed in this section.

FR1 <0> manual software synchronization bit.

FR1 <0> = 0 (default), the software manual synchronization feature of multiple devices is inactive. FR1 <0> = 1. The manual software synchronization feature of multiple devices is active. See the Synchronizing Multiple AD9959 Devices section for details.

FR1 <1> manual hardware synchronization bit.

FR1<1> = 0 (default), the manual hardware synchronization feature of multiple devices is inactive. FR1 <1> = 1, the manual hardware synchronization feature of multiple devices is active.

FR1 <2:3>. See the Synchronizing Multiple AD9959 Devices section for details.

FR1 <4> DAC reference power-down.

FR1 <4> = 0 (default). DAC reference is enabled. FR1 <4> = 1. DAC reference is powered down.

FR1 <5> SYNC_CLK disable.

FR1 <5> = 0 (default), the SYNC_CLK pin is active.
FR1 <5> = 1. The SYNC_CLK pin assumes a static Logic 0 state (disabled). In this state, the pin drive logic is shut down. However, the synchronization circuitry remains active internally to maintain normal device operation.

FR1 <6> external power-down mode.

FR1 <6> = 0 (default). The external power-down mode is in the fast recovery power-down mode. In this mode, when the PWR_DWN_CTL input pin is high, the digital logic and the DAC digital logic are powered down. The DAC bias circuitry, PLL, oscillator, and clock input circuitry are not powered down.

FR1 <6> = 1. The external power down mode is in the full power-down mode. In this mode, when the PWR_DWN_CTL input pin is high, all functions are powered down. This includes the DAC and PLL, which take a significant amount of time to power up.

FR1 <7> clock input power-down.

FR1 <7> = 0 (default). The clock input circuitry is enabled for operation. FR1 <7> = 1. The clock input circuitry is disabled and is in a low power dissipation state.

FR1 <9:8> modulation level bits.

The modulation (FSK, PSK, and ASK) level bits control the level (2/4/8/16) of modulation to be performed for a channel. See the Modulation Mode section for more details.

FR1<10:11> RU/RD bit (ramp-up/ramp-down).

The RU/RD bits control the amplitude ramp up/ramp down time of a channel. See the Output Amplitude Control Mode section for more details.

FR1 <12:14> profile pin configuration bits.

The profile pin configuration bits control the configuration of the data and SDIO pins for the different modulation modes. See the Modulation Mode section in this document for details.

FR1 <15> open.

FR1 <17:16> charge pump current control.

FR1 <17:16> = 00 (default), the charge pump current is 75 μA.
= 01 charge pump current is 100 μA.
= 10 charge pump current is 125 μA.
= 11 charge pump current is 150 μA.

FR1 <22:18> PLL divider values.

FR1 <22:18>, if the value is 4 or 20 (decimal) or between 4 and 20, the PLL is enabled and the value sets the multiplication factor. If the value is outside of 4 and 20 (decimal), the PLL is disabled.

FR1 <23> PLL VCO gain.

FR1 <23> = 0 (default), the low range (system clock below 160 MHz). FR1 <23> = 1, the high range (system clock above 255 MHz).

Function Register 2 (FR2) Description

The FR2 is comprised of two bytes located in Register 0x02.

The FR2 is used to control the various functions, features, and modes of the AD9959. The functionality of each bit is detailed as follows:

FR2 <1:0> system clock offset.

See the Synchronizing Multiple AD9959 Devices section for more details.

FR2 <3:2> open.

FR2 <4> multidevice synchronization mask bit.

FR2 <5> multidevice synchronization status bit.

FR2 <6> multidevice synchronization master enable bit.

FR2<7> multidevice synchronization slave enable bit.

FR2 <4:7>. see the Synchronizing Multiple AD9959 Devices section for more details.

FR2 <11:8> open.

FR2 <12> all channels clear phase accumulator.

FR2 <12> = 0 (default), the phase accumulator functions as normal. FR2 <12> = 1, the phase accumulator memory elements for all four channels are asynchronously cleared

FR2 <13> all channels autoclear phase accumulator

FR2 <13> = 0 (default). A new frequency tuning word is applied to the inputs of the phase accumulator, but not loaded into the accumulator.

FR2 <13> = 1. This bit automatically synchronously clears (loads zeros into) the phase accumulator for one cycle upon reception of the I/O update sequence indicator on all four channels.

FR2 <14> all channels clear sweep accumulator.

FR2 <14> = 0 (default), the sweep accumulator functions as normal. FR2 <14> = 1, the sweep accumulator memory elements for all four channels are asynchronously cleared.

FR2 <15> all channels autoclear sweep accumulator.

FR2 <15> = 0 (default). A new delta word is applied to the input, as in normal operation, but not loaded into the accumulator. FR2 <15> = 1. This bit automatically synchronously clears (loads zeros into) the sweep accumulator for one cycle upon reception of the I/O_UPDATE sequence indicator on all four channels.

Channel Function Register (CFR) Description

CFR <0> enable sine output.

CFR <0> = 0 (default): The angle-to-amplitude conversion logic employs a cosine function. CFR <0> = 1: The angle-to-amplitude conversion logic employs a sine function.

CFR <1> clear phase accumulator.

CFR <1> = 0 (default): The phase accumulator functions as normal. CFR <1> = 1: The phase accumulator memory elements are asynchronously cleared.

CFR <2> clear phase accumulator.

CFR <2> = 0 (default): A new frequency tuning word is applied to the inputs of the phase accumulator, but not loaded into the accumulator. CFR <2> = 1: This bit automatically synchronously clears (loads 0s) the phase accumulator for one cycle upon reception of the I/O_UPDATE sequence indicator.

CFR <3> clear frequency accumulator.

CFR <3> = 0 (default): The sweep accumulator functions as normal. CFR <3> = 1: The sweep accumulator memory elements are asynchronously cleared.

CFR <4> autoclear sweep accumulator.

CFR <4> = 0 (default): A new delta word is applied to the input, as in normal operation, but not loaded into the accumulator. CFR <4> = 1: This bit automatically synchronously clears (loads 0s) the sweep accumulator for one cycle upon reception of the I/O_UPDATE sequence indicator.

CFR <5> match pipe delays active.

CFR <5> = 0 (default): match pipe delay mode is inactive. CFR <5> = 1: match pipe delay mode is active. See the Single-Tone Mode—Matched Pipeline Delay section for details.

CFR <6> DAC power-down.

CFR <6> = 0 (default): The DAC is enabled for operation. CFR <6> = 1: The DAC is disabled and is in its lowest power dissipation state.

CFR <7> digital power-down.

CFR <7> = 0 (default). The digital core is enabled for operation.

CFR <7> = 1. The digital core is disabled and is in its lowest power dissipation state.

CFR <8:9> DAC LSB control.

CFR <8:9> = 00 (default). The DAC is at the largest LSB value.

CFR <10> must be set to 0.

CFR <13> linear sweep ramp rate load at I/O_UPDATE.

CFR <13> = 0 (default): The linear sweep ramp rate timer is loaded only upon timeout (timer =1) and is not loaded because of an I/O_UPDATE input signal.

CFR <13> = 1. The linear sweep ramp rate timer is loaded upon timeout (timer =1) or at the time of an I/O_UPDATE input signal.

CFR <14> linear sweep enable.

CFR <14> = 0 (default): The linear sweep capability of the AD9959 is inactive. CFR <14> = 1: The linear sweep capability of the AD9959 is enabled. When enabled, the delta frequency tuning word is applied to the frequency accumulator at the programmed ramp rate.

CFR <15> linear sweep no-dwell.

CFR <15> = 0 (default): The linear sweep no-dwell function is inactive. CFR <15> = 1: The linear sweep no-dwell function is active. If CFR <15> is active, the linear sweep no-dwell function is activated. See the Linear Sweep (Shaped) Modulation Mode section for details. If CFR <14> is clear, this bit is don't care.

CFR <18:16> open.

CFR <23:22> amplitude frequency phase select controls what type of modulation is to be performed for that channel. See the Modulation Mode section for details.

Channel Frequency Tuning Word (CFTWO) Description

CFTW0 <32:0> Frequency Tuning Word 0 for each channel.

Channel Phase Offset Word (CPOW) Description

CPO0 <13:0> Phase Offset Word 0 for each channel.

CPO0 <15:14> open.

Amplitude Control Register (ACR) Description

ACR <9:0> amplitude scale factor for each channel.

ACR <10> amplitude ramp rate load control bit.

ACR <10> = 0 (default). The amplitude ramp rate timer is loaded only upon timeout (timer = 1) and is not loaded due to a I/O_UPDATE input signal (or change in the profile bits).

ACR <10> = 1. The amplitude ramp rate timer is loaded upon timeout (timer =1) or at the time of an I/O_UPDATE input signal (or change in PS bits).

ACR <11> auto RU/RD enable (only valid when ACR <12> is active high).

ACR <11> = 0 (default). When ACR <12> is active, Logic 0 on ACR <11> enables the manual RU/RD operation. See the Output Amplitude Control Mode section of this document for details. ACR <11> = 1. If ACR <12> is active, a Logic 1 on ACR <11> enables the AUTO RU/RD operation. See the Output Amplitude Control Mode section of this document for details.

ACR <12> amplitude multiplier enable.

ACR <12> = 0 (default). Amplitude multiplier is disabled. The clocks to this scaling function (auto RU/RD) are stopped for power saving and the data from the DDS core is routed around the multipliers.

ACR <12> = 1, amplitude multiplier is enabled.

ACR <13> open.

ACR <15:14> amplitude increment/decrement step size.

ACR <23:16> amplitude ramp rate value.

Channel Linear Sweep Register (LSR) Description

LSR <15:0> linear sweep rising ramp rate.

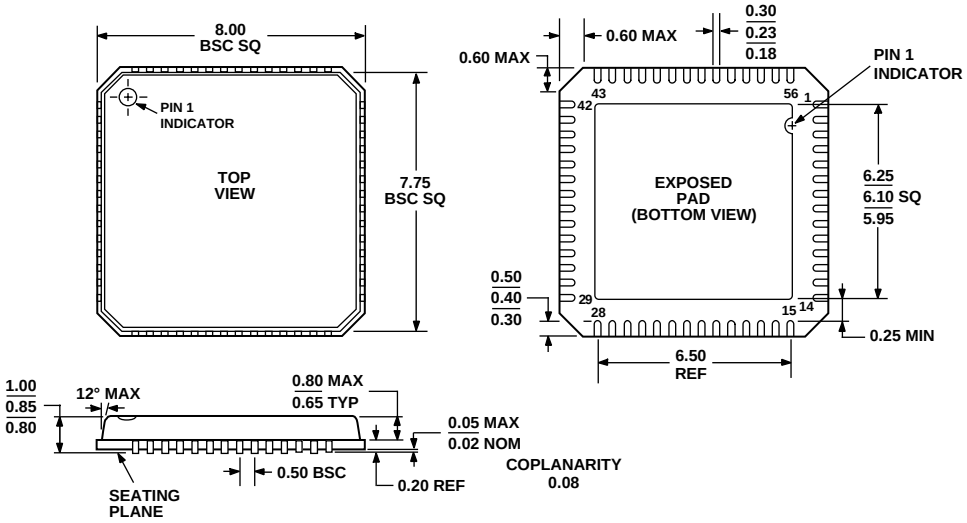
Channel Linear Sweep Rising Delta Word Register (RDW) Description

RDW <31:0> 32-bit rising delta tuning word.

Channel Linear Sweep Falling Delta Word Register (FDW) Description

FDW <31:0> 32-bit falling delta tuning word.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VLLD-2

Figure 49. 56-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
8 × 8 mm Body, Very Thin Quad
(CP-56)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Outline
AD9959BCPZ[1]	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-56
AD9959BCPZ-REEL7[1]	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-56
AD9959/PCB		Evaluation Board	

[1] Z = Pb-free part.

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