查询AD8334供应商 捷多邦，专业PCB打样工厂，24小时加急出货

Quad VGA with Ultralow Noise Preamplifier and Programmable R_{IN}

PRELIMINARY TECHNICAL DATA

AD8334

FEATURES

Ultralow Input Noise at Maximum Gain
Voltage Noise = 0.74nV/√Hz typ.
Current Noise = 2.5 pA√Hz typ.
Active Termination Match, Selected with an External resistor.
Ultra Low Noise LNA Pre-amp.
Single Ended Output Gain = 13 dB.
Differential Output Gain = 19 dB.
Bandwidth:
120 MHz (-3 dB)
Wide Gain Range w/Programmable Post-amp
-4.5 dB to +43.5dB
+7.5 dB to +55.5 dB.
Fully Differential Signal Path after LNA.
Selectable Output Clamping Level.
Trimmed for Gain, Offset and Clamping Levels.
Optimized for 10/12 bit ADCs.
Single +5V Supply

APPLICATIONS

Ultrasound and Sonar
High Performance AGC Systems
Low IF Signal Processing
High Speed ADC Driver

FUNCTIONAL BLOCK DIAGRAM

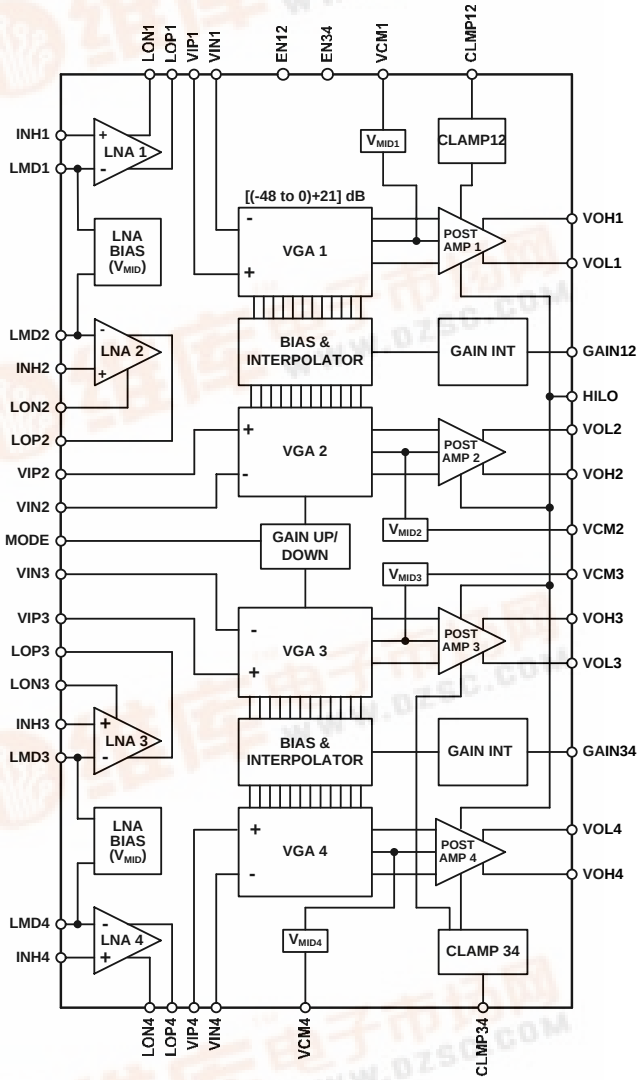

Figure 1 Functional Block Diagram

GENERAL DESCRIPTION

The AD8334 is a quad version of the AD8331 Variable Gain Amplifier. Except for mechanical details, all electrical specifications are the same. Mechanical details unique to the AD8334 are listed below. For a complete description of the AD8331 please follow this link:
http://www.analog.com/UploadedFiles/Data_Sheets/32688401738561AD8331_2_c.pdf

REV. Pra 7/14/2005
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AD8334—SPECIFICATIONS

Table 1. T_A = 25°C, V_S = 5 V, R_L = 500 Ω, R_S = R_{IN} = 50 Ω, R_{FB} = 280 Ω, C_{SH} = 22 pF, f = 10 MHz, R_{CLMP} = ∞, C_L = 1 pF, V_{CM} pin floating, −4.5 dB to +43.5 dB gain (HILO = LO), and differential output voltage, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Unit
LNA CHARACTERISTICS					
Gain	Single-Ended Input to Differential Output		19		dB
	Input to Output (Single-Ended)		13		dB
Input Voltage Range	AC-Coupled		±275		mV
Input Resistance	R_{FB} = 280 Ω		50		Ω
	R_{FB} = 412 Ω		75		Ω
	R_{FB} = 562 Ω		100		Ω
	R_{FB} = 1.13 kΩ		200		Ω
	R_{FB} = ∞		6		kΩ
Input Capacitance			13		pF
Output Impedance	Single-Ended, Either Output		5		Ω
−3 dB Small Signal Bandwidth	V_{OUT} = 0.2 V p-p		130		MHz
Slew Rate			650		V/µs
Input Voltage Noise	R_S = 0 Ω, HI or LO Gain, R_{FB} = ∞, f = 5 MHz		0.74		nV/√Hz
Input Current Noise	R_{FB} = ∞, HI or LO Gain, f = 5 MHz		2.5		pA/√Hz
Noise Figure	f = 10 MHz, LOP Output				
Active Termination Match	R_S = R_{IN} = 50 Ω		3.7		dB
Unterminated	R_S = 50 Ω, R_{FB} = ∞		2.5		dB
Harmonic Distortion @ LOP1 or LOP2					
HD2	V_{OUT} = 0.5 V p-p, Single-Ended, f = 10 MHz		−56		dBc
HD3			−70		dBc
Output Short-Circuit Current	Pins LON, LOP		165		mA
LNA + VGA CHARACTERISTICS					
−3 dB Small Signal Bandwidth	V_{OUT} = 0.2 V p-p		120		MHz
−3 dB Large Signal Bandwidth	V_{OUT} = 2 V p-p		110		MHz
Slew Rate	LO Gain		300		V/µs
	HI Gain		1200		V/µs
Input Voltage Noise	R_S = 0 Ω, HI or LO Gain, R_{FB} = ∞, f = 5 MHz		0.82		nV/√Hz
Noise Figure	V_{GAIN} = 1.0 V				
Active Termination Match	R_S = R_{IN} = 50 Ω, f = 10 MHz, Measured		4.15		dB
	R_S = R_{IN} = 200 Ω, f = 5 MHz, Simulated		2.0		dB
Unterminated	R_S = 50 Ω, R_{FB} = ∞, f = 10 MHz, Measured		2.5		dB
	R_S = 200 Ω, R_{FB} = ∞, f = 5 MHz, Simulated		1.0		dB
Output-Referred Noise	V_{GAIN} = 0.5 V, LO Gain		48		nV/√Hz
	V_{GAIN} = 0.5 V, HI Gain		178		nV/√Hz
Output Impedance, Postamplifier	DC to 1 MHz		1		Ω
Output Signal Range, Postamplifier	R_L ≥ 500 Ω, Unclamped, Either Pin		V_{CM} ± 1.125		V
Differential			4.5		V p-p
Output Offset Voltage					
Differential	V_{GAIN} = 0.5 V	−50	±5	+50	mV
Common-Mode		−125	−25	+100	mV
Output Short-Circuit Current			45		mA

Parameter	Conditions	Min	Typ	Max	Unit
Harmonic Distortion	V_{GAIN} = 0.5 V, V_{OUT} = 1 V p-p				
HD2	f = 1 MHz		−88		dBc
HD3			−85		dBc
HD2	f = 10 MHz		−68		dBc
HD3			−65		dBc
Input 1 dB Compression Point	V_{GAIN} = 0.25 V, V_{OUT} = 1 V p-p, f = 1 MHz–10 MHz		7		dBm[1]
Two-Tone Intermodulation Distortion (IMD3)	V_{GAIN} = 0.72 V, V_{OUT} = 1 V p-p, f = 1 MHz		−80		dBc
	V_{GAIN} = 0.5 V, V_{OUT} = 1 V p-p, f = 10 MHz		−72		dBc
Output Third Order Intercept	V_{GAIN} = 0.5 V, V_{OUT} = 1 V p-p, f = 1 MHz		38		dBm
	V_{GAIN} = 0.5 V, V_{OUT} = 1 V p-p, f = 10 MHz		33		dBm
Channel-to-Channel Crosstalk (AD8332)	V_{GAIN} = 0.5 V, V_{OUT} = 1 V p-p, f = 1 MHz		−84		dB
Overload Recovery	V_{GAIN} = 1.0 V, V_{IN} = 50 mV p-p/1 V p-p, f = 10 MHz		5		ns
Group Delay Variation	5 MHz < f < 50 MHz, Full Gain Range		±2		ns
ACCURACY					
Absolute Gain Error[2]	0.05 V < V_{GAIN} < 0.10 V	−1	+0.5	+2	dB
	0.10 V < V_{GAIN} < 0.95 V	−1	±0.3	+1	dB
	0.95 V < V_{GAIN} < 1.0 V	−2	−1	+1	dB
Gain Law Conformance[3]	0.1 V < V_{GAIN} < 0.95 V		±0.2		dB
Channel-to-Channel Gain Matching	0.1 V < V_{GAIN} < 0.95 V		±0.1		dB
GAIN CONTROL INTERFACE (Pin GAIN)					
Gain Scaling Factor	0.10 V < V_{GAIN} < 0.95 V		50		dB/V
Gain Range	LO Gain		−4.5 to +43.5		dB
	HI Gain		+7.5 to +55.5		dB
Input Voltage (V_{GAIN}) Range			0 to 1.0		V
Input Impedance			10		MΩ
Response Time	48 dB Gain Change to 90% Full Scale		750		ns
COMMON-MODE INTERFACE (Pin VCMn)					
Input Resistance	Current Limited to ±1 mA		30		Ω
Output CM Offset Voltage	V_{CM} = 2.5 V	−125	−25	+100	mV
Voltage Range	V_{OUT} = 2.0 V p-p		1.5 to 3.5		V
ENABLE INTERFACE (Pins ENB, ENBL, ENBV)					
Logic Level to Enable Power		2.25		5	V
Logic Level to Disable Power		0		1.0	V
Input Resistance	Pin ENB		25		kΩ
	Pin ENBL		40		kΩ
	Pin ENBV		70		kΩ
Power-Up Response Time	V_{INH} = 30 mV p-p		300		µs
	V_{INH} = 150 mV p-p		4		ms
HILO GAIN RANGE INTERFACE (Pin HILO)					
Logic Level to Select HI Gain Range		2.25		5	V
Logic Level to Select LO Gain Range		0		1.0	V
Input Resistance			50		kΩ

[1] All dBm values are referred to 50 Ω, unless otherwise noted.
[2] Conformance to theoretical gain expression (see Equation 1).
[3] Conformance to best fit dB linear curve.

Parameter	Conditions	Min	Typ	Max	Unit
OUTPUT CLAMP INTERFACE (Pin RCLMP; HI or LO Gain)					
Accuracy					
HILO = LO	R_{CLMP} = 2.74 kΩ, V_{OUT} = 1 V p-p (Clamped)		±50		mV
HILO = HI	R_{CLMP} = 2.21 kΩ, V_{OUT} = 1 V p-p (Clamped)		±75		mV
MODE INTERFACE (Pin MODE)					
Logic Level for Positive Gain Slope		0		1.0	V
Logic Level for Negative Gain Slope		2.25		5	V
Input Resistance			200		kΩ
POWER SUPPLY (Pins VPS1, VPS2, VPSV, VPSL, VPOS)					
Supply Voltage		4.5	5.0	5.5	V
Quiescent Current per Channel			25		mA
Power Dissipation per channel	No Signal		125		mW
Disable Current					
AD8332 (VGA and LNA)			300	600	µA
AD8331 (VGA and LNA)			240	400	µA
AD8332 (ENBL)	Each Channel		12		mA
AD8332 (ENBV)	Each Channel		13		mA
AD8331 (ENBL)			11		mA
AD8331 (ENBV)			14		mA
PSRR	V_{GAIN} = 0, f = 100 kHz		−68		dB

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTION

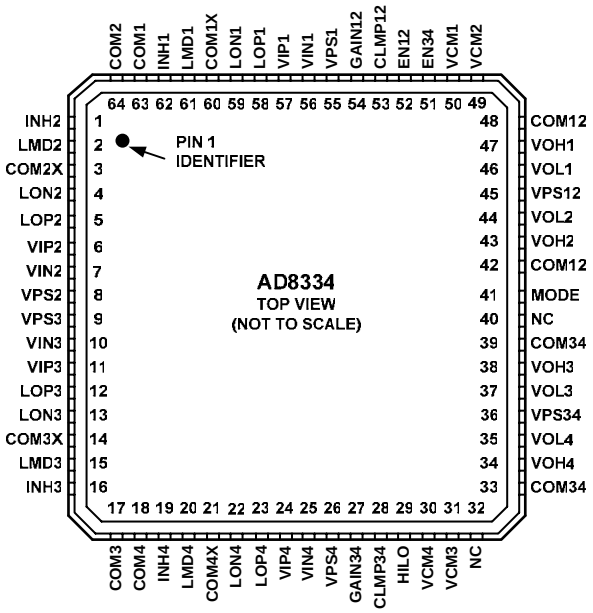

Table 1 LFCSP–64 - LFCSP (CP – 64 PACKAGE)

Pin	Name	Description
1	INH2	CH2 LNA Input
2	LMD2	CH2 LNA V_{mid} bypass (AC coupled to GND)
3	COM2X	CH2 LNA Ground Shield
4	LON2	CH2 LNA Feedback Output (for R_{FBK})
5	LOP2	CH2 LNA Output
6	VIP2	CH2 VGA Positive Input
7	VIN2	CH2VGA Negative Input
8	VPS2	CH2 LNA Supply 5V
9	VPS3	CH3 LNA Supply 5V
10	VIN3	CH3VGA Negative Input
11	VIP3	CH3 VGA Positive Input
12	LOP3	CH3 LNA Positive Output
13	LON3	CH3 LNA Feedback Output (for R_{FBK})
14	COM3X	CH3 LNA Ground Shield
15	LMD3	CH3 LNA V_{mid} bypass (AC coupled to GND)
16	INH3	CH3 LNA Input
17	COM3	CH3 LNA Ground
18	COM4	CH4 LNA Ground
19	INH4	CH4 LNA Input
20	LMD4	CH4 LNA V_{mid} bypass (AC coupled to GND)
21	COM4X	CH4 LNA Ground Shield
22	LON4	CH4 LNA Feedback Output (for R_{FBK})
23	LOP4	CH4 LNA Positive Output
24	VIP4	CH4 VGA Positive Input
25	VIN4	CH4VGA Negative Input
26	VPS4	CH4 LNA Supply 5V
27	GAIN34	Gain Control Voltage for CH3 and CH4
28	CLMP34	Output Clamping Level Input for CH3 and CH4
29	HILO	Gain Select for Post-Amp 0 dB or 12 dB
30	VCM4	CH4 Common Mode Voltage – AC Bypass
31	VCM3	CH3 Common Mode Voltage – AC Bypass
32	NC	
33	COM34	VGA Ground, CH3 and CH4
34	VOH4	CH4 Positive VGA Output
35	VOL4	CH4 Negative VGA Output
36	VPS34	VGA Supply 5V CH 3 and CH4
37	VOL3	CH3 Negative VGA Output
38	VOH3	CH3 Positive VGA Output
39	COM34	VGA ground CH 3 and CH4
40	NC	No Connect
41	MODE	Gain Control SLOPE, Logic Input, 0 = Positive
42	COM12	VGA ground CH1 and CH2
43	VOH2	CH2 Positive VGA Output
44	VOL2	CH2 Negative VGA Output
45	VPS12	CH2 VGA Supply 5V CH1 and CH2
46	VOL1	CH1 Negative VGA Output
47	VOH1	CH1 Positive VGA Output
48	COM12	VGA ground CH1 and CH2
49	VCM2	CH2 Common Mode Voltage – AC Bypass
50	VCM1	CH1 Common Mode Voltage – AC Bypass
51	EN34	Shared LNA/VGA Enable, CH3 and CH4
52	EN12	Shared LNA/VGA Enable, CH1 and CH2
53	CLMP12	Output Clamping Level Input, CH1 and CH2
54	GAIN12	Gain Control Voltage CH1 and CH2
55	VPS1	CH1 LNA Supply 5V
56	VIN1	CH1 VGA Negative Input
57	VIP1	CH1 VGA Positive Input
58	LOP1	CH1 LNA Positive Output
59	LON1	CH1 LNA Feedback Output (for R_{FBK})
60	COM1X	CH1 LNA Ground Shield
61	LMD1	CH1 LNA V_{mid} bypass (AC coupled to GND)
62	INH1	CH1 LNA Input
63	COM1	CH1 LNA Ground
64	COM2	CH2 LNA Ground

OUTLINE DIMENSIONS

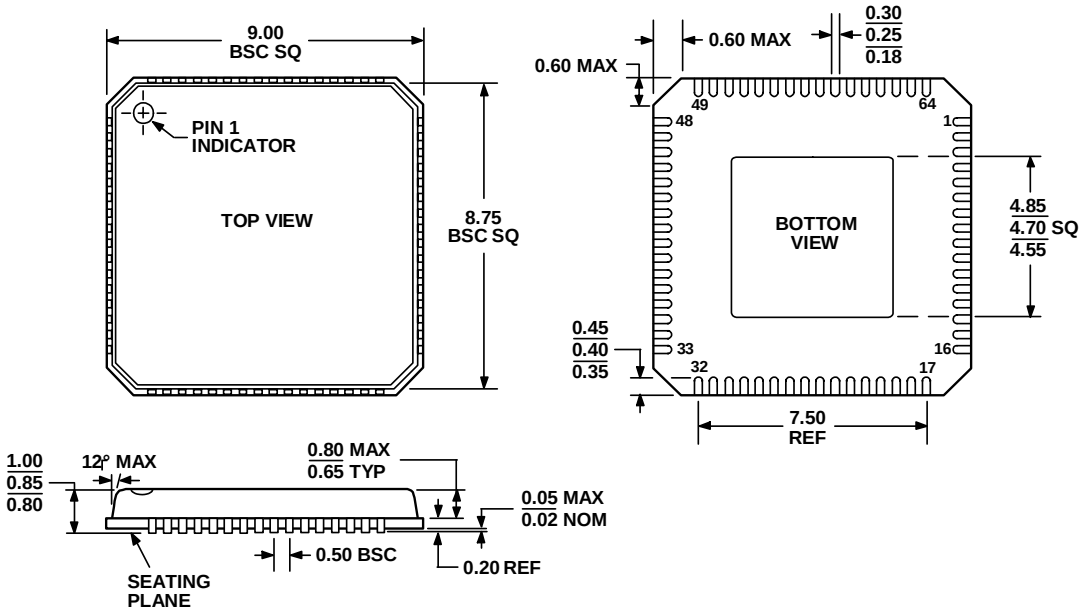

Figure TBD. 64-Lead Frame Chip Scale Package [LFCSP] (CP-64-1)—Dimensions shown in millimeters

ORDERING GUIDE

AD8334 Products	Temperature Range	Package Description	Package Outline
AD8334ACPZ	–40°C to +85°C	64-Lead Frame Chip Scale Package (LFCSP)	CP-64
AD8334ACPZ-REEL	–40°C to +85°C	64-Lead Frame Chip Scale Package (LFCSP)	CP-64
AD8334ACPZ-REEL7	–40°C to +85°C	64-Lead Frame Chip Scale Package (LFCSP)	CP-64
AD8334-EVAL		Evaluation Board with AD8334ACP	

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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