# ANALOG DEVICES

# LC²MOS
# 14-Bit µP Compatible DAC

# AD7536

## FEATURES
**Full 4-Quadrant Multiplication without External Resistors**
**All Grades 14-Bit Monotonic over the Full Temperature Range**
**Low Output Leakage (<20nA) over the Full Temperature Range**
**Low Gain Temperature Coefficient, 2ppm/°C**

## APPLICATIONS
**Control and Measurement in High Temperature Environments**
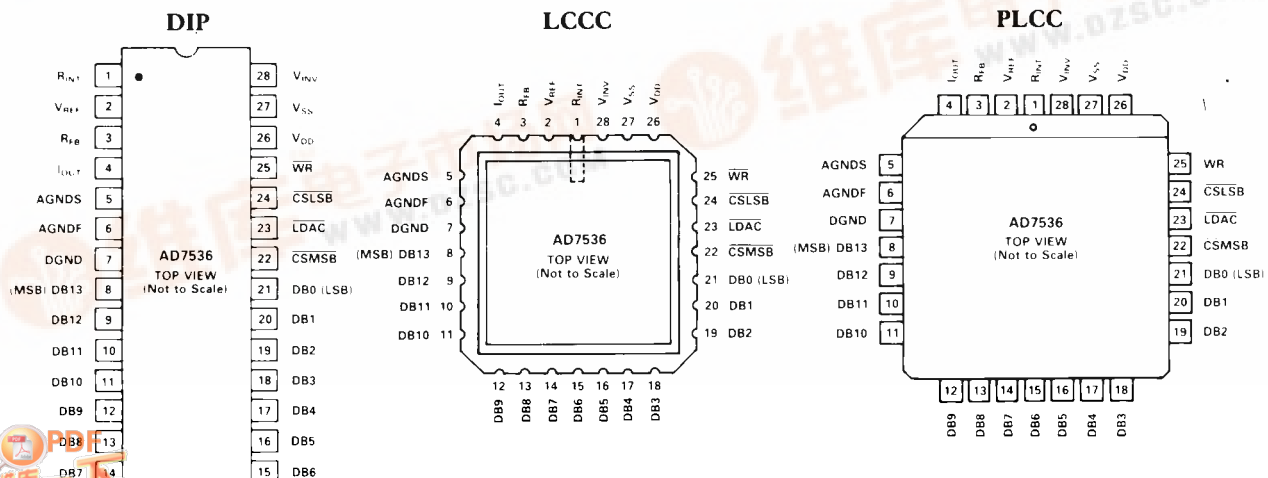**Digital Audio**
**Precision Servo Control**
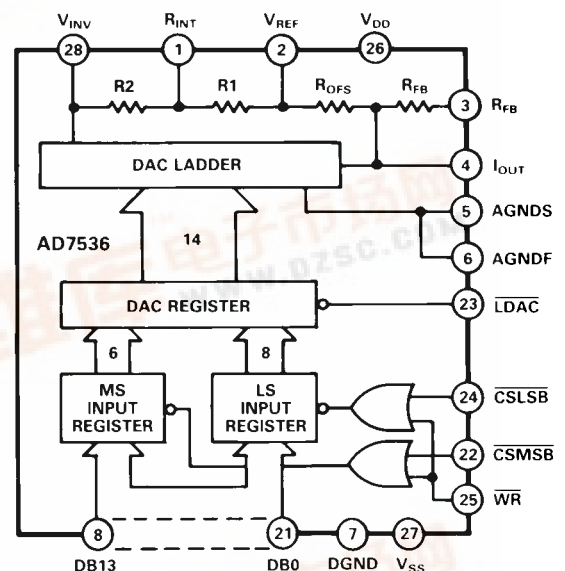**All Microprocessor Based Control Systems**

## GENERAL DESCRIPTION
The AD7536 is a 14-bit monolithic CMOS D/A converter. The part is laser trimmed and specified as a dedicated bipolar DAC. The resistors needed for 4-quadrant multiplication are contained on the chip. Thus, the user requires only the AD7536, a voltage reference and two op-amps for bipolar operation. The AD7536 has the same low leakage configuration (patent pending) as the other members of the 14-bit CMOS DAC family. The excellent output leakage current characteristics also ensure exceptional stability of linearity and gain error over the full temperature range.

The device is speed compatible with most microprocessors and accepts TTL or 5V CMOS logic level inputs. There is standard Chip Select and Memory Write logic for easy interfacing. The AD7536 has full protection against CMOS "latch-up" phenomena and does not require the use of external Schottky diodes or the use of a FET Input op-amp.

## FUNCTIONAL BLOCK DIAGRAM



## PRODUCT HIGHLIGHTS
1. Bipolar Operation
   The AD7536 gives the user 4-Quadrant Multiplication without any external resistors.

2. Guaranteed Monotonicity
   14-bit monotonicity is guaranteed over the full temperature range for all grades.

3. Low Output Leakage
   The device has excellent output leakage current characteristics at all temperatures.

## PIN CONFIGURATIONS



DIP

LCCC

PLCC

# AD7536—SPECIFICATIONS[1]

$(V_{DD} = +11.4V$ to $+15.75V^2$, $V_{REF} = +10V$, $+V_{PIN4} = V_{PIN5} = 0V$, $V_{SS} = -300$ mV. All specifications $T_{min}$ to $T_{max}$ unless otherwise stated. See Figure 6 for Suggested Specification Circuit[3])

| Parameter | AD7536JN AD7536AQ | AD7536KN AD7536BQ | AD7536SQ | AD7536TQ | Units | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| ACCURACY | | | | | | |
| Resolution | 14 | 14 | 14 | 14 | Bits | $1 LSB = 2V_{REF}/2^{14}$ |
| Relative Accuracy | ± 2 | ± 1 | ± 2 | ± 1 | LSB max | All grades guaranteed monotonic |
| Differential Nonlinearity | ± 1 | ± 1 | ± 1 | ± 1 | LSB max | over temperature. |
| Gain Error | ± 16 | ± 8 | ± 16 | ± 8 | LSB max | Measured using internal $R_{FB}$ and includes effects of leakage current and gain T.C. |
| Offset Error | ± 4 | ± 4 | ± 4 | ± 4 | LSB max | Error due to mismatch between $R_{FB}$ and offset resistor. It also includes leakage current to $I_{OUT}$ and is measured when DAC is loaded with all 0's. |
| Gain Temperature Coefficient[4], $\Delta Gain/\Delta Temperature$ | ± 5 | ± 5 | ± 5 | ± 5 | ppm/°C max | Typical Value is 2ppm/°C |
| Offset Temperature Coefficient[4] $\Delta Offset/\Delta Temperature$ | ± 5 | ± 2.5 | ± 5 | ± 2.5 | ppm/°C max | Typical Value is 1ppm/°C |
| INPUT RESISTANCES | | | | | | |
| $V_{REF}$ Input Resistance, Pin 2 | 3 | 3 | 3 | 3 | kΩ min | Typical Input Resistance = 6kΩ |
|  | 13 | 13 | 13 | 13 | kΩ max | |
| $V_{INV}$ Input Resistance, Pin 28 | 2 | 2 | 2 | 2 | kΩ min | Typical Input Resistance = 4kΩ |
|  | 8 | 8 | 8 | 8 | kΩ max | |
| DIGITAL INPUTS | | | | | | |
| $V_{IH}$ (Input High Voltage) | 2.4 | 2.4 | 2.4 | 2.4 | V min | |
| $V_{IL}$ (Input Low Voltage) | 0.8 | 0.8 | 0.8 | 0.8 | V max | |
| $I_{IN}$ (Input Current) | | | | | | |
| + 25°C | ± 1 | ± 1 | ± 1 | ± 1 | μA max | $V_{IN}$ 0V or $V_{DD}$ |
| $T_{min}$ to $T_{max}$ | ± 10 | ± 10 | ± 10 | ± 10 | μA max | |
| $C_{IN}$ (Input Capacitance)[4] | 7 | 7 | 7 | 7 | pF max | |
| POWER SUPPLY | | | | | | |
| $V_{DD}$ Range | 11.4/15.75 | 11.4/15.75 | 11.4/15.75 | 11.4/15.75 | $V_{min}/V_{max}$ | Specification guaranteed over |
| $V_{SS}$ Range | 200/ 500 | 200/ – 500 | 200/ 500 | 200/ – 500 | mV min/mV max | this range. |
| $I_{DD}$ | 4 | 4 | 4 | 4 | mA max | All digital inputs $V_{IL}$ or $V_{IH}$ |
|  | 500 | 500 | 500 | 500 | μA max | All digital inputs 0V or $V_{DD}$ |
| Power Supply Rejection $\Delta Gain/\Delta V_{DD}$ | ± 0.02 | ± 0.02 | ± 0.02 | ± 0.02 | % per % max | $\Delta V_{DD} - V_{DD}$ max $- V_{DD}$ min |

# AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test.
$(V_{DD} = +11.4V$ to $+15.75V$, $V_{REF} = +10V$, $V_{PIN4} = V_{PIN5} = 0V$, $V_{SS} = 0V$ OR $-300$mV, See Figure 6 for Suggested Specification Circuit[3]).

| Parameter | $T_A = 25°C$ | $T_A = T_{min}, T_{max}$ | Units | Test Conditions/Comments |
|---|---|---|---|---|
| Current Settling Time | 1.5 | – | μs max | To 0.003% of full scale range. $I_{OUT}$ load – 100Ω, $C_{EXT} = 13pF$. DAC register alternately loaded with all 1's and all 0's. Typical value of Settling Time is 0.8μs. |
| Digital-to-Analog Glitch Impulse | 50 | – | nV-sec typ | Measured with $V_{REF} = 0V$. $I_{OUT}$ load = 100Ω, $C_{EXT} = 13pF$. DAC register alternately loaded with all 1's and all 0's. |
| Multiplying Feedthrough Error[5] | 4 | – | mV p-p typ | $V_{REF} = ± 10V$, 1kHz sine wave DAC register loaded with 10 0000 0000 0000 |
| Output Capacitance | | | | |
| $C_{OUT}$ (Pin 4) | 260 | 260 | pF max | DAC register loaded with all 1's |
| $C_{OUT}$ (Pin 4) | 130 | 130 | pF max | DAC register loaded with all 0's |
| Output Noise Voltage Density (10Hz – 100kHz) | 50 | – | nV/√Hz typ | Measured between $R_{FB}$ and $I_{OUT}$ |

NOTES
[1]Temperature range as follows:  JN, KN Versions:  0 to + 70°C
　　　　　　　　　　　　　AQ, BQ Versions:  – 25°C to + 85°C
　　　　　　　　　　　　　SQ, TQ Versions:  – 55°C to + 125°C
[2]Specifications are guaranteed for a $V_{DD}$ of + 11.4V to + 15.75V. At $V_{DD}$ = 5V, the device is fully functional with degraded specifications.
[3]Only the D.U.T. (i.e., AD7536) is subjected to full temperature conditions.
[4]Guaranteed by Product Assurance testing.
[5]Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.
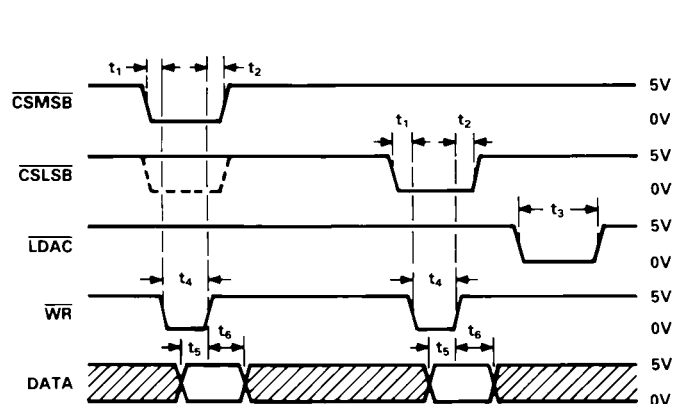
Specifications subject to change without notice.

# TIMING CHARACTERISTICS

($V_{DD}$ = + 11.4V to + 15.75V, $V_{REF}$ = + 10V, $V_{PIN4}$ = $V_{PIN5}$ = 0V, $V_{SS}$ = 0V or − 300mV
All specifications $T_{min}$ to $T_{max}$ unless otherwise stated. See Figure 1 for Timing Diagram.)

| Parameter | Limit at $T_A = 25°C$ | Limit at $T_A = 0$ to $+70°C$ $T_A = -25°C$ to $+85°C$ | Limit at $T_A = -55°C$ to $+125°C$ | Units | Test Conditions/Comments |
|---|---|---|---|---|---|
| $t_1$ | 0 | 0 | 0 | ns min | $\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Setup Time |
| $t_2$ | 0 | 0 | 0 | ns min | $\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Hold Time |
| $t_3$ | 170 | 200 | 240 | ns min | LDAC Pulse Width |
| $t_4$ | 170 | 200 | 240 | ns min | Write Pulse Width |
| $t_5$ | 140 | 160 | 180 | ns min | Data Setup Time |
| $t_6$ | 20 | 20 | 30 | ns min | Data Hold Time |

Specifications subject to change without notice.



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20ns$.

2. TIMING MEASUREMENT REFERENCE LEVEL IS $\dfrac{V_{IH} + V_{IL}}{2}$

3. IF $\overline{LDAC}$ IS ACTIVATED PRIOR TO THE RISING EDGE OF $\overline{WR}$, THEN IT MUST STAY LOW FOR $t_3$ OR LONGER AFTER $\overline{WR}$ GOES HIGH.
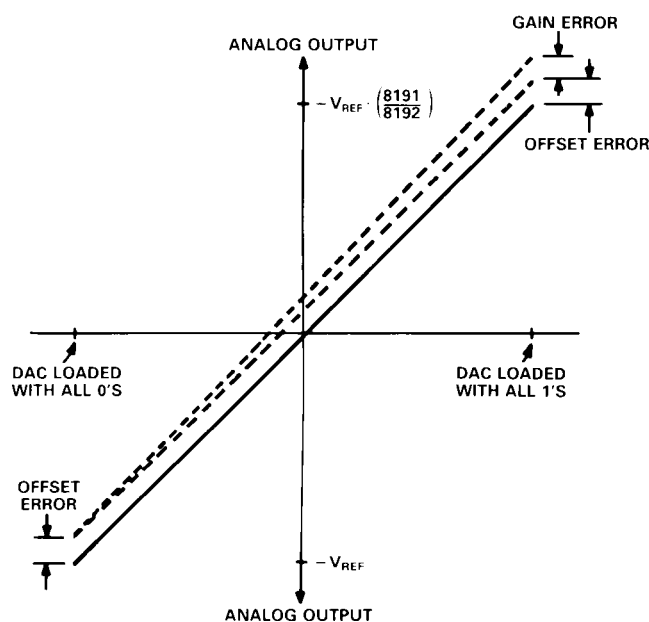
Figure 1. AD7536 Timing Diagram



Figure 2. AD7536 Transfer Function

## ORDERING INFORMATION

| Model | Temperature Range | Relative Accuracy | Full Scale Error | Package Options* |
|---|---|---|---|---|
| AD7536JN | 0°C to + 70°C | ± 2LSB | ± 16LSB | N-28 |
| AD7536KN | 0°C to + 70°C | ± 1LSB | ± 8LSB | N-28 |
| AD7536JP | 0°C to + 70°C | ± 2LSB | ± 16LSB | P-28A |
| AD7536KP | 0°C to + 70°C | ± 1LSB | ± 8LSB | P-28A |
| AD7536AQ | − 25°C to + 85°C | ± 2LSB | ± 16LSB | Q-28 |
| AD7536BQ | − 25°C to + 85°C | ± 1LSB | ± 8LSB | Q-28 |
| AD7536SQ | − 55°C to + 125°C | ± 2LSB | ± 16LSB | Q-28 |
| AD7536TQ | − 55°C to + 125°C | ± 1LSB | ± 8LSB | Q-28 |
| AD7536SE | − 55°C to + 125°C | ± 2LSB | ± 16LSB | E-28A |
| AD7536TE | − 55°C to + 125°C | ± 1LSB | ± 8LSB | E-28A |

## PRICING (100 + )$

| | |
|---|---|
| AD7536JN | $18.95 |
| AD7536KN | $28.45 |
| AD7536AD | $28.95 |
| AD7536BD | $38.45 |
| AD7536SD | $80.70 |
| AD7536TD | $113.05 |

NOTE
*E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier;
Q = Cerdip; R = SOIC.

# AD7536

## ABSOLUTE MAXIMUM RATINGS
($T_A = 25°C$ unless otherwise stated)

$V_{DD}$ (pin 26) to DGND . . . . . . . . . . . . . $-0.3V, +17V$
$V_{SS}$ (pin 27) to AGND . . . . . . . . . . . . . $-15V, +0.3V$
$V_{REF}$ (pin 2) to AGND . . . . . . . . . . . . . . . . . $\pm 25V$
$V_{INV}$ (pin 28) to AGND . . . . . . . . . . . . . . . . . $\pm 25V$
$R_{INT}$ (pin 1) to AGND . . . . . . . . . . . . . . . . . $\pm 25V$
$R_{FB}$ (pin 3) to AGND . . . . . . . . . . . . . . . . . $\pm 25V$
Digital Input Voltage (pins 8–25) to DGND . . $-0.3V, V_{DD}$
$V_{PIN4}$ to DGND . . . . . . . . . . . . . . . . . $-0.3V, V_{DD}$
AGND to DGND . . . . . . . . . . . . . . . . . $-0.3V, V_{DD}$
Power Dissipation (Any package)
To +75°C . . . . . . . . . . . . . . . . . . . . . . . 1000mW

Derates above +75°C . . . . . . . . . . . . . . . 10mW/°C
Operating Temperature Range
  Commercial Plastic (JN, KN versions) . . . 0 to +70°C
  Industrial Ceramic (AQ, BQ versions) . $-25°C$ to $+85°C$
  Extended Ceramic (SQ, TQ versions) . $-55°C$ to $+125°C$
  Storage Temperature . . . . . . . . . $-65°C$ to $+150°C$
Lead Temperature (Soldering, 10 secs) . . . . . . $+300°C$

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## CAUTION
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

**WARNING!**
ESD SENSITIVE DEVICE

## TERMINOLOGY

### LEAST SIGNIFICANT BIT (LSB)
This is the analog weighting of 1 bit of the digital word in a DAC. For the AD7536 $1LSB = \dfrac{2V_{REF}}{2^{14}}$

### RELATIVE ACCURACY
Relative accuracy or end point nonlinearity is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after adjusting for both endpoints (i.e., Offset and Gain Error are adjusted out) and is normally expressed in Least Significant Bits or as a percentage of full scale range.

### DIFFERENTIAL NONLINEARITY
Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of +1LSB max over the operating temperature range ensures monotonicity.

### GAIN ERROR
Gain error is a measure of the output error between an ideal DAC and the actual device output with all one's loaded after offset error has been adjusted out. Gain error is adjustable to zero with an external potentiometer.

### OFFSET ERROR
Offset error is a measure of the mismatch between $R_{FB}$ and the internal offset resistor, $R_{OFS}$. It also includes the leakage component from the DAC (see Figure 8). It is present for all codes and is expressed in Least Significant Bits.

### DIGITAL-TO-ANALOG GLITCH IMPULSE
The amount of charge injected from the digital inputs to the analog output when the inputs change state is called Digital-to-Analog Glitch Impulse. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage. It is measured with $V_{REF} = AGND$.

### OUTPUT CAPACITANCE
This is the capacitance from $I_{OUT}$ to AGND.

### LEAKAGE CURRENT
Leakage current flows into $I_{OUT}$ from the 14-bit DAC when all the DAC switches are off. It contributes to the Linearity, Gain and Offset error (see Figure 8).

### MULTIPLYING FEEDTHROUGH ERROR
This is the ac error due to capacitive feedthrough from $V_{REF}$ terminal to $I_{OUT}$ with DAC register loaded with 10 0000 0000 0000.

| Pin | Function | Description |
|-----|----------|-------------|
| 1 | $R_{INT}$ | Contact point for internal resistors R1 and R2 which perform the inverting function on $V_{REF}$ with external op-amp. See Figure 3. |
| 2 | $V_{REF}$ | Reference input to the DAC. It is internally connected to $R_{OFS}$ and R1. See Figure 3. |
| 3 | $R_{FB}$ | Feedback resistor. Used to close the loop around an external op-amp. |
| 4 | $I_{OUT}$ | Current Output Terminal. |
| 5 | $A_{GNDS}$ | Analog ground sense line. Reference point for external circuitry. This pin should carry minimal current. |
| 6 | $A_{GNDF}$ | Analog ground force line; carries current from internal analog ground connections. $A_{GNDF}$ and $A_{GNDS}$ are tied together internally. |
| 7 | DGND | Digital Ground |
| 8 | DB13 | Data Bit 13. DAC MSB |
| 9 | DB12 | Data Bit 12 |
| 10 | DB11 | Data Bit 11 |
| 11 | DB10 | Data Bit 10 |
| 12 | DB9 | Data Bit 9 |
| 13 | DB8 | Data Bit 8 |
| 14 | DB7 | Data Bit 7 |
| 15 | DB6 | Data Bit 6 |
| 16 | DB5 | Data Bit 5 |
| 17 | DB4 | Data Bit 4 |
| 18 | DB3 | Data Bit 3 |
| 19 | DB2 | Data Bit 2 |
| 20 | DB1 | Data Bit 1 |
| 21 | DB0 | Data Bit 0. DAC LSB |
| 22 | $\overline{CSMSB}$ | Chip Select Most Significant (MS) Byte. Active LOW input. |
| 23 | $\overline{LDAC}$ | Asynchronous Load DAC input. Active LOW. |
| 24 | $\overline{CSLSB}$ | Chip Select Least Significant (LS) Byte. Active LOW input. |
| 25 | $\overline{WR}$ | Write input. Active LOW. |

| $\overline{CSMSB}$ | $\overline{CSLSB}$ | $\overline{LDAC}$ | $\overline{WR}$ | Operation |
|-------|-------|------|-----|-----------|
| 0 | 1 | 1 | 0 | Load MS Input Register |
| 1 | 0 | 1 | 0 | Load LS Input Register |
| 0 | 0 | 1 | 0 | Load MS and LS Input Registers |
| 1 | 1 | 0 | X | Load DAC Register from Input Registers |
| 0 | 0 | 0 | 0 | All Registers are transparent |
| 1 | 1 | 1 | X | No operation |
| X | X | 1 | 1 | No operation |

NOTE   X = Don't Care

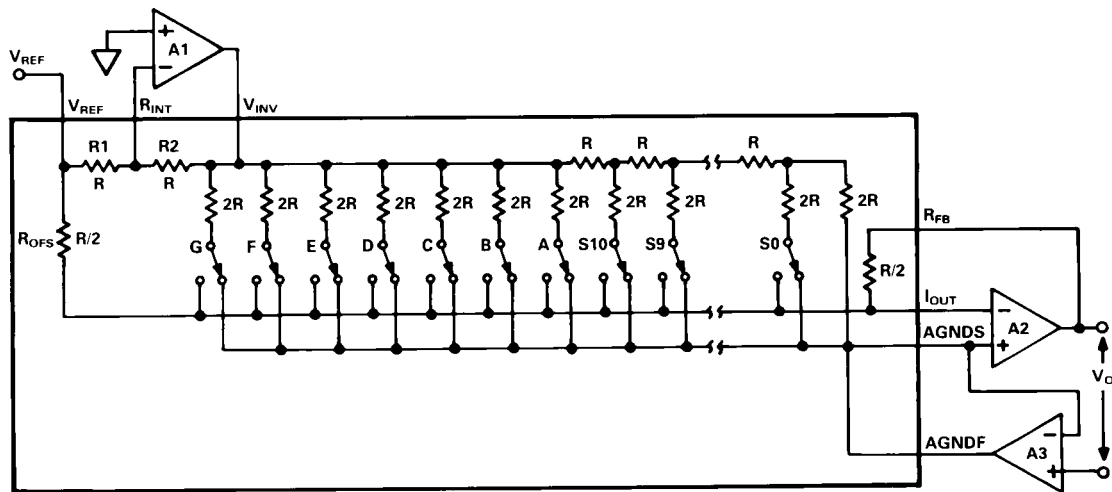| | | |
|----|-----|---|
| 26 | $V_{DD}$ | Power supply input. Specifications apply for $V_{DD}$ = + 12V ± 5% to + 15V ± 5%. |
| 27 | $V_{SS}$ | Bias pin for High Temperature Low Leakage configuration. To implement low leakage system, the pin should be at a negative voltage. See Figure 5 or 6 for recommended circuitry. |
| 28 | $V_{INV}$ | This pin must be connected to the output of the external inverting op-amp. See Figure 3. |

# AD7536



*Figure 3. Simplified Circuit Diagram of the AD7536
D/A Section Showing Connection of External Op-Amps*

## CIRCUIT INFORMATION – D/A SECTION

Figure 3 is a simplified circuit diagram of the AD7536 D/A
section and it also shows the external op-amp connection. The
device is a 14-bit DAC with three extra resistors on chip for
bipolar operation. It is configured so that the coding is Offset
Binary. The 14-bit DAC consists of an R-2R ladder for the
lower eleven bits (switches S0–S10). The three MSB's are decoded
to drive switches A–G sequentially. Each of these carries an
equally weighted current which is also equal to the current in
the R-2R ladder. $R_{OFS}$ has the same magnitude as $R_{FB}$ so that
the output is offset by a constant $-V_{REF}$. R1 and R2 (together
with external op-amp A1) invert $V_{REF}$ and apply it to the 14-bit
DAC ($V_{INV}$). See Table I for complete Offset Binary Code
Table.

To eliminate any slight variations in analog ground potential
with changing code, there are two analog ground pins. AGNDF
sinks all the current flowing through the switches to ground
while AGNDS is used as a reference point with minimal current
flowing in it. Figure 3 shows A3 maintaining AGNDS at Signal
Ground. The connection of AGNDS and AGNDF may be changed
depending on required system accuracy and output drive re-
quirements (see Figures 5 and 6).

## EQUIVALENT CIRCUIT ANALYSIS

Figure 4 shows an equivalent output circuit for the analog section
of the AD7536 D/A converter. The current source $I_{LEAKAGE}$ is
composed of surface and junction leakages. The resistor R0
denotes the equivalent output resistance of the DAC and associated
resistors. This varies with input code. $C_{OUT}$ is the capacitance
due to the current steering switches and varies from about
90pF to 180pF (typical values) depending on the digital input.
$g(V_{REF}, N)$ is the Thevenin equivalent voltage generator due
to the reference input voltage, $V_{REF}$, and the circuit transfer
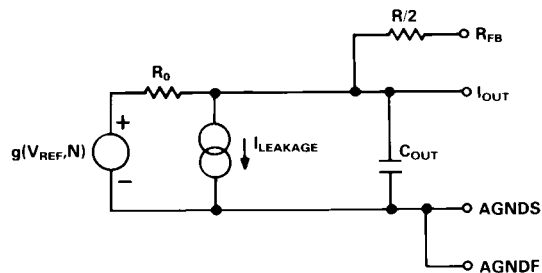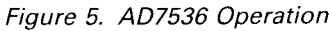function, N.



*Figure 4. AD7536 Equivalent Analog Output Circuit*

## CIRCUIT INFORMATION – DIGITAL SECTION

The digital inputs are designed to be both TTL and 5V CMOS
compatible. All logic inputs are static protected MOS gates with
typical input currents of less than 1nA. Internal input protection
is achieved by an on-chip distributed diode from DGND to
each MOS gate. To minimize power supply currents, it is re-
commended that the digital input voltages be driven as close as
possible to 0 and 5V logic levels.

*Figure 5. AD7536 Operation*

## BIPOLAR OPERATION
### (4-Quadrant Multiplication)

Figure 5 shows the AD7536 connected for bipolar operation. Specified accuracy is attained without the need for expensive closely matched external resistors. R1 and R2 provide an optional gain adjustment and capacitor C1 helps prevent overshoot and ringing when high-speed op-amps are used. The −300mV bias voltage for $V_{SS}$ is derived from R3, R4 and C2. Op-amp A3 (Figure 3 and Figure 6) is omitted from Figure 5. AGNDS and AGNDF are externally shorted to Signal Ground.

Table I shows the Offset Binary Code Table obtained with the circuit of Figure 5. It should be noted that the user can get a 2's Complement transfer function by inverting the MSB of the DAC word.

| Binary Number in DAC Register | Analog Output $V_{OUT}$ |
|---|---|
| **MSB          LSB**<br>11 1111 1111 1111 | $+V_{IN}\left(\dfrac{8191}{8192}\right)$ |
| 10 0000 0000 0001 | $+V_{IN}\left(\dfrac{1}{8192}\right)$ |
| 10 0000 0000 0000 | 0V |
| 00 0000 0000 0001 | $-V_{IN}\left(\dfrac{8191}{8192}\right)$ |
| 00 0000 0000 0000 | $-V_{IN}\left(\dfrac{8192}{8192}\right) = -V_{IN}$ |

*Table I. Offset Binary Code Table for AD7536*

## OFFSET AND GAIN ADJUSTMENT FOR FIGURE 5.
### Offset Adjustment

1. Adjust offset of amplifier A1 so that potential at $R_{INT}$ is <10μV with respect to Signal Ground.
2. Load DAC register with 10 0000 0000 0000.
3. Adjust offset of amplifier A2 until $V_O$ =0V (<10μV).

### Gain Adjustment

1. Load DAC register with all 1's.
2. Trim potentiometer R2 so that $V_O = +V_{IN}\dfrac{(8191)}{(8192)}$

For high-temperature applications, resistors and potentiometers should have a low Temperature Coefficient. In many applications, because of the excellent Offset Error, Full Scale Error and Gain T.C. specifications of the AD7536, trimming of the Offset and Gain is not necessary.
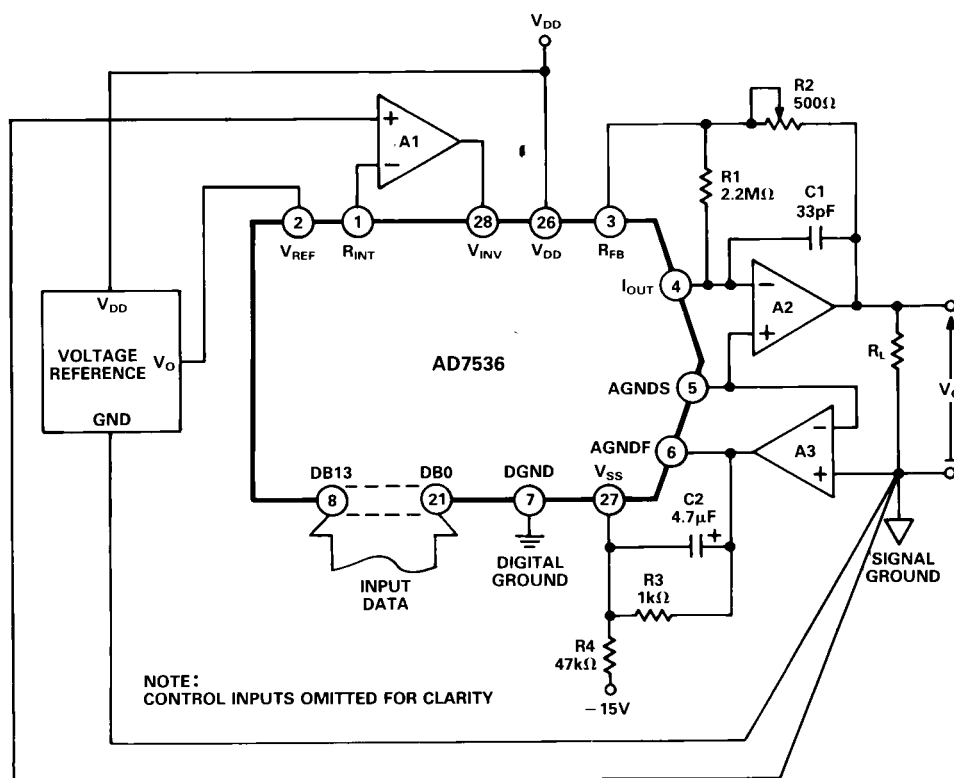
# AD7536



Figure 6. AD7536 Operation with Forced Ground

## GROUNDING CONSIDERATIONS

In the circuits of Figures 5 and 6, with $V_{REF} = +10V$, 1LSB has a value of 1.2mV. So, factors which are not important in less accurate systems must, in this case, be given careful consideration. Among these, the whole question of grounding is crucial. Voltage reference ground, the $I_{OUT}$ pin on the DAC, the noninverting pin of A1 and SIGNAL GROUND must all be at the same potential. Note that in Figure 5, AGNDS and AGNDF are externally shorted and A3 is not used. Voltage drops due to bond wire resistance are not compensated for in this circuit. This means that an extra linearity error of less than 0.1LSB is added to the DAC linearity error. If the user wishes to eliminate this extra error, then the circuit of Figure 6 should be used.

Here, A3 is used to maintain AGNDS at Signal Ground potential. $I_{OUT}$ is also at Signal Ground potential. By using the Force, Sense technique all switch contacts on the DAC are at exactly the same potential and any error due to bond wire resistance is eliminated. If A3 is not a low offset voltage ($<100\mu V$) op-amp, it should be trimmed with a potentiometer until the voltage at AGNDS is $<10\mu V$ with respect to SIGNAL GROUND. Figure 7 shows how the circuit of Figure 5 might be be laid out. Gain trim components R1 and R2 have been omitted for clarity. Note how the input to $V_{REF}$ (pin 2) is shielded to reduce ac feedthrough while the digital inputs are shielded to minimize digital feedthrough.
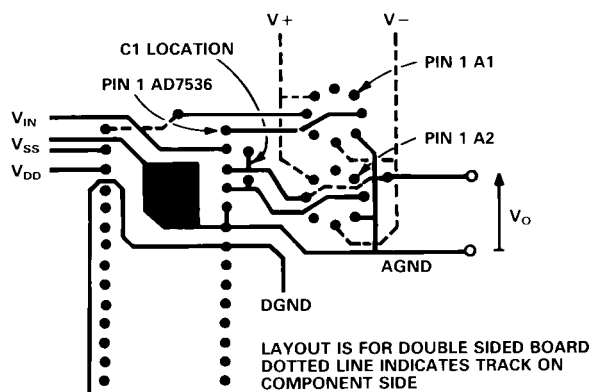


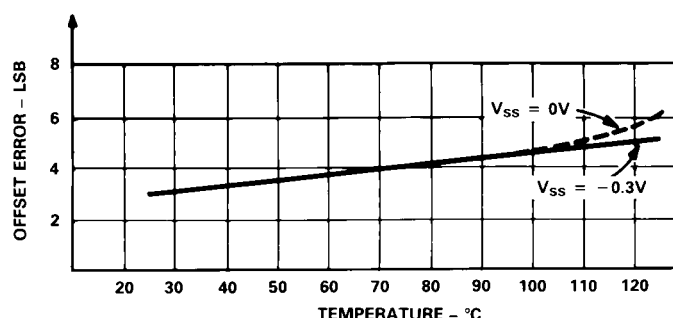Figure 7. Suggested Layout for AD7536 Circuit of Figure 5

Figure 8. Typical Graph of Offset Error vs. Temperature
With and Without Low Leakage Configuration

## LOW LEAKAGE CONFIGURATION

Leakage current in CMOS D/A converters has two components. Current leaks from $V_{DD}$ into the $I_{OUT}$ line and is present at all DAC codes. There is also leakage across the off switches in the DAC. The polarity of this current depends on $V_{INV}$ and its magnitude is related to the code in the DAC register. At high temperatures (above 90°C) it is normal for the leakage current to increase dramatically. By its nature it will affect all critical dc parameters (Linearity Error, Gain Error and Offset Error). The AD7536 features a leakage reduction configuration (patent pending) to keep the leakage current low (typically <10nA) over an extended temperature range. This ensures that the DAC maintains its 25°C performance very well at temperatures up to 125°C.

The AD7536 can be operated with or without the leakage reduction configuration. If $V_{SS}$ (pin 27) is tied to AGND, then the DAC will exhibit normal output leakage current at high temperatures. To use the low leakage facility, $V_{SS}$ should be tied to $-0.3V$ as in Figures 5 and 6. The current taken by $V_{SS}$ is very low (<10μA) allowing a simple resistor divider (R3, R4) to produce the required $-300mV$ from $-15V$. The capacitor C2 in parallel with R3 is an integral part of the low leakage configuration and must be 4.7μF or greater. Figure 8 is a plot of Offset Error versus temperature for both conditions. It clearly shows the improvement when the low leakage configuration is used.

## OP-AMP SELECTION

In choosing an amplifier to be used with the AD7536, three parameters are of prime importance. These are:

1. Input Offset Voltage ($V_{OS}$)
2. Input Bias Current ($I_B$)
3. Offset Voltage Drift (TC $V_{OS}$).

To maintain specified accuracy with $V_{REF}$ at 10V, A1 and A2 of Figures 5 and 6 must have $V_{OS}$ <100μV and $I_B$ <10nA. It is important that the amplifier Open Loop Gain, $A_{VOL}$, be sufficiently large to keep $V_{OS}$ <100μV for the full output voltage range. For a maximum output of 10V, $A_{VOL}$ must be greater than 100,000.

In the Forced Ground configuration of Figure 6, one can use an AD OP-07 for amplifier A3, without any external adjustment for $V_{OS}$. In low frequency or fixed reference applications where fast output settling time is not required, the AD OP-07 is also recommended for A1 and A2. Because of its low $V_{OS}$ no external potentiometers are needed. For faster settling time, one can use the AD544 series of op-amps.

Offset Voltage Drift and Bias Current drift are critical parameters for operation over a wide temperature range. The AD OP-07, AD OP-27 and AD OP-37 all exhibit very low offset drift while the AD544 has very low bias current drift. Table II summarizes the important specifications of the op-amps mentioned above.

| Op-Amp | Input Offset Voltage ($V_{OS}$) | Input Bias Current ($I_B$) | Offset Voltage Drift (TC $V_{OS}$) | Settling Time to 0.003% FS |
|---|---|---|---|---|
| AD544L | 500μV | 25pA | 5μV/°C | 5μs |
| AD OP-07H | 75μV | 3nA | 0.6μV/°C | 50μs typ |
| AD OP-27CH | 100μV | 80nA | 0.6μV/°C | 6μs typ |
| AD OP-37CH | 100μV | 80nA | 0.6μV/°C | 1μs typ |
| HA-2620 | 4mV | 35nA | 20μV/°C | 0.8μs typ |

Table II. Guide to Op-Amp Selection

# AD7536

## MICROPROCESSOR INTERFACING
### AD7536 – 8086A INTERFACE

The versatility of the AD7536 loading sturcture allows interfacing to both 8- and 16-bit microprocessor systems. Figure 9 shows the 8086 16-bit processor interfacing to a single device. In this circuit the double buffering feature of the DAC is not used. AD0-AD13 of the 16-bit data bus are connected to the DAC data bus (DB0-DB13). The 14-bit word is written to the DAC in one MOV instruction and the analog output responds immediately. In this example the DAC address is D000. A software routine for Figure 9 is given in Table III. In a multiple DAC system the double buffering of the AD7536 allows the user to simultaneously update all DAC's. In Figure 10, a 14-bit word is loaded to the Input Registers of each of the DACs in sequence. Then, with one instruction to the appropriate address, CS4 (i.e., LDAC) is brought low, updating all the DACs simultaneously.
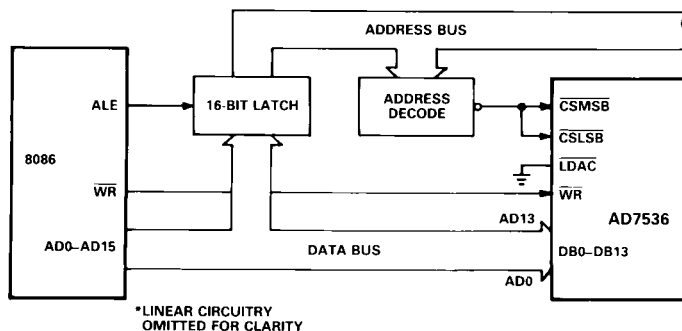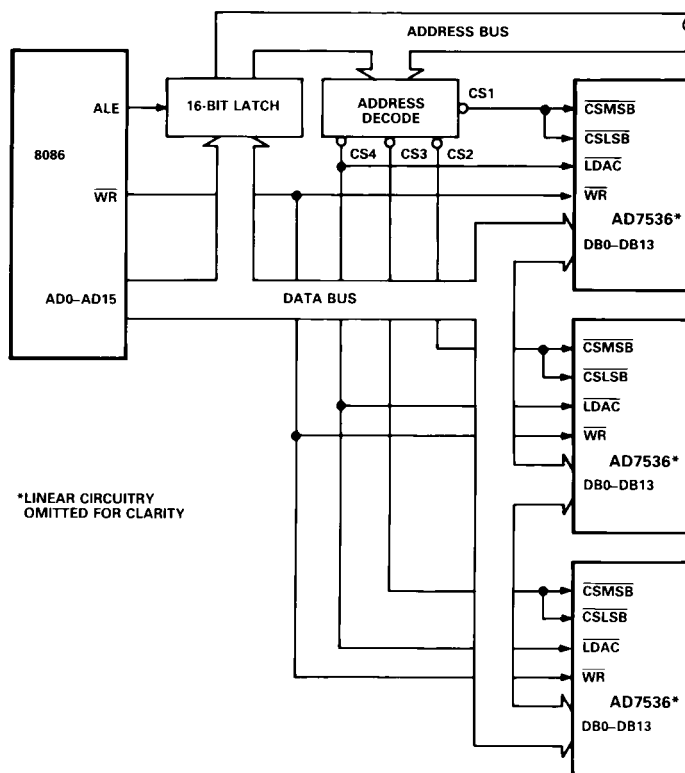


*Figure 9. AD7536 – 8086 Interface Circuit*



*Figure 10. AD7536 – 8086 Interface: Multiple DAC System*

### ASSUME DS: DACLOAD, CS : DACLOAD
### DACLOAD SEGMENT AT 000

| 00 | 8CC9 | MOV CX, CS | : | DEFINE DATA SEGMENT REGISTER EQUAL |
| 02 | 8ED9 | MOV DS, CX | : | TO CODE SEGMENT REGISTER |
| 04 | BF00D0 | MOV DI, # D000 | : | LOAD DI WITH D000 |
| 07 | C705"YZWX" | MOV MEM, # YZWX" | : | DAC LOADED WITH WXYZ |
| 0B | EA0000 | | : | CONTROL IS RETURNED TO THE |
| 0E | 00FF | | | MONITOR PROGRAM |

*Table III. Sample Program for Loading AD7536 from 8086*

## AD7536 – MC68000 INTERFACE

Interfacing between the MC68000 and the AD7536 is accomplished using the circuit of Figure 11. The following routine writes data to the DAC input registers and then outputs the data via the DAC register.

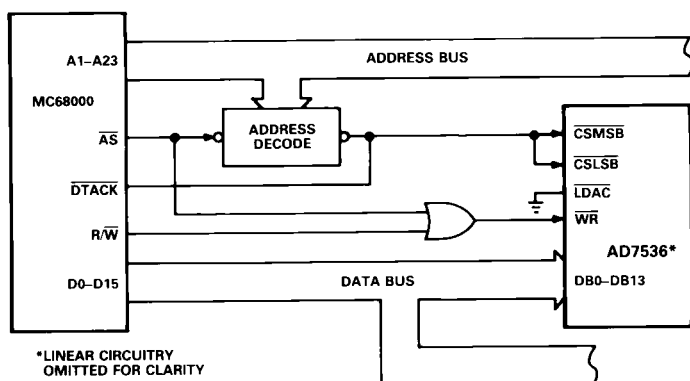| 01000 | MOVE.W | #W, D0 | The desired DAC data, W, is loaded into Data Register 0. W may be any value between 0 and 16383 (decimal) or 0 and 3FFF (hexademical). |
| | MOVE.W | D0,$E000 | The data W is transferred between D0 and the DAC Register. |
| | MOVE.B | #228,D7 | Control is returned to the System Monitor Program using these tow |
| | TRAP | #14 | instructions. |



Figure 11. AD7536 – MC68000 Interface

## AD7536 – Z80 INTERFACE

Though the AD7536 is ideally suited for use either with 16-bit microprocessors or in stand-alone applications, it can also be interfaced to 8-bit processor systems. Figure 12 is an interface circuit for the popular Z80 microprocessor.
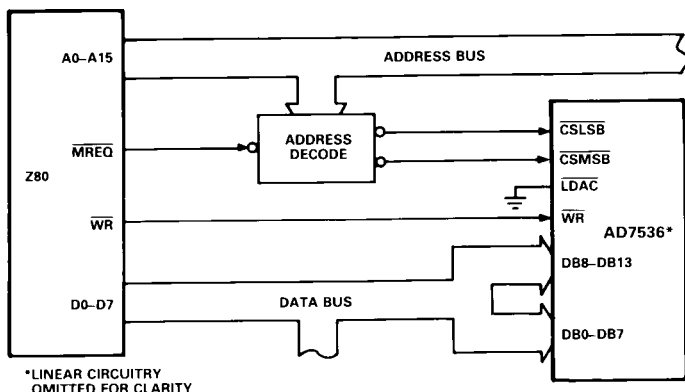


Figure 12. AD7536 – Z80 Interface

## DIGITAL FEEDTHROUGH

In the preceding interface configurations, most digital inputs to the AD7536 are directly connected to the microprocessor bus. Even when the device is not selected, these inputs will be constantly changing. The high frequency logic activity on the bus can feed through the DAC package capacitance to show up as noise on the analog output. To minimize this Digital Feedthrough isolate the DAC from the noise source. Figure 13 shows an interface circuit which physically isolates the DAC from the bus. One may also use other means, such as peripheral interface devices, to reduce the Digital Feedthrough.
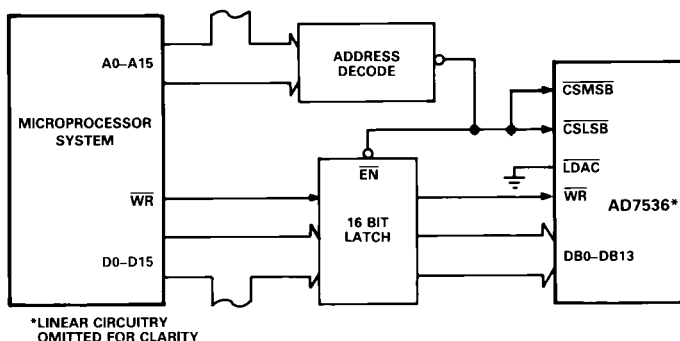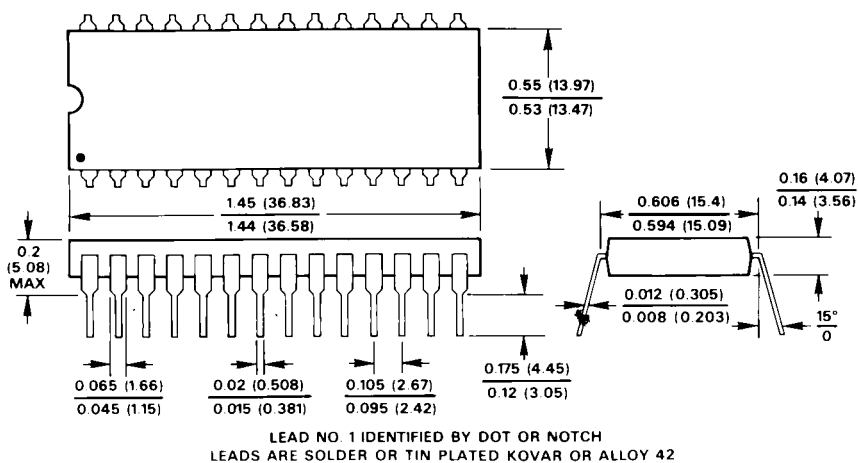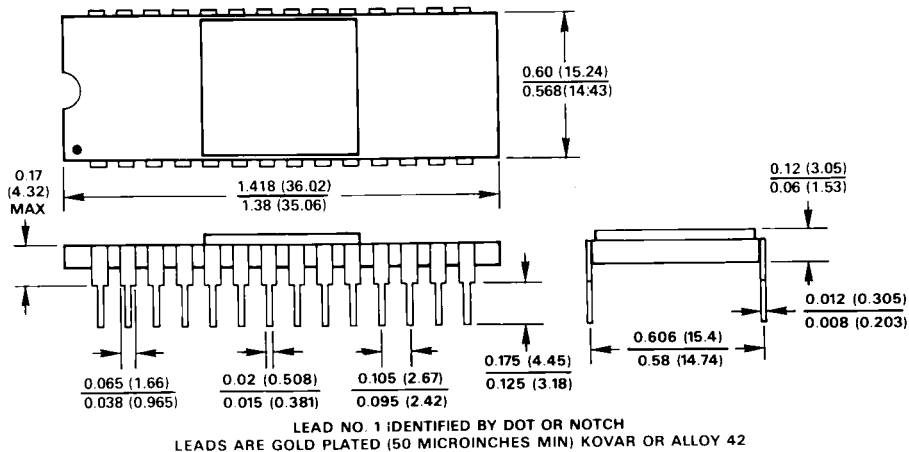


Figure 13. AD7536 Interface Circuit Using Latches to Minimize Digital Feedthrough

**AD7536**

## MECHANICAL INFORMATION
## OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

### 28-PIN CERAMIC DIP (SUFFIX D)

0.60 (15.24)
0.568 (14.43)

0.17 (4.32) MAX

1.418 (36.02)
1.38 (35.06)

0.12 (3.05)
0.06 (1.53)

0.012 (0.305)
0.008 (0.203)

0.606 (15.4)
0.58 (14.74)

0.175 (4.45)
0.125 (3.18)

0.065 (1.66)
0.038 (0.965)

0.02 (0.508)
0.015 (0.381)

0.105 (2.67)
0.095 (2.42)

LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE GOLD PLATED (50 MICROINCHES MIN) KOVAR OR ALLOY 42

### 28-PIN PLASTIC DIP (SUFFIX N)

0.55 (13.97)
0.53 (13.47)

0.2 (5.08) MAX

1.45 (36.83)
1.44 (36.58)

0.16 (4.07)
0.14 (3.56)

0.606 (15.4)
0.594 (15.09)

0.012 (0.305)
0.008 (0.203)

15°
0

0.175 (4.45)
0.12 (3.05)

0.065 (1.66)
0.045 (1.15)

0.02 (0.508)
0.015 (0.381)

0.105 (2.67)
0.095 (2.42)

LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN PLATED KOVAR OR ALLOY 42