40-Channel, 3 V/5 V, Single-Supply, Serial, 14-Bit Voltage Output DAC

AD5384

FEATURES

- Guaranteed monotonic
- INL error: ±4 LSB max
- On-chip 1.25 V/2.5 V, 10 ppm/°C reference
- Temperature range: –40°C to +85°C
- Rail-to-rail output amplifier
- Power-down
- Package type: 100-lead CSPBGA (10 mm × 10 mm)
- User Interfaces:
  - Serial (SPI-®/QSPI-™/MICROWIRE-™/DSP-compatible, featuring data readback)
  - I²C-®compatible

INTEGRATED FUNCTIONS

- Channel monitor
- Simultaneous output update via $\overline{\text{LDAC}}$
- Clear function to user-programmable code
- Amplifier boost mode to optimize slew rate
- User-programmable offset and gain adjust
- Toggle mode enables square wave generation
- Thermal monitor

APPLICATIONS

- Variable optical attenuators (VOA)
- Level setting (ATE)
- Optical micro-electro-mechanical systems (MEMS)
- Control systems
- Instrumentation

FUNCTIONAL BLOCK DIAGRAM

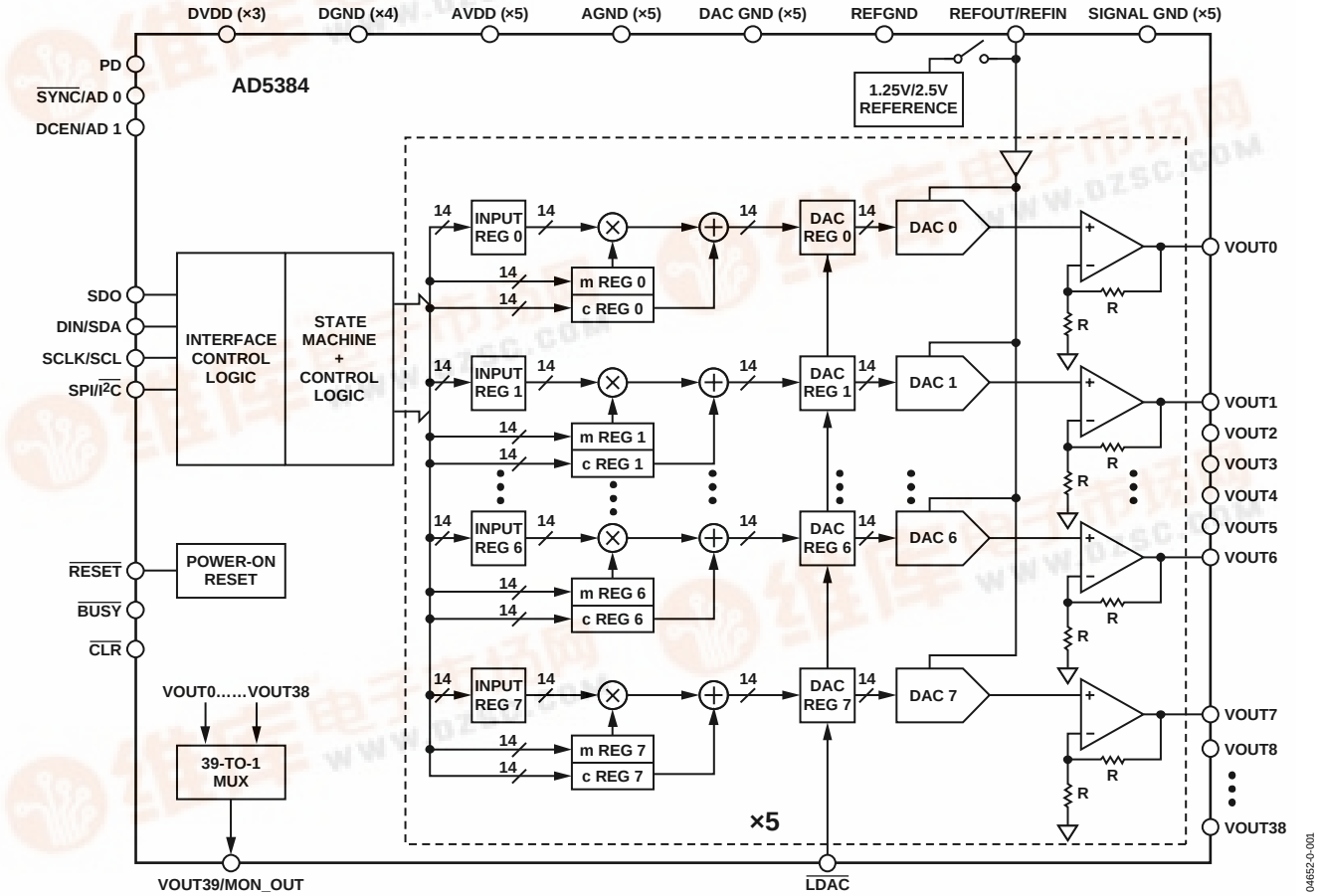

Figure 1.

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TABLE OF CONTENTS

REVISION HISTORY

10/04—Changed from Rev. 0 to Rev. A

Changes to Table 19 24
Changes to Ordering Guide 35

7/04—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD5384 is a complete single-supply, 40-channel, 14-bit DAC available in a 100-lead CSPBGA package. All 40 channels have an on-chip output amplifier with rail-to-rail operation. The AD5384 includes an internal 1.25 V/2.5 V, 10 ppm/°C reference, an on-chip channel monitor function that multiplexes the analog outputs to a common MON_OUT pin for external monitoring, and an output amplifier boost mode that allows the amplifier slew rate to be optimized. The AD5384 contains a serial interface compatible with SPI, QSPI, MICROWIRE, and DSP interface standards with interface speeds in excess of 30 MHz and an I^2C-compatible interface supporting 400 kHz data transfer rate. An input register followed by a DAC register provides double buffering, allowing the DAC outputs to be updated independently or simultaneously. using the $\overline{\text{LDAC}}$ input. Each channel has a programmable gain and offset adjust register letting the user fully calibrate any DAC channel. Power consumption is typically 0.25 mA/channel with boost mode off.

Table 1. Complete Family of High Channel Count, Low Voltage, Single-Supply DACs in Portfolio

Model	Resolution	AV_{DD} Range	Output Channels	Linearity Error (LSB)	Package Description	Package Option
AD5380BST-5	14 Bits	4.5 V to 5.5 V	40	±4	100-Lead LQFP	ST-100
AD5380BST-3	14 Bits	2.7 V to 3.6 V	40	±4	100-Lead LQFP	ST-100
AD5381BST-5	12 Bits	4.5 V to 5.5 V	40	±1	100-Lead LQFP	ST-100
AD5381BST-3	12 Bits	2.7 V to 3.6 V	40	±1	100-Lead LQFP	ST-100
AD5384BBC-5	14 Bits	4.5 V to 5.5 V	40	±4	100-Lead CSPBGA	BC-100
AD5384BBC-3	14 Bits	2.7 V to 3.6 V	40	±4	100-Lead CSPBGA	BC-100
AD5382BST-5	14 Bits	4.5 V to 5.5 V	32	±4	100-Lead LQFP	ST-100
AD5382BST-3	14 Bits	2.7 V to 3.6 V	32	±4	100-Lead LQFP	ST-100
AD5383BST-5	12 Bits	4.5 V to 5.5 V	32	±1	100-Lead LQFP	ST-100
AD5383BST-3	12 Bits	2.7 V to 3.6 V	32	±1	100-Lead LQFP	ST-100
AD5390BST-5	14 Bits	4.5 V to 5.5 V	16	±3	52-Lead LQFP	ST-52
AD5390BCP-5	14 Bits	4.5 V to 5.5 V	16	±3	64-Lead LFCSP	CP-64
AD5390BST-3	14 Bits	2.7 V to 3.6 V	16	±4	52-Lead LQFP	ST-52
AD5390BCP-3	14 Bits	2.7 V to 3.6 V	16	±4	64-Lead LFCSP	CP-64
AD5391BST-5	12 Bits	4.5 V to 5.5 V	16	±1	52-Lead LQFP	ST-52
AD5391BCP-5	12 Bits	4.5 V to 5.5 V	16	±1	64-Lead LFCSP	CP-64
AD5391BST-3	12 Bits	2.7 V to 3.6 V	16	±1	52-Lead LQFP	ST-52
AD5391BCP-3	12 Bits	2.7 V to 3.6 V	16	±1	64-Lead LFCSP	CP-64
AD5392BST-5	14 Bits	4.5 V to 5.5 V	8	±3	52-Lead LQFP	ST-52
AD5392BCP-5	14 Bits	4.5 V to 5.5 V	8	±3	64-Lead LFCSP	CP-64
AD5392BST-3	14 Bits	2.7 V to 3.6 V	8	±4	52-Lead LQFP	ST-52
AD5392BCP-3	14 Bits	2.7 V to 3.6 V	8	±4	64-Lead LFCSP	CP-64

Table 2. 40-Channel, Bipolar Voltage Output DAC

Model	Resolution	Analog Supplies	Output Channels	Linearity Error (LSB)	Package	Package Option
AD5379ABC	14 Bits	±11.4 V to ±16.5 V	40	±3	108-Lead CSPBGA	BC-108

SPECIFICATIONS

AD5384-5 SPECIFICATIONS

AV_{DD} = 4.5 V to 5.5 V; DV_{DD} = 2.7 V to 5.5 V, AGND = DGND = 0 V; external REFIN = 2.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	AD5384-5[1]	Unit	Test Conditions/Comments
ACCURACY			
Resolution	14	Bits	
Relative Accuracy[2] (INL)	±4	LSB max	±1 LSB typical
Differential Nonlinearity (DNL)	−1/+2	LSB max	Guaranteed monotonic by design over temperature
Zero-Scale Error	4	mV max	
Offset Error	±4	mV max	Measured at code 32 in the linear region
Offset Error TC	±5	µV/°C typ	
Gain Error	±0.024	% FSR max	At 25°C
	±0.06	% FSR max	T_{MIN} to T_{MAX}
Gain Temperature Coefficient[3]	2	ppm FSR/°C typ	
DC Crosstalk[3]	0.5	LSB max	
REFERENCE INPUT/OUTPUT			
Reference Input[3]			
Reference Input Voltage	2.5	V	±1% for specified performance, $AV_{DD} = 2 \times REFIN + 50$ mV
DC Input Impedance	1	MΩ min	Typically 100 MΩ
Input Current	±1	µA max	Typically ±30 nA
Reference Range	1 to $V_{DD}/2$	V min/max	
Reference Output[4]			Enabled via CR10 in the AD5384 control register, CR12, selects the output voltage.
Output Voltage	2.495/2.505	V min/max	At ambient; CR12 = 1; optimized for 2.5 V operation
	1.22/1.28	V min/max	CR12 = 0
Reference TC	±10	ppm/°C max	Temperature range: +25°C to +85°C
	±15	ppm/°C max	Temperature range: −40°C to +85°C
OUTPUT CHARACTERISTICS[3]			
Output Voltage Range[2]	$0/AV_{DD}$	V min/max	
Short-Circuit Current	40	mA max	
Load Current	±1	mA max	
Capacitive Load Stability			
$R_L = \infty$	200	pF max	
R_L = 5 kΩ	1000	pF max	
DC Output Impedance	0.5	Ω max	
MONITOR PIN			
Output Impedance	500	Ω typ	
Three-State Leakage Current	100	nA typ	
LOGIC INPUTS (EXCEPT SDA/SCL)[3]			DV_{DD} = 2.7 V to 5.5 V
V_{IH}, Input High Voltage	2	V min	
V_{IL}, Input Low Voltage	0.8	V max	
Input Current	±10	µA max	Total for all pins. $T_A = T_{MIN}$ to T_{MAX}
Pin Capacitance	10	pF max	
LOGIC INPUTS (SDA, SCL ONLY)			
V_{IH}, Input High Voltage	$0.7\ DV_{DD}$	V min	SMBus-compatible at $DV_{DD} < 3.6$ V
V_{IL}, Input Low Voltage	$0.3\ DV_{DD}$	V max	SMBus-compatible at $DV_{DD} < 3.6$ V
I_{IN}, Input Leakage Current	±1	µA max	
V_{HYST}, Input Hysteresis	$0.05\ DV_{DD}$	V min	
C_{IN}, Input Capacitance	8	pF typ	
Glitch Rejection	50	ns max	Input filtering suppresses noise spikes of less than 50 ns

Parameter	AD5384-5[1]	Unit	Test Conditions/Comments
LOGIC OUTPUTS ($\overline{BUSY}$, SDO)[3]			
V_{OL}, Output Low Voltage	0.4	V max	DV_{DD} = 5 V ± 10%, sinking 200 µA
V_{OH}, Output High Voltage	DV_{DD} – 1	V min	DV_{DD} = 5 V ± 10%, sourcing 200 µA
V_{OL}, Output Low Voltage	0.4	V max	DV_{DD} = 2.7 V to 3.6 V, sinking 200 µA
V_{OH}, Output High Voltage	DV_{DD} – 0.5	V min	DV_{DD} = 2.7 V to 3.6 V, sourcing 200 µA
High Impedance Leakage Current	±1	µA max	SDO only
High Impedance Output Capacitance	5	pF typ	SDO only
LOGIC OUTPUT (SDA)[3]			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 3 mA
	0.6	V max	I_{SINK} = 6 mA
Three-State Leakage Current	±1	µA max	
Three-State Output Capacitance	8	pF typ	
POWER REQUIREMENTS			
AV_{DD}	4.5/5.5	V min/max	
DV_{DD}	2.7/5.5	V min/max	
Power Supply Sensitivity[3]			
ΔMidscale/ΔAV_{DD}	–85	dB typ	
AI_{DD}	0.375	mA/channel max	Outputs unloaded, boost off; 0.25 mA/channel typ
	0.475	mA/channel max	Outputs unloaded, boost on; 0.32 5mA/channel typ
DI_{DD}	1	mA max	V_{IH} = DV_{DD}, V_{IL} = DGND
AI_{DD} (Power-Down)	2	µA max	Typically 200 nA
DI_{DD} (Power-Down)	20	µA max	Typically 3 µA
Power Dissipation	80	mW max	Outputs unloaded, boost off, AV_{DD} = DV_{DD} = 5 V

[1] AD5384-5 is calibrated using an external 2.5 V reference. Temperature range for all versions: –40°C to +85°C.
[2] Accuracy guaranteed from V_{OUT} = 10 mV to AV_{DD} – 50 mV.
[3] Guaranteed by characterization, not production tested.
[4] Default on the AD5384-5 is 2.5 V. Programmable to 1.25 V via CR12 in the AD5384 control register; operating the AD5384-5 with a 1.25 V reference will lead to degraded accuracy specifications.

AC CHARACTERISTICS[1]

AV_{DD} = 2.7 V to 3.6 V; DV_{DD} = 2.7 V to 5.5 V, AGND = DGND = 0 V.

Table 4.

Parameter	AD5384-5	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time			Boost mode off, CR11 = 0 1/4 scale to 3/4 scale change settling to ±1 LSB
	8	µs typ	
	10	µs max	
Slew Rate[2]	2	V/µs typ	Boost mode off, CR11 = 0
	3	V/µs typ	Boost mode on, CR11 = 1
Digital-to-Analog Glitch Energy	12	nV-s typ	
Glitch Impulse Peak Amplitude	15	mV typ	
Channel-to-Channel Isolation	100	dB typ	See the Terminology section
DAC-to-DAC Crosstalk	1	nV-s typ	See the Terminology section
Digital Crosstalk	0.8	nV-s typ	
Digital Feedthrough	0.1	nV-s typ	Effect of input bus activity on DAC output under test
Output Noise 0.1 Hz to 10 Hz	15	µV p-p typ	External reference, midscale loaded to DAC
	40	µV p-p typ	Internal reference, midscale loaded to DAC
Output Noise Spectral Density			
@ 1 kHz	150	nV/√Hz typ	
@ 10 kHz	100	nV/√Hz typ	

[1] Guaranteed by design and characterization, not production tested.
[2] The slew rate can be programmed via the current boost control bit (CR11) in the AD5384 control register.

AD5384-3 SPECIFICATIONS

AV_{DD} = 2.7 V to 3.6 V; DV_{DD} = 2.7 V to 5.5 V, AGND = DGND = 0 V; external REFIN = 1.25 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 5.

Parameter	AD5384-3[1]	Unit	Test Conditions/Comments
ACCURACY			
Resolution	14	Bits	
Relative Accuracy[2]	±4	LSB max	
Differential Nonlinearity	−1/+2	LSB max	Guaranteed monotonic over temperature
Zero-Scale Error	4	mV max	
Offset Error	±4	mV max	Measured at Code 64 in the linear region
Offset Error TC	±5	µV/°C typ	
Gain Error	±0.024	% FSR max	At 25°C
	±0.1	% FSR max	T_{MIN} to T_{MAX}
Gain Temperature Coefficient[3]	2	ppm FSR/°C typ	
DC Crosstalk[3]	0.5	LSB max	
REFERENCE INPUT/OUTPUT			
Reference Input[3]			
Reference Input Voltage	1.25	V	±1% for specified performance
DC Input Impedance	1	MΩ min	Typically 100 MΩ
Input Current	±1	µA max	Typically ±30 nA
Reference Range	1 to $AV_{DD}/2$	V min/max	
Reference Output[4]			
Output Voltage	1.245/1.255	V min/max	At ambient; CR12 = 0; optimized for 1.25 V operation
	2.47/2.53	V min/max	CR12 = 1
Reference TC	±10	ppm/°C max	Temperature range: +25°C to +85°C
	±15	ppm/°C max	Temperature range: −40°C to +85°C
OUTPUT CHARACTERISTICS[3]			
Output Voltage Range[2]	$0/AV_{DD}$	V min/max	
Short-Circuit Current	40	mA max	
Load Current	±1	mA max	
Capacitive Load Stability			
$R_L = \infty$	200	pF max	
R_L = 5 kΩ	1000	pF max	
DC Output Impedance	0.5	Ω max	
MONITOR PIN			
Output Impedance	500	Ω typ	
Three-State Leakage Current	100	nA typ	
LOGIC INPUTS (EXCEPT SDA/SCL)[3]			DV_{DD} = 2.7 V to 3.6 V
V_{IH}, Input High Voltage	2	V min	
V_{IL}, Input Low Voltage	0.8	V max	
Input Current	±10	µA max	Total for all pins; $T_A = T_{MIN}$ to T_{MAX}
Pin Capacitance	10	pF max	
LOGIC INPUTS (SDA, SCL ONLY)			
V_{IH}, Input High Voltage	$0.7\ DV_{DD}$	V min	SMBus-compatible at $DV_{DD} < 3.6$ V
V_{IL}, Input Low Voltage	$0.3\ DV_{DD}$	V max	SMBus-compatible at $DV_{DD} < 3.6$ V
I_{IN}, Input Leakage Current	±1	µA max	
V_{HYST}, Input Hysteresis	$0.05\ DV_{DD}$	V min	
C_{IN}, Input Capacitance	8	pF typ	
Glitch Rejection	50	ns max	Input filtering suppresses noise spikes of less than 50 ns

Parameter	AD5384-3[1]	Unit	Test Conditions/Comments
LOGIC OUTPUTS ($\overline{BUSY}$, SDO)[3]			
V_{OL}, Output Low Voltage	0.4	V max	Sinking 200 µA
V_{OH}, Output High Voltage	DV_{DD} – 0.5	V min	Sourcing 200 µA
High Impedance Leakage Current	±1	µA max	SDO only
High Impedance Output Capacitance	5	pF typ	SDO only
LOGIC OUTPUT (SDA)[3]			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 3 mA
	0.6	V max	I_{SINK} = 6 mA
Three-State Leakage Current	±1	µA max	
Three-State Output Capacitance	8	pF typ	
POWER REQUIREMENTS			
AV_{DD}	2.7/3.6	V min/max	
DV_{DD}	2.7/3.6	V min/max	
Power Supply Sensitivity[3]			
ΔMidscale/ΔAV_{DD}	–85	dB typ	
AI_{DD}	0.375	mA/channel max	Outputs unloaded, boost off; 0.25 mA/channel typ
	0.475	mA/channel max	Outputs unloaded, boost on; 0.325 mA/channel typ
DI_{DD}	1	mA max	V_{IH} = DV_{DD}, V_{IL} = DGND
AI_{DD} (Power-Down)	2	µA max	Typically 200 nA
DI_{DD} (Power-Down)	20	µA max	Typically 1 µA
Power Dissipation	48	mW max	Outputs unloaded, boost off, AV_{DD} = DV_{DD} = 3 V

[1] AD5384-3 is calibrated using an external 1.25 V reference. Temperature range is –40°C to +85°C.
[2] Accuracy guaranteed from V_{OUT} = 10 mV to AV_{DD} – 50 mV.
[3] Guaranteed by characterization, not production tested.
[4] Default on the AD5384-3 is 1.25 V. Programmable to 2.5 V via CR12 in the AD5384 control register; operating the AD5384-3 with a 2.5 V reference will lead to degraded accuracy specifications and limited input code range.

AC CHARACTERISTICS[1]

AV_{DD} = 2.7 V to 3.6 V and 4.5 V to 5.5 V; DV_{DD} = 2.7 V to 5.5 V; AGND = DGND = 0 V.

Table 6.

Parameter	AD5384-3	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time			Boost mode off, CR11 = 0 1/4 scale to 3/4 scale change settling to ±1 LSB
	8	µs typ	
	10	µs max	
Slew Rate[2]	2	V/µs typ	Boost mode off, CR11 = 0
	3	V/µs typ	Boost mode on, CR11 = 1
Digital-to-Analog Glitch Energy	12	nV-s typ	
Glitch Impulse Peak Amplitude	15	mV typ	
Channel-to-Channel Isolation	100	dB typ	See the Terminology section
DAC-to-DAC Crosstalk	1	nV-s typ	See the Terminology section
Digital Crosstalk	0.8	nV-s typ	
Digital Feedthrough	0.1	nV-s typ	Effect of input bus activity on DAC output under test
Output Noise 0.1 Hz to 10 Hz	15	µV p-p typ	External reference, midscale loaded to DAC
	40	µV p-p typ	Internal reference, midscale loaded to DAC
Output Noise Spectral Density			
@ 1 kHz	150	nV/√Hz typ	
@ 10 kHz	100	nV/√Hz typ	

[1] Guaranteed by design and characterization, not production tested.
[2] The slew rate can be programmed via the current boost control bit (CR11) in the AD5384 control register.

TIMING CHARACTERISTICS

SERIAL INTERFACE

DV_{DD} = 2.7 V to 5.5 V; AV_{DD} = 4.5 V to 5.5 V or 2.7 V to 3.6 V; AGND = DGND = 0 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 7.

Parameter[1, 2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	33	ns min	SCLK cycle time
t_2	13	ns min	SCLK high time
t_3	13	ns min	SCLK low time
t_4	13	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5 [4]	13	ns min	24th SCLK falling edge to $\overline{SYNC}$ falling edge
t_6[4]	33	ns min	Minimum $\overline{SYNC}$ low time
t_7	10	ns min	Minimum $\overline{SYNC}$ high time
t_{7A}	50	ns min	Minimum $\overline{SYNC}$ high time in readback mode
t_8	5	ns min	Data setup time
t_9	4.5	ns min	Data hold time
t_{10}[4]	30	ns max	24th SCLK falling edge to $\overline{BUSY}$ falling edge
t_{11}	670	ns max	$\overline{BUSY}$ pulse width low (single channel update)
t_{12}[4]	20	ns min	24th SCLK falling edge to $\overline{LDAC}$ falling edge
t_{13}	20	ns min	$\overline{LDAC}$ pulse width low
t_{14}	100	ns max	$\overline{BUSY}$ rising edge to DAC output response time
t_{15}	0	ns min	$\overline{BUSY}$ rising edge to $\overline{LDAC}$ falling edge
t_{16}	100	ns min	$\overline{LDAC}$ falling edge to DAC output response time
t_{17}	8	µs typ	DAC output settling time boost mode off
t_{18}	20	ns min	$\overline{CLR}$ pulse width low
t_{19}	12	µs max	$\overline{CLR}$ pulse activation time
t_{20}[5]	20	ns max	SCLK rising edge to SDO valid
t_{21}[5]	5	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_{22}[5]	8	ns min	$\overline{SYNC}$ rising edge to SCLK rising edge
t_{23}	20	ns min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge

[1] Guaranteed by design and characterization, not production tested.
[2] All input signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of DV_{DD}), and are timed from a voltage level of 1.2 V.
[3] See Figure 2, Figure 3, Figure 5, and Figure 6.
[4] Standalone mode only.
[5] Daisy-chain mode only.

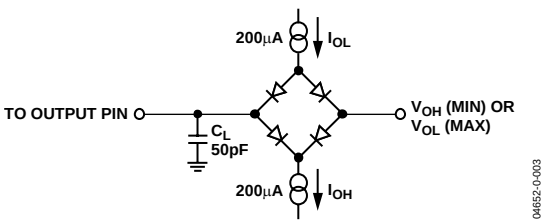

Figure 2. Load Circuit for Digital Output Timing

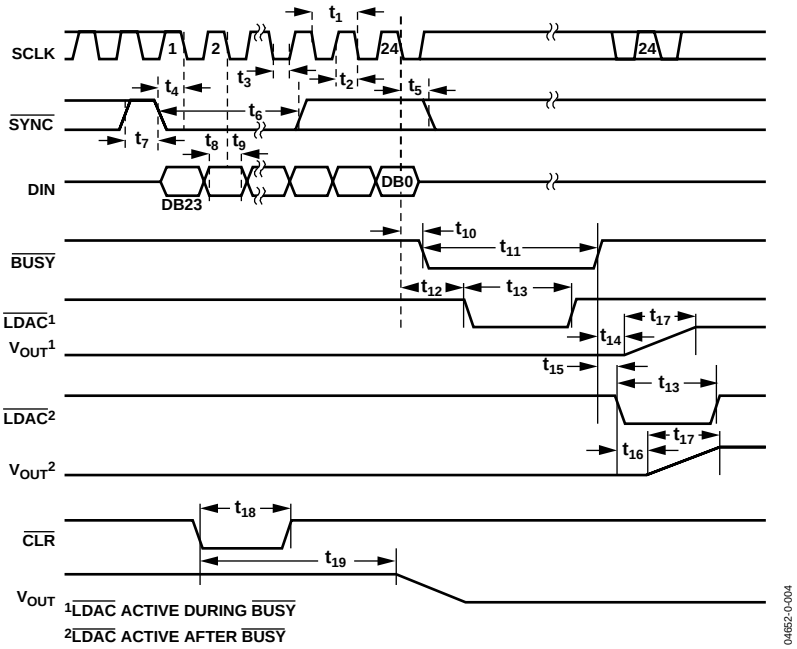

Figure 3. Serial Interface Timing Diagram (Standalone Mode)

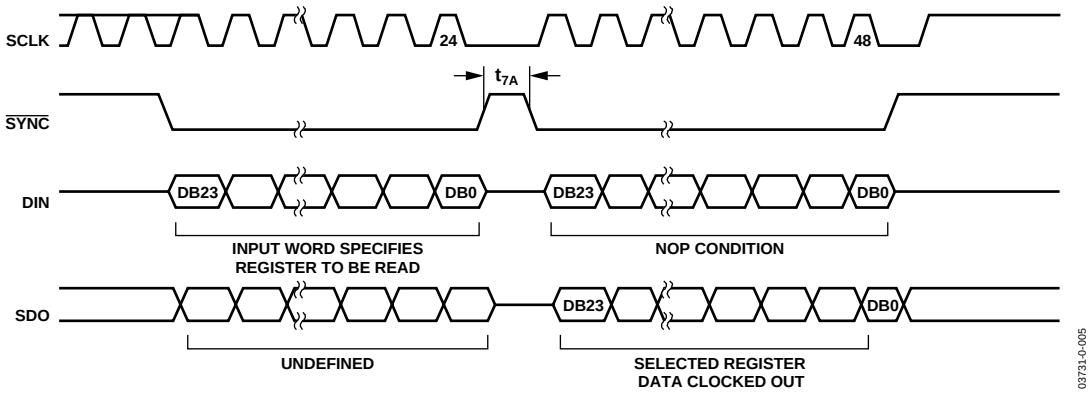

Figure 4. Serial Interface Timing Diagram (Data Readback Mode)

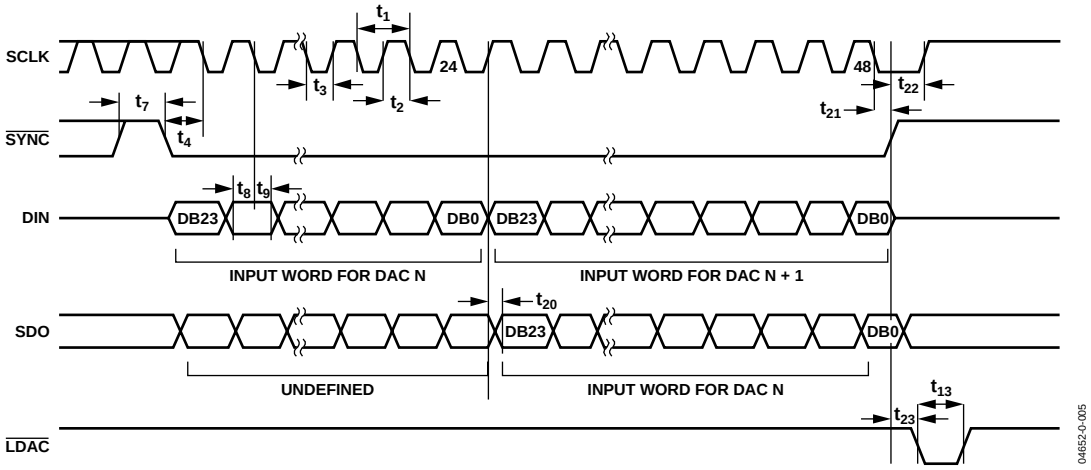

Figure 5. Serial Interface Timing Diagram (Daisy-Chain Mode)

I²C SERIAL INTERFACE

DV_{DD} = 2.7 V to 5.5 V; AV_{DD} = 4.5 V to 5.5 V or 2.7 V to 3.6 V; AGND = DGND = 0 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 8.

Parameter[1]	Limit at T_{MIN}, T_{MAX}	Unit	Description
F_{SCL}	400	kHz max	SCL clock frequency
t_1	2.5	µs min	SCL cycle time
t_2	0.6	µs min	t_{HIGH}, SCL high time
t_3	1.3	µs min	t_{LOW}, SCL low time
t_4	0.6	µs min	$t_{HD,STA}$, start/repeated start condition hold time
t_5	100	ns min	$t_{SU,DAT}$, data setup time
t_6[2]	0.9	µs max	$t_{HD,DAT}$, data hold time
	0	µs min	$t_{HD,DAT}$, data hold time
t_7	0.6	µs min	$t_{SU,STA}$, setup time for repeated start
t_8	0.6	µs m0in	$t_{SU,STO}$, stop condition setup time
t_9	1.3	µs min	t_{BUF}, bus free time between a STOP and a START condition
t_{10}	300	ns max	t_R, rise time of SCL and SDA when receiving
	0	ns min	t_R, rise time of SCL and SDA when receiving (CMOS-compatible)
t_{11}	300	ns max	t_F, fall time of SDA when transmitting
	0	ns min	t_F, fall time of SDA when receiving (CMOS-compatible)
	300	ns max	t_F, fall time of SCL and SDA when receiving
	$20 + 0.1C_b$ [3]	ns min	t_F, fall time of SCL and SDA when transmitting
C_b	400	pF max	Capacitive load for each bus line

[1] See Figure 6.
[2] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal) in order to bridge the undefined region of SCL's falling edge.
[3] C_b is the total capacitance, in pF, of one bus line. t_R and t_F are measured between 0.3 DV_{DD} and 0.7 DV_{DD}.

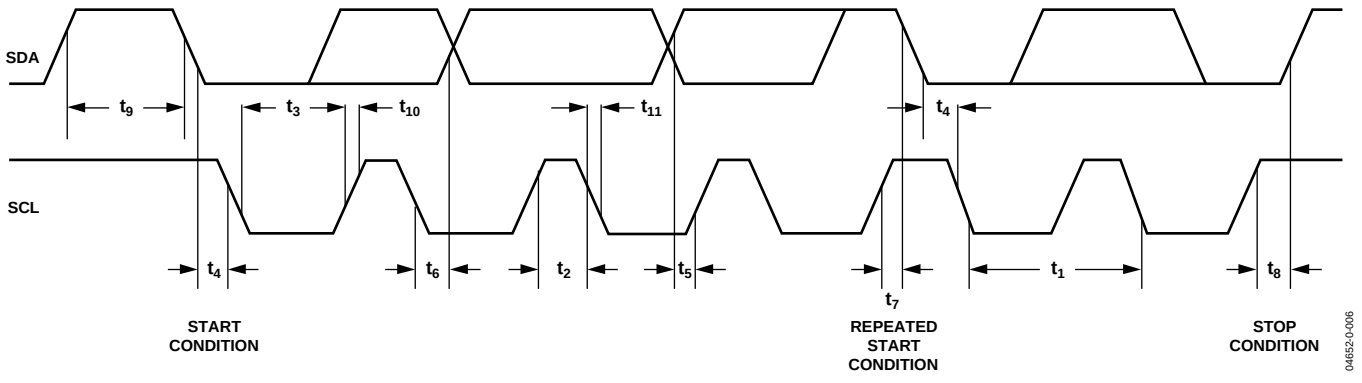

Figure 6. I²C-Compatible Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.[1]

Table 9.

Parameter	Rating
AV_{DD} to AGND	–0.3 V to +7 V
DV_{DD} to DGND	–0.3 V to +7 V
Digital Inputs to DGND	–0.3 V to DV_{DD} + 0.3 V
SDA/SCL to DGND	–0.3 V to + 7 V
Digital Outputs to DGND	–0.3 V to DV_{DD} + 0.3 V
REFIN/REFOUT to AGND	–0.3 V to AV_{DD} + 0.3 V
AGND to DGND	–0.3 V to +0.3 V
VOUTx to AGND	–0.3 V to AV_{DD} + 0.3 V
Analog Inputs to AGND	–0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range	
Commercial (B Version)	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
JunctionTemperature (T_J max)	150°C
100-lead CSPBGA Package	
θ_{JA}Thermal Impedance	40°C/W
Reflow Soldering	
Peak Temperature	230°C

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

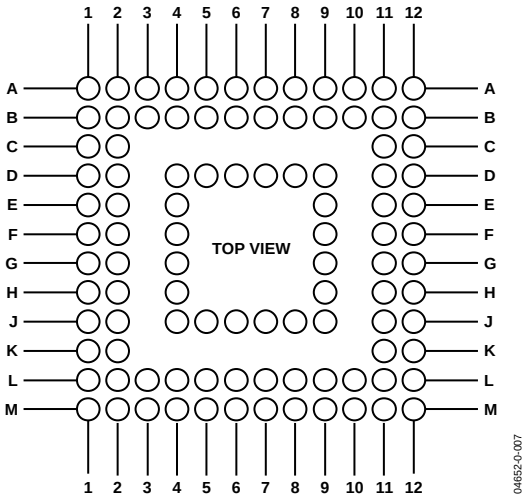

Figure 7. 100-Lead CSPBGA Pin Configuration

Table 10. Pin Number and Name

CSPBGA Number	Ball Name	CSPBGA Number	Ball Name	CSPBGA Number	Ball Name	CSPBGA Number	Ball Name	CSPBGA Number	Ball Name
A1	NC	B9	$\overline{\text{RESET}}$	E4	DACGND4	H11	VOUT13	L5	AGND5
A2	VOUT24	B10	VOUT22	E9	DACGND3	H12	VOUT14	L6	VOUT6
A3	$\overline{\text{CLR}}$	B11	NC	E11	VOUT17	J1	AVDD1	L7	VOUT32
A4	$\overline{\text{SYNC}}$	B12	VOUT23	E12	VOUT19	J2	VOUT30	L8	VOUT34
A5	SCLK	C1	VOUT26	F1	REFGND	J4	DACGND5	L9	VOUT36
A6	DVDD1	C2	SIGNAL GND4	F2	SIGNAL GND1	J5	AGND1	L10	VOUT38
A7	DGND	C11	NC	F4	DACGND1	J6	DACGND2	L11	NC
A8	PD	C12	VOUT21	F9	SIGNAL GND3	J7	DACGND2	L12	VOUT9
A9	DCEN	D1	VOUT27	F11	VOUT16	J8	AGND2	M1	NC
A10	$\overline{\text{LDAC}}$	D2	SIGNAL GND4	F12	VOUT18	J9	SIGNAL GND2	M2	VOUT3
A11	$\overline{\text{BUSY}}$	D4	DACGND4	G1	VOUT28	J11	VOUT12	M3	VOUT4
A12	NC	D5	AGND4	G2	VOUT29	J12	VOUT11	M4	VOUT5
B1	VOUT25	D6	DVDD2	G4	DACGND1	K1	VOUT0	M5	AVDD5
B2	NC	D7	DGND	G9	SIGNAL GND3	K2	VOUT1	M6	VOUT7
B3	DGND	D8	AGND3	G11	VOUT15	K11	NC	M7	VOUT33
B4	DIN	D9	DACGND3	G12	AVDD2	K12	VOUT10	M8	VOUT35
B5	SDO	D11	VOUT20	H1	REFOUT/REFIN	L1	VOUT2	M9	VOUT37
B6	DVDD3	D12	AVDD3	H2	VOUT31	L2	NC	M10	VOUT39/ MON_OUT
B7	DGND	E1	AVDD4	H4	DACGND5	L3	SIGNAL GND5	M11	VOUT8
B8	SPI/$\overline{\text{I}^2\text{C}}$	E2	SIGNAL GND1	H9	SIGNAL GND2	L4	SIGNAL GND5	M12	NC

Table 11. Pin Function Descriptions

Mnemonic	Function
VOUTx	Buffered Analog Outputs for Channel x. Each analog output is driven by a rail-to-rail output amplifier operating at a gain of 2. Each output is capable of driving an output load of 5 kΩ to ground. Typical output impedance is 0.5 Ω.
SIGNAL GND(1–5)	Analog Ground Reference Points for Each Group of Eight Output Channels. All SIGNAL_GND pins are tied together internally and should be connected to the AGND plane as close as possible to the AD5384.
DAC GND(1–5)	Each group of eight channels contains a DAC_GND pin. This is the ground reference point for the internal 14-bit DAC. These pins shound be connected to the AGND plane.
AGND(1–5)	Analog Ground Reference Point. Each group of eight channels contains an AGND pin. All AGND pins should be connected externally to the AGND plane.
AVDD(1–5)	Analog Supply Pins. Each group of eight channels has a separate AVDD pin. These pins are shorted internally and should be decoupled with a 0.1 µF ceramic capacitor and a 10 µF tantalum capacitor. Operating range for the AD5384-5 is 4.5 V to 5.5 V; operating range for the AD5384-3 is 2.7 V to 3.6 V.
DGND	Ground for All Digital Circuitry.
DVDD	Logic Power Supply. Guaranteed operating range is 2.7 V to 5.5 V. It is recommended that these pins be decoupled with 0.1 µF ceramic and 10 µF tantalum capacitors to DGND.
REF GND	Ground Reference Point for the Internal Reference.
REFOUT/REFIN	The AD5384 contains a common REFOUT/REFIN pin. The default for this pin is a reference input. When the internal reference is selected, this pin is the reference output. If the application requires an external reference, it can be applied to this pin. The internal reference is enabled/disabled via the control register.
VOUT39/MON_OUT	This pin has a dual function. It acts a a buffered output for Channel 39 in default mode. But when the monitor function is enabled, this pin acts as the output of a 39-to-1 channel multiplexer that can be programmed to multiplex one of Channels 0 to 38 to the MON_OUT pin. The MON_OUT pin output impedance typically is 500 Ω and is intended to drive a high input impedance like that exhibited by SAR ADC inputs.
$\overline{\text{SYNC}}$/AD0	Serial Interface Mode. This is the frame synchronization input signal for the serial clocks before the addressed register is updated.
	I^2C Mode. This pin acts as a hardware address pin used in conjunction with AD1 to determine the software address for the device on the I^2C bus.
DCEN/ AD1	Multifunction Pin. In serial interface mode, this pin acts as a daisy-chain enable in SPI mode and as a hardware address pin in I^2C mode.
	Serial Interface. Daisy-chain select input (level sensitive, active high). When high, this signal is used in conjunction with SPI/ $\overline{I^2C}$ high to enable the SPI serial interface daisy-chain mode.
	I^2C Mode. This pin acts as a hardware address pin used in conjunction with AD0 to determine the software address for this device on the I^2C bus.
SDO	Serial Data Output in Serial Interface Mode. Three-stateable CMOS output. SDO can be used for daisy-chaining a number of devices together. Data is clocked out on SDO on the rising edge of SCLK, and is valid on the falling edge of SCLK.
	Digital CMOS Output. $\overline{\text{BUSY}}$ goes low during internal calculations of the data (x2) loaded to the DAC data register. During this time, the user can continue writing new data to the x1, c, and m registers, but no further updates to the DAC registers and DAC outputs can take place. If $\overline{\text{LDAC}}$ is taken low while $\overline{\text{BUSY}}$ is low, this event is stored. $\overline{\text{BUSY}}$ also goes low during power-on reset, and when the $\overline{\text{BUSY}}$ pin is low. During this time, the interface is disabled and any events on $\overline{\text{LDAC}}$ are ignored. A $\overline{\text{CLR}}$ operation also brings $\overline{\text{BUSY}}$ low.
$\overline{\text{LDAC}}$	Load DAC Logic Input (Active Low). If $\overline{\text{LDAC}}$ is taken low while $\overline{\text{BUSY}}$ is inactive (high), the contents of the input registers are transferred to the DAC registers, and the DAC outputs are updated. If $\overline{\text{LDAC}}$ is taken low while $\overline{\text{BUSY}}$ is active and internal calculations are taking place, the $\overline{\text{LDAC}}$ event is stored and the DAC registers are updated when $\overline{\text{BUSY}}$ goes inactive. However, any events on $\overline{\text{LDAC}}$ during power-on reset or on $\overline{\text{RESET}}$ are ignored.
$\overline{\text{CLR}}$	Asynchronous Clear Input. The CLR input is falling edge sensitive. When $\overline{\text{CLR}}$ is activated, all channels are updated with the data in the $\overline{\text{CLR}}$ code register. $\overline{\text{BUSY}}$ is low for a duration of 35 µs while all channels are being updated with the $\overline{\text{CLR}}$ code.
$\overline{\text{RESET}}$	Asynchronous Digital Reset Input (Falling Edge Sensitive). The function of this pin is equivalent to that of the power-on reset generator. When this pin is taken low, the state machine initiates a reset sequence to digitally reset the x1, m, c, and x2 registers to their default power-on values. This sequence typically takes 270 µs. The falling edge of $\overline{\text{RESET}}$ initiates the $\overline{\text{RESET}}$ process and $\overline{\text{BUSY}}$ goes low for the duration, returning high when $\overline{\text{RESET}}$ is complete. While $\overline{\text{BUSY}}$ is low, all interfaces are disabled and all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{BUSY}}$ returns high, the part resumes normal operation and the status of the $\overline{\text{RESET}}$ pin is ignored until the next falling edge is detected.

Mnemonic	Function
PD	Power Down (Level Sensitive, Active High). PD is used to place the device in low power mode, where AI_{DD} reduces to 2 µA and DI_{DD} to 20 µA. In power-down mode, all internal analog circuitry is placed in low power mode, and the analog output is configured as a high impedance output or provides a 100 kΩ load to ground, depending on how the power-down mode is configured. The serial interface remains active during power-down.
NC	No Connect. The user is advised not to connect any signals to these pins.
SPI/ $\overline{I^2C}$	This pin acts as serial interface mode select. When this input is high SPI mode is selected. When low, I^2C is selected.
SCLK/SCL	Serial Interface Mode. In serial interface mode, data is clocked into the shift register on the falling edge of SCLK. This operates at clock speeds up to 30 MHz.
	I^2C Mode. In I^2C mode, this pin performs the SCL function, clocking data into the device. The data transfer rate in I^2C mode is compatible with both 100 kHz and 400 kHz operating modes.
DIN/SDA	Serial Interface Mode. In serial interface mode, this pin acts as the serial data input. Data must be valid on the falling edge of SCLK.
	I^2C Mode. In I^2C mode, this pin is the serial data pin (SDA) operating as an open-drain input/output.

TERMINOLOGY

Relative Accuracy

Relative accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero-scale error and full-scale error, and is expressed in LSB.

Differential Nonlinearity

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB maximum ensures monotonicity.

Zero-Scale Error

Zero-scale error is the error in the DAC output voltage when all 0s are loaded into the DAC register. Ideally, with all 0s loaded to the DAC and m = all 1s, c = 2^{n-1}

$$VOUT_{(Zero\text{-}Scale)} = 0\ V$$

Zero-scale error is a measure of the difference between VOUT (actual) and VOUT (ideal), expressed in mV. It is mainly due to offsets in the output amplifier.

Offset Error

Offset error is a measure of the difference between VOUT (actual) and VOUT (ideal) in the linear region of the transfer function, expressed in mV. Offset error is measured on the AD5384-5 with Code 32 loaded into the DAC register, and on the AD5384-3 with Code 64.

Gain Error

Gain Error is specified in the linear region of the output range between V_{OUT} = 10 mV and V_{OUT} = AV_{DD} – 50 mV. It is the deviation in slope of the DAC transfer characteristic from the ideal and is expressed in %FSR with the DAC output unloaded.

DC Crosstalk

This is the dc change in the output level of one DAC at midscale in response to a full-scale code (all 0s to all 1s, and vice versa) and output change of all other DACs. It is expressed in LSB.

DC Output Impedance

This is the effective output source resistance. It is dominated by package lead resistance.

Output Voltage Settling Time

This is the amount of time it takes for the output of a DAC to settle to a specified level for a ¼ to ¾ full-scale input change, and is measured from the $\overline{BUSY}$ rising edge.

Digital-to-Analog Glitch Energy

This is the amount of energy injected into the analog output at the major code transition. It is specified as the area of the glitch in nV-s. It is measured by toggling the DAC register data between 0x1FFF and 0x2000.

DAC-to-DAC Crosstalk

DAC-to-DAC crosstalk is the glitch impulse that appears at the output of one DAC due to both the digital change and the subsequent analog output change at another DAC. The victim channel is loaded with midscale. DAC-to-DAC crosstalk is specified in nV-s.

Digital Crosstalk

Digital crosstalk is the glitch impulse transferred to the output of one converter due to a change in the DAC register code of another converter. It is specified is specified in nV-s.

Digital Feedthrough

When the device is not selected, high frequency logic activity on the device's digital inputs can be capacitively coupled both across and through the device to show up as noise on the VOUT pins. It can also be coupled along the supply and ground lines. This noise is digital feedthrough.

Output Noise Spectral Density

This is a measure of internally generated random noise. Random noise is characterized as a spectral density (voltage per √Hertz). It is measured by loading all DACs to midscale and measuring noise at the output. It is measured in nV/√Hz in a 1 Hz bandwidth at 10 kHz.

TYPICAL PERFORMANCE CHARACTERISTICS

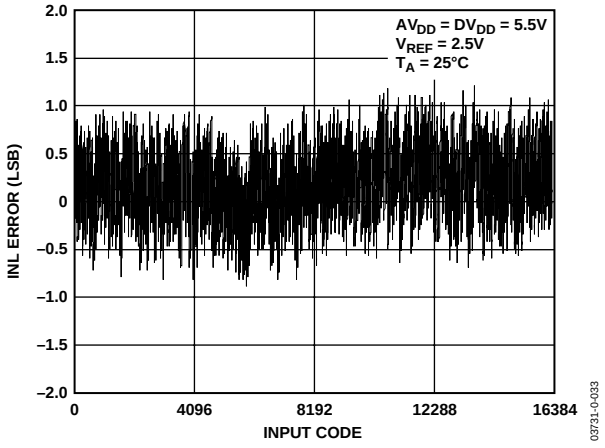

Figure 8. Typical AD5384-5 INL Plot

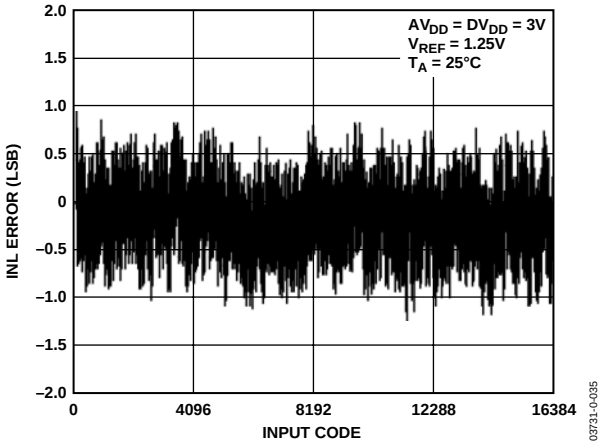

Figure 11. Typical AD5384-3 INL Plot

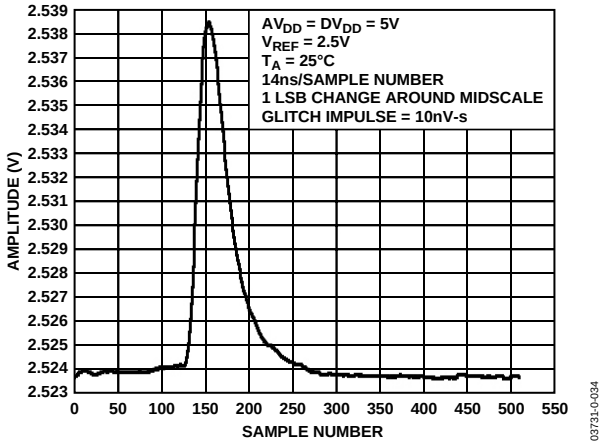

Figure 9. AD5384-5 Glitch Impulse

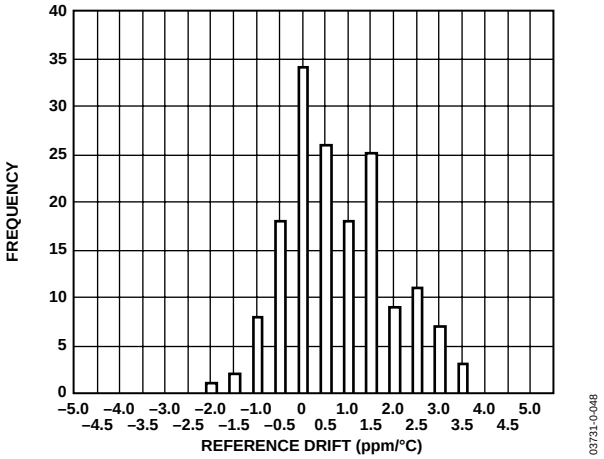

Figure 12. AD5384-REFOUT Temperature Coefficient

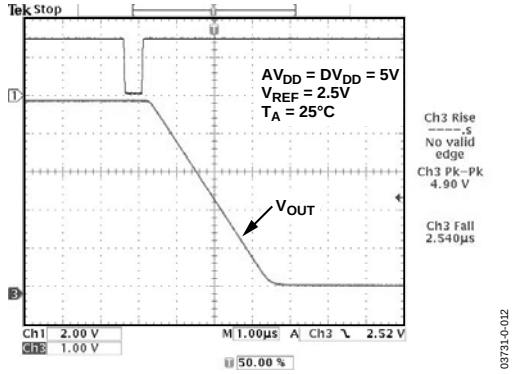

Figure 10. Slew Rate with Boost Off

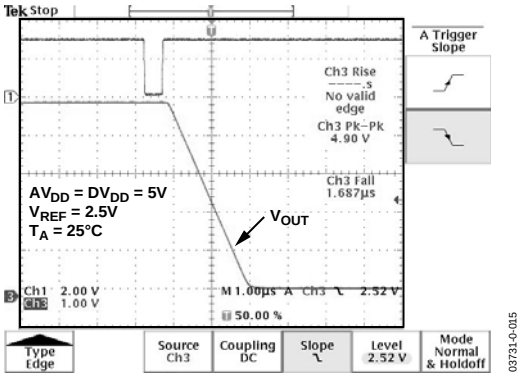

Figure 13. Slew Rate with Boost On

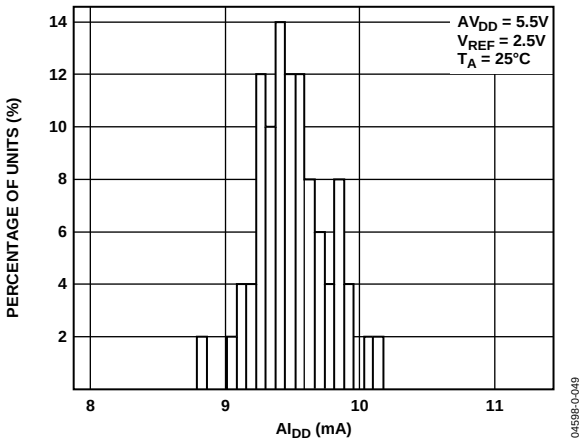

Figure 14. Histogram with Boost Off

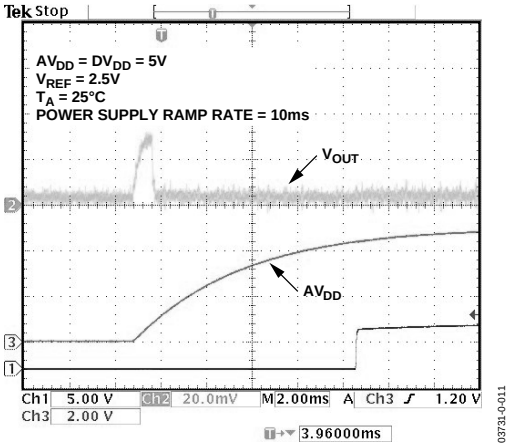

Figure 17. AD5384 Power-Up Transient

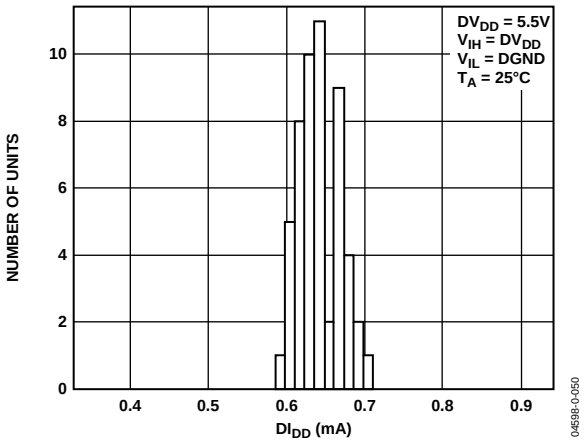

Figure 15. DI_{DD} Histogram

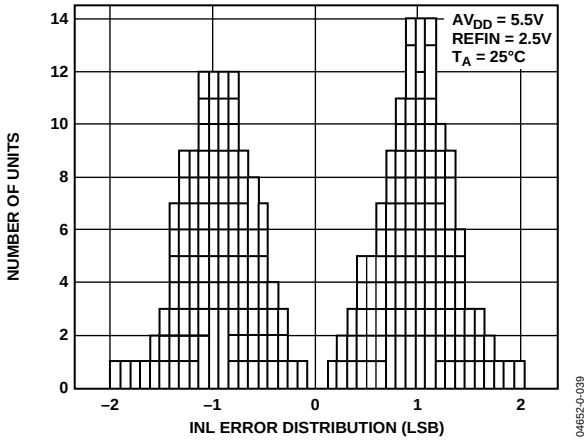

Figure 18. INL Distribution

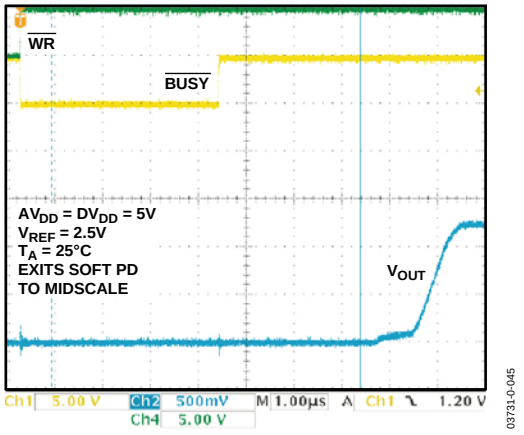

Figure 16. Exiting Soft Power Down

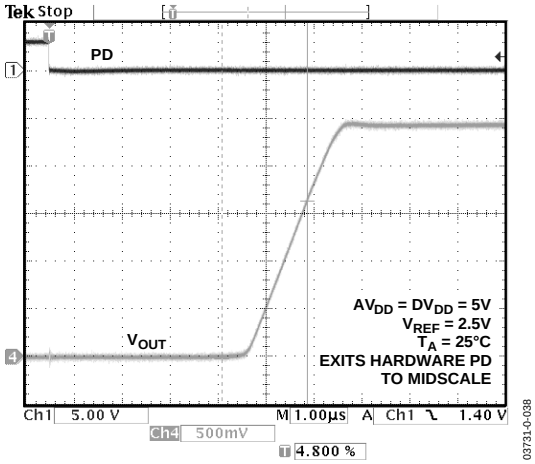

Figure 19. Exiting Hardware Power Down

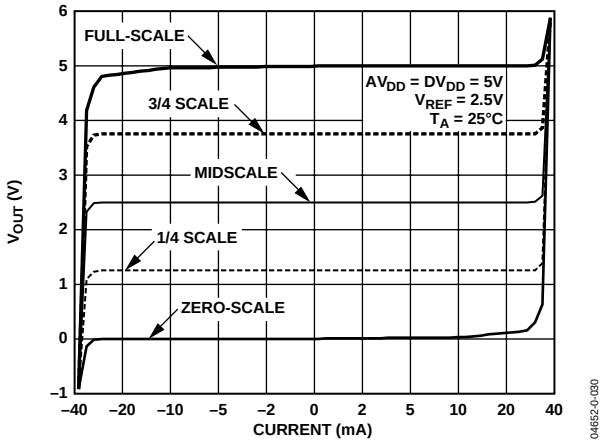

Figure 20. AD5384-5 Output Amplifier Source and Sink Capability

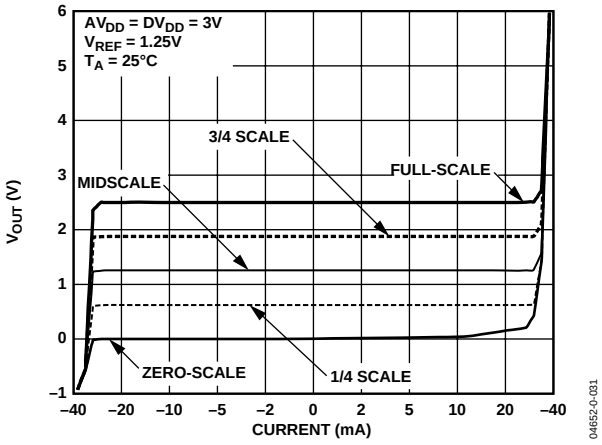

Figure 23. AD5384-3 Output Amplifier Source and Sink Capability

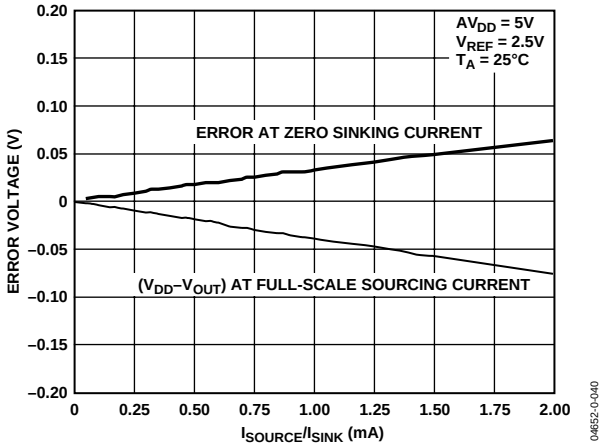

Figure 21. Headroom at Rail vs. Source/Sink Current

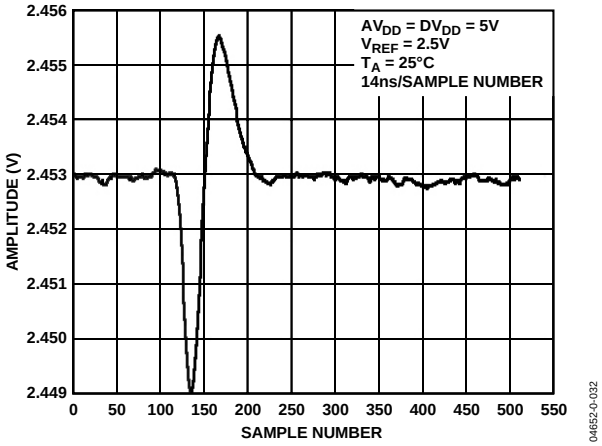

Figure 24. Adjacent Channel DAC to DAC Crosstalk

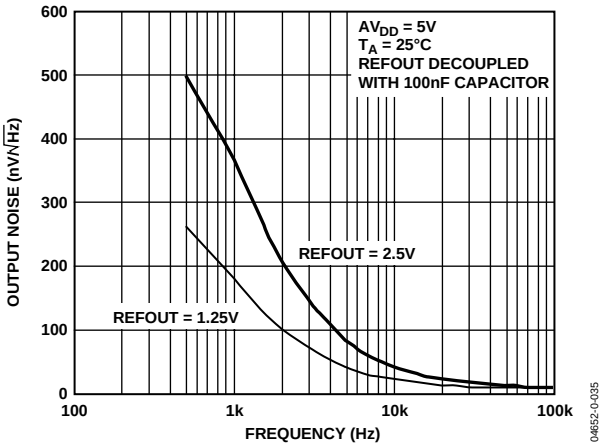

Figure 22. REFOUT Noise Spectral Density

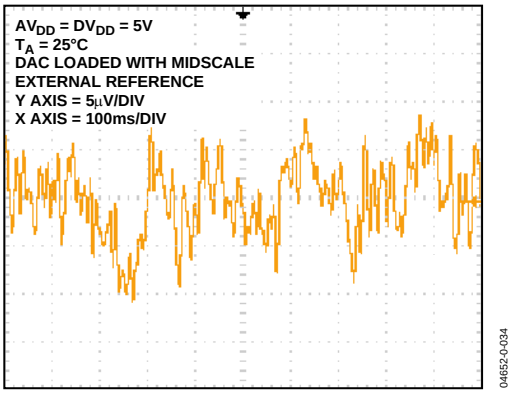

Figure 25. 0.1 Hz to 10 Hz Noise Plot

FUNCTIONAL DESCRIPTION

DAC ARCHITECTURE—GENERAL

The AD5384 is a complete single-supply, 40-channel, voltage output DAC offering 14-bit resolution, available in a 100-lead CSPBGA package. It features two serial interfaces, SPI and I²C. This family includes an internal1.25/2.5 V, 10 ppm/°C reference that can be used to drive the buffered reference inputs. Alternatively, an external reference can be used to drive these inputs. Reference selection is via a bit in the control register. Internal/external reference selection is via the CR10 bit in the control register; CR12 selects the reference magnitude if the internal reference is selected. All channels have an on-chip output amplifier with rail-to-rail output capable of driving 5 kΩ in parallel with a 200 pF load.

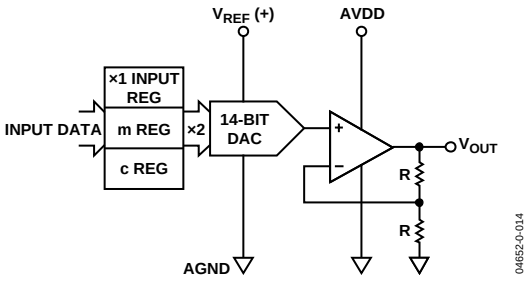

Figure 26. Single-Channel Architecture

The architecture of a single DAC channel consists of a14-bit resistor-string DAC followed by an output buffer amplifier operating at a gain of 2. This resistor-string architecture guarantees DAC monotonicity. The 14-bitbinary digital code loaded to the DAC register determines at which node on the string the voltage is tapped off before being fed to the output amplifier.

Each channel on these devices contains independent offset and gain control registers allowing the user to digitally trim offset and gain. These registers let the user calibrate out errors in the complete signal chain including the DAC using the internal m and c registers which hold the correction factors. All channels are double buffered allowing synchronous updating of all channels using the $\overline{\text{LDAC}}$ pin. Figure 26 shows a block diagram of a single channel on the AD5384. The digital input transfer function for each DAC can be represented as

$$x2 = [(m + 2)/ 2^n \times x1] + (c - 2^{n-1})$$

where:
x2 is the data-word loaded to the resistor string DAC.
x1 is the 14-bit data-word written to the DAC input register.
m is the gain coefficient (default is 0x3FFE on the AD5384). The gain coefficient is written to the 13 most significant bits (DB13 to DB1) and the LSB (DB0) is 0.
n is the DAC resolution (*n* = 14 for AD5384).
c is the14-bit offset coefficient (default is 0x2000).

The complete transfer function for these devices can be represented as

$$V_{OUT} = 2 \times V_{REF} \times x2/2^n$$

where:
x2 is the data-word loaded to the resistor string DAC.
V_{REF} is the internal reference voltage or the reference voltage externally applied to the DAC REFOUT/REFIN pin. For specified performance, an external reference voltage of 2.5 V is recommended for the AD5384-5, and 1.25 V for the AD5384-3.

DATA DECODING

The AD5384 contains a 14-bit data bus, DB13-DB0. Depending on the value of REG1 and REG0 outlined in Table 12, this data is loaded into the addressed DAC input register(s), offset (c) register(s), or gain (m) register(s). The format data, offset (c) and gain (m) register contents are outlined in Table 13, Table 14, and Table 15.

Table 12. Register Selection

REG1	REG0	Register Selected
1	1	Input Data Register (x1)
1	0	Offset Register (c)
0	1	Gain Register (m)
0	0	Special Function Registers (SFRs)

Table 13. DAC Data Format (REG1 = 1, REG0 = 1)

DB13 to DB0				DAC Output (V)
11	1111	1111	1111	2 V_{REF} × (16383/16384)
11	1111	1111	1110	2 V_{REF} × (16382/16384)
10	0000	0000	0001	2 V_{REF} × (8193/16384)
10	0000	0000	0000	2 V_{REF} × (8192/16384)
01	1111	1111	1111	2 V_{REF} × (8191/16384)
00	0000	0000	0001	2 V_{REF} × (1/16384)
00	0000	0000	0000	0

Table 14. Offset Data Format (REG1 = 1, REG0 = 0)

DB13 to DB0				Offset (LSB)
11	1111	1111	1111	+8191
11	1111	1111	1110	+8190
10	0000	0000	0001	+1
10	0000	0000	0000	0
01	1111	1111	1111	–1
00	0000	0000	0001	–8191
00	0000	0000	0000	–8192

Table 15. Gain Data Format (REG1 = 0, REG0 = 1)

DB13 to DB0				Gain Factor
11	1111	1111	1110	1
10	1111	1111	1110	0.75
01	1111	1111	1110	0.5
00	1111	1111	1110	0.25
00	0000	0000	0000	0

ON-CHIP SPECIAL FUNCTION REGISTERS (SFR)

The AD5384 contains a number of special function registers (SFRs), as outlined in Table 16. SFRs are addressed with REG1 = REG0 = 0 and are decoded using Address Bits A5 to A0.

Table 16. SFR Register Functions (REG1 = 0, REG0 = 0)

R/$\overline{W}$	A5	A4	A3	A2	A1	A0	Function
X	0	0	0	0	0	0	NOP (No Operation)
0	0	0	0	0	0	1	Write CLR Code
0	0	0	0	0	1	0	Soft CLR
0	0	0	1	0	0	0	Soft Power-Down
0	0	0	1	0	0	1	Soft Power-Up
0	0	0	1	1	0	0	Control Register Write
1	0	0	1	1	0	0	Control Register Read
0	0	0	1	0	1	0	Monitor Channel
0	0	0	1	1	1	1	Soft Reset

SFR COMMANDS

NOP (No Operation)

REG1 = REG0 = 0, A5–A0 = 000000

Performs no operation but is useful in serial readback mode to clock out data on D_{OUT} for diagnostic purposes. $\overline{BUSY}$ pulses low during a NOP operation.

Write CLR Code

REG1 = REG0 = 0, A5–A0 = 000001
DB13–DB0 = Contain the CLR data

Bringing the $\overline{CLR}$ line low or exercising the soft clear function loads the contents of the DAC registers with the data contained in the user-configurable CLR register, and sets VOUT0 to VOUT39, accordingly. This can be very useful for setting up a specific output voltage in a clear condition. It is also beneficial for calibration purposes; the user can load full scale or zero scale to the clear code register and then issue a hardware or software clear to load this code to all DACs, removing the need for individual writes to each DAC. Default on power-up is all 0s.

Soft CLR

REG1 = REG0 = 0, A5–A0 = 000010
DB13–DB0 = Don't Care

Executing this instruction performs the CLR, which is functionally the same as that provided by the external $\overline{CLR}$ pin. The DAC outputs are loaded with the data in the CLR code register. It takes 35 µs to fully execute the SOFT CLR, as indicated by the $\overline{BUSY}$ low time.

Soft Power-Down

REG1 = REG0 = 0, A5–A0 = 001000
DB13–DB0 = Don't Care

Executing this instruction performs a global power-down that puts all channels into a low power mode that reduces the analog supply current to 2 µA maximum and the digital current to 20 µA maximum. In power-down mode, the output amplifier can be configured as a high impedance output or can provide a 100 kΩ load to ground. The contents of all internal registers are retained in power-down mode. No register can be written to while in power-down.

Soft Power-Up

REG1 = REG0 = 0, A5–A0 = 001001
DB13–DB0 = Don't Care

This instruction is used to power up the output amplifiers and the internal reference. The time to exit power-down is 8 µs. The hardware power-down and software function are internally combined in a digital OR function.

Soft RESET

REG1 = REG0 = 0, A5–A0 = 001111
DB13–DB0 = Don't Care

This instruction is used to implement a software reset. All internal registers are reset to their default values, which correspond to m at full scale and c at zero. The contents of the DAC registers are cleared, setting all analog outputs to 0 V. The soft reset activation time is 135 µs.

Table 17. Control Register Contents

MSB													LSB
CR13	CR12	CR11	CR10	CR9	CR8	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0

Control Register Write/Read

REG1 = REG0 = 0, A5–A0 = 001100, R/$\overline{W}$ status determines if the operation is a write (R/$\overline{W}$ = 0) or a read (R/$\overline{W}$ = 1). DB13 to DB0 contain the control register data.

Control Register Contents

CR13: Power-Down Status. This bit is used to configure the output amplifier state in power-down.

CR13 = 1: Amplifier output is high impedance (default on power-up).

CR13 = 0: Amplifier output is 100 kΩ to ground.

CR12: REF Select. This bit selects the operating internal reference for the AD5384. CR12 is programmed as follows:

CR12 = 1: Internal reference is 2.5 V (AD5384-5 default), the recommended operating reference for AD5384-5.

CR12 = 0: Internal reference is 1.25 V (AD5384-3 default), the recommended operating reference for AD5384-3.

CR11: Current Boost Control. This bit is used to boost the current in the output amplifier, thereby altering its slew rate. This bit is configured as follows:

CR11 = 1: Boost Mode On. This maximizes the bias current in the output amplifier, optimizing its slew rate but increasing the power dissipation.

CR11 = 0: Boost Mode Off (default on power-up). This reduces the bias current in the output amplifier and reduces the overall power consumption.

CR10: Internal/External Reference. This bit determines if the DAC uses its internal reference or an externally applied reference.

CR10 = 1: Internal Reference Enabled. The reference output depends on data loaded to CR12.

CR10 = 0: External Reference Selected (default on power-up).

CR9: Channel Monitor Enable (see Channel Monitor Function).

CR9 = 1: Monitor Enabled. This enables the channel monitor function. After a write to the monitor channel in the SFR register, the selected channel output is routed to the MON_OUT pin. VOUT39 operates as the MON_OUT pin.

CR9 = 0: Monitor Disabled (default on power-up). When the monitor is disabled, the MON_OUT pin assumes its normal DAC output function.

CR8: Thermal Monitor Function. This function is used to monitor the AD5384 internal die temperature, when enabled. The thermal monitor powers down the output amplifiers when the temperature exceeds 130°C. This function can be used to protect the device when power dissipation might be exceeded if a number of output channels are simultaneously short-circuited. A soft power-up re-enables the output amplifiers if the die temperature drops below 130°C.

CR8 = 1: Thermal Monitor Enabled.

CR8 = 0: Thermal Monitor Disabled (default on power-up).

CR7: Don't Care.

CR6 to CR2: Toggle Function Enable. This function allows the user to toggle the output between two codes loaded to the A and B register for each DAC. Control register bits CR6 to CR2 are used to enable individual groups of eight channels for operation in toggle mode. A Logic 1 written to any bit enables a group of channels; a Logic 0 disables a group. $\overline{LDAC}$ is used to toggle between the two registers. Table 18 shows the decoding for toggle mode operation. For example, CR6 controls group w, which contains Channels 32 to 39, CR6 = 1 enables these channels.

CR1 and CR0: Don't Care.

Table 18.

CR Bit	Group	Channels
CR6	4	32–39
CR5	3	24–31
CR4	2	16–23
CR3	1	8–15
CR2	0	0–7

Channel Monitor Function

REG1 = REG0 = 0, A5–A0 = 001010

DB13–DB8 = Contain data to address the monitored channel.

A channel monitor function is provided on the AD5384. This feature, which consists of a multiplexer addressed via the interface, allows any channel output to be routed to the MON_OUT pin for monitoring using an external ADC. In channel monitor mode, VOUT39 becomes the MON_OUT pin, to which all monitored pins are routed. The channel monitor function must be enabled in the control register before any channels are routed to MON_OUT. On the AD5384, DB13 to DB8 contain the channel address for the monitored channel. Selecting Channel Address 63 three-states MON_OUT.

Table 19. AD5384 Channel Monitor Decoding

REG1	REG0	A5	A4	A3	A2	A1	A0	DB13	DB12	DB11	DB10	DB9	DB8	DB7–DB0	MON_OUT
0	0	0	0	1	0	1	0	0	0	0	0	0	0	X	VOUT0
0	0	0	0	1	0	1	0	0	0	0	0	0	1	X	VOUT1
0	0	0	0	1	0	1	0	0	0	0	0	1	0	X	VOUT2
0	0	0	0	1	0	1	0	0	0	0	0	1	1	X	VOUT3
0	0	0	0	1	0	1	0	0	0	0	1	0	0	X	VOUT4
0	0	0	0	1	0	1	0	0	0	0	1	0	1	X	VOUT5
0	0	0	0	1	0	1	0	0	0	0	1	1	0	X	VOUT6
0	0	0	0	1	0	1	0	0	0	0	1	1	1	X	VOUT7
0	0	0	0	1	0	1	0	0	0	1	0	0	0	X	VOUT8
0	0	0	0	1	0	1	0	0	0	1	0	0	1	X	VOUT9
0	0	0	0	1	0	1	0	0	0	1	0	1	0	X	VOUT10
0	0	0	0	1	0	1	0	0	0	1	0	1	1	X	VOUT11
0	0	0	0	1	0	1	0	0	0	1	1	0	0	X	VOUT12
0	0	0	0	1	0	1	0	0	0	1	1	0	1	X	VOUT13
0	0	0	0	1	0	1	0	0	0	1	1	1	0	X	VOUT14
0	0	0	0	1	0	1	0	0	0	1	1	1	1	X	VOUT15
0	0	0	0	1	0	1	0	0	1	0	0	0	0	X	VOUT16
0	0	0	0	1	0	1	0	0	1	0	0	0	1	X	VOUT17
0	0	0	0	1	0	1	0	0	1	0	0	1	0	X	VOUT18
0	0	0	0	1	0	1	0	0	1	0	0	1	1	X	VOUT19
0	0	0	0	1	0	1	0	0	1	0	1	0	0	X	VOUT20
0	0	0	0	1	0	1	0	0	1	0	1	0	1	X	VOUT21
0	0	0	0	1	0	1	0	0	1	0	1	1	0	X	VOUT22
0	0	0	0	1	0	1	0	0	1	0	1	1	1	X	VOUT23
0	0	0	0	1	0	1	0	0	1	1	0	0	0	X	VOUT24
0	0	0	0	1	0	1	0	0	1	1	0	0	1	X	VOUT25
0	0	0	0	1	0	1	0	0	1	1	0	1	0	X	VOUT26
0	0	0	0	1	0	1	0	0	1	1	0	1	1	X	VOUT27
0	0	0	0	1	0	1	0	0	1	1	1	0	0	X	VOUT28
0	0	0	0	1	0	1	0	0	1	1	1	0	1	X	VOUT29
0	0	0	0	1	0	1	0	0	1	1	1	1	0	X	VOUT30
0	0	0	0	1	0	1	0	0	1	1	1	1	1	X	VOUT31
0	0	0	0	1	0	1	0	1	0	0	0	0	0	X	VOUT32
0	0	0	0	1	0	1	0	1	0	0	0	0	1	X	VOUT33
0	0	0	0	1	0	1	0	1	0	0	0	1	0	X	VOUT34
0	0	0	0	1	0	1	0	1	0	0	0	1	1	X	VOUT35
0	0	0	0	1	0	1	0	1	0	0	1	0	0	X	VOUT36
0	0	0	0	1	0	1	0	1	0	1	1	0	1	X	VOUT37
0	0	0	0	1	0	1	0	1	0	0	1	1	0	X	VOUT38
0	0	0	0	1	0	1	0	1	0	0	1	1	1	X	VOUT39
0	0	0	0	1	0	1	0	1	0	1	0	0	0	X	Undefined
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
0	0	0	0	1	0	1	0	1	1	1	1	1	0	X	Undefined
0	0	0	0	1	0	1	0	1	1	1	1	1	1	X	Three-State

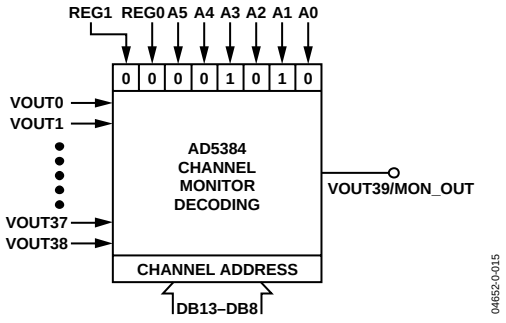

Figure 27. Channel Monitor Decoding

HARDWARE FUNCTIONS

RESET FUNCTION

Bringing the $\overline{\text{RESET}}$ line low resets the contents of all internal registers to their power-on reset state. Reset is a negative edge-sensitive input. The default corresponds to m at full scale and to c at zero. The contents of the DAC registers are cleared, setting VOUT0 to VOUT39 to 0 V. The hardware reset activation time takes 270 µs. The falling edge of $\overline{\text{RESET}}$ initiates the reset process; $\overline{\text{BUSY}}$ goes low for the duration, returning high when $\overline{\text{RESET}}$ is complete. While $\overline{\text{BUSY}}$ is low, all interfaces are disabled and all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{BUSY}}$ returns high, the part resumes normal operation and the status of the $\overline{\text{RESET}}$ pin is ignored until the next falling edge is detected.

ASYNCHRONOUS CLEAR FUNCTION

Bringing the $\overline{\text{CLR}}$ line low clears the contents of the DAC registers to the data contained in the user configurable CLR register and sets VOUT0 to VOUT39 accordingly. This function can be used in system calibration to load zero scale and full scale to all channels. The execution time for a CLR is 35 µs.

$\overline{\text{BUSY}}$ AND $\overline{\text{LDAC}}$ FUNCTIONS

$\overline{\text{BUSY}}$ is a digital CMOS output that indicates the status of the AD5384. The value of x2, the internal data loaded to the DAC data register, is calculated each time the user writes new data to the corresponding x1, c ,or m registers. During the calculation of x2, the $\overline{\text{BUSY}}$ output goes low. While $\overline{\text{BUSY}}$ is low, the user can continue writing new data to the x1, m, or c registers, but no DAC output updates can take place. The DAC outputs are updated by taking the $\overline{\text{LDAC}}$ input low. If $\overline{\text{LDAC}}$ goes low while $\overline{\text{BUSY}}$ is active, the $\overline{\text{LDAC}}$ event is stored and the DAC outputs update immediately after $\overline{\text{BUSY}}$ goes high. The user can hold the $\overline{\text{LDAC}}$ input permanently low, in which case the DAC outputs update immediately after $\overline{\text{BUSY}}$ goes high. $\overline{\text{BUSY}}$ also goes low during power-on reset and when a falling edge is detected on the $\overline{\text{RESET}}$ pin. During this time, all interfaces are disabled and any events on $\overline{\text{LDAC}}$ are ignored. The AD5384 contains an extra feature whereby a DAC register is not updated unless its x2 register has been written to since the last time $\overline{\text{LDAC}}$ was brought low. Normally, when $\overline{\text{LDAC}}$ is brought low, the DAC registers are filled with the contents of the x2 registers. However, the AD5384 updates the DAC register only if the x2 data has changed, thereby removing unnecessary digital crosstalk.

POWER-ON RESET

The AD5384 contains a power-on reset generator and state machine. The power-on reset resets all registers to a predefined state and configures the analog outputs as high impedance. The $\overline{\text{BUSY}}$ pin goes low during the power-on reset sequencing, preventing data writes to the device.

POWER-DOWN

The AD5384 contains a global power-down feature that puts all channels into a low power mode and reduces the analog power consumption to 2 µA maximum and digital power consumption to 20 µA maximum. In power-down mode, the output amplifier can be configured as a high impedance output or it can provide a 100 kΩ load to ground. The contents of all internal registers are retained in power-down mode. When exiting power-down, the settling time of the amplifier elapses before the outputs settles to their correct values.

INTERFACES

The AD5384 contains a serial interface that can be programmed either as DSP-, SPI-, MICROWIRE-, or I²C-compatible. The SPI/$\overline{\text{I2C}}$ pin is used to select DSP, SPI, MICROWIRE, or I²C interface mode. To minimize both the power consumption of the device and the on-chip digital noise, the active interface powers up fully only when the device is being written to, i.e., on the falling edge of $\overline{\text{SYNC}}$.

DSP-, SPI-, MICROWIRE-COMPATIBLE SERIAL INTERFACES

The serial interface can be operated with a minimum of three wires in standalone mode or five wires in daisy-chain mode. Daisy chaining allows many devices to be cascaded together to increase system channel count. The SPI/$\overline{\text{I2C}}$ (Ball B8) should be tied high to enable the DSP-, SPI-, MICROWIRE-compatible serial interface. The serial interface control pins are

$\overline{\text{SYNC}}$, DIN, SCLK—Standard 3-Wire Interface Pins.
DCEN—Selects Standalone Mode or Daisy-Chain Mode.
SDO—Data Out Pin for Daisy-Chain Mode.

Figure 3 and Figure 5 show the timing diagrams for a serial write to the AD5384 in standalone and in daisy-chain modes. The 24-bit data-word format for the serial interface is shown in Table 20.

$\overline{\text{A}}$/B. When toggle mode is enabled, this selects whether the data write is to the A or B register, with Toggle disabled this bit should be set to zero to select the A data register.

R/$\overline{\text{W}}$ is the read or write control bit.

A5–A0 are used to address the input channels.

REG1 and **REG0** select the register to which data is written, as shown in Table 12.

DB13–DB0 contain the input data-word.

X is a don't care condition.

Standalone Mode

By connecting DCEN (daisy-chain enable) pin low, standalone mode is enabled. The serial interface works with both a continuous and a noncontinuous serial clock. The first falling edge of $\overline{\text{SYNC}}$ starts the write cycle and resets a counter that counts the number of serial clocks to ensure that the correct number of bits are shifted into the serial shift register. Any further edges on $\overline{\text{SYNC}}$, except for a falling edge, are ignored until 24 bits are clocked in. Once 24 bits are shifted in, the SCLK is ignored. For another serial transfer to take place, the counter must be reset by the falling edge of $\overline{\text{SYNC}}$.

Table 20. 40-Channel, 14-Bit DAC Serial Input Register Configuration

MSB																							LSB
$\overline{\text{A}}$/B	R/$\overline{\text{W}}$	A5	A4	A3	A2	A1	A0	REG1	REG0	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Daisy-Chain Mode

For systems that contain several devices, the SDO pin can be used to daisy-chain several devices together. This daisy-chain mode can be useful in system diagnostics and in reducing the number of serial interface lines.

By connecting DCEN (daisy-chain enable) pin high, the daisy-chain mode is enabled. The first falling edge of $\overline{\text{SYNC}}$ starts the write cycle. The SCLK is applied continuously to the input shift register when $\overline{\text{SYNC}}$ is low. If more than 24 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting the SDO of the first device to the DIN input on the next device in the chain, a multidevice interface is constructed. 24 clock pulses are required for each device in the system. Therefore, the total number of clock cycles must equal 24N where N is the total number of AD5384 devices in the chain.

When the serial transfer to all devices is complete, $\overline{\text{SYNC}}$ is taken high. This latches the input data in each device in the daisy-chain and prevents any further data being clocked into the input shift register.

If the $\overline{\text{SYNC}}$ is taken high before 24 clocks are clocked into the part, this is considered a bad frame and the data is discarded.

The serial clock may be either a continuous or a gated clock. A continuous SCLK source can be used only if it can be arranged that $\overline{\text{SYNC}}$ is held low for the correct number of clock cycles. In gated clock mode a burst clock containing the exact number of clock cycles must be used and $\overline{\text{SYNC}}$ taken high after the final clock to latch the data.

Readback Mode

Readback mode is invoked by setting the R/$\overline{\text{W}}$ bit = 1 in the serial input register write. With R/$\overline{\text{W}}$ = 1, Bits A5 to A0, in association with Bits REG1 and REG0, select the register to be read. The remaining data bits in the write sequence are don't cares. During the next SPI write, the data appearing on the SDO output contains the data from the previously addressed register. For a read of a single register, the NOP command can be used in clocking out the data from the selected register on SDO. Figure 28 shows the readback sequence.

For example, to read back the m register of Channel 0 on the AD5384, the following sequence should be followed. First, write 0x404XXX to the AD5384 input register. This configures the AD5384 for read mode with the m register of Channel 0 selected. Note that Data Bits DB13 to DB0 are don't cares. Follow this with a second write, a NOP condition, 0x000000. During this write, the data from the m register is clocked out on the SDO line, i.e., data clocked out contains the data from the m register in Bits DB13 to DB0, and the top 10 bits contain the address information as previously written. In readback mode, the $\overline{\text{SYNC}}$ signal must frame the data. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of the SCLK signal. If the SCLK idles high between the write and read operations of a readback operation, the first bit of data is clocked out on the falling edge of $\overline{\text{SYNC}}$.

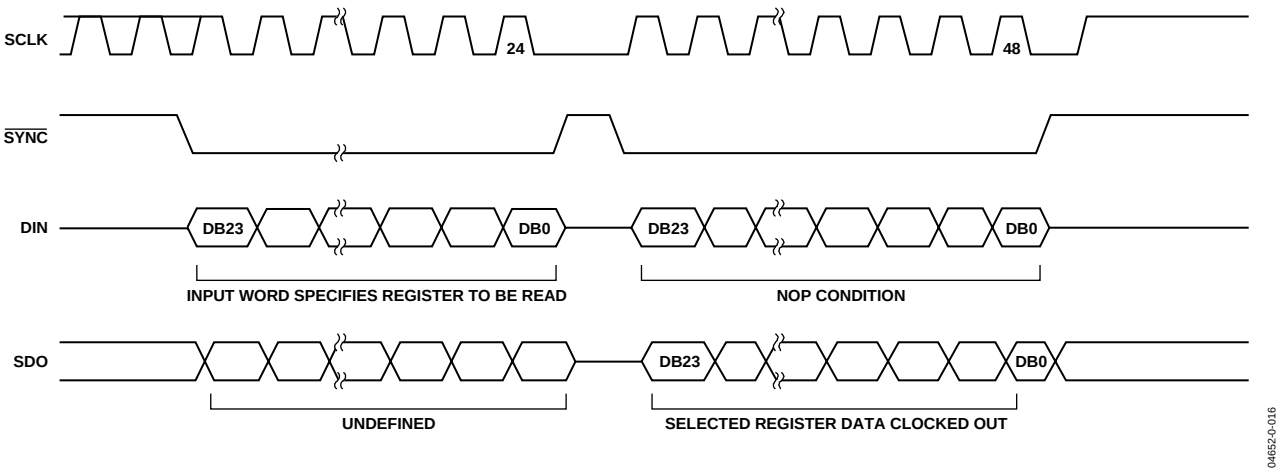

Figure 28. Serial Readback Operation

I²C SERIAL INTERFACE

The AD5384 features an I²C-compatible 2-wire interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the AD5384 and the master at rates up to 400 kHz. Figure 6 shows the 2-wire interface timing diagrams that incorporate three different modes of operation.

Select I²C mode by configuring the SPI/$\overline{\text{I2C}}$ pin to a Logic 0. The device is connected to this bus as slave devices, i.e., no clock is generated by the AD5384. The AD5384 has a 7-bit slave address 1010 1(AD1)(AD0). The 5 MSBs are hard coded, and the two LSBs are determined by the state of the AD1 AD0 pins. The ability to hardware-configure AD1 and AD0 allows four of these devices to be configured on the bus.

I²C Data Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are control signals, which configure start and stop conditions. Both SDA and SCL are pulled high by the external pull-up resistors when the I²C bus is not busy.

Start and Stop Conditions

A master device initiates communication by issuing a start condition. A start condition is a high-to-low transition on SDA with SCL high. A stop condition is a low-to-high transition on SDA while SCL is high. A start condition from the master signals the beginning of a transmission to the AD5384. The stop condition frees the bus. If a repeated start condition (Sr) is generated instead of a stop condition, the bus remains active.

Repeated START Conditions

A repeated start (Sr) condition may indicate a change of data direction on the bus. Sr may be used when the bus master is writing to several I²C devices and wants to maintain control of the bus.

Acknowledge Bit (ACK)

The acknowledge bit (ACK) is the ninth bit attached to any 8-bit data-word. ACK is always generated by the receiving device. The AD5384 devices generate an ACK when receiving an address or data by pulling SDA low during the ninth clock period. Monitoring ACK allows detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault occurs. In the event of an unsuccessful data transfer, the bus master should re-attempt communication.

Slave Addresses

A bus master initiates communication with a slave device by issuing a start condition followed by the 7-bit slave address. When idle, the AD5384 waits for a start condition followed by its slave address. The LSB of the address word is the Read/Write (R/$\overline{\text{W}}$) bit. The AD5384 devices are receive-only devices; when communicating with these, R/$\overline{\text{W}}$ = 0. After receiving the proper address 1010 1(AD1)(AD0), the AD5384 issues an ACK by pulling SDA low for one clock cycle.

The AD5384 has four different user programmable addresses determined by the AD1 and AD0 bits.

Write Operation

There are three specific modes in which data can be written to the AD5384 family of DACs.

4-Byte Mode

When writing to the AD5384 DACs, the user must begin with an address byte (R/$\overline{\text{W}}$ = 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. The address byte is followed by the pointer byte; this addresses the specific channel in the DAC to be addressed and also is acknowledged by the DAC. Two bytes of data are then written to the DAC, as shown in Figure 29. A stop condition follows. This lets the user update a single channel within the AD5384 at any time and requires four bytes of data to be transferred from the master.

3-Byte Mode

In 3-byte mode, the user can update more than one channel in a write sequence without having to write the device address byte each time. The device address byte is required only once; subsequent channel updates require the pointer byte and the data bytes. In 3-byte mode, the user begins with an address byte (R/$\overline{\text{W}}$ = 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. The address byte is followed by the pointer byte. This addresses the specific channel in the DAC to be addressed and also is acknowledged by the DAC. This is then followed by the two data bytes, REG1 and REG0, which determine the register to be updated.

If a stop condition does not follow the data bytes, another channel can be updated by sending a new pointer byte followed by the data bytes. This mode requires only three bytes to be sent to update any channel once the device is initially addressed, and reduces the software overhead in updating the AD5384 channels. A stop condition at any time exits this mode. Figure 30 shows a typical configuration.

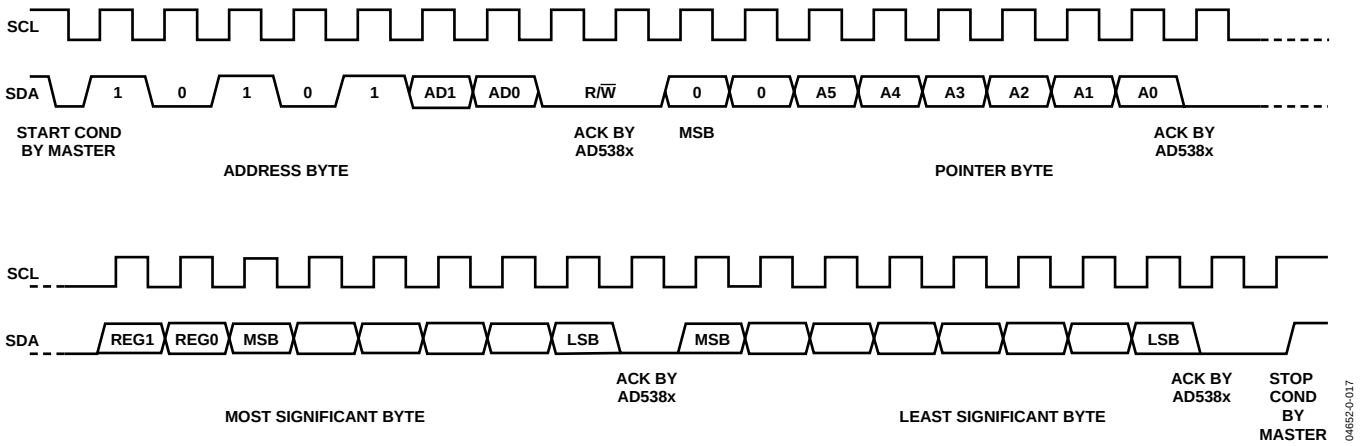

Figure 29. 4-Byte AD5384, I²C Write Operation

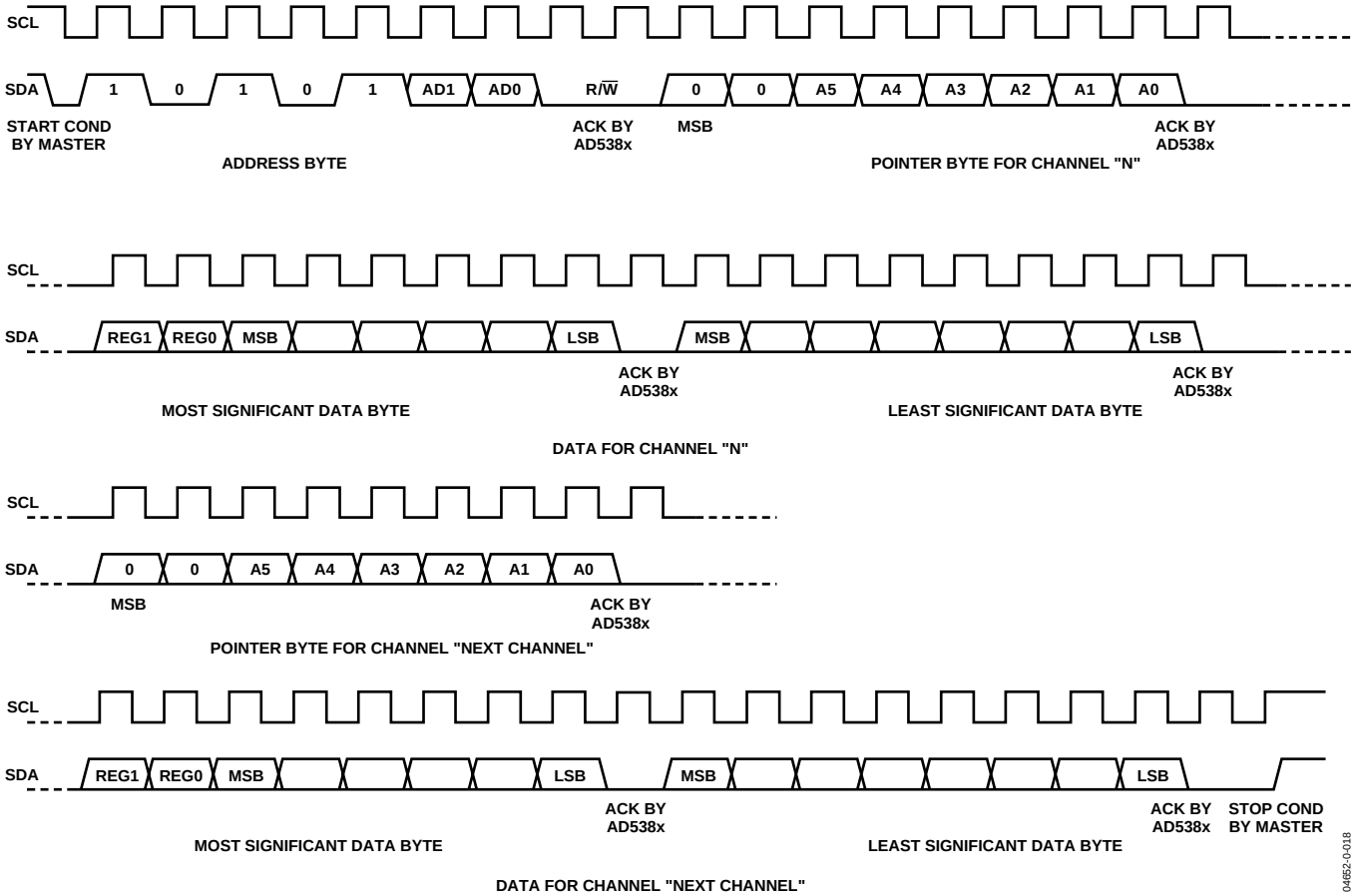

Figure 30. 3-Byte AD5384, I²C Write Operation

2-Byte Mode

Following initialization of 2-byte mode, the user can update channels sequentially. The device address byte is required only once, and the pointer address pointer is configured for auto-increment or burst mode.

The user must begin with an address byte ($R/\overline{W} = 0$), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. The address byte is followed by a specific pointer byte (0xFF) that initiates the burst mode of operation. The address pointer initializes to Channel 0,and, upon receiving the two data bytes for the present address, automatically increments to the next address.

The REG0 and REG1 bits in the data byte determine which register is updated. In this mode, following the initialization, only the two data bytes are required to update a channel. The channel address automatically increments from Address 0. This mode allows transmission of data to all channels in one block and reduces the software overhead in configuring all channels. A stop condition at any time exits this mode. Toggle mode is not supported in 2-byte mode. Figure 31 shows a typical configuration.

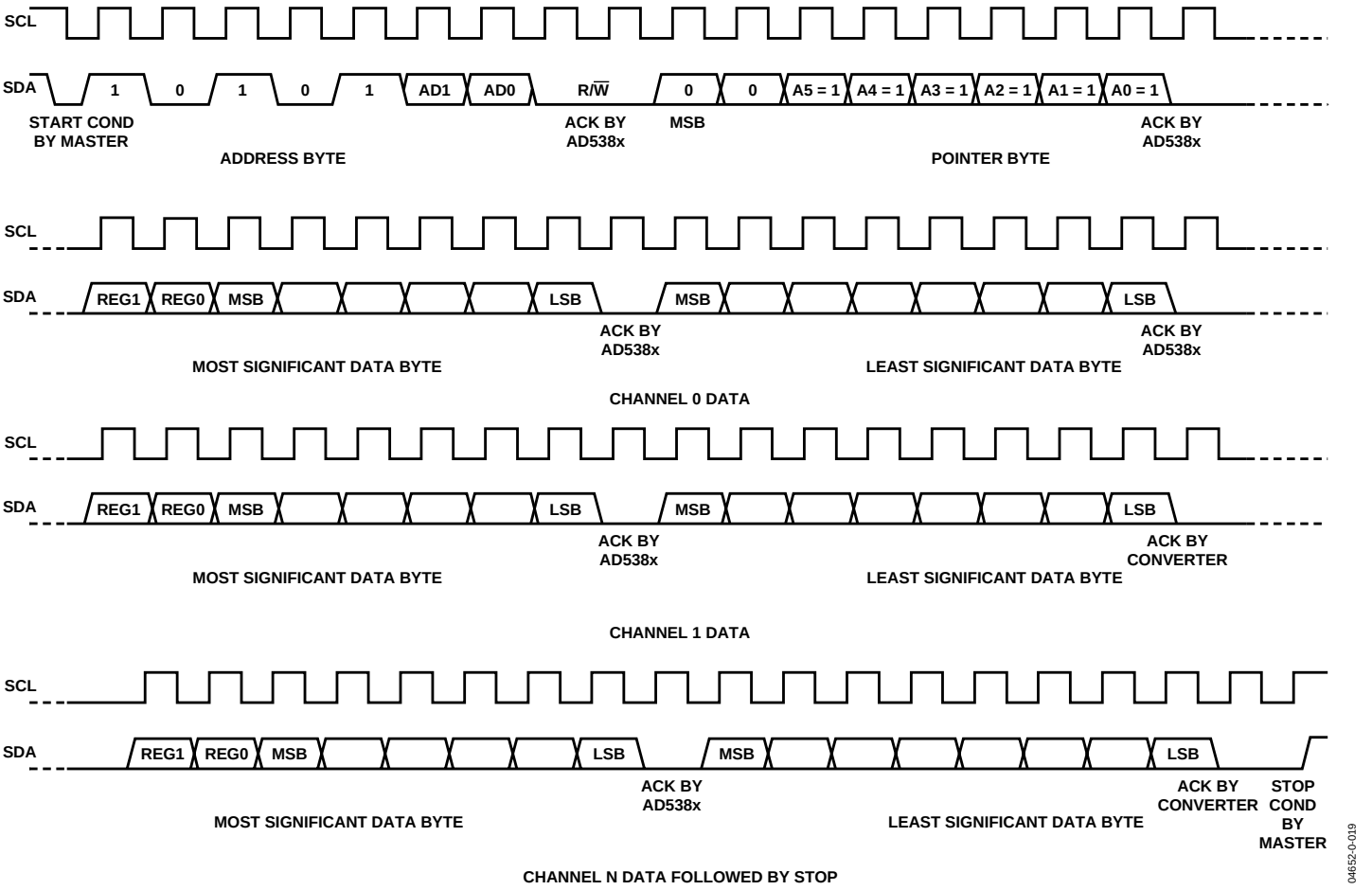

Figure 31. 2-Byte, I^2C Write Operation

MICROPROCESSOR INTERFACING

AD5384 to MC68HC11

The serial peripheral interface (SPI) on the MC68HC11 is configured for master mode (MSTR = 1), the Clock Polarity bit (CPOL) = 0, and the Clock Phase bit (CPHA) = 1. The SPI is configured by writing to the SPI control register (SPCR)—see the 68HC11 User Manual. SCK of the 68HC11 drives the SCLK of the AD5384, the MOSI output drives the serial data line (D_{IN}) of the AD5384, and the MISO input is driven from D_{OUT}.

The $\overline{SYNC}$ signal is derived from a port line (PC7). When data is being transmitted to the AD5384, the SYNC line is taken low (PC7). Data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle.

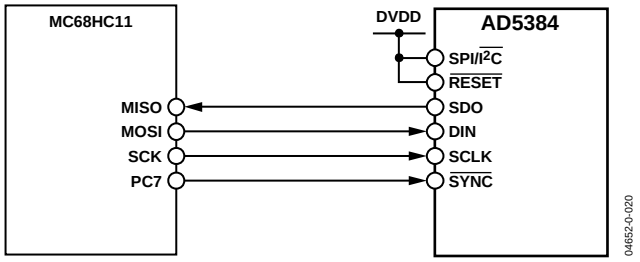

Figure 32. AD5384-toMC68HC11 Interface

AD5384 to PIC16C6x/7x

The PIC16C6x/7x synchronous serial port (SSP) is configured as an SPI master with the Clock Polarity bit = 0. This is done by writing to the synchronous serial port control register (SSPCON). See the PIC16/17 Microcontroller User Manual. In this example I/O, port RA1 is being used to pulse $\overline{SYNC}$ and enable the serial port of the AD5384. This microcontroller transfers only eight bits of data during each serial transfer operation; therefore, three consecutive read/write operations could be needed, depending on the mode. Figure 33 shows the connection diagram.

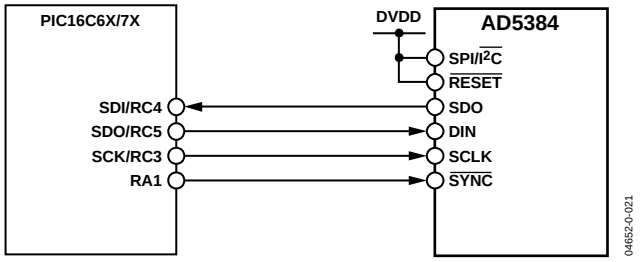

Figure 33. AD5384-to-PIC16C6x/7x Interface

AD5384 to 8051

The AD5384 requires a clock synchronized to the serial data. The 8051 serial interface must therefore be operated in Mode 0. In this mode, serial data enters and exits through RxD, and a shift clock is output on TxD. Figure 34 shows how the 8051 is connected to the AD5384. Because the AD5384 shifts data out on the rising edge of the shift clock and latches data in on the falling edge, the shift clock must be inverted. The AD5384 requires its data to be MSB first. Since the 8051 outputs the LSB first, the transmit routine must take this into account.

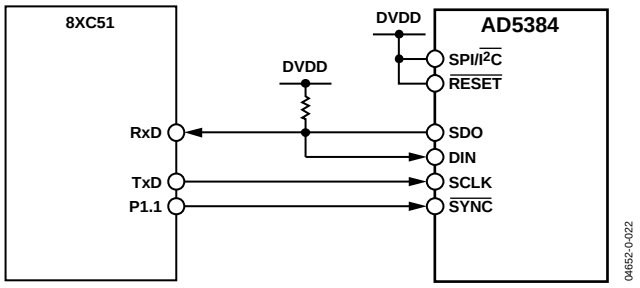

Figure 34. AD5384-to-8051 Interface

AD5384 to ADSP-2101/ADSP-2103

Figure 35 shows a serial interface between the AD5384 and the ADSP-2101/ADSP-2103. The ADSP-2101/ADSP-2103 should be set up to operate in SPORT transmit alternate framing mode. The ADSP-2101/ADSP-2103 SPORT is programmed through the SPORT control register and should be configured as follows: internal clock operation, active low framing, and 16-bit word length. Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled.

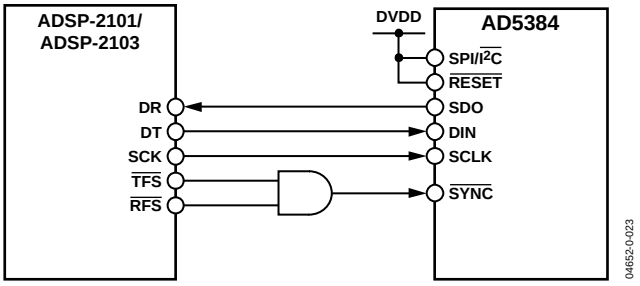

Figure 35. AD5384-to-ADSP-2101/ADSP-2103 Interface

APPLICATION INFORMATION

POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5384 is mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5384 is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only, a star ground point established as close to the device as possible.

For supplies with multiple pins (AV_{DD}, AV_{CC}), these pins should be tied together. The AD5384 should have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply, located as close to the package as possible and ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low effective series resistance (ESR) and effective series inductance (ESI), like the common ceramic types that provide a low impedance path to ground at high frequencies, to handle transient currents due to internal logic switching.

The power supply lines of the AD5384 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals, such as clocks, should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs. A ground line routed between the D_{IN} and SCLK lines helps to reduce crosstalk between them (this is not required on a multilayer board because there is a separate ground plane, but separating the lines helps). It is essential to minimize noise on the V_{IN} and REFIN lines.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane while signal traces are placed on the solder side.

MONITOR FUNCTION

The AD5384 contains a channel monitor function that consists of a multiplexer addressed via the interface, allowing any channel output to be routed to this pin for monitoring using an external ADC. In channel monitor mode, VOUT39 becomes the MON_OUT pin, to which all monitored signals are routed. The channel monitor function must be enabled in the control register before any channels are routed to MON_OUT. contains the decoding information required to route any channel to MON_OUT. Selecting Channel Address 63 three-states MON_OUT. Figure 36 shows a typical monitoring circuit implemented using a 12-bit SAR ADC in a 6-lead SOT package. The controller output port selects the channel to be monitored, and the input port reads the converted data from the ADC.

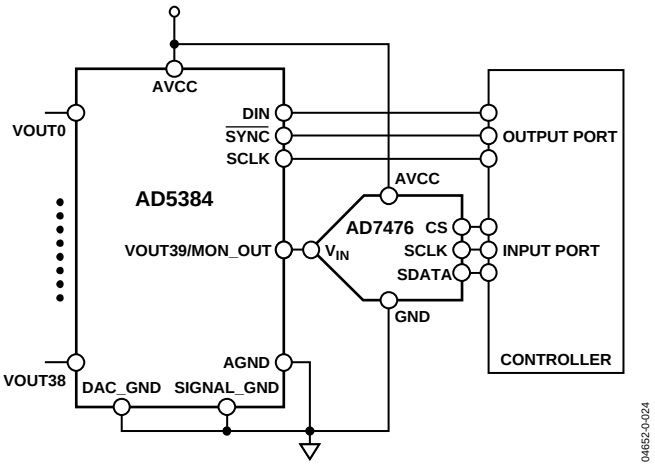

Figure 36. Typical Channel Monitoring Circuit

TOGGLE MODE FUNCTION

The toggle mode function allows an output signal to be generated using the $\overline{\text{LDAC}}$ control signal, which switches between two DAC data registers. This function is configured using the SFR control register as follows. A write with REG1 = REG0 = 0 and A5–A0 = 001100 specifies a control register write. The toggle mode function is enabled in groups of eight channels using Bits CR6 to CR2 in the control register (see Table 17). Figure 37 shows a block diagram of toggle mode implementation.

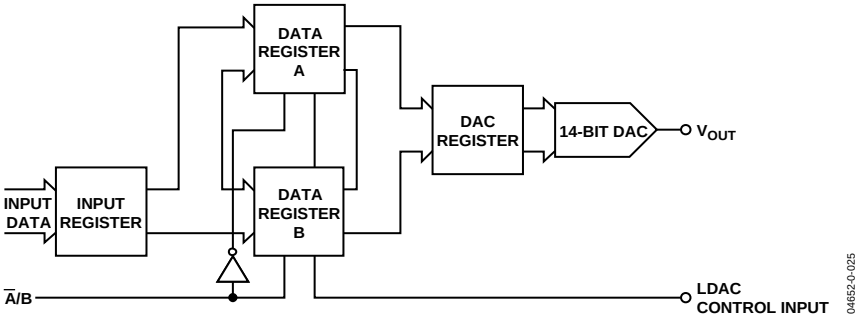

Figure 37. Toggle Mode Function

Each of the 40 DAC channels on the AD5384 contains an A and B data register. Note that the B registers can be loaded only when toggle mode is enabled. The sequence of events when configuring the AD5384 for toggle mode is

1. Enable toggle mode for the required channels via the control register.
2. Load data to A registers.
3. Load data to B registers.
4. Apply $\overline{\text{LDAC}}$.

The $\overline{\text{LDAC}}$ is used to switch between the A and B registers in determining the analog output. The first $\overline{\text{LDAC}}$ configures the output to reflect the data in the A registers. This mode offers significant advantages if the user wants to generate a square wave at the output of all 40 channels, as might be required to drive a liquid crystal-based variable optical attenuator. In this case, the user writes to the control register and enables the toggle function by setting CR6 to CR2 = 1, thus enabling the five groups of eight for toggle mode operation. The user must then load data to all 40 A and B registers. Toggling $\overline{\text{LDAC}}$ sets the output values to reflect the data in the A and B registers. The frequency of the $\overline{\text{LDAC}}$ determines the frequency of the square wave output.

Toggle mode is disabled via the control register. The first $\overline{\text{LDAC}}$ following the disabling of the toggle mode updates the outputs with the data contained in the A registers.

THERMAL MONITOR FUNCTION

The AD5384 contains a temperature shutdown function to protect the chip if multiple outputs are shorted. The short-circuit current of each output amplifier is typically 40 mA. Operating the AD5384 at 5 V leads to a power dissipation of 200 mW per shorted amplifier. With five channels shorted, this leads to an extra watt of power dissipation. For the 100-lead CSPBGA, the θ_{JA} is typically 44°C/W.

The thermal monitor is enabled by the user via CR8 in the control register. The output amplifiers on the AD5384 are automatically powered down if the die temperature exceeds approximately 130°C. After a thermal shutdown has occurred, the user can re-enable the part by executing a soft power-up if the temperature drops below 130°C, or by turning off the thermal monitor function via the control register.

AD5384 IN A MEMS-BASED OPTICAL SWITCH

In their feed-forward control paths, MEMS based optical switches require high resolution DACs that offer high channel density with 14-bit monotonic behavior. The 40-channel, 14-bit AD5384 DAC satisfies these requirements. In the circuit in Figure 38, the 0 V to 5 V outputs of the AD5384 are amplified to achieve an output range of 0 V to 200 V, which is used to control actuators that determine the position of MEMS mirrors in an optical switch. The exact position of each mirror is measured using sensors. The sensor outputs are multiplexed into a high resolution ADC in determining the mirror position. The control loop is closed and driven by an ADSP-21065L, a 32-bit SHARC® DSP with an SPI-compatible SPORT interface. The ADSP-21065L writes data to the DAC, controls the multiplexer, and reads data from the ADC via the serial interface.

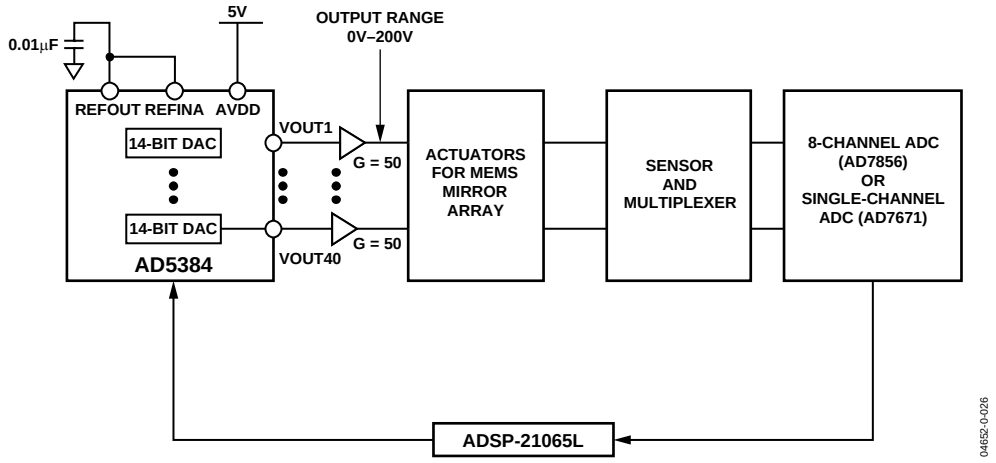

Figure 38. AD5384 in a MEMS-Based Optical Switch

OPTICAL ATTENUATORS

Based on its high channel count, high resolution, monotonic behavior, and high level of integration, the AD5384 is ideally targeted at optical attenuation applications used in dynamic gain equalizers, variable optical attenuators (VOA), and optical add-drop multiplexers (OADMs). In these applications, each wavelength is individually extracted using an arrayed wave guide; its power is monitored using a photodiode, transimpedance amplifier, and an ADC in a closed-loop control system.

The AD5384 controls the optical attenuator for each wavelength, ensuring that the power is equalized in all wavelengths before being multiplexed onto the fiber. This prevents information loss and saturation from occurring at amplification stages further along the fiber.

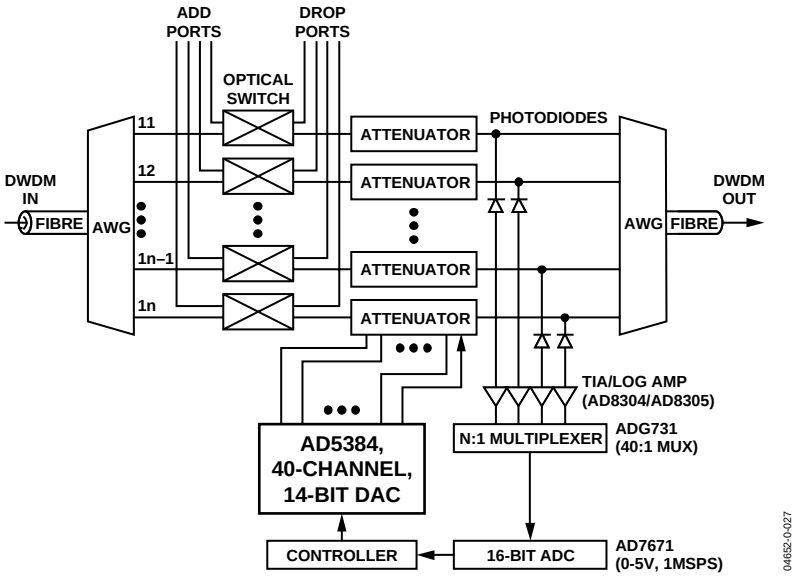

Figure 39. OADM Using the AD5384 as Part of an Optical Attenuator

OUTLINE DIMENSIONS

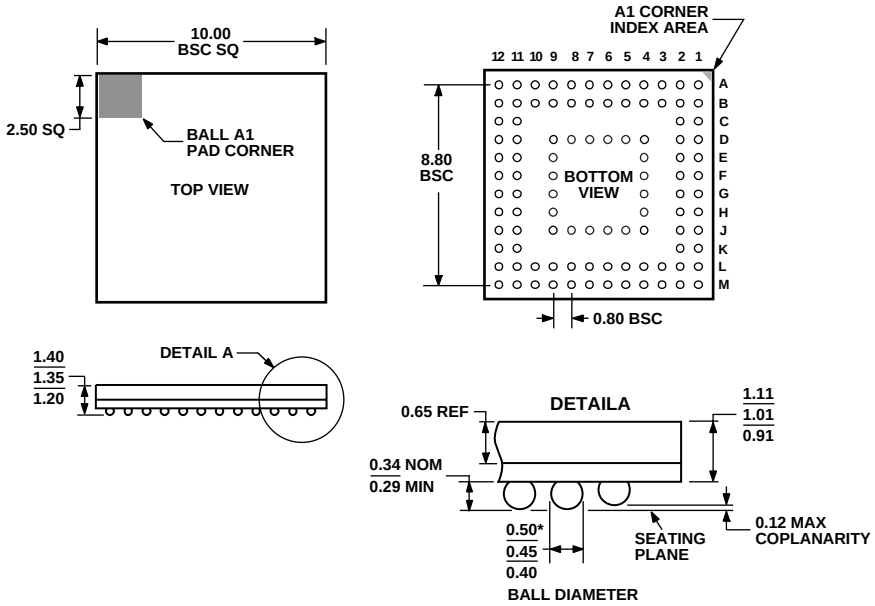

Figure 40. 100-Lead Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-100-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Resolution	Temperature Range	AV_{DD} Range	Output Channels	Linearity Error (LSB)	Package Description	Package Option
AD5384BBC-5	14 Bits	–40°C to +85°C	4.5 V to 5.5 V	40	±4	100-Lead CSPBGA	BC-100-2
AD5384BBC-5REEL7	14 Bits	–40°C to +85°C	4.5 V to 5.5 V	40	±4	100-Lead CSPBGA	BC-100-2
AD5384BBC-3	14 Bits	–40°C to +85°C	2.7 V to 3.6 V	40	±4	100-Lead CSPBGA	BC-100-2
AD5384BBC-3REEL7	14 Bits	–40°C to +85°C	2.7 V to 3.6 V	40	±4	100-Lead CSPBGA	BC-100-2

NOTES

D04652–0–10/04(A)