MA31750 - Pipelining Instructions On The MA31750

Application Note

Replaces July 2000 version, AN4058-2.0

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When analysing the behaviour of the MA31750, the pipelining of instructions must be considered.

1.0 PIPELINING INSTRUCTIONS

Instructions are pre-fetched from system memory and are stored in the pipeline of the processor. They are then pulled from the pipeline to be executed. Whilst the instructions are being executed, the pipeline has emptied and the pre-fetch of the next instruction can take place. This pre-fetch is limited to times when the system address and data busses are free as it utilises these busses to access the system memory. See Figure 1.

2.0 PIPELINING ON THE MA31750

The pipeline on the MA31750 always holds 2 16-bit words. If the instruction being executed is a single word instruction, then only one word has been removed from the pipeline. The second word in the pipeline moves up to the first position and one extra word is pre-fetched from system memory. If the instruction being executed is a double word instruction, then the pipeline has emptied and two pre-fetches are necessary to fill it up again.

Occasionally the pipeline needs emptying and reloading, eg. after initialisation or after an interrupt service routine or if a branch or jump is executed. This will take 2 machine cycles dedicated to pre-fetching the new pipeline. Execution can then resume.

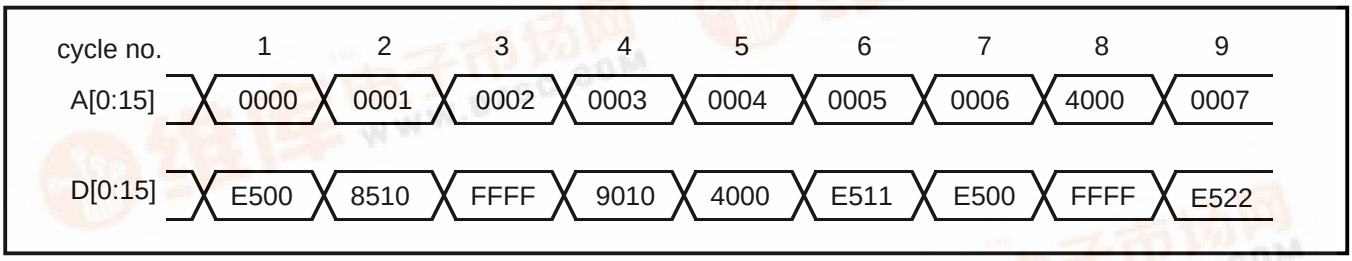

Figure 1: Example of Operation

3.0 EXAMPLE

Figure 1 shows the address and data busses for the following code:

```
0000    E500:       XORR R0,    R0
0001    8510 FFFF:  LIM  R1,    FFFF
0003    9010 4000:  ST   R1,    4000
0005    E511:       XORR R1,    R1
0006    E500:       XORR R0,    R0
0007    E522:       XORR R2,    R2
```

Cycles 1 and 2 are used to fill the pipeline. No instruction execution occurs.

On cycle 3, the XORR instruction is taken from the pipeline and the registers are exor'ed internally. At the same time, the data from address 0002 is loaded into the pipeline.

The next instruction in the pipeline is a double word instruction, therefore cycles 4 and 5 are both needed to refill the pipeline. Whilst the data from addresses 0004 and 0005 are being pre-fetched, register 1 is loaded across internal busses with data FFFF.

Again, the pipeline contains a double word instruction, so cycles 6 and 7 are both needed to refill the pipeline. However, the store instruction needs to use the external address and data busses. This is done on cycle 8 after the pre-fetches have finished.

Once the store has completed, the next instruction is executed. This is a single word instruction (XORR), hence cycle 9 is used for the pre-fetch, as the exor instruction is executed internally.

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