

## Transistors

# 4V Drive Nch+Pch MOS FET

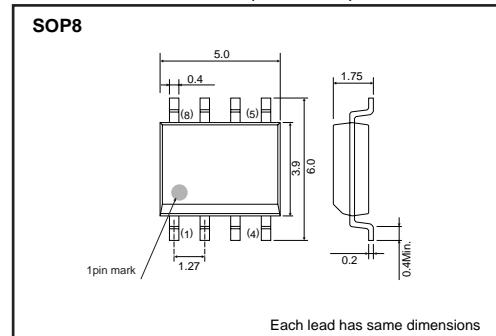
## SP8M24

**●Structure**

Silicon N-channel MOS FET /  
Silicon P-channel MOS FET

**●Features**

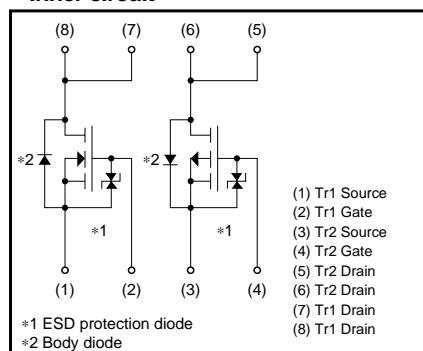
- 1) Low on-resistance.
- 2) Built-in G-S protection diode.
- 3) Small surface mount package (SOP8).

**●External dimensions (Unit : mm)****●Applications**

Switching

**●Packaging specifications**

Type	Package	Taping
Code	TB	
Basic ordering unit (pieces)	2500	
SP8M24	○	

**●Inner circuit****●Absolute maximum ratings (Ta=25°C)**

Parameter	Symbol	Limits		Unit	
		Tr1 : N-ch	Tr2 : P-ch		
Drain-source voltage	V <sub>DSS</sub>	45	-45	V	
Gate-source voltage	V <sub>GSS</sub>	20	-20	V	
Drain current	Continuous	I <sub>D</sub>	±4.5	±3.5	A
	Pulsed	I <sub>DP</sub>	±18	±14	A
Source current (Body diode)	Continuous	I <sub>S</sub>	1.0	-1.0	A
	Pulsed	I <sub>SP</sub>	18	-14	A
Total power dissipation	P <sub>D</sub>	2.0		W / TOTAL	
		1.4		W / ELEMENT	
Channel temperature	T <sub>ch</sub>	150		°C	
Storage temperature	T <sub>stg</sub>	-55 to +150		°C	

\*1 Pw≤10μs, Duty cycle≤1%

\*2 Mounted on a ceramic board.

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**N-ch****●Electrical characteristics (Ta=25°C)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I <sub>GSS</sub>	—	—	10	µA	V <sub>GS</sub> = 20V, V <sub>DS</sub> =0V
Drain-source breakdown voltage	V <sub>(BR) DSS</sub>	45	—	—	V	I <sub>D</sub> = 1mA, V <sub>GS</sub> =0V
Zero gate voltage drain current	I <sub>DSS</sub>	—	—	1	µA	V <sub>DS</sub> = 45V, V <sub>GS</sub> =0V
Gate threshold voltage	V <sub>GS (th)</sub>	1.0	—	2.5	V	V <sub>DS</sub> = 10V, I <sub>D</sub> = 1mA
Static drain-source on-state resistance	R <sub>DS (on)*</sub>	—	33	46	mΩ	I <sub>D</sub> = 4.5A, V <sub>GS</sub> = 10V
		—	41	57	mΩ	I <sub>D</sub> = 4.5A, V <sub>GS</sub> = 4.5V
		—	46	64	mΩ	I <sub>D</sub> = 4.5A, V <sub>GS</sub> = 4V
Forward transfer admittance	Y <sub>fs</sub>   *	3.5	—	—	S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 4.5A
Input capacitance	C <sub>iss</sub>	—	550	—	pF	V <sub>DS</sub> = 10V
Output capacitance	C <sub>oss</sub>	—	140	—	pF	V <sub>GS</sub> = 0V
Reverse transfer capacitance	C <sub>rss</sub>	—	70	—	pF	f=1MHz
Turn-on delay time	t <sub>d (on)*</sub>	—	12	—	ns	V <sub>DD</sub> = 25V I <sub>D</sub> = 2.5A
Rise time	t <sub>r</sub> *	—	18	—	ns	V <sub>GS</sub> = 10V
Turn-off delay time	t <sub>d (off)*</sub>	—	42	—	ns	R <sub>L</sub> = 10Ω
Fall time	t <sub>f</sub> *	—	12	—	ns	R <sub>G</sub> = 10Ω
Total gate charge	Q <sub>g</sub> *	—	6.8	9.6	nC	V <sub>DD</sub> = 25V, V <sub>GS</sub> = 5V
Gate-source charge	Q <sub>gs</sub> *	—	2.0	—	nC	I <sub>D</sub> = 4.5A
Gate-drain charge	Q <sub>gd</sub> *	—	2.9	—	nC	R <sub>L</sub> = 5.6Ω, R <sub>G</sub> = 10Ω

\*Pulsed

**●Body diode characteristics (Source-drain) (Ta=25°C)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V <sub>SD</sub> *	—	—	1.2	V	I <sub>S</sub> = 4.5A, V <sub>GS</sub> =0V

\* Pulsed

## Transistors

**P-ch****●Electrical characteristics (Ta=25°C)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I <sub>GSS</sub>	—	—	-10	μA	V <sub>GS</sub> =-20V, V <sub>DS</sub> =0V
Drain-source breakdown voltage	V <sub>(BR) DSS</sub>	-45	—	—	V	I <sub>D</sub> = -1mA, V <sub>GS</sub> =0V
Zero gate voltage drain current	I <sub>DSS</sub>	—	—	-1	μA	V <sub>DS</sub> = -45V, V <sub>GS</sub> =0V
Gate threshold voltage	V <sub>GS (th)</sub>	-1.0	—	-2.5	V	V <sub>DS</sub> = -10V, I <sub>D</sub> = -1mA
Static drain-source on-state resistance	R <sub>DSS (on)</sub> *	—	45	63	mΩ	I <sub>D</sub> = -3.5A, V <sub>GS</sub> = -10V
		—	60	84	mΩ	I <sub>D</sub> = -3.5A, V <sub>GS</sub> = -4.5V
		—	66	92	mΩ	I <sub>D</sub> = -3.5A, V <sub>GS</sub> = -4V
Forward transfer admittance	Y <sub>fs</sub>   *	4.5	—	—	S	V <sub>DS</sub> = -10V, I <sub>D</sub> = -3.5A
Input capacitance	C <sub>iss</sub>	—	1700	—	pF	V <sub>DS</sub> = -10V
Output capacitance	C <sub>oss</sub>	—	200	—	pF	V <sub>GS</sub> =0V
Reverse transfer capacitance	C <sub>rss</sub>	—	135	—	pF	f=1MHz
Turn-on delay time	t <sub>d (on)</sub> *	—	16	—	ns	V <sub>DD</sub> = -25V I <sub>D</sub> = -2.0A
Rise time	t <sub>r</sub> *	—	17	—	ns	V <sub>GS</sub> = -10V
Turn-off delay time	t <sub>d (off)</sub> *	—	70	—	ns	R <sub>L</sub> =12.5Ω R <sub>G</sub> =10Ω
Fall time	t <sub>f</sub> *	—	14	—	ns	
Total gate charge	Q <sub>g</sub> *	—	13.0	18.2	nC	V <sub>DD</sub> = -25V, V <sub>GS</sub> = -5V
Gate-source charge	Q <sub>gs</sub> *	—	3.6	—	nC	I <sub>D</sub> = -3.5A
Gate-drain charge	Q <sub>gd</sub> *	—	4.7	—	nC	R <sub>L</sub> = 7.1Ω, R <sub>G</sub> = 10Ω

\* Pulsed

**●Body diode characteristics (Source-drain) (Ta=25°C)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V <sub>SD</sub> *	—	—	-1.2	V	I <sub>S</sub> = -3.5A, V <sub>GS</sub> =0V

\* Pulsed

## Appendix

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