4V Drive Nch+Pch MOS FET

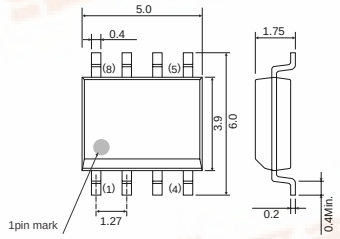
SP8M24

●Structure
Silicon N-channel MOS FET /
Silicon P-channel MOS FET

●Features
1) Low on-resistance.
2) Built-in G-S protection diode.
3) Small surface mount package (SOP8).

●External dimensions (Unit : mm)

SOP8



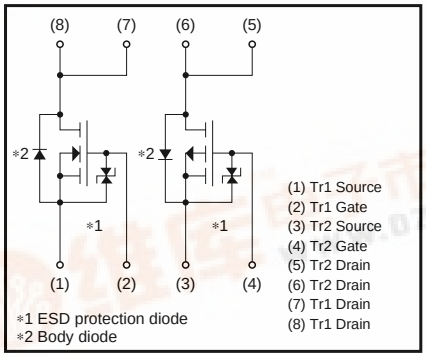
Each lead has same dimensions

●Applications
Switching

●Packaging specifications

Type	Package	Taping
	Code	TB
	Basic ordering unit (pieces)	2500
SP8M24		○

●Inner circuit



●Absolute maximum ratings (Ta=25°C)

Parameter		Symbol	Limits		Unit
			Tr1 : N-ch	Tr2 : P-ch	
Drain-source voltage		V_{DSS}	45	−45	V
Gate-source voltage		V_{GSS}	20	−20	V
Drain current	Continuous	I_D	±4.5	±3.5	A
	Pulsed	I_{DP} ∗1	±18	±14	A
Source current (Body diode)	Continuous	I_S	1.0	−1.0	A
	Pulsed	I_{SP} ∗1	18	−14	A
Total power dissipation		P_D ∗2	2.0		W / TOTAL
			1.4		W / ELEMENT
Channel temperature		Tch	150		°C
Storage temperature		Tstg	−55 to +150		°C

∗1 Pw≤10μs, Duty cycle≤1%
∗2 Mounted on a ceramic board.

N-ch

●**Electrical characteristics** (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	10	μA	V_{GS}= 20V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	45	–	–	V	I_D= 1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	–	–	1	μA	V_{DS}= 45V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	1.0	–	2.5	V	V_{DS}= 10V, I_D= 1mA
Static drain-source on-state resistance	$R_{DS\ (on)}$ *	–	33	46	mΩ	I_D= 4.5A, V_{GS}= 10V
		–	41	57	mΩ	I_D= 4.5A, V_{GS}= 4.5V
		–	46	64	mΩ	I_D= 4.5A, V_{GS}= 4V
Forward transfer admittance	$\|Y_{fs}\|$ *	3.5	–	–	S	V_{DS}= 10V, I_D= 4.5A
Input capacitance	C_{iss}	–	550	–	pF	V_{DS}= 10V
Output capacitance	C_{oss}	–	140	–	pF	V_{GS}= 0V
Reverse transfer capacitance	C_{rss}	–	70	–	pF	f=1MHz
Turn-on delay time	$t_{d\ (on)}$ *	–	12	–	ns	V_{DD}≒ 25V
Rise time	t_r *	–	18	–	ns	I_D= 2.5A
Turn-off delay time	$t_{d\ (off)}$ *	–	42	–	ns	V_{GS}= 10V R_L= 10Ω
Fall time	t_f *	–	12	–	ns	R_G= 10Ω
Total gate charge	Q_g *	–	6.8	9.6	nC	V_{DD}≒ 25V, V_{GS}= 5V
Gate-source charge	Q_{gs} *	–	2.0	–	nC	I_D= 4.5A
Gate-drain charge	Q_{gd} *	–	2.9	–	nC	R_L= 5.6Ω, R_G= 10Ω

*Pulsed

●**Body diode characteristics** (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD} *	–	–	1.2	V	I_S= 4.5A, V_{GS}=0V

* Pulsed

P-ch

●**Electrical characteristics** (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	–10	μA	V_{GS}=–20V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	–45	–	–	V	I_D= –1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	–	–	–1	μA	V_{DS}= –45V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	–1.0	–	–2.5	V	V_{DS}= –10V, I_D= –1mA
Static drain-source on-state resistance	$R_{DS\ (on)}$ *	–	45	63	mΩ	I_D= –3.5A, V_{GS}= –10V
		–	60	84	mΩ	I_D= –3.5A, V_{GS}= –4.5V
		–	66	92	mΩ	I_D= –3.5A, V_{GS}= –4V
Forward transfer admittance	$\|Y_{fs}\|$ *	4.5	–	–	S	V_{DS}= –10V, I_D= –3.5A
Input capacitance	C_{iss}	–	1700	–	pF	V_{DS}= –10V
Output capacitance	C_{oss}	–	200	–	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	–	135	–	pF	f=1MHz
Turn-on delay time	$t_{d\ (on)}$ *	–	16	–	ns	V_{DD} ≒ –25V I_D= –2.0A V_{GS}= –10V R_L=12.5Ω R_G=10Ω
Rise time	t_r *	–	17	–	ns	
Turn-off delay time	$t_{d\ (off)}$ *	–	70	–	ns	
Fall time	t_f *	–	14	–	ns	
Total gate charge	Q_g *	–	13.0	18.2	nC	V_{DD} ≒ –25V, V_{GS}= –5V
Gate-source charge	Q_{gs} *	–	3.6	–	nC	I_D= –3.5A
Gate-drain charge	Q_{gd} *	–	4.7	–	nC	R_L= 7.1Ω, R_G= 10Ω

* Pulsed

●**Body diode characteristics** (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD} *	–	–	–1.2	V	I_S= –3.5A, V_{GS}=0V

* Pulsed

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