STRUCTURE Silicon monolithic integrated circuits

PRODUCT SERIES 3-PHASE Brushless motor driver for porigon mirror motor

TYPE **BD6792FM**

FUNCTION
- 3-phase MOS direct PWM driver
- Built-in PLL control circuit

○Absolute maximum ratings (Ta=25℃)

Item	Symbol	Limit	Unit
Supply voltage	VCC	36	V
FG、LD pin applied voltage	VOD	33	V
Power dissipation	Pd	2200 *1	mW
Hall signal input voltage	VHALL	7	V
Input voltage for control pin (CLK, SS, SB)	VCTL	7	V
Maximum output current	IOUT	2000 *2	mA
Operating temperature range	Topr	-25～+75	℃
Storage temperature range	Tstg	-55～+150	℃
Junction temperature	Tjmax	150	℃

*1 70mm×70mm×1.6mm glass epoxy board. Derating in done at 17.6mW/℃ for operating above Ta=25℃.

*2 Do not, however exceed Pd, ASO and Tjmax=150℃.

○Recommended operating conditions (Ta=-25～+75℃)

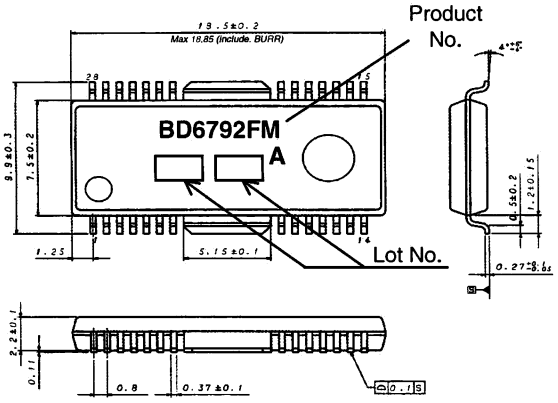
Item	Symbol	Min	Typ	Max	Unit
Supply voltage	VCC	18	24	30	V
5V constant voltage output current	IREG	0	-	20	mA
LD pin supply voltage	VLD	0	-	30	V
LD pin output current	ILD	0	-	15	mA
FG pin supply voltage	VFG	0	-	30	V
FG pin output current	IFG	0	-	15	mA

This product described in this specification isn't judged whether it applies to COCOM regulations.
Please confirm in case of export.
This product isn't designed for protection against radioactive rays.

○Electrical characteristics (Unless otherwise specified, Ta=25℃, VCC=24V)

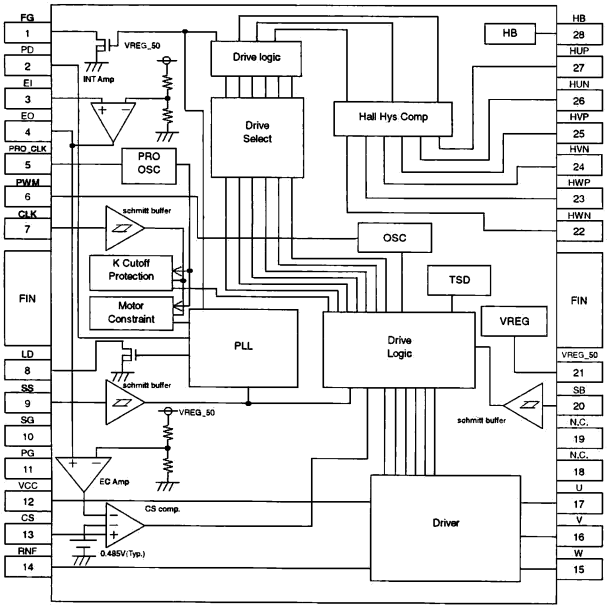
Item	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Power supply voltage	ICC1	6.4	10.6	14.8	mA	
Standby current	ICC2	1.20	2.65	4.00	mA	Standby mode
5V constant-voltage output						
Output voltage	VREG	4.65	5.00	5.35	V	
Output, Block						
Output on resistance	RON(H+L)	-	2.0	2.6	Ω	1.0A, on high and low sides in total
Forward voltage of diode on low side	VD1	0.70	1.10	1.55	V	1.0A
Forward voltage of diode on high side	VD2	0.70	1.10	1.55	V	1.0A
Hall comparator						
In-phase input voltage range	VICM	1.5	-	3.5	V	
Hysteresis width	ΔVIN	15	24	42	mV	
FG output						
Low output voltage	VFGL	-	0.15	0.50	V	7mA
Phase comparison output						
High output voltage	VPDH	VREG-0.2	VREG-0.1	-	V	100uA
Low output voltage	VPDL	-	0.2	0.3	V	-100uA
LD output						
Low output voltage	VLDL	-	0.15	0.50	V	10mA
Integral amplifier						
High output voltage	VERH	VREG-1.4	VREG-1.0	-	V	IEO=-500μA
Current limiting circuit						
Drive gain	GDF	0.4	0.5	0.6	2×	When phase locked
Limiter voltage	VRNF	0.450	0.485	0.550	V	
CLK pin						
External input frequency	FCKI	0.1	-	10	KHz	
High level input voltage	VCKIH	3.0	-	VREG	V	
Low level input voltage	VCKIL	0	-	1.5	V	
High level input current	ICKIH	-10	-	10	μA	VCLK=VREG
Low level input current	ICKIL	-75	-50	-25	μA	VCLK=0
SS pin						
High level input voltage	VSSIH	3.0	-	VREG	V	Stop
Low level input voltage	VSSIL	0	-	1.5	V	Start
High level input current	ISSIF	-10	-	10	μA	VSS=VREG
Low level input current	ISSIL	-75	-50	-25	μA	VSS=0
SB pin						
High level input voltage	VSBIH	3.0	-	VREG	V	Free run
Low level input voltage	VSBIL	0	-	1.5	V	Short brake
High level input current	ISBIH	-10	-	10	μA	VSB=VREG
Low level input current	ISBIL	-75	-50	-25	μA	VSB=0
PWM						
Oscillating frequency	FPWM	130	200	270	KHz	CPWM C=220pF
High triangular waveform voltage	VOSCH	2.50	2.75	3.00	V	
Low triangular waveform voltage	VOSCL	2.00	2.25	2.50	V	
PRO_CLK						
CLK cycle for protection circuit	TPCLK	13	20	27	msec	CPCLK=0.1μF
Hall bias						
Hall bias voltage	VHB	0.82	0.95	1.08	V	IHB=10mA

○Package outline



HSOP-M28 (Unit: mm)

○Block diagram



○Pin No. / Pin name

Pin No.	Pin name	Pin No.	Pin name
1	FG	15	W
2	PD	16	V
3	EI	17	U
4	EO	18	N.C.
5	PRO_CLK	19	N.C.
6	PWM	20	SB
7	CLK	21	VREG_50
8	LD	22	HWN
9	SS	23	HWP
10	SG	24	HVN
11	PG	25	HVP
12	VCC	26	HUN
13	CS	27	HUP
14	RNF	28	HB

＊FIN : GND

○Operation Notes

(1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range (Topr) may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. The implementation of a physical safety measure such as a fuse should be considered when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

(2) Power supply lines

Regenerated current may flow as a result of the motor's back electromotive force. Insert capacitors between the power supply and ground pins to serve as a route for regenerated current. Determine the capacitance in full consideration of all the characteristics of the electrolytic capacitor, because the electrolytic capacitor may loose some capacitance at low temperatures. If the connected power supply does not have sufficient current absorption capacity, regenerative current will cause the voltage on the power supply line to rise, which combined with the product and its peripheral circuitry may exceed the absolute maximum ratings. It is recommended to implement a physical safety measure such as the insertion of a voltage clamp diode between the power supply and GND pins.

(3) Ground potential

Ensure a minimum GND pin potential in all operating conditions.

(4) Setting of heat

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

(5) Actions in strong magnetic field

Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

(6) ASO

When using the IC, set the output transistor for the motor so that it does not exceed absolute maximum ratings or ASO.

(7) Thermal shutdown circuit

This IC incorporates a TSD (thermal shutdown) circuit (TSD circuit). If the temperature of the chip reaches the following temperature, the motor coil output will be opened. The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

TSD on temperature [°C] (typ.)	Hysteresis temperature [°C] (typ.)
175	25

(8) Ground Wiring Pattern

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

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As of 18th. April 2005