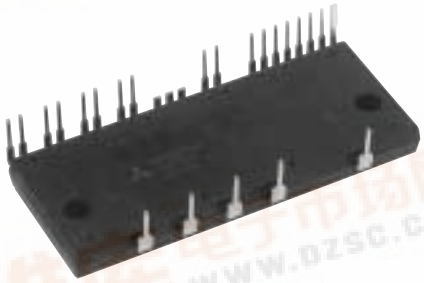
PS51277-A

TRANSFER-MOLD TYPE
INSULATED TYPE

PS51277-A



INTEGRATED POWER FUNCTIONS

- DC input, three-phase AC output inverter
- 600V, 15Arms (Input current)

INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

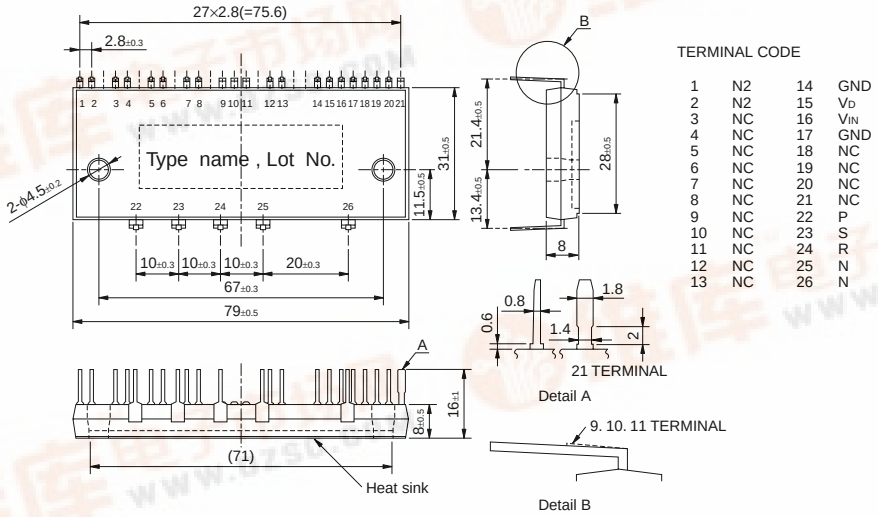
- IGBTs driver circuit
- Control supply under-voltage (UV) protection
- Input interface : 5~15V line CMOS/TTL compatible, Schmitt Trigger receiver circuit

APPLICATION

AC100~200V Active-Converter for PFC (Power Factor Correction), of Air-conditioner and so on.

Fig. 1 PACKAGE OUTLINES

Dimensions in mm



TERMINAL CODE

1	N2	14	GND
2	N2	15	V_D
3	NC	16	V_{IN}
4	NC	17	GND
5	NC	18	NC
6	NC	19	NC
7	NC	20	NC
8	NC	21	NC
9	NC	22	P
10	NC	23	S
11	NC	24	R
12	NC	25	N
13	NC	26	N

MAXIMUM RATINGS (Tj = 25°C, unless otherwise noted)

MAIN CIRCUIT PART

Symbol	Parameter	Conditions	Ratings	Unit
V_i	Supply Voltage	Applied between : S-R	264	V_{rms}
$V_{i(surge)}$	Supply Voltage (surge)	Applied between : S-R, Surge value, Non-operating	500	V
V_O	Output Voltage	Applied between : P-N	450	V
$V_{O(surge)}$	Output Voltage (surge)	Applied between : P-N, Surge value, Non-operating	500	V
V_{CES}	Collector-Emitter Voltage	—	600	V
V_{RRM}	Repetitive Peak Reverse Voltage	—	600	V
I_i	Input Current (100% Load)	$T_C \leq +90°C$, V_i = 200V, V_O = 300V, f_{PWM} = 20kHz	15	A_{rms}
$I_{i(125\%)}$	Input Current (125% Load)	$T_C \leq +90°C$, V_i = 200V, V_O = 300V, f_{PWM} = 20kHz, 1 min Non-repetitive	18.7	A_{rms}
I^2t	I^2t for Fu sing	Value for 1msec of Surge Current	75	A^2s
Tj	Junction Temperature	(Note 1)	–20~+125	°C

Note 1 : The maximum junction temperature rating of the power chips integrated within the DIP-PFC is 150°C (@ $T_C \leq 100°C$) however, to ensure safe operation of the DIP-PFC, the average junction temperature should be limited to $T_{j(ave)} \leq 125°C$ (@ $T_C \leq 100°C$).

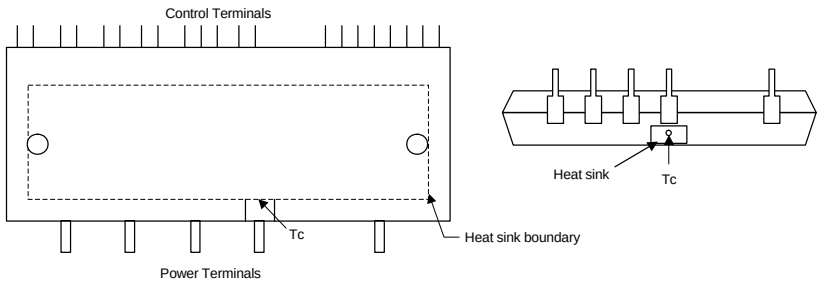
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Applied between : V_D-GND	20	V
V_{IN}	Control input voltage	Applied between : V_{IN}-GND	0~V_D+0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
T_C	Module case operation temperature	(Note 2)	–20~+100	°C
T_{stg}	Storage temperature		–40~+125	°C
V_{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1 minute, connection pins to heat-sink plate	1500	V_{rms}

Note 2 : T_C MEASUREMENT POINT



THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Junction to case thermal resistance	Inverter IGBT part	—	—	2.05	°C/W
$R_{th(j-c)F}$		Inverter FWDi part	—	—	2.50	°C/W
$R_{th(c-f)}$	Contact thermal resistance	Case to fin, (per 1 module) thermal grease applied	—	—	0.067	°C/W

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_D = 15V, V_{IN} = 5V, I_C = 30A		—	2.0	2.6	V
V_F	Forward voltage	I_F = 30A		—	1.6	2.2	V
t_{on}	Switching times	V_{CC} = 300V, V_D = 15V I_C = 20A, T_j = 125°C, V_{IN} = 5V ↔ 0V Inductive load		—	0.23	—	µs
t_{rr}				—	0.14	—	µs
$t_{c(on)}$				—	0.14	—	µs
t_{off}				—	0.43	—	µs
$t_{c(off)}$				—	0.23	—	µs
I_{CES}	Collector-emitter cut-off current	V_{CE} = 600V	T_j = 25°C	—	—	1	mA
			T_j = 125°C	—	—	10	
I_R	Reverse current	V_R = 600V	T_j = 25°C	—	—	1	mA
			T_j = 125°C	—	—	10	
I_{rr}	FWDi reverse recovery current	V_{CC} = 300V, V_D = 15V, I_C = 20A, T_j = 25°C		—	13	—	A

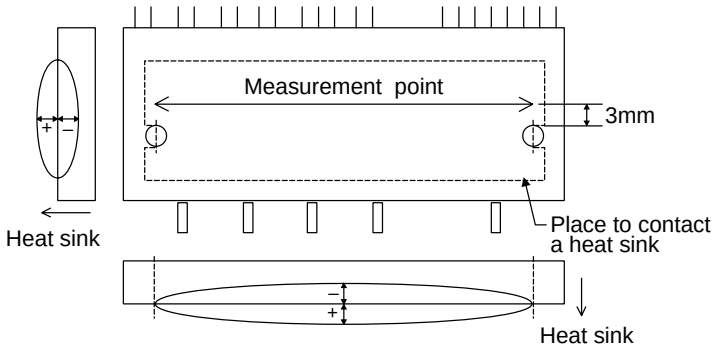
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
V_D	Control supply voltage	Applied between : V_D-GND		13.5	15.0	16.5	V
I_D	Circuit current	Applied between : V_D-GND	V_D = 15V, V_{IN} = 5V	—	0.8	3.0	mA
			V_D = 15V, V_{IN} = 0V	—	0.7	3.0	
I_{IN}	Control input current	V_D = 15V, V_{IN} = 5V		—	0.3	0.45	mA
$V_{th(on)}$	ON threshold voltage	Applied between : V_{IN}-GND		—	3.0	3.7	V
$V_{th(off)}$	OFF threshold voltage			1.3	2.0	—	V
UV_{Dt}	Supply circuit under-voltage protection	$T_j \leq 125°C$	Trip level	10.3	—	12.5	V
UV_{Dr}			Reset level	10.8	—	13.0	V

MECHANICAL CHARACTERISTICS AND RATINGS

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
—	Mounting torque	Mounting screw : M4	0.98	1.18	1.47	N·m
—	Weight		—	54	—	g
—	Heat-sink flatness	(Note 3)	–50	—	100	μm

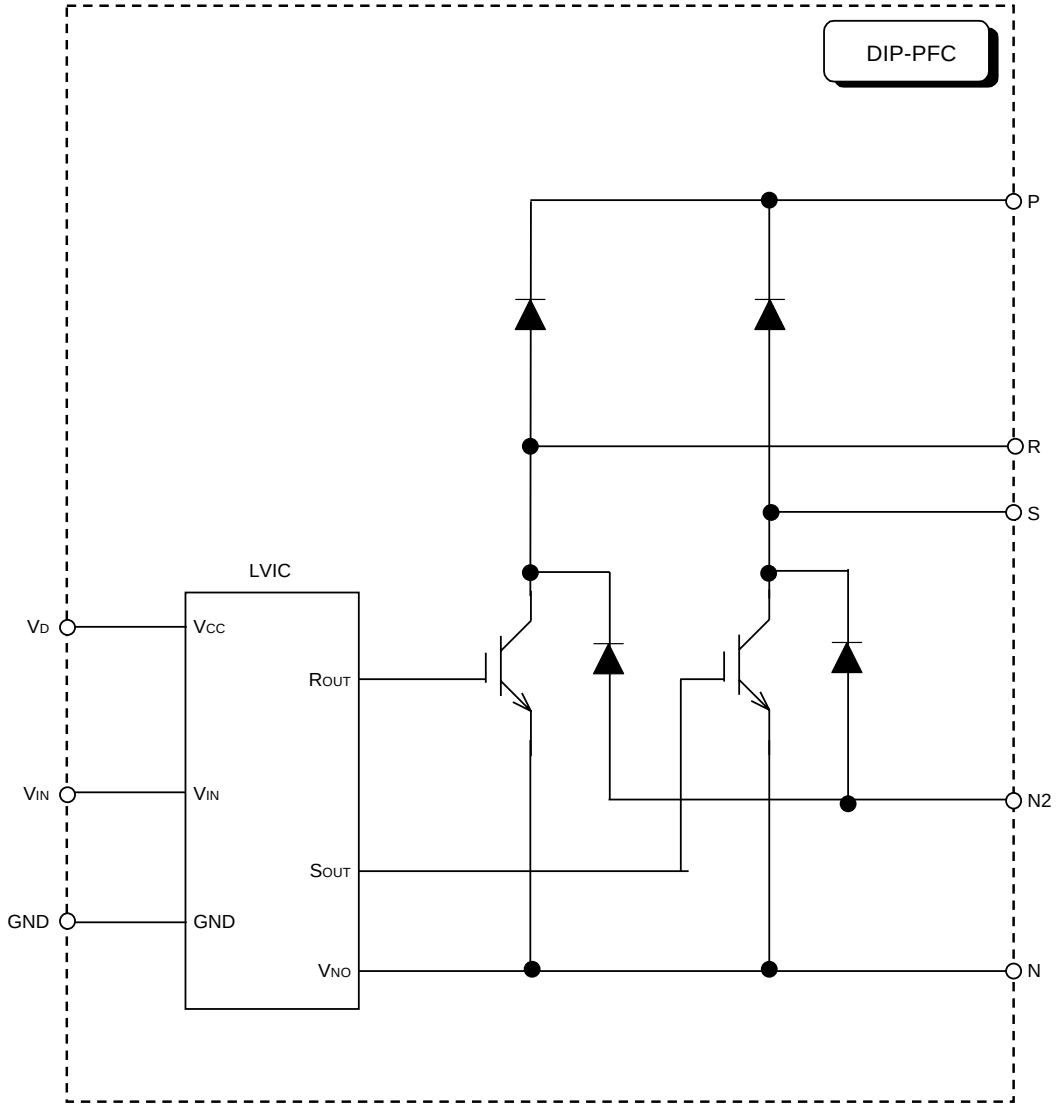
Note 3: Measurement point of heat-sink flatness



RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V_i	Supply voltage	Applied between : S-R	90	—	264	Vrms
V_D	Control supply voltage	Applied between : V_D-GND	13.5	15.0	16.5	V
ΔV_D	Control supply variation		–1	—	1	V/μs
f_{PWM}	PWM input frequency	$T_C \leq 100°C$, $T_j \leq 125°C$	—	20	—	kHz
$V_{IN(on)}$	Input ON threshold voltage	Applied between : V_{IN}-GND	4.0~V_D			V
$V_{IN(off)}$	Input OFF threshold voltage		0~1.0			V

Fig. 2 THE DIP-PFC INTERNAL CIRCUIT



DIP-PFC Wiring Guidelines

Because DIP-PFC switches large current at a very high speed, considerable large surge voltage is generated easily between P and N terminals. Please pay attention to the following items:

- The area of P-Co-N shown in Fig. 3 should be as small as possible because the rectangle shaped switching current flows on this route. In addition, please add a bypass condenser Co' with good frequency response such as a polypropylene film condenser closely to the P and N terminals.
- The two IGBT emitters are connected to the VNO terminal of LVIC inside the DIP-PFC. If the internal wiring inductance shown as L1 and L2 in Fig. 4 is too large, large surge voltage will be generated by di/dt. Especially, the lower the temperature, the faster the switching speed, therefore the larger the di/dt. This surge voltage applies to the VNO and N terminals, which is possible to destruct LVIC.
- In order to suppress the surge voltage, the external wiring method shown in Fig. 4 is recommended. To reduce the parasitic wiring inductance, the wiring of the external terminals of $N_{(N-1)}$ and $N_{(N-2)}$ should be made as short as possible.
- Please mount a fast clamp diode (EG01Y@Sanken) between N and control GND terminals to prevent control GND potential variation from the minus voltage of N terminal.

Fig. 3 DIP-PFC INTERFACE

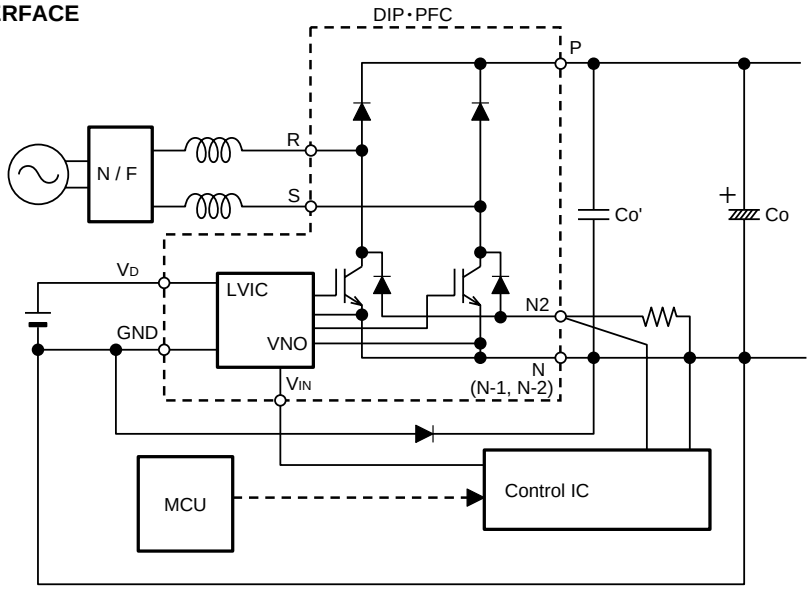


Fig. 4 RECOMMENDED WIRING METHOD