



LTC4008

4A, High Efficiency, Multi-Chemistry Battery Charger

FEATURES

- General Purpose Charger Controller
- High Conversion Efficiency: Up to 96%
- Output Currents Exceeding 4A
- $\pm 0.8\%$ Voltage Accuracy
- AC Adapter Current Limiting Maximizes Charge Rate*
- Thermistor Input for Temperature Qualified Charging
- Wide Input Voltage Range: 6V to 28V
- Wide Output Voltage: 3V to 28V
- 0.5V Dropout Voltage; Maximum Duty Cycle: 98%
- Programmable Charge Current: $\pm 4\%$ Accuracy
- Indicator Outputs for Charging, C/10 Current Detection, AC Adapter Present, Input Current Limiting and Faults
- Charging Current Monitor Output
- Available in a 20-Pin Narrow SSOP Package

APPLICATIONS

- Notebook Computers
- Portable Instruments
- Battery Backup Systems

DESCRIPTION

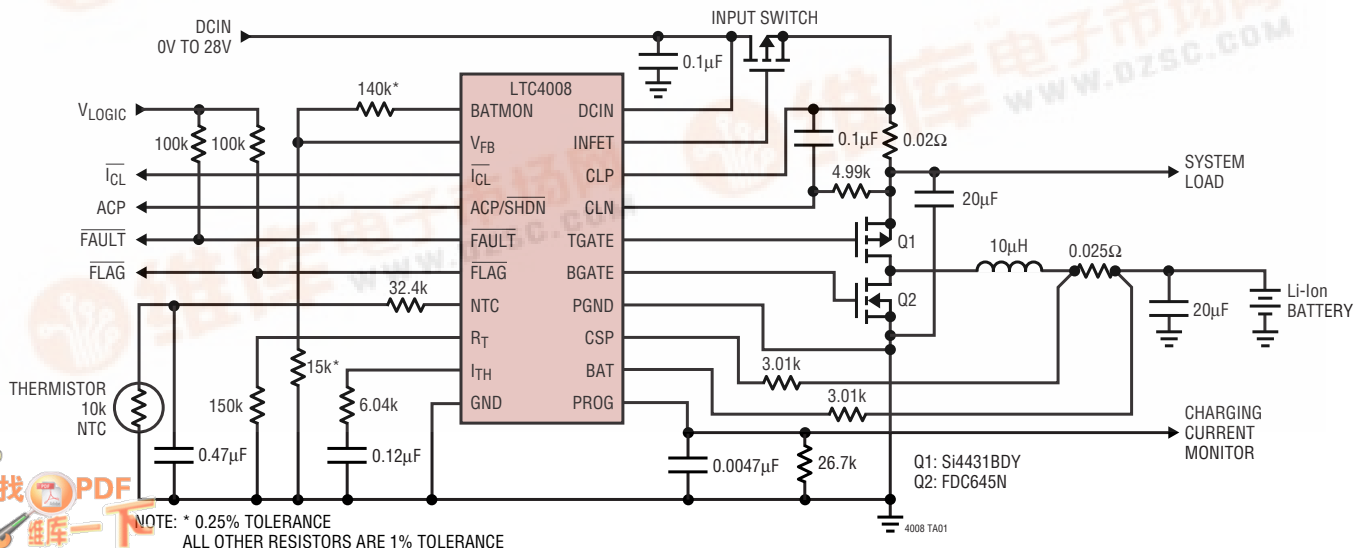
The LTC[®]4008 is a constant-current/constant-voltage charger controller. The PWM controller uses a synchronous, quasi-constant frequency, constant off-time architecture that will not generate audible noise even when using ceramic capacitors. Charging current is programmable with a sense resistor and programming resistor to $\pm 4\%$ typical accuracy. Charging current can be monitored as a voltage across the programming resistor. An external resistor divider and precision internal reference set the final float voltage.

The LTC4008 includes a thermistor sensor input that will suspend charging if an unsafe temperature condition is detected and will automatically resume charging when battery temperature returns to within safe limits; a FAULT pin indicates this condition. A FLAG pin indicates when charging current has decreased below 10% of the programmed current. An external sense resistor programs AC adapter current limiting. The I_{CL} pin indicates when the charging current is being reduced by input current limiting so that the charging algorithm can adapt.

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TYPICAL APPLICATION

12.3V, 4A Li-Ion Charger



LTC4008

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage from DCIN, CLP, CLN to GND	+32V/−0.3V	CLP to CLN	+0.5V
PGND with Respect to GND	±0.3V	Operating Ambient Temperature Range	
CSP, BAT to GND	+28V/−0.3V	(Note 4)	−40°C to 85°C
V _{FB} , R _T to GND	+7V/−0.3V	Operating Junction Temperature	−40°C to 125°C
NTC	+10V/−0.3V	Storage Temperature Range	−65°C to 150°C
ACP/SHDN, FLAG, FAULT, I _{CL}	+32V/−0.3V	Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER LTC4008EGN		ORDER PART NUMBER LTC4008EGN-1 THE LTC4008EGN-1 Does Not Have the Input FET Function
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Order Options Tape and Reel: Add #TR
 Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF Lead Free Part Marking: <http://www.linear.com/leadfree/>

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range (Note 4), otherwise specifications are at T_A = 25°C. V_{DCIN} = 20V, V_{BAT} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
	DCIN Operating Range		6		28	V	
I _Q	Operating Current	Charging Sum of Current from CLP, CLN, DCIN		3	5	mA	
V _{TOL}	Voltage Accuracy	(Notes 2, 5)	● −0.8 −1.0		0.8 1.0	% %	
	BATMON Error (Note 5)	Measured from BAT to BATMON, R _{LOAD} = 100k		0	35	80	mV
I _{TOL}	Charge Current Accuracy (Note 3)	V _{CSP} − V _{BAT} Target = 100mV	● −4 −5		4 5	% %	
Shutdown							
	Battery Leakage Current	DCIN = 0V (LTC4008 Only) ACP/SHDN = 0V	● ● −10	20	35	μA μA	
UVLO	Undervoltage Lockout Threshold	DCIN Rising, V _{BAT} = 0V	●	4.2	4.7	5.5	V
	Shutdown Threshold at ACP/SHDN		●	1	1.6	2.5	V
	Operating Current in Shutdown	V _{SHDN} = 0V, Sum of Current from CLP, CLN, DCIN		2	3	mA	

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range (Note 4), otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{\text{DCIN}} = 20\text{V}$, $V_{\text{BAT}} = 12\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
Current Sense Amplifier, CA1							
	Input Bias Current Into BAT Pin			11.66		μA	
CMSL	CA1/I ₁ Input Common Mode Low		● 0			V	
CMSH	CA1/I ₁ Input Common Mode High	$V_{\text{DCIN}} \leq 28\text{V}$	●		$V_{\text{CLN}} - 0.2$	V	
V _{OS}	Input Voltage Offset		-3.5		3.5	mV	
Current Comparators I_{CMP} and I_{REV}							
I _{TMAX}	Maximum Current Sense Threshold ($V_{\text{CSP}} - V_{\text{BAT}}$)	$V_{\text{ITH}} = 2.5\text{V}$	● 140	165	200	mV	
I _{TREV}	Reverse Current Threshold ($V_{\text{CSP}} - V_{\text{BAT}}$)			-30		mV	
Current Sense Amplifier, CA2							
	Transconductance			1		mmho	
	Source Current	Measured at I _{TH} , V _{ITH} = 1.4V		-40		μA	
	Sink Current	Measured at I _{TH} , V _{ITH} = 1.4V		40		μA	
Current Limit Amplifier							
	Transconductance			1.4		mmho	
V _{CLP}	Current Limit Threshold		● 93	100	107	mV	
I _{CLN}	CLN Input Bias Current			100		nA	
Voltage Error Amplifier, EA							
	Transconductance			1		mmho	
V _{REF}	Reference Voltage Used to Calculate V _{FLOAT}			1.19		V	
I _{BEA}	Input Bias Current			±4	±25	nA	
	Sink Current	Measured at I _{TH} , V _{ITH} = 1.4V		36		μA	
OVSD	Overvoltage Shutdown Threshold as a Percent of Programmed Charger Voltage		● 102	107	110	%	
Input P-Channel FET Driver (INFET) (LTC4008 Only)							
	DCIN Detection Threshold ($V_{\text{DCIN}} - V_{\text{CLP}}$)	DCIN Voltage Ramping Up from $V_{\text{CLP}} - 0.1\text{V}$	● 0	0.17	0.25	V	
	Forward Regulation Voltage ($V_{\text{DCIN}} - V_{\text{CLP}}$)		●	25	50	mV	
	Reverse Voltage Turn-Off Voltage ($V_{\text{DCIN}} - V_{\text{CLP}}$)	DCIN Voltage Ramping Down	● -60	-25		mV	
	INFET "On" Clamping Voltage ($V_{\text{CLP}} - V_{\text{INFET}}$)	I _{INFET} = 1 μA	● 5	5.8	6.5	V	
	INFET "Off" Clamping Voltage ($V_{\text{CLP}} - V_{\text{INFET}}$)	I _{INFET} = -25 μA			0.25	V	
Thermistor							
NTCVR	Reference Voltage During Sample Time			4.5		V	
	High Threshold	V _{NTC} Rising	●	NTCVR • 0.48	NTCVR • 0.5	NTCVR • 0.52	V
	Low Threshold	V _{NTC} Falling	●	NTCVR • 0.115	NTCVR • 0.125	NTCVR • 0.135	V
	Thermistor Disable Current	V _{NTC} ≤ 10V			10	μA	
Indicator Outputs (ACP/SHDN, FLAG, I_{CL}, FAULT)							
C10TOL	FLAG (C/10) Accuracy	Voltage Falling at PROG	● 0.375	0.397	0.420	V	
	I _{CL} Threshold Accuracy	$V_{\text{CLP}} - V_{\text{CLN}}$		83	93	105	mV
V _{OL}	Low Logic Level of ACP/SHDN, FLAG, I _{CL} , FAULT	I _{OL} = 100 μA			0.5	V	
V _{OH}	High Logic Level of ACP/SHDN, I _{CL}	I _{OH} = -1 μA	● 2.7			V	
I _{OFF}	Off State Leakage Current of FLAG, FAULT	V _{OH} = 3V		-1	1	μA	
I _{PO}	Pull-Up Current on ACP/SHDN, I _{CL}	V = 0V		-10		μA	

LTC4008

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator						
f_{OSC}	Regulator Switching Frequency		255	300	345	kHz
f_{MIN}	Regulator Switching Frequency in Drop Out	Duty Cycle $\geq 98\%$	20	25		kHz
DC_{MAX}	Regulator Maximum Duty Cycle	$V_{\text{CSP}} = V_{\text{BAT}}$	98	99		%
Gate Drivers (TGATE, BGATE)						
	V_{TGATE} High ($V_{\text{CLP}} - V_{\text{TGATE}}$)	$I_{\text{TGATE}} = -1\text{mA}$			50	mV
	V_{BGATE} High	$C_{\text{LOAD}} = 3000\text{pF}$		5.6	10	V
	V_{TGATE} Low ($V_{\text{CLP}} - V_{\text{TGATE}}$)	$C_{\text{LOAD}} = 3000\text{pF}$		5.6	10	V
	V_{BGATE} Low	$I_{\text{BGATE}} = 1\text{mA}$			50	mV
TGTR	TGATE Transition Time					
TGTR	TGATE Rise Time	$C_{\text{LOAD}} = 3000\text{pF}$, 10% to 90%		50	110	ns
TGTF	TGATE Fall Time	$C_{\text{LOAD}} = 3000\text{pF}$, 10% to 90%		50	100	ns
BGTR	BGATE Transition Time					
BGTR	BGATE Rise Time	$C_{\text{LOAD}} = 3000\text{pF}$, 10% to 90%		40	90	ns
BGTF	BGATE Fall Time	$C_{\text{LOAD}} = 3000\text{pF}$, 10% to 90%		40	80	ns
	V_{TGATE} at Shutdown ($V_{\text{CLP}} - V_{\text{TGATE}}$)	$I_{\text{TGATE}} = -1\mu\text{A}$, $\text{DCIN} = 0\text{V}$, $\text{CLP} = 12\text{V}$			100	mV
	V_{BGATE} at Shutdown	$I_{\text{BGATE}} = 1\mu\text{A}$, $\text{DCIN} = 0\text{V}$, $\text{CLP} = 12\text{V}$			100	mV

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: See Test Circuit.

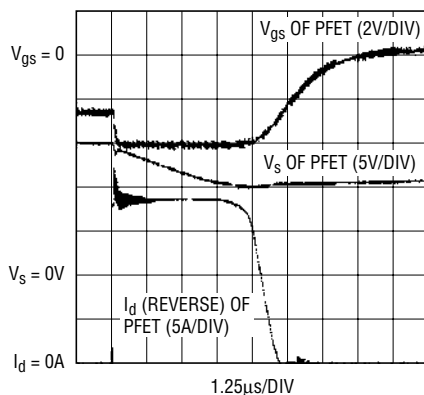
Note 3: Does not include tolerance of current sense resistor or current programming resistor.

Note 4: The LTC4008E is guaranteed to meet performance specifications from 0°C to 70°C . Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 5: Voltage accuracy includes BATMON error and voltage reference error. Does not include error of external resistor divider.

TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

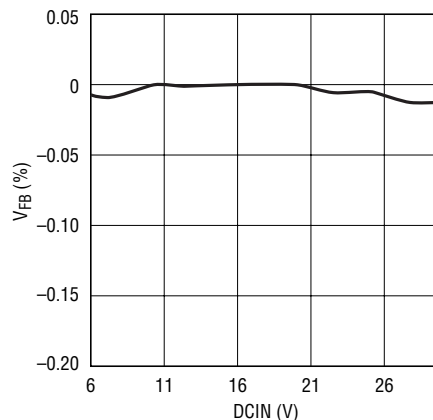
INFET Response Time to Reverse Current



TEST PERFORMED ON DEMOBOARD
 $V_{\text{IN}} = 15\text{VDC}$ $V_{\text{CHARGE}} = 12.6\text{V}$
 CHARGER = ON INFET = 1/2 Si4925DY
 $I_{\text{CHARGE}} < 10\text{mA}$

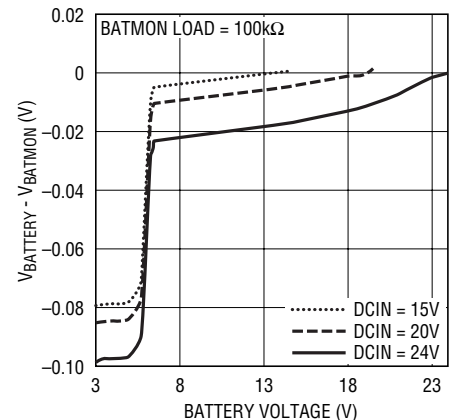
4008 G01

V_{FB} vs DCIN



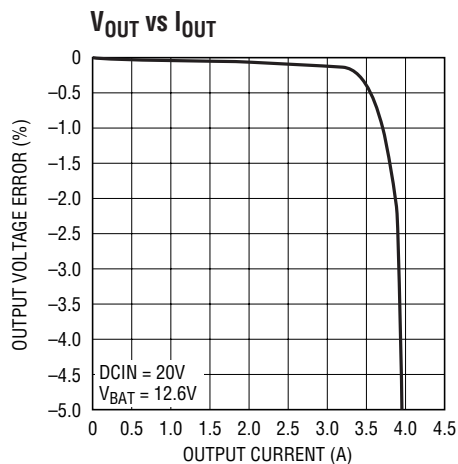
4008 G02

BATMON Offset

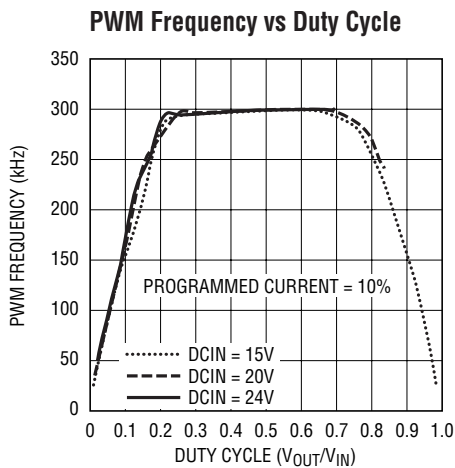


4008 G03

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise noted)

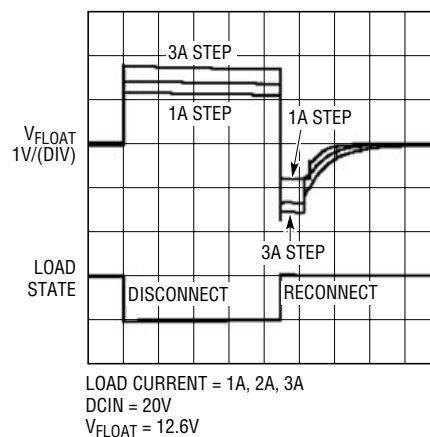


4008 G04



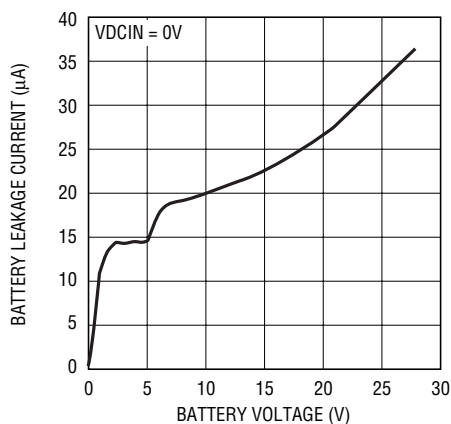
4008 G05

Disconnect/Reconnect Battery (Load Dump)



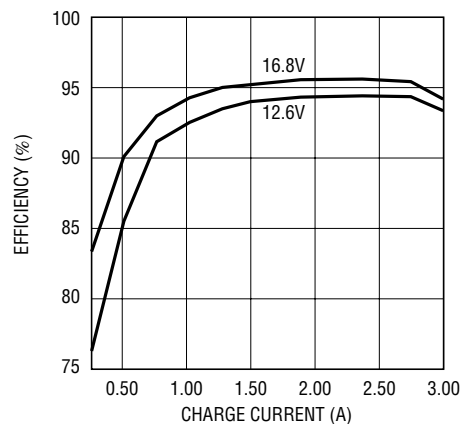
4008 G06

Battery Leakage Current vs Battery Voltage



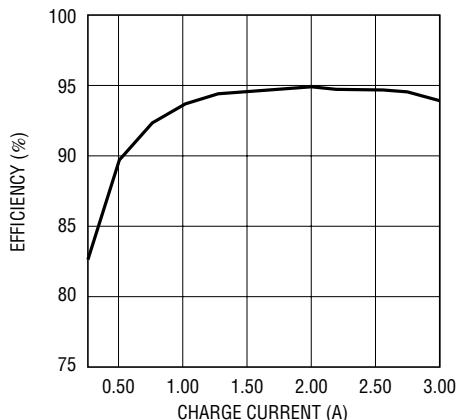
4008 G07

Efficiency at 19VDC V_{IN}



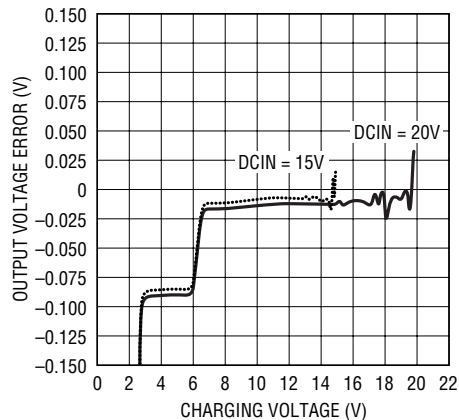
4008 G09

Efficiency at 12.6V with 15VDC V_{IN}



4008 G10

Charging Voltage Error TEMP = 27°C, I_{LOAD} = 0.120A



4008 G11

PIN FUNCTIONS

DCIN (Pin 1): External DC Power Source Input. Bypass this pin with at least 0.01 μ F. See Applications Information section.

$\overline{\text{ICL}}$ (Pin 2): Input Current Limit Indicator. Active low digital output. Internal 10 μ A pull-up to 3.5V. Pulled low if the charger current is being reduced by the input current limiting function. The pin is capable of sinking at least 100 μ A. If $V_{\text{LOGIC}} > 3.3\text{V}$, add an external pull-up.

ACP/ $\overline{\text{SHDN}}$ (Pin 3): Open-drain output used to indicate if the AC adapter voltage is adequate for charging. Active high digital output. Internal 10 μ A pull-up to 3.5V. The charger can also be shutdown by pulling this pin below 1V. The pin is capable of sinking at least 100 μ A. If $V_{\text{LOGIC}} > 3.3\text{V}$, add an external pull-up. (LTC4008-1: ACP function disabled.)

R_T (Pin 4): Thermistor Clamping Resistor. Use a 150k resistor as a nominal value. This resistor is always required. If this resistor is not present, the charger will not start.

$\overline{\text{FAULT}}$ (Pin 5): Active low open-drain output that indicates that charger operation has suspended due to the thermistor exceeding allowed values. A pull-up resistor is required if this function is used. The pin is capable of sinking at least 100 μ A.

GND (Pin 6): Ground for Low Power Circuitry.

V_{FB} (Pin 7): Input of Voltage Feedback Error Amplifier, EA, in the Block Diagram.

NTC (Pin 8): A thermistor network is connected from NTC to GND. This pin determines if the battery temperature is safe for charging. The charger and timer are suspended and the $\overline{\text{FAULT}}$ pin is driven low if the thermistor indicates a temperature that is unsafe for charging. The thermistor function may be disabled with a 300k to 500k resistor from DCIN to NTC.

I_{TH} (Pin 9): Control Signal of the Inner Loop of the Current Mode PWM. Higher I_{TH} voltage corresponds to higher charging current in normal operation. A 6k resistor in series with a capacitor of at least 0.1 μ F to GND provides loop compensation. Typical full-scale output current is 40 μ A. Nominal voltage range for this pin is 0V to 3V.

PROG (Pin 10): Current Programming/Monitoring Input/Output. An external resistor to GND programs the peak

charging current in conjunction with the current sensing resistor. The voltage at this pin provides a linear indication of charging current. Peak current is equivalent to 1.19V. Zero current is approximately 0.309V. A capacitor from PROG to ground is required to filter higher frequency components. The maximum program resistance to ground is 100k. Values higher than 100k can cause the charger to shut down.

CSP (Pin 11): Current Amplifier CA1 Input. The CSP and BAT pins measure the voltage across the sense resistor, R_{SENSE} , to provide the instantaneous current signals required for both peak and average current mode operation.

BAT (Pin 12): Battery Sense Input and the Negative Reference for the Current Sense Resistor.

BATMON (Pin 13): Output Voltage Representing Battery Voltage. Switched off to reduce standby current drain when AC is not present. An external voltage divider from BATMON to V_{FB} sets the charger float voltage. Recommended minimum load resistance is 100k.

$\overline{\text{FLAG}}$ (Pin 14): Active low open-drain output that indicates when charging current has declined to 10% of max programmed current. A pull-up resistor is required if this function is used. The pin is capable of sinking at least 100 μ A. This function is latching. To clear it, user must cycle the ACP/ $\overline{\text{SHDN}}$ pin.

CLN (Pin 15): Negative Input to the Input Current Limiting Amplifier CL1. The threshold is set at 100mV below the voltage at the CLP pin. When used to limit input current, a filter is needed to filter out the switching noise. If no current limit function is desired, connect this pin to CLP.

CLP (Pin 16): This pin serves as a positive reference for the input current limit amplifier, CL1. It also serves as the power supply for the IC.

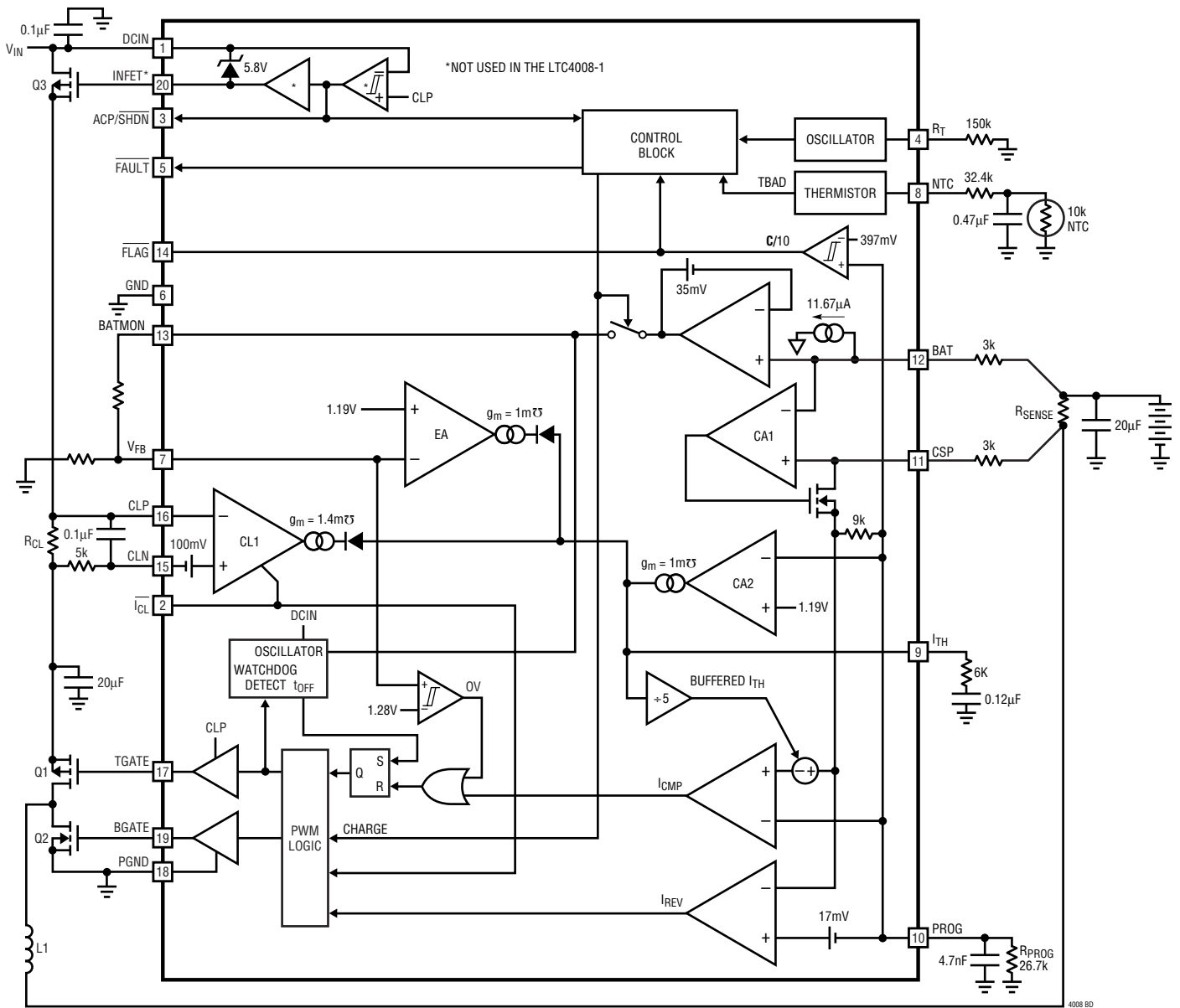
TGATE (Pin 17): Drives the top external PMOSFET of the battery charger buck converter.

PGND (Pin 18): High Current Ground Return for BGATE Driver.

BGATE (Pin 19): Drives the bottom external N-MOSFET of the battery charger buck converter.

INFET (Pin 20): Drives the gate of the external input P-MOSFET. (LTC4008-1: No Connection)

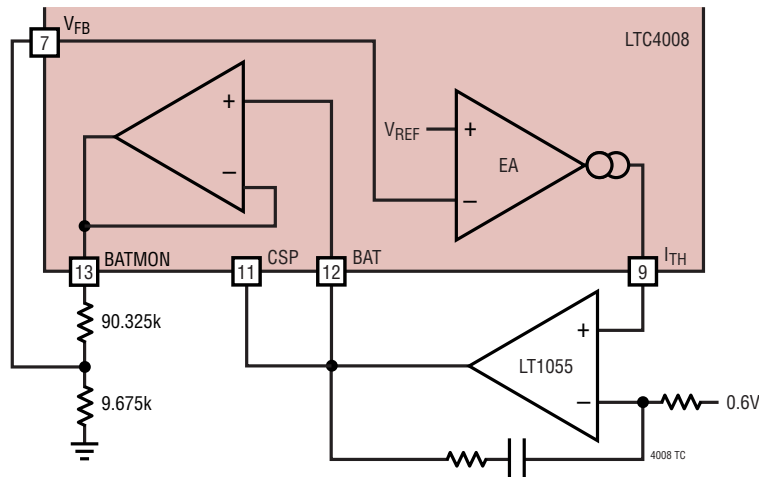
BLOCK DIAGRAM



4008 BD

LTC4008

TEST CIRCUIT



OPERATION

OVERVIEW

The LTC4008 is a synchronous current mode PWM step down (buck) switcher battery charger controller. The charge current is programmed by the combination of a program resistor (R_{PROG}) from the PROG pin to ground and a sense resistor (R_{SENSE}) between the CSP and BAT pins. The final float voltage is programmed with an external resistor divider and the internal 1.19V reference voltage. Charging begins when the potential at the DCIN pin rises above the voltage at BAT (and the UVLO voltage) and the ACP/SHDN pin is high. An external thermistor network is sampled at regular intervals. If the thermistor value exceeds design limits, charging is suspended and the FAULT pin is set low. If the thermistor value returns to an acceptable value, charging resumes and the FAULT pin is set high. An external resistor on the R_T pin sets the sampling interval for the thermistor.

As the battery approaches the final float voltage, the charge current will begin to decrease. When the current drops to 10% of the full-scale charge current, an internal C/10 comparator will indicate this condition by latching the FLAG pin low. If this condition is caused by an input current limit condition, described below, then the FLAG indicator will be inhibited. When the input voltage is not present, the charger goes into a sleep mode, dropping battery current drain to 15 μ A. This greatly reduces the current drain on the battery and increases the standby time. The charger can be inhibited at any time by forcing the ACP/SHDN pin to a low voltage. Forcing ACP/SHDN low, or removing the voltage from DCIN, will also clear the FLAG pin if it is low.

Table 1. Truth Table For Indicator States

MODE	DCIN	ACP/SHDN	FLAG**	FAULT**	I_{CL}
Shutdown by low adapter voltage (Disabled on LTC4008-1)	<BAT	LOW	HIGH	HIGH	LOW
Normal charging	>BAT	HIGH	HIGH	HIGH*	HIGH*
Input current limited charging	>BAT	HIGH	HIGH*	HIGH*	LOW
Charger shut down due to thermistor out of range	>BAT	HIGH	X	LOW	HIGH
Shut down by ACP/SHDN pin (USER)	X	Forced LOW	HIGH	HIGH	LOW
Shut down by undervoltage lockout	>BAT + <UVL	HIGH	HIGH	HIGH*	LOW

*Most probable condition, **Open-drain output, HIGH = Open with pull-up, X = Don't care

OPERATION

Input FET (LTC4008)

The input FET circuit performs two functions. It enables the charger if the input voltage is higher than the CLP pin and provides the logic indicator of AC present on the ACP/SHDN pin. It controls the gate of the input FET to keep a low forward voltage drop when charging and also prevents reverse current flow through the input FET.

If the input voltage is less than V_{CLP} , it must go at least 170mV higher than V_{CLN} to activate the charger. When this occurs the ACP/SHDN pin is released and pulled up with an external load to indicate that the adapter is present. The gate of the input FET is driven to a voltage sufficient to keep a low forward voltage drop from drain to source. If the voltage between DCIN and CLP drops to less than 25mV, the input FET is turned off slowly. If the voltage between DCIN and CLP is ever less than -25mV , then the input FET is turned off in less than $10\mu\text{s}$ to prevent significant reverse current from flowing in the input FET. In this condition, the ACP/SHDN pin is driven low and the charger is disabled.

Input FET (LTC4008-1)

The input FET circuit is disabled for the LTC4008-1. There is no low current shutdown mode when DCIN falls below the CLP pin. The ACP/SHDN pin functions only to shut down the charger.

Battery Charger Controller

The LTC4008 charger controller uses a constant off-time, current mode step-down architecture. During normal operation, the top MOSFET is turned on each cycle when the oscillator sets the SR latch and turned off when the main current comparator I_{CMP} resets the SR latch. While the top MOSFET is off, the bottom MOSFET is turned on until either the inductor current trips the current comparator I_{REV} or the beginning of the next cycle. The oscillator uses the equation:

$$t_{\text{OFF}} = \frac{V_{\text{DCIN}} - V_{\text{BAT}}}{V_{\text{DCIN}} \cdot f_{\text{OSC}}}$$

to set the bottom MOSFET on time. This activity is diagrammed in Figure 1.

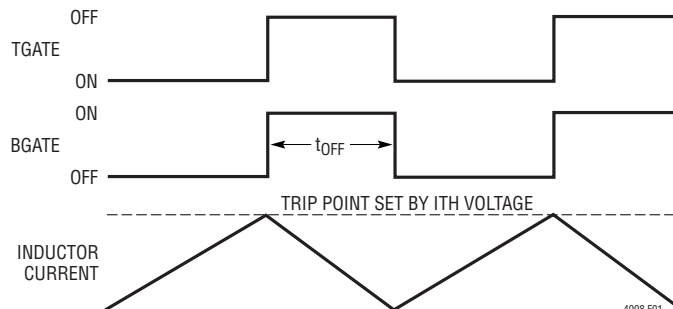


Figure 1

The peak inductor current, at which I_{CMP} resets the SR latch, is controlled by the voltage on I_{TH} . I_{TH} is in turn controlled by several loops, depending upon the situation at hand. The average current control loop converts the voltage between CSP and BAT to a representative current. Error amp CA2 compares this current against the desired current programmed by R_{PROG} at the PROG pin and adjusts I_{TH} until:

$$\frac{V_{\text{REF}}}{R_{\text{PROG}}} = \frac{V_{\text{CSP}} - V_{\text{BAT}} + 11.67\mu\text{A} \cdot 3.01\text{k}\Omega}{3.01\text{k}\Omega}$$

therefore,

$$I_{\text{CHARGE(MAX)}} = \left(\frac{V_{\text{REF}}}{R_{\text{PROG}}} - 11.67\mu\text{A} \right) \cdot \frac{3.01\text{k}\Omega}{R_{\text{SENSE}}}$$

The voltage at BATMON is divided down by an external resistor divider and is used by error amp EA to decrease I_{TH} if the divider voltage is above the 1.19V reference. When the charging current begins to decrease, the voltage at PROG will decrease in direct proportion. The voltage at PROG is then given by:

$$V_{\text{PROG}} = (I_{\text{CHARGE}} \cdot R_{\text{SENSE}} + 11.67\mu\text{A} \cdot 3.01\text{k}\Omega) \cdot \frac{R_{\text{PROG}}}{3.01\text{k}\Omega}$$

The accuracy of V_{PROG} will range from 0% to I_{TOL} .

V_{PROG} is plotted in Figure 2.

The amplifier CL1 monitors and limits the input current, normally from the AC adapter to a preset level ($100\text{mV}/R_{\text{CL}}$). At input current limit, CL1 will decrease the I_{TH} voltage, thereby reducing charging current. The $\overline{I_{\text{CL}}}$ indicator output will go low when this condition is detected and the $\overline{\text{FLAG}}$ indicator will be inhibited if it is not already low.

OPERATION

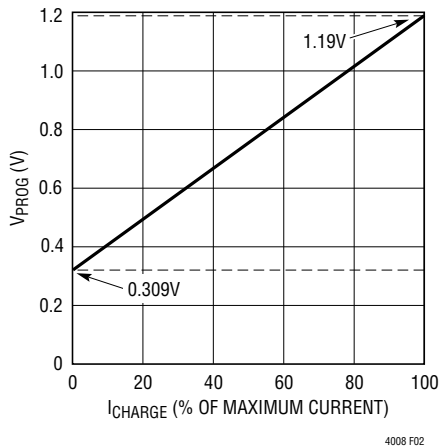


Figure 2. V_{PROG} vs I_{CHARGE}

If the charging current decreases below 10% to 15% of programmed current, while engaged in input current limiting, BGATE will be forced low to prevent the charger from discharging the battery. Audible noise can occur in this mode of operation.

An overvoltage comparator guards against voltage transient overshoots (>7% of programmed value). In this case, both MOSFETs are turned off until the overvoltage condition is cleared. This feature is useful for batteries which “load dump” themselves by opening their protection switch to perform functions such as calibration or pulse mode charging.

PWM Watchdog Timer

There is a watchdog timer that observes the activity on the BGATE and TGATE pins. If TGATE stops switching for more than 40 μ s, the watchdog activates and turns off the top MOSFET for about 400ns. The watchdog engages to prevent very low frequency operation in dropout which is a potential source of audible noise when using ceramic input and output capacitors.

Charger Startup

When the charger is enabled, it will not begin switching until the I_{TH} voltage exceeds a threshold that assures initial current will be positive. This threshold is 5% to 15% of the maximum programmed current ($100\text{mV}/R_{SENSE}$). After the charger begins switching, the various loops will control the current at a level that is higher or lower than the initial current. The duration of this transient condition depends upon the loop compensation but is typically less than 100 μ s.

Thermistor Detection

The thermistor detection circuit is shown in Figure 3. It requires an external resistor and capacitor in order to function properly.

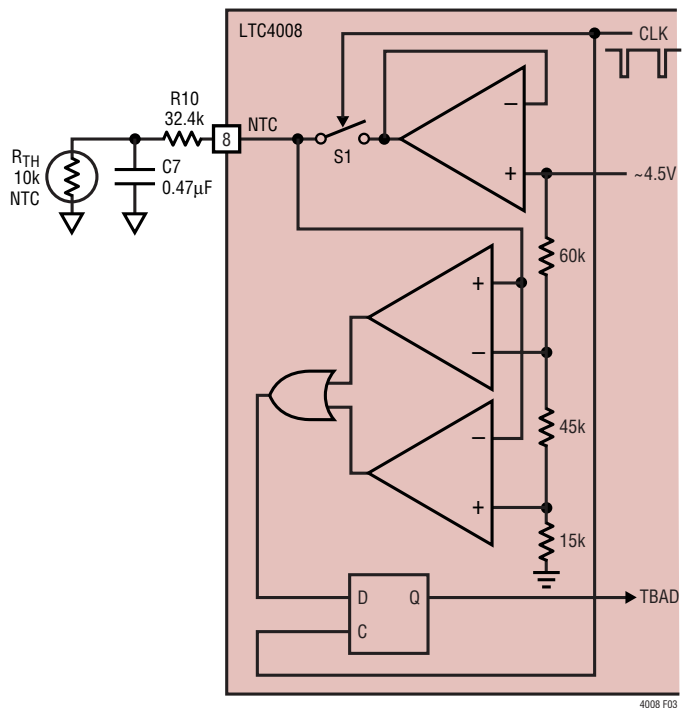


Figure 3

OPERATION

The thermistor detector performs a sample-and-hold function. An internal clock, whose frequency is determined by the timing resistor connected to R_T , keeps switch S1 closed to sample the thermistor:

$$t_{\text{SAMPLE}} = 127.5 \cdot 20 \cdot R_{\text{RT}} \cdot 17.5\text{pF} = 6.7\text{ms},$$

$$\text{for } R_{\text{RT}} = 150\text{k}$$

The external RC network is driven to approximately 4.5V and settles to a final value across the thermistor of:

$$V_{\text{RTH(FINAL)}} = \frac{4.5\text{V} \cdot R_{\text{TH}}}{R_{\text{TH}} + R_{10}}$$

This voltage is stored by C7. Then the switch is opened for a short period of time to read the voltage across the thermistor.

$$t_{\text{HOLD}} = 10 \cdot R_{\text{RT}} \cdot 17.5\text{pF} = 26\mu\text{s},$$

$$\text{for } R_{\text{RT}} = 150\text{k}$$

When the t_{HOLD} interval ends the result of the thermistor testing is stored in the D flip-flop (DFF). If the voltage at NTC is within the limits provided by the resistor divider feeding the comparators, then the NOR gate output will be low and the DFF will set T_{BAD} to zero and charging will continue. If the voltage at NTC is outside of the resistor divider limits, then the DFF will set T_{BAD} to one, the charger will be shut down, **FAULT** pin is set low and the timer will be suspended until T_{BAD} returns to zero (see Figure 4).

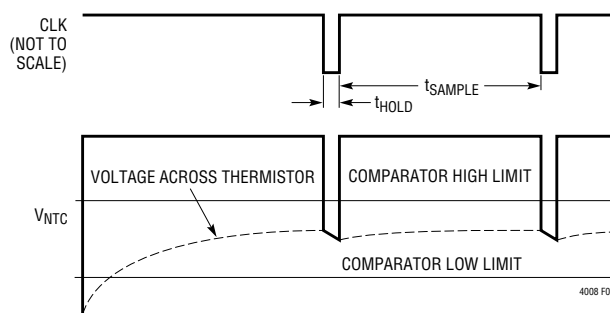


Figure 4

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Charger Current Programming

The basic formula for charging current is:

$$I_{\text{CHARGE(MAX)}} = \frac{V_{\text{REF}} \cdot 3.01\text{k}\Omega / R_{\text{PROG}} - 0.035\text{V}}{R_{\text{SENSE}}}$$

$V_{\text{REF}} = 1.19\text{V}$. This leaves two degrees of freedom: R_{SENSE} and R_{PROG} . The 3.01k input resistors must not be altered since internal currents and voltages are trimmed for this value. Pick R_{SENSE} by setting the average voltage between CSP and BAT to be close to 100mV during maximum charger current. Then R_{PROG} can be determined by solving the above equation for R_{PROG} .

$$R_{\text{PROG}} = \frac{V_{\text{REF}} \cdot 3.01\text{k}\Omega}{R_{\text{SENSE}} \cdot I_{\text{CHARGE(MAX)}} + 0.035\text{V}}$$

Table 2. Recommended R_{SNS} and R_{PROG} Resistor Values

I_{MAX} (A)	R_{SENSE} (Ω) 1%	R_{SENSE} (W)	R_{PROG} (k Ω) 1%
1.0	0.100	0.25	26.7
2.0	0.050	0.25	26.7
3.0	0.033	0.5	26.7
4.0	0.025	0.5	26.7

Charging current can be programmed by pulse width modulating R_{PROG} with a switch Q1 to R_{PROG} at a frequency higher than a few kHz (Figure 5). C_{PROG} must be increased to reduce the ripple caused by the R_{PROG} switching. The compensation capacitor at I_{TH} will probably need to be increased also to improve stability and

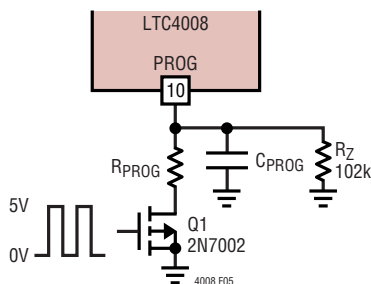


Figure 5. PWM Current Programming

prevent large overshoot currents during start-up conditions. Charging current will be proportional to the duty cycle of the switch with full current at 100% duty cycle and zero current when Q1 is off.

Maintaining C/10 Accuracy

The C/10 comparator threshold that drives the $\overline{\text{FLAG}}$ pin has a fixed threshold of approximately $V_{\text{PROG}} = 400\text{mV}$. This threshold works well when R_{PROG} is 26.7k, but will not yield a 10% charging current indication if R_{PROG} is a different value. There are situations where a standard value of R_{SENSE} will not allow the desired value of charging current when using the preferred R_{PROG} value. In these cases, where the full-scale voltage across R_{SENSE} is within $\pm 20\text{mV}$ of the 100mV full-scale target, the input resistors connected to CSP and BAT can be adjusted to provide the desired maximum programming current as well as the correct $\overline{\text{FLAG}}$ trip point.

For example, the desired max charging current is 2.5A but the best R_{SENSE} value is 0.033 Ω . In this case, the voltage across R_{SENSE} at maximum charging current is only 82.5mV, normally R_{PROG} would be 30.1k but the nominal $\overline{\text{FLAG}}$ trip point is only 5% of maximum charging current. If the input resistors are reduced by the same amount as the full-scale voltage is reduced then, $R_4 = R_5 = 2.49\text{k}$ and $R_{\text{PROG}} = 26.7\text{k}$, the maximum charging current is still 2.5A but the $\overline{\text{FLAG}}$ trip point is maintained at 10% of full scale.

There are other effects to consider. The voltage across the current comparator is scaled to obtain the same values as the 100mV sense voltage target, but the input referred sense voltage is reduced, causing some careful consideration of the ripple current. Input referred maximum comparator threshold is 117mV, which is the same ratio of 1.4x the DC target. Input referred I_{REV} threshold is scaled back to -24mV . The current at which the switcher starts will be reduced as well so there is some risk of boost activity. These concerns can be addressed by using a slightly larger inductor to compensate for the reduction of tolerance to ripple current.

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Battery Conditioning

Some batteries require a small charging current to condition them when they are severely depleted. The charging current is switched to a high rate after the battery voltage has reached a “safe” voltage to do so. Figure 6 illustrates how to do this 2-level charging. When Q1 is on, the charger current is set to maximum. When Q1 is off, the charging current is set to 10% of the maximum.

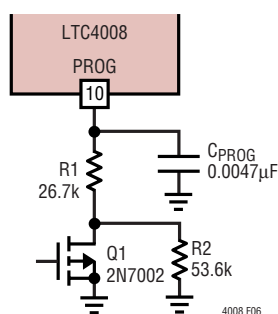


Figure 6. 2-Level Current Programming

Charger Voltage Programming

A resistor divider, R8 and R9 (see Figure 10), programs the final float voltage of the charger. The equation for float voltage is (the input bias current of EA is typically -4nA and can be ignored):

$$V_{\text{FLOAT}} = V_{\text{REF}} (1 + R8/R9)$$

It is recommended that the sum of R8 and R9 not be less than 100k. Accuracy of the LTC4008 voltage reference is $\pm 0.8\%$ at 25°C , and $\pm 1\%$ over the full temperature range. This leads to the possibility that very accurate (0.1%) resistors might be needed for R8 and R9. Actually, the temperature of the LTC4008 will rarely exceed 50°C near the float voltage because charging currents have tapered to a low level, so 0.25% resistors will normally provide the required level of overall accuracy. Table 3 contains recommended values for R8 and R9 for popular float voltages.

Table 3

FLOAT VOLTAGE (V)	R9 (k Ω) 0.25%	R8 (k Ω) 0.25%
8.2	24.9	147
8.4	26.1	158
12.3	15	140
12.6	16.9	162
16.4	11.5	147
16.8	13.3	174

Soft-Start

The LTC4008 is soft started by the $0.12\mu\text{F}$ capacitor on the I_{TH} pin. On start-up, I_{TH} pin voltage will rise quickly to 0.5V, then ramp up at a rate set by the internal $40\mu\text{A}$ pull-up current and the external capacitor. Battery charging current starts ramping up when I_{TH} voltage reaches 0.8V and full current is achieved with I_{TH} at 2V. With a $0.12\mu\text{F}$ capacitor, time to reach full charge current is about 2ms and it is assumed that input voltage to the charger will reach full value in less than 2ms. The capacitor can be increased up to $1\mu\text{F}$ if longer input start-up times are needed.

Input and Output Capacitors

The input capacitor (C2) is assumed to absorb all input switching ripple current in the converter, so it must have adequate ripple current rating. Worst-case RMS ripple current will be equal to one-half of output charging current. Actual capacitance value is not critical. Solid tantalum low ESR capacitors have high ripple current rating in a relatively small surface mount package, *but caution must be used when tantalum capacitors are used for input or output bypass*. High input surge currents can be created when the adapter is hot-plugged to the charger or when a battery is connected to the charger. Solid tantalum capacitors have a known failure mechanism when subjected to very high turn-on surge currents. Only Kemet T495 series of “Surge Robust” low ESR tantalums are rated for high surge conditions such as battery to ground.

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The relatively high ESR of an aluminum electrolytic for C1, located at the AC adapter input terminal, is helpful in reducing ringing during the hot-plug event. Refer to Application Note 88 for more information.

Highest possible voltage rating on the capacitor will minimize problems. Consult with the manufacturer before use. Alternatives include new high capacity ceramic (at least 20 μ F) from Tokin, United Chemi-Con/Marcon, et al. Other alternative capacitors include OS-CON capacitors from Sanyo.

The output capacitor (C3) is also assumed to absorb output switching current ripple. The general formula for capacitor current is:

$$I_{RMS} = \frac{0.29(V_{BAT}) \left(1 - \frac{V_{BAT}}{V_{DCIN}}\right)}{(L1)(f)}$$

For example:

$$V_{DCIN} = 19V, V_{BAT} = 12.6V, L1 = 10\mu H, \text{ and } f = 300kHz, I_{RMS} = 0.41A.$$

EMI considerations usually make it desirable to minimize ripple current in the battery leads, and beads or inductors may be added to increase battery impedance at the 300kHz switching frequency. Switching ripple current splits between the battery and the output capacitor depending on the ESR of the output capacitor and the battery impedance. If the ESR of C3 is 0.2 Ω and the battery impedance is raised to 4 Ω with a bead or inductor, only 5% of the current ripple will flow in the battery.

Inductor Selection

Higher operating frequencies allow the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of MOSFET gate charge losses. In addition, the effect of inductor value on ripple current and low current operation must also be considered. The inductor ripple current ΔI_L decreases with higher frequency and increases with higher V_{IN} .

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.4(I_{MAX})$. In no case should ΔI_L exceed 0.6(I_{MAX}) due to limits imposed by I_{REV} and CA1. Remember the maximum ΔI_L occurs at the maximum input voltage. In practice 10 μ H is the lowest value recommended for use.

Lower charger currents generally call for larger inductor values. Use Table 4 as a guide for selecting the correct inductor value for your application.

Table 4

MAXIMUM AVERAGE CURRENT (A)	INPUT VOLTAGE (V)	MINIMUM INDUCTOR VALUE (μ H)
1	≤ 20	40 \pm 20%
1	> 20	56 \pm 20%
2	≤ 20	20 \pm 20%
2	> 20	30 \pm 20%
3	≤ 20	15 \pm 20%
3	> 20	20 \pm 20%
4	≤ 20	10 \pm 20%
4	> 20	15 \pm 20%

Charger Switching Power MOSFET and Diode Selection

Two external power MOSFETs must be selected for use with the charger: a P-channel MOSFET for the top (main) switch and an N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak gate drive levels are set internally. This voltage is typically 6V. Consequently, logic-level threshold MOSFETs must be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; many of the logic level MOSFETs are limited to 30V or less.

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Selection criteria for the power MOSFETs include the “ON” resistance $R_{DS(ON)}$, total gate capacitance Q_G , reverse transfer capacitance C_{RSS} , input voltage and maximum output current. The charger is operating in continuous mode so the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = V_{OUT}/V_{IN}$$

$$\text{Synchronous Switch Duty Cycle} = (V_{IN} - V_{OUT})/V_{IN}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = V_{OUT}/V_{IN}(I_{MAX})^2(1 + \delta\Delta T)R_{DS(ON)} + k(V_{IN})^2(I_{MAX})(C_{RSS})(f_{OSC})$$

$$P_{SYNC} = (V_{IN} - V_{OUT})/V_{IN}(I_{MAX})^2(1 + \delta\Delta T)R_{DS(ON)}$$

Where $\delta\Delta T$ is the temperature dependency of $R_{DS(ON)}$ and k is a constant inversely related to the gate drive current. Both MOSFETs have I^2R losses while the P_{MAIN} equation includes an additional term for transition losses, which are highest at high input voltages. For $V_{IN} < 20V$ the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$ the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{RSS} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage or during a short circuit when the duty cycle in this switch is nearly 100%. The term $(1 + \delta\Delta T)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but $\delta = 0.005/^\circ C$ can be used as an approximation for low voltage MOSFETs. $C_{RSS} = Q_G/\Delta V_{DS}$ is usually specified in the MOSFET characteristics. The constant $k = 2$ can be used to estimate the contributions of the two terms in the main switch dissipation equation.

If the charger is to operate in low dropout mode or with a high duty cycle greater than 85%, then the topside P-channel efficiency generally improves with a larger MOSFET. Using asymmetrical MOSFETs may achieve cost savings or efficiency gains.

The Schottky diode D1, shown in the Typical Application on the back page, conducts during the dead-time between the conduction of the two power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on and storing charge during the dead-time, which could cost as much as 1% in efficiency. A 1A Schottky is generally a good size for 4A regulators due to the relatively small average current. Larger diodes can result in additional transition losses due to their larger junction capacitance.

The diode may be omitted if the efficiency loss can be tolerated.

Calculating IC Power Dissipation

The power dissipation of the LTC4008 is dependent upon the gate charge of the top and bottom MOSFETs (Q_{G1} & Q_{G2} respectively) The gate charge is determined from the manufacturer’s data sheet and is dependent upon both the gate voltage swing and the drain voltage swing of the MOSFET. Use 6V for the gate voltage swing and V_{DCIN} for the drain voltage swing.

$$PD = V_{DCIN} \cdot (f_{OSC} (Q_{G1} + Q_{G2}) + I_Q)$$

Example:

$$V_{DCIN} = 19V, f_{OSC} = 345kHz, Q_{G1} = Q_{G2} = 15nC, I_Q = 5mA$$

$$PD = 292mW$$

Adapter Limiting

An important feature of the LTC4008 is the ability to automatically adjust charging current to a level which avoids overloading the wall adapter. This allows the product to operate at the same time that batteries are being charged without complex load management algorithms. Additionally, batteries will automatically be charged at the maximum possible rate of which the adapter is capable.

This feature is created by sensing total adapter output current and adjusting charging current downward if a preset adapter current limit is exceeded. True analog

APPLICATIONS INFORMATION

control is used, with closed-loop feedback ensuring that adapter load current remains within limits. Amplifier CL1 in Figure 7 senses the voltage across R_{CL} , connected between the CLP and CLN pins. When this voltage exceeds 100mV, the amplifier will override programmed charging current to limit adapter current to $100\text{mV}/R_{CL}$. A lowpass filter formed by $5\text{k}\Omega$ and 15nF is required to eliminate switching noise. If the current limit is not used, CLN should be connected to CLP.

Note that the $\overline{I_{CL}}$ pin will be asserted when the voltage across R_{CL} is 93mV , before the adapter limit regulation threshold.

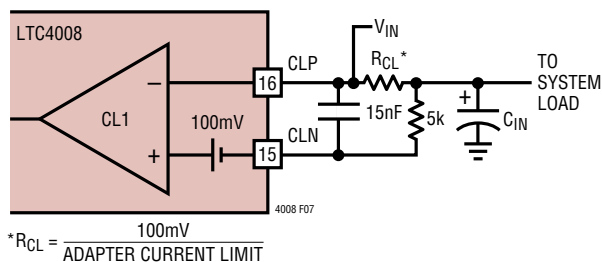


Figure 7. Adapter Current Limiting

Setting Input Current Limit

To set the input current limit, you need to know the minimum wall adapter current rating. Subtract 7% for the input current limit tolerance and use that current to determine the resistor value.

$$R_{CL} = 100\text{mV}/I_{LIM}$$

$$I_{LIM} = \text{Adapter Min Current} - (\text{Adapter Min Current} \cdot 7\%)$$

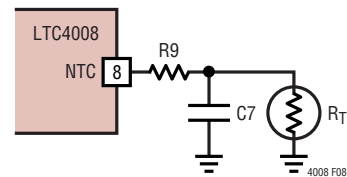


Figure 8. Voltage Divider Thermistor Network

Table 5. Common R_{CL} Resistor Values

ADAPTER RATING (A)	R_{CL} VALUE* (Ω) 1%	R_{CL} POWER DISSIPATION (W)	R_{CL} POWER RATING (W)
1.5	0.06	0.135	0.25
1.8	0.05	0.162	0.25
2	0.045	0.18	0.25
2.3	0.039	0.206	0.25
2.5	0.036	0.225	0.5
2.7	0.033	0.241	0.5
3	0.03	0.27	0.5

* Values shown above are rounded to nearest standard value.

As is often the case, the wall adapter will usually have at least a +10% current limit margin and many times one can simply set the adapter current limit value to the actual adapter rating (see Table 5).

Designing the Thermistor Network

There are several networks that will yield the desired function of voltage vs temperature needed for proper operation of the thermistor. The simplest of these is the voltage divider shown in Figure 8. Unfortunately, since the HIGH/LOW comparator thresholds are fixed internally, there is only one thermistor type that can be used in this network; the thermistor must have a HIGH/LOW resistance ratio of 1:7. If this happy circumstance is true for you, then simply set $R9 = R_{TH(Low)}$

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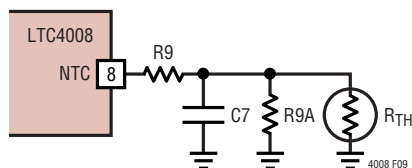


Figure 9. General Thermistor Network

If you are using a thermistor that doesn't have a 1:7 HIGH/LOW ratio, or you wish to set the HIGH/LOW limits to different temperatures, then the more generic network in Figure 9 should work.

Once the thermistor, R_{TH} , has been selected and the thermistor value is known at the temperature limits, then resistors R_9 and R_{9A} are given by:

For NTC thermistors:

$$R_9 = 6 R_{TH(Low)} \cdot R_{TH(High)} / (R_{TH(Low)} - R_{TH(High)})$$

$$R_{9A} = 6 R_{TH(Low)} \cdot R_{TH(High)} / (R_{TH(Low)} - 7 \cdot R_{TH(High)})$$

$$\text{Where } R_{TH(Low)} > 7 \cdot R_{TH(High)}$$

For PTC thermistors:

$$R_9 = 6 R_{TH(Low)} \cdot R_{TH(High)} / (R_{TH(High)} - R_{TH(Low)})$$

$$R_{9A} = 6 R_{TH(Low)} \cdot R_{TH(High)} / (R_{TH(High)} - 7 \cdot R_{TH(Low)})$$

$$\text{Where } R_{TH(High)} > 7 \cdot R_{TH(Low)}$$

Example #1: 10k Ω NTC with custom limits

$$T_{LOW} = 0^\circ\text{C}, T_{HIGH} = 50^\circ\text{C}$$

$$R_{TH} = 10\text{k at } 25^\circ\text{C},$$

$$R_{TH(Low)} = 32.582\text{k at } 0^\circ\text{C}$$

$$R_{TH(High)} = 3.635\text{k at } 50^\circ\text{C}$$

$$R_9 = 24.55\text{k} \rightarrow 24.3\text{k (nearest 1\% value)}$$

$$R_{9A} = 99.6\text{k} \rightarrow 100\text{k (nearest 1\% value)}$$

Example #2: 100k Ω NTC

$$T_{LOW} = 5^\circ\text{C}, T_{HIGH} = 50^\circ\text{C}$$

$$R_{TH} = 100\text{k at } 25^\circ\text{C},$$

$$R_{TH(Low)} = 272.05\text{k at } 5^\circ\text{C}$$

$$R_{TH(High)} = 33.195\text{k at } 50^\circ\text{C}$$

$$R_9 = 226.9\text{k} \rightarrow 226\text{k (nearest 1\% value)}$$

$$R_{9A} = 1.365\text{M} \rightarrow 1.37\text{M (nearest 1\% value)}$$

Example #3: 22k Ω PTC

$$T_{LOW} = 0^\circ\text{C}, T_{HIGH} = 50^\circ\text{C}$$

$$R_{TH} = 22\text{k at } 25^\circ\text{C},$$

$$R_{TH(Low)} = 6.53\text{k at } 0^\circ\text{C}$$

$$R_{TH(High)} = 61.4\text{k at } 50^\circ\text{C}$$

$$R_9 = 43.9\text{k} \rightarrow 44.2\text{k (nearest 1\% value)}$$

$$R_{9A} = 154\text{k}$$

Sizing the Thermistor Hold Capacitor

During the hold interval, C_7 must hold the voltage across the thermistor relatively constant to avoid false readings. A reasonable amount of ripple on NTC during the hold interval is about 10mV to 15mV. Therefore, the value of C_7 is given by:

$$C_7 = t_{HOLD} / (R_9 / 7 \cdot -\ln(1 - 8 \cdot 15\text{mV} / 4.5\text{V}))$$

$$= 10 \cdot R_{RT} \cdot 17.5\text{pF} / (R_9 / 7 \cdot -\ln(1 - 8 \cdot 15\text{mV} / 4.5\text{V}))$$

Example:

$$R_9 = 24.3\text{k}$$

$$R_{RT} = 150\text{k}$$

$$C_7 = 0.28\mu\text{F} \rightarrow 0.27\mu\text{F (nearest value)}$$

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Disabling the Thermistor Function

If the thermistor is not needed, connecting a resistor between DCIN and NTC will disable it. The resistor should be sized to provide at least 10 μ A with the minimum voltage applied to DCIN and 10V at NTC. Do not exceed 30 μ A. Generally, a 301k resistor will work for DCIN less than 15V. A 499k resistor is recommended for DCIN between 15V and 24V.

Using the LTC4008-1 (Refer to Figure 10)

The LTC4008-1 is intended for applications where the battery power is fully isolated from the charger and wall adapter connections. An example application is a system with multiple batteries such that the charger's output power passes through a downstream power path or selector system. Typically these systems also provide isolation and control the wall adapter power. To reduce cost in such systems, the LTC4008-1 removes the re-

quirement for the wall adapter INFET function or blocking diode. Wall adapter or ACP detection is also removed along with micropower shutdown mode. Asserting of the SHDN pin only puts the charger into standby mode. Failure to isolate the battery power from ANY of the LTC4008-1 pins when wall adapter power is removed or lost will only drain the battery at the IC quiescent current rate. More specifically, high current is drawn from the DCIN, CLP and CLN pins. Suggested devices to isolate power from the charger include simple diodes, electrical or mechanical switches or power path control devices such as the LTC4412 low loss PowerPath™ controller.

Because the switcher operation is continuous under nearly all conditions, precautions must be taken to prevent the charger from boosting the input voltage above maximum voltage values on the input capacitors or adapter. Z1 and Q3 will shut down the charger if the input voltage exceeds a safe value.

PowerPath is a trademark of Linear Technology Corporation.

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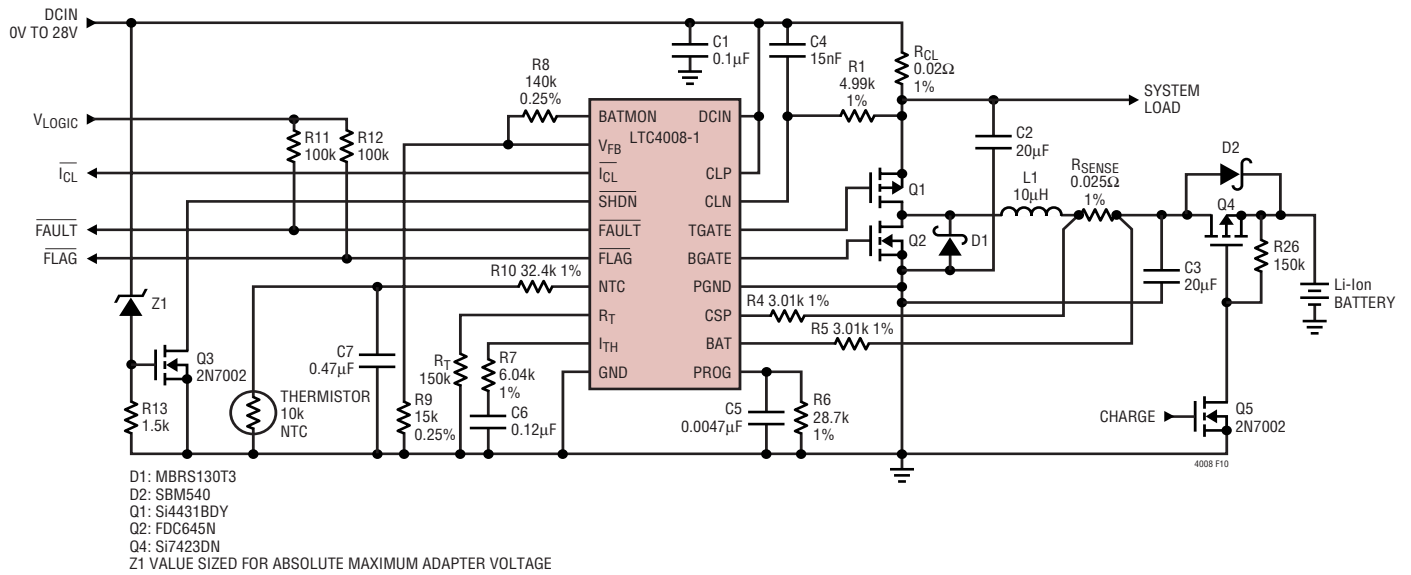


Figure 10. Typical LTC4008-1 Application (12.3V/4A)

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PCB Layout Considerations

For maximum efficiency, the switch node rise and fall times should be minimized. To prevent magnetic and electrical field radiation and high frequency resonant problems, proper layout of the components connected to the IC is essential. (See Figure 11.) Here is a PCB layout priority list for proper layout. Layout the PCB using this specific order.

1. Input capacitors need to be placed as close as possible to switching FET's supply and ground connections. Shortest copper trace connections possible. These parts must be on the same layer of copper. Vias must not be used to make this connection.
2. The control IC needs to be close to the switching FET's gate terminals. Keep the gate drive signals short for a clean FET drive. This includes IC supply pins that connect to the switching FET source pins. The IC can be placed on the opposite side of the PCB relative to above.
3. Place inductor input as close as possible to switching FET's output connection. Minimize the surface area of this trace. Make the trace width the minimum amount needed to support current—no copper fills or pours. Avoid running the connection using multiple layers in parallel. Minimize capacitance from this node to any other trace or plane.
4. Place the output current sense resistor right next to the inductor output but oriented such that the IC's current sense feedback traces going to resistor are not long. The feedback traces need to be routed together as a single pair on the same layer at any given time with smallest trace spacing possible. Locate any filter component on these traces next to the IC and not at the sense resistor location.
5. Place output capacitors next to the sense resistor output and ground.
6. Output capacitor ground connections need to feed into same copper that connects to the input capacitor ground before tying back into system ground.

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PCB Layout Considerations (cont.)

7. Connection of switching ground to system ground or internal ground plane should be single point. If the system has an internal system ground plane, a good way to do this is to cluster vias into a single star point to make the connection.
8. Route analog ground as a trace tied back to IC ground (analog ground pin if present) before connecting to any other ground. Avoid using the system ground plane. CAD trick: make analog ground a separate ground net and use a 0Ω resistor to tie analog ground to system ground.
9. A good rule of thumb for via count for a given high current path is to use 0.5A per via. Be consistent.
10. If possible, place all the parts listed above on the same PCB layer.
11. Copper fills or pours are good for all power connections except as noted above in Rule 3. You can also use copper planes on multiple layers in parallel too—this helps with thermal management and lower trace inductance improving EMI performance further.
12. For best current programming accuracy provide a Kelvin connection from R_{SENSE} to CSP and BAT. See Figure 12 as an example.

It is important to keep the parasitic capacitance on the R_{T} , CSP and BAT pins to a minimum. The traces connecting these pins to their respective resistors should be as short as possible.

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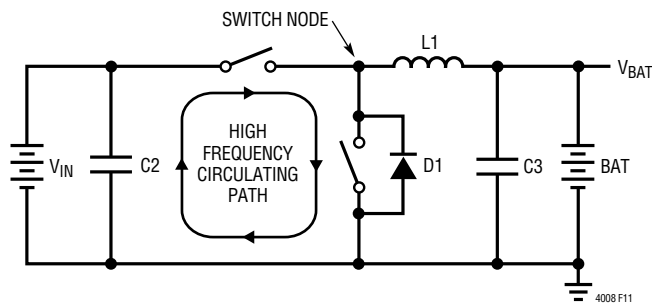


Figure 11. High Speed Switching Path

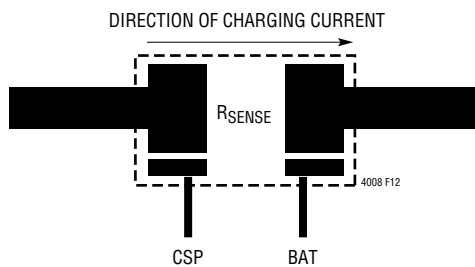
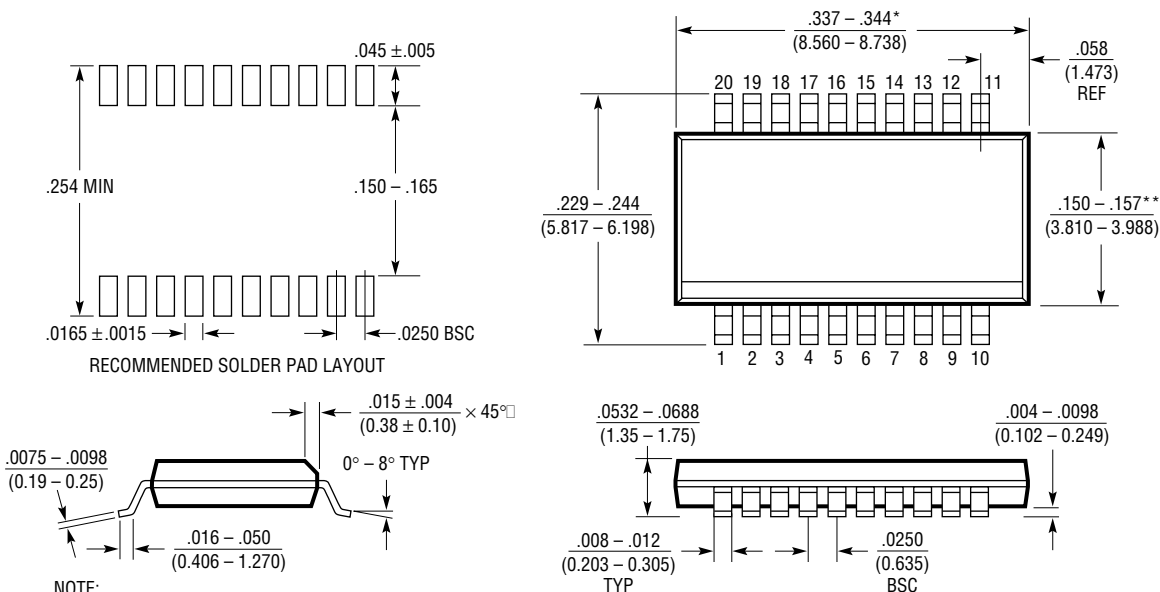


Figure 12. Kelvin Sensing of Charging Current

PACKAGE DESCRIPTION

GN Package 20-Lead Plastic SSOP (Narrow .150 Inch) (Reference LTC DWG # 05-08-1641)



NOTE:

1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

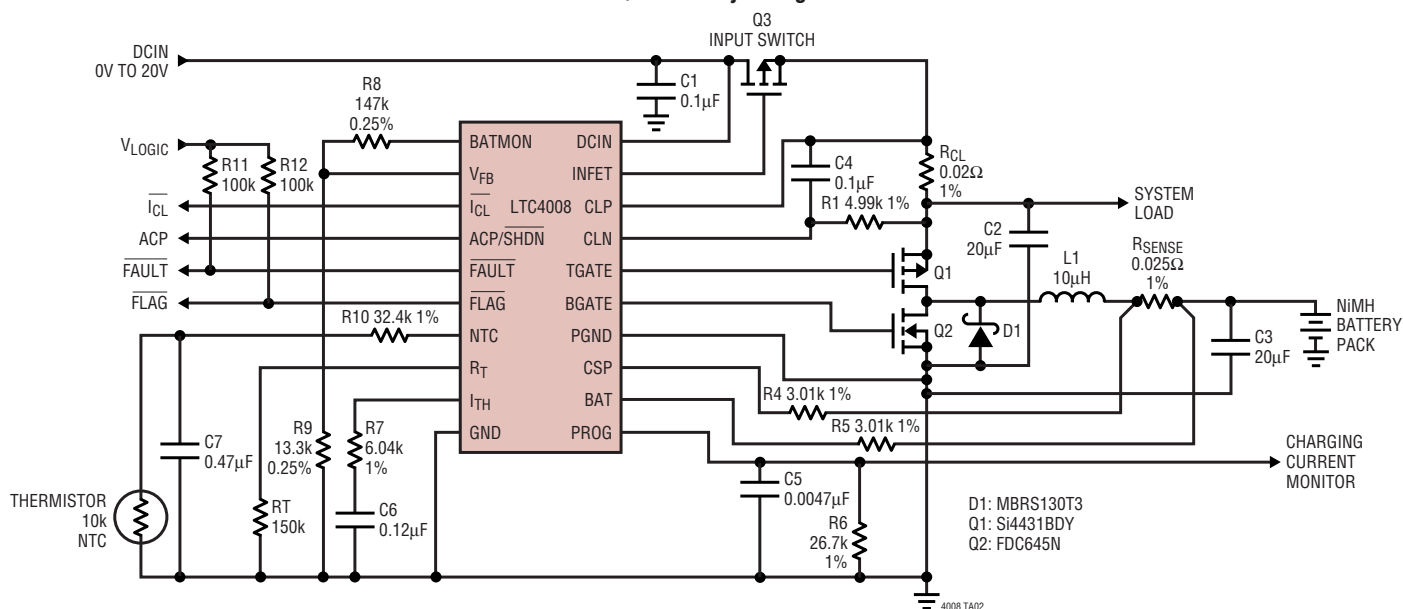
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN20 (SSOP) 0204

LTC4008

TYPICAL APPLICATION

NiMH/4A Battery Charger



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT [®] 1511	3A Constant-Current/Constant-Voltage Battery Charger	High Efficiency, Minimum External Components to Fast Charge Lithium, NiMH and NiCd Batteries
LT1513	Sepic Constant- or Programmable- Current/Constant-Voltage Battery Charger	Charger Input Voltage May be Higher, Equal to or Lower Than Battery Voltage, 500kHz Switching Frequency
LT1571	1.5A Switching Charger	1- or 2-Cell Li-Ion, 500kHz or 200kHz Switching Frequency, Termination Flag
LTC1628-PG	2-Phase, Dual Synchronous Step-Down Controller	Minimizes C _{IN} and C _{OUT} , Power Good Output, 3.5V ≤ V _{IN} ≤ 36V
LTC1709 Family	2-Phase, Dual Synchronous Step-Down Controller with VID	Up to 42A Output, Minimum C _{IN} and C _{OUT} , Uses Smallest Components for Intel and AMD Processors
LTC1729	Li-Ion Battery Charger Termination Controller	Trickle Charge Preconditioning, Temperature Charge Qualification, Time or Charge Current Termination, Automatic Charger and Battery Detection, and Status Output
LT1769	2A Switching Battery Charger	Constant-Current/Constant-Voltage Switching Regulator, Input Current Limiting Maximizes Charge Current
LTC1778	Wide Operating Range, No R _{SENSE} [™] Synchronous Step-Down Controller	2% to 90% Duty Cycle at 200kHz, Stable with Ceramic C _{OUT}
LTC1960	Dual Battery Charger/Selector with SPI Interface	Simultaneous Charge or Discharge of Two Batteries, DAC Programmable Current and Voltage, Input Current Limiting Maximizes Charge Current
LTC3711	No R _{SENSE} Synchronous Step-Down Controller with VID	3.5V ≤ V _{IN} ≤ 36V, 0.925V ≤ V _{OUT} ≤ 2V, for Transmeta, AMD and Intel Mobile Processors
LTC4006	Small, High Efficiency, Fixed Voltage, Lithium-Ion Battery Charger with Termination	Complete Charger for 3- or 4-Cell Li-Ion Batteries, AC Adapter Current Limit and Thermistor Sensor, 16-Pin Narrow SSOP Package
LTC4007	High Efficiency, Programmable Voltage Battery Charger with Termination	Complete Charger for 3- or 4-Cell Li-Ion Batteries, AC Adapter Current Limit, Thermistor Sensor and Indicator Outputs
LTC4100	Smart Battery Charger Controller	SMBus Rev 1.1 Compliant

No R_{SENSE} is a trademark of Linear Technology Corporation.