LTC3405A-1.375

1.375V, 1.5MHz, 300mA Synchronous Step-Down Regulators in ThinSOT

FEATURES

- **High Efficiency: Up to 90%**
- **Very Low Quiescent Current: Only 20μA During Operation**
- **300mA Output Current at V_{IN} = 3V**
- **2.5V to 5.5V Input Voltage Range**
- **1.5MHz Constant Frequency Operation**
- **No Schottky Diode Required**
- **Low Dropout Operation: 100% Duty Cycle**
- **Stable with Ceramic Capacitors**
- Shutdown Mode Draws <1μA Supply Current
- ±3% Output Voltage Accuracy
- Current Mode Operation for Excellent Line and Load Transient Response
- Overtemperature Protected
- Low Profile (1mm) ThinSOT™ Package

APPLICATIONS

- Cellular Telephones
- Personal Information Appliances
- Wireless and DSL Modems
- Digital Still Cameras
- MP3 Players
- Portable Instruments

DESCRIPTION

The LTC®3405A-1.375 is a high efficiency monolithic synchronous buck regulator using a constant frequency, current mode architecture. Supply current during operation is only 20μA and drops to <1μA in shutdown. The 2.5V to 5.5V input voltage range makes the LTC3405A-1.375 ideally suited for single Li-Ion battery-powered applications. 100% duty cycle provides low dropout operation, extending battery life in portable systems.

Switching frequency is internally set at 1.5MHz, allowing the use of small surface mount inductors and capacitors.

The LTC3405A-1.375 is specifically designed to work well with ceramic output capacitors, achieving very low output voltage ripple and a small PCB footprint.

The internal synchronous switch increases efficiency and eliminates the need for an external Schottky diode. The LTC3405A-1.375 is available in a low profile (1mm) ThinSOT package.

For other output voltages, refer to the LTC3405A and LTC3405A-1.5/LTC3405A-1.8 data sheets.

TYPICAL APPLICATION

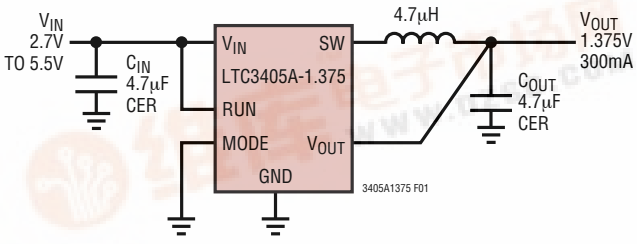


Figure 1a. High Efficiency Step-Down Converter

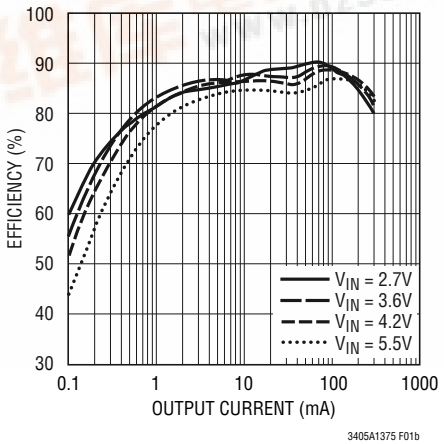


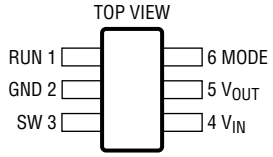
Figure 1b. Efficiency vs Load Current

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage ..... –0.3V to 6V
MODE, RUN, V_{OUT} Voltages ..... –0.3V to V_{IN}
SW Voltage ..... –0.3V to (V_{IN} + 0.3V)
P-Channel Switch Source Current (DC) 400mA
N-Channel Switch Sink Current (DC) 400mA
Peak SW Sink and Source Current 630mA
Operating Temperature Range (Note 2) .. –40°C to 85°C
Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S6 PACKAGE
6-LEAD PLASTIC TSOT-23

T_{JMAX} = 125°C, θ_{JA} = 250°C/W

ORDER PART NUMBER
LTC3405AES6-1.375
S6 PART MARKING
LTBRP

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = 3.6V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{PK}	Peak Inductor Current	V_{IN} = 3V, V_{OUT} = 1.238V, Duty Cycle < 35%		375	500	625	mA
V_{OUT}	Regulated Output Voltage	MODE = 3.6V	●	1.334	1.375	1.416	V
ΔV_{OVL}	ΔOutput Overvoltage Lockout	$\Delta V_{OVL} = V_{OVL} - V_{OUT}$		2	5.6	9.3	%
ΔV_{OUT}	Output Voltage Line Regulation	V_{IN} = 2.5V to 5.5V	●		0.04	0.4	%/V
$V_{LOADREG}$	Output Voltage Load Regulation				0.5		%
V_{IN}	Input Voltage Range		●	2.5		5.5	V
I_S	Input DC Bias Current Pulse Skipping Mode Burst Mode® Operation Shutdown	(Note 4) V_{OUT} = 1.238V, MODE = 3.6V, I_{LOAD} = 0A V_{OUT} = 1.42V, MODE = 0V, I_{LOAD} = 0A V_{RUN} = 0V, V_{IN} = 4.2V			 300 20 0.1	 400 35 1	 µA µA µA
f_{OSC}	Oscillator Frequency	V_{OUT} = 1.375V V_{OUT} = 0V	●	1.2	1.5 170	1.8	MHz kHz
R_{PFET}	$R_{DS(ON)}$ of P-Channel FET	I_{SW} = 100mA			0.7	0.85	Ω
R_{NFET}	$R_{DS(ON)}$ of N-Channel FET	I_{SW} = –100mA			0.6	0.90	Ω
I_{LSW}	SW Leakage	V_{RUN} = 0V, V_{SW} = 0V or 5V, V_{IN} = 5V			±0.01	±1	µA
V_{RUN}	RUN Threshold		●	0.3	1	1.5	V
I_{RUN}	RUN Leakage Current		●		±0.01	±1	µA
V_{MODE}	MODE Threshold		●	0.3	1.5	2	V
I_{MODE}	MODE Leakage Current		●		±0.01	±1	µA

Burst Mode is a registered trademark of Linear Technology Corporation.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC3405A-1.375 is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

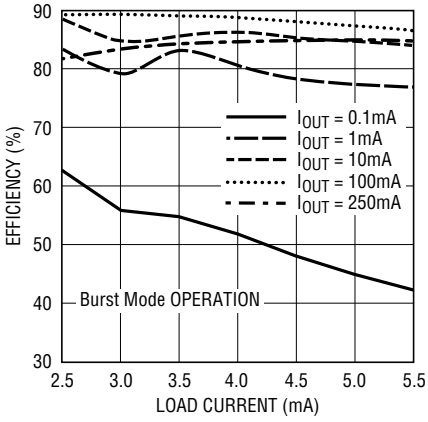
LTC3405A-1.375: $T_J = T_A + (P_D)(250°C/W)$

Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

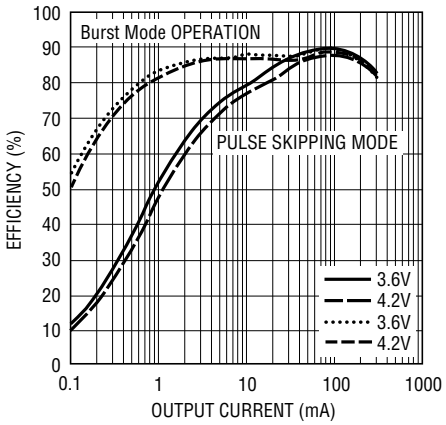
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

(From Figure1a)

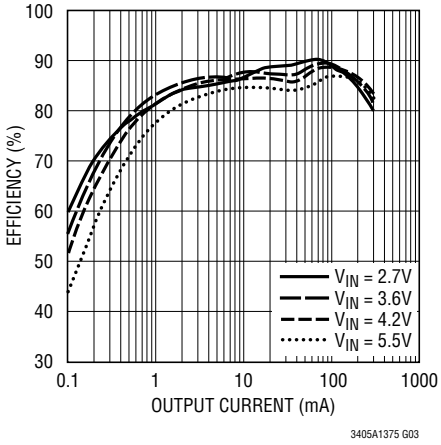
Efficiency vs Input Voltage



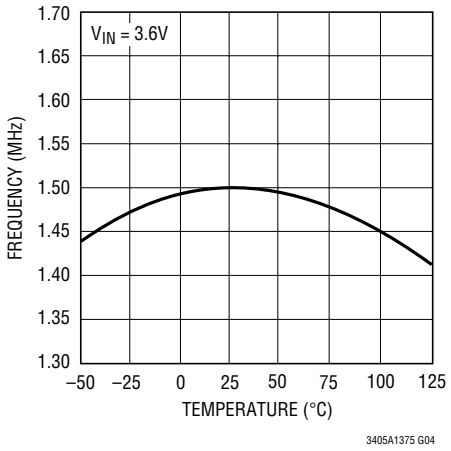
Efficiency vs Output Current



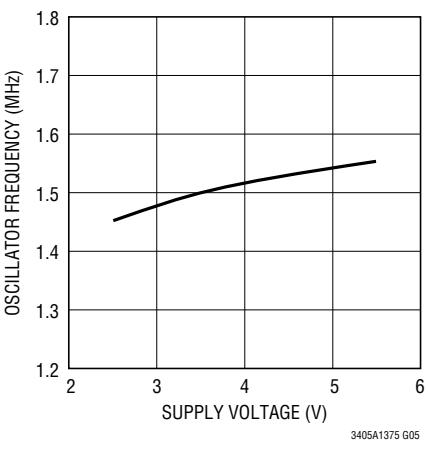
Efficiency vs Output Current



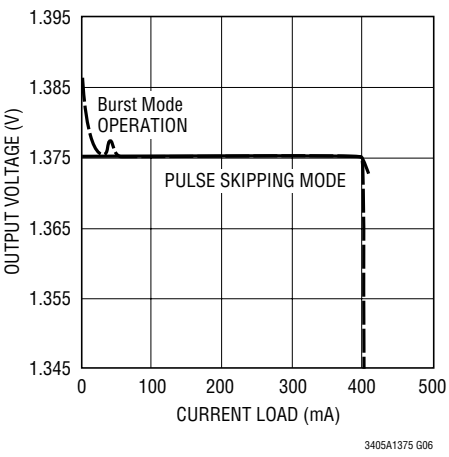
Oscillator Frequency vs Temperature



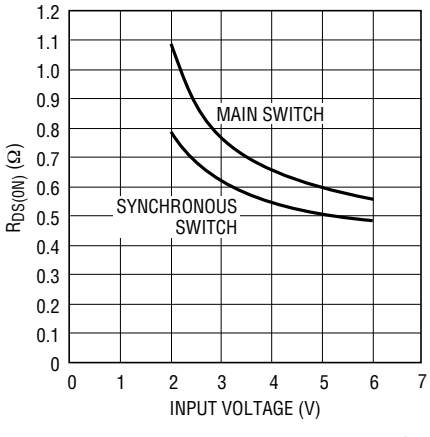
Oscillator Frequency vs Supply Voltage



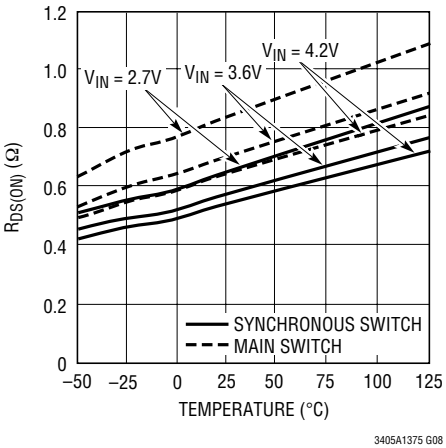
Output Voltage vs Load Current



$R_{DS(ON)}$ vs Input Voltage



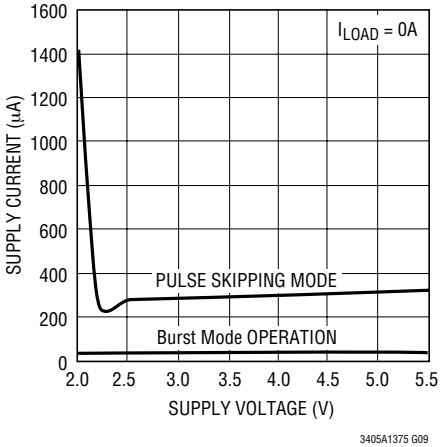
$R_{DS(ON)}$ vs Temperature



TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

(From Figure 1a)

Dynamic Supply Current vs Supply Voltage



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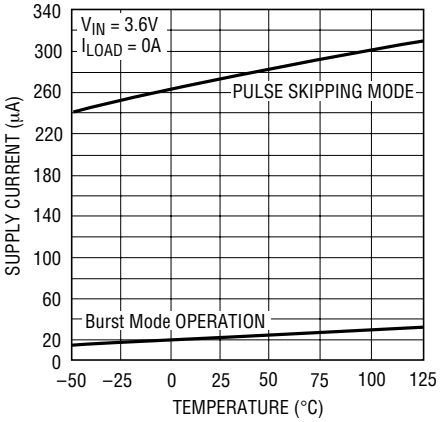
Dynamic Supply Current vs Temperature



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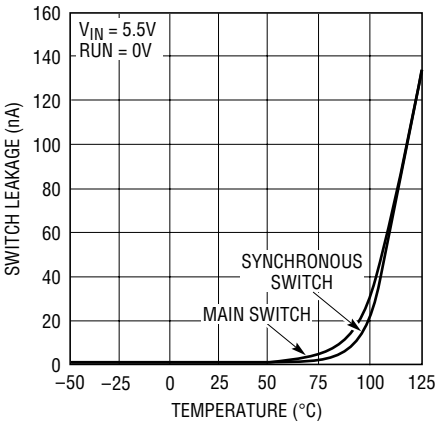
Switch Leakage vs Temperature



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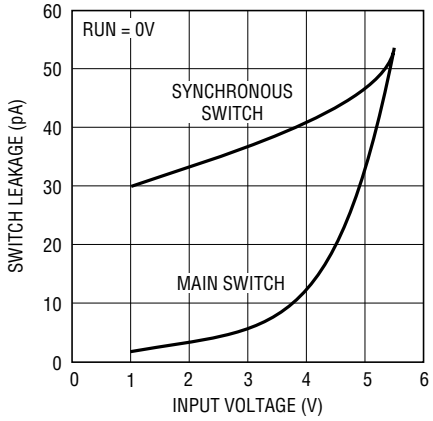
Switch Leakage vs Input Voltage



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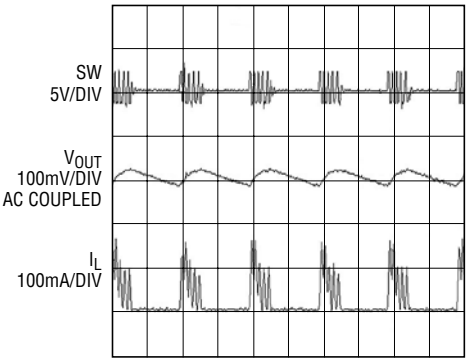
Burst Mode Operation



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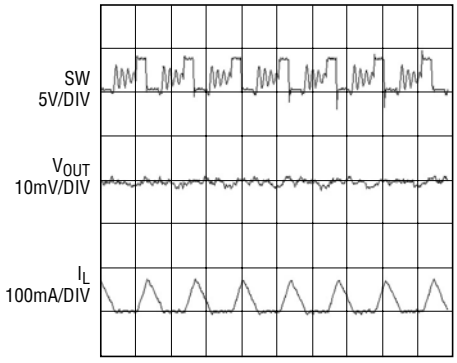
Pulse Skipping Mode Operation



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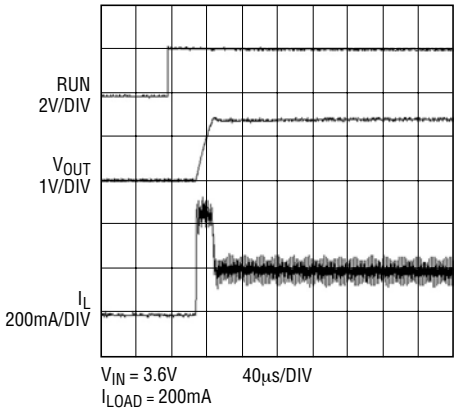
Start-Up from Shutdown



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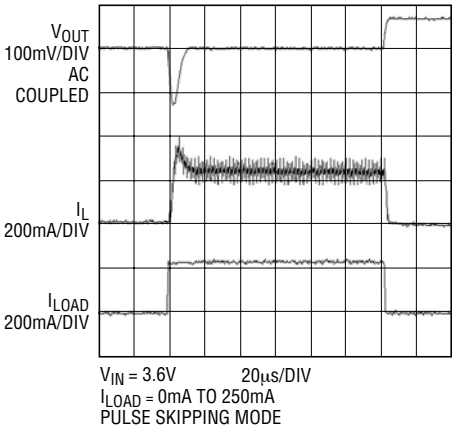
Load Step



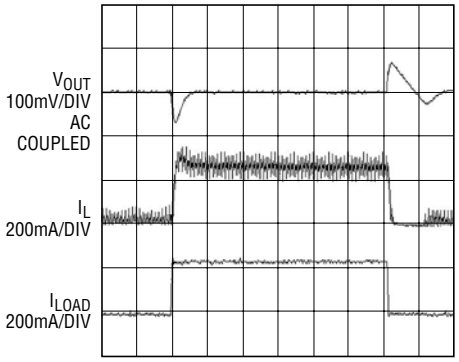
3405A1375 G16

TYPICAL PERFORMANCE CHARACTERISTICS

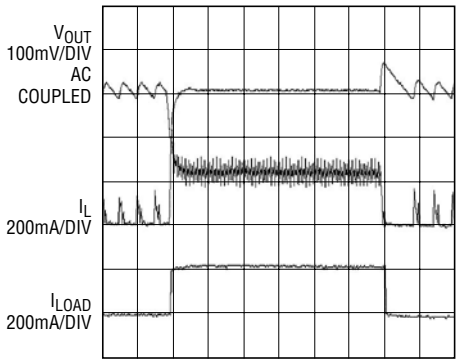
T_A = 25°C unless otherwise noted.

(From Figure 1a)

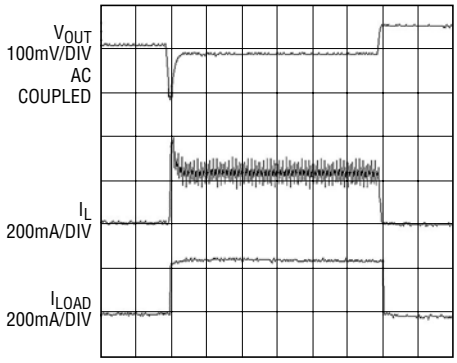
Load Step



Load Step



Load Step



PIN FUNCTIONS

RUN (Pin 1): Run Control Input. Forcing this pin above 1.5V enables the part. Forcing this pin below 0.3V shuts down the device. In shutdown, all functions are disabled drawing <1μA supply current. Do not leave RUN floating.

GND (Pin 2): Ground Pin.

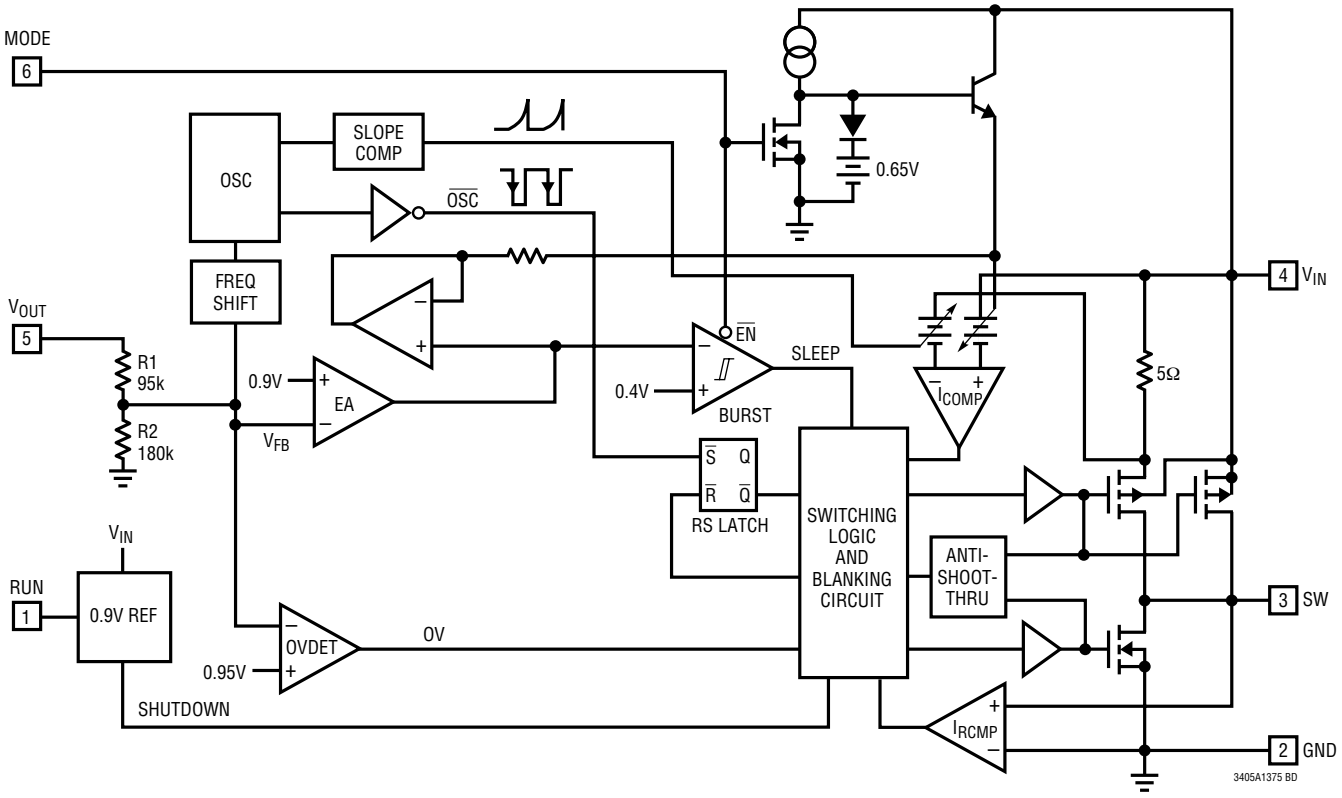
SW (Pin 3): Switch Node Connection to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.

V_{IN} (Pin 4): Main Supply Pin. Must be closely decoupled to GND, Pin 2, with a 2.2μF or greater ceramic capacitor.

V_{OUT} (Pin 5): Output Voltage Feedback Pin. An internal resistive divider divides the output voltage down for comparison to the internal 0.9V reference voltage.

MODE (Pin 6): Mode Select Input. To select pulse skipping mode, tie to V_{IN}. Grounding this pin selects Burst Mode operation. Do not leave this pin floating.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC3405A-1.375 uses a constant frequency, current mode step-down architecture. The main (P-channel MOSFET) and synchronous (N-channel MOSFET) switches are internal. During normal operation, the internal top power MOSFET is turned on each cycle when the oscillator sets the RS latch, and turned off when the current comparator, I_{COMP}, resets the RS latch. The peak inductor current at which I_{COMP} resets the RS latch, is controlled by the output of error amplifier EA. When the load current increases, the output voltage decreases which causes a slight decrease in V_{FB} relative to the 0.9V reference, which in turn, causes the EA amplifier's output voltage to increase until the average inductor current matches the new load current. While the top MOSFET is off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current reversal comparator I_{RCMP}, or the beginning of the next clock cycle.

Comparator OVDET guards against transient overshoots >5.6% by turning the main switch off and keeping it off until the fault is removed.

Burst Mode Operation

The LTC3405A-1.375 is capable of Burst Mode operation in which the internal power MOSFETs operate intermittently based on load demand. To enable Burst Mode operation, simply connect the MODE pin to GND. To disable Burst Mode operation and enable PWM pulse skipping mode, connect the MODE pin to V_{IN} or drive it with a logic high (V_{MODE} > 1.5V). In this mode, the efficiency is lower at light loads, but becomes comparable to Burst Mode operation when the output load exceeds 25mA. The advantage of pulse skipping mode is lower output ripple and less interference to audio circuitry.

OPERATION (Refer to Functional Diagram)

When the converter is in Burst Mode operation, the peak current of the inductor is set to approximately 100mA regardless of the output load. Each burst event can last from a few cycles at light loads to almost continuously cycling with short sleep intervals at moderate loads. In between these burst events, the power MOSFETs and any unneeded circuitry are turned off, reducing the quiescent current to 20μA. In this sleep state, the load current is being supplied solely from the output capacitor. As the output voltage droops, the EA amplifier's output rises above the sleep threshold signaling the BURST comparator to trip and turn the top MOSFET on. This process repeats at a rate that is dependent on the load demand.

Short-Circuit Protection

When the output is shorted to ground, the frequency of the oscillator is reduced to about 210kHz, 1/7 the nominal frequency. This frequency foldback ensures that the inductor current has more time to decay, thereby preventing runaway. The oscillator's frequency will progressively increase to 1.5MHz when V_{OUT} rises above 0V.

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant frequency architectures by preventing subharmonic oscillations at high duty cycles. It is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 40%. Normally, this results in a reduction of maximum inductor peak current for duty cycles >40%. However, the LTC3405A-1.375 uses a patented scheme that counteracts this compensating ramp, which allows the maximum inductor peak current to remain unaffected throughout all duty cycles.

APPLICATIONS INFORMATION

The basic LTC3405A-1.375 application circuit is shown in Figure 1. External component selection is driven by the load requirement and begins with the selection of L followed by C_{IN} and C_{OUT}.

Inductor Selection

For most applications, the inductor value will fall in the range of 2.2μH to 10μH. Its value is determined by the desired ripple current. Large value inductors lower ripple current and small value inductors result in higher ripple currents. Higher V_{IN} or V_{OUT} also increases the ripple current as shown in equation 1. A reasonable starting point for setting ripple current is ΔI_L = 120mA (40% of 300mA).

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (1)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 360mA rated inductor should be enough for most applications (300mA + 60mA). For better efficiency, choose a low DC-resistance inductor.

The inductor value also has an effect on Burst Mode operation. The transition to low current operation begins when the inductor current peaks fall to approximately 100mA. Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to increase.

Inductor Core Selection

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs size requirements and any radiated field/EMI requirements than on what the LTC3405A-1.375 requires to operate.

APPLICATIONS INFORMATION

Table 1 shows some typical surface mount inductors that work well in LTC3405A-1.375 applications.

Table 1. Representative Surface Mount Inductors

MANUFACTURER	PART NUMBER	VALUE	MAX DC CURRENT	DCR	HEIGHT
Taiyo Yuden	LB2016T2R2M	2.2µH	315mA	0.13Ω	1.6mm
	LB2012T2R2M	2.2µH	240mA	0.23Ω	1.25mm
	LB2016T3R3M	3.3µH	280mA	0.2Ω	1.6mm
Panasonic	ELT5KT4R7M	4.7µH	950mA	0.2Ω	1.2mm
Murata	LQH32CN2R2M33	4.7µH	450mA	0.2Ω	2mm
Taiyo Yuden	LB2016T4R7M	4.7µH	210mA	0.25Ω	1.6mm
Panasonic	ELT5KT6R8M	6.8µH	760mA	0.3Ω	1.2mm
Panasonic	ELT5KT100M	10µH	680mA	0.36Ω	1.2mm
Sumida	CMD4D116R8MC	6.8µH	620mA	0.23Ω	1.2mm

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ required } I_{RMS} \cong I_{OMAX} \frac{\left[V_{OUT}\left(V_{IN} - V_{OUT}\right)\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}}\right)$$

where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum. These are specially constructed and tested for low ESR so they give the lowest ESR for a given volume. Other capacitor types include Sanyo POSCAP, Kemet T510 and T495 series, and Sprague 593D and 595D series. Consult the manufacturer for other specific recommendations.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. Because the LTC3405A-1.375's control loop does not depend on the output capacitor's ESR for stable operation, ceramic capacitors can be used freely to achieve very low output ripple and small circuit size.

Care must be taken when ceramic capacitors are used at the input and the output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN}, large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

APPLICATIONS INFORMATION

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses in LTC3405A-1.375 circuits: V_{IN} quiescent current and I^2R losses. The V_{IN} quiescent current loss dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence as illustrated in Figure 2.

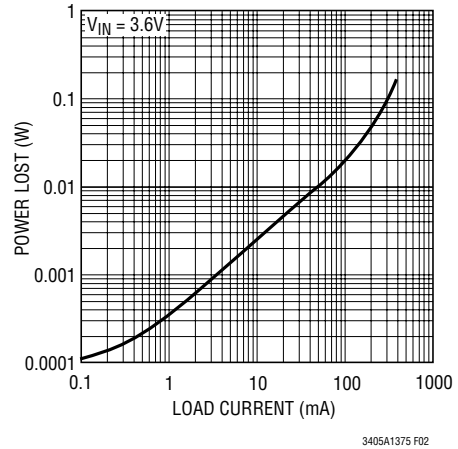


Figure 2. Power Lost vs Load Current

1. The V_{IN} quiescent current is due to two components: the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge, dQ, moves from V_{IN} to ground. The resulting dQ/dt is the current out of V_{IN} that is typically larger than the DC bias current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$ where Q_T and Q_B are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.
2. I^2R losses are calculated from the resistances of the internal switches, R_{SW}, and external inductor R_L. In continuous mode, the average output current flowing through inductor L is "chopped" between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

   $$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 – DC)$$

   The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Charateristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% total additional loss.

Thermal Considerations

In most applications, the LTC3405A-1.375 does not dissipate much heat due to its high efficiency. But, in applications where they run at high ambient temperature with low supply voltage, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the SW node will become high impedance.

To keep the LTC3405A-1.375 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_R = (P_D)(\theta_{JA})$$

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where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature, T_J, is given by:

$$T_J = T_A + T_R$$

where T_A is the ambient temperature.

As an example, consider the LTC3405A-1.375 with an input voltage of 2.7V, a load current of 300mA and an ambient temperature of 70°C. From the typical performance graph of switch resistance, the $R_{DS(ON)}$ of the P-channel switch at 70°C is approximately 0.94Ω and the $R_{DS(ON)}$ of the N-channel synchronous switch is approximately 0.75Ω.

The series resistance looking into the SW pin is:

$$R_{SW} = 0.95\Omega\ (0.51) + 0.75\Omega\ (0.49) = 0.85\Omega$$

Therefore, power dissipated by the part is:

$$P_D = I_{LOAD}^2 \bullet R_{SW} = 76.5mW$$

For the SOT-23 package, the θ_{JA} is 250°C/W. Thus, the junction temperature of the regulator is:

$$T_J = 70°C + (0.0765)(250) = 89.1°C$$

which is well below the maximum junction temperature of 125°C.

Note that at higher supply voltages, the junction temperature is lower due to reduced switch resistance ($R_{DS(ON)}$).

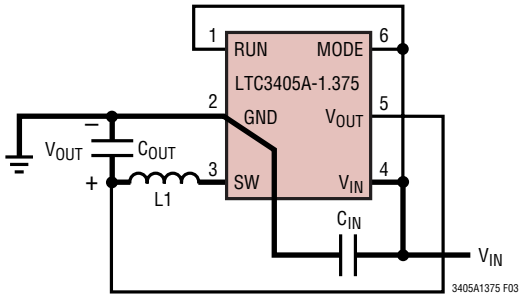
Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to (ΔI_{LOAD} • ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, which generates a feedback error signal. The regulator loop then acts to return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem. For a detailed explanation of switching control loop theory, see Application Note 76.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3405A-1.375. These items are also illustrated graphically in Figures 3 and 4. Check the following in your layout:

1. The power traces, consisting of the GND trace, the SW trace and the V_{IN} trace should be kept short, direct and wide.
2. Does the (+) plate of C_{IN} connect to V_{IN} as closely as possible? This capacitor provides the AC current to the internal power MOSFETs.
3. Keep the (–) plates of C_{IN} and C_{OUT} as close as possible.



BOLD LINES INDICATE HIGH CURRENT PATHS

Figure 3. LTC3405A-1.375 Layout Diagram

Design Example

As a design example, assume the LTC3405A-1.375 is used in a single lithium-ion battery-powered cellular phone application. The V_{IN} will be operating from a maximum of 4.2V down to about 2.7V. The load current requirement is a maximum of 0.15A but most of the time it will be in standby mode, requiring only 2mA. Efficiency at both low and high load currents is important. Output voltage is 1.375V. With this information we can calculate L using equation (1),

$$L = \frac{1}{(f)(\Delta I_L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (3)$$

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Substituting V_{OUT} = 1.375V, V_{IN} = 4.2V, ΔI_L = 60mA and f = 1.5MHz in equation (3) gives:

$$L = \frac{1.375V}{1.5MHz(60mA)}\left(1-\frac{1.375V}{4.2V}\right) \cong 10\mu H$$

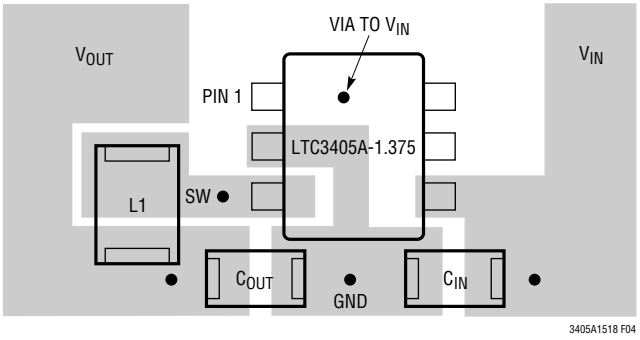


Figure 4. LTC3405A-1.375 Suggested Layout

For best efficiency choose a 200mA or greater inductor with less than 0.3Ω series resistance.

C_{IN} will require an RMS current rating of at least 0.125A ≅ $I_{LOAD(MAX)}$/2 at temperature and C_{OUT} will require an ESR of less than 0.5Ω. In most cases, a ceramic capacitor will satisfy this requirement.

Figure 5 shows the complete circuit along with its efficiency curve.

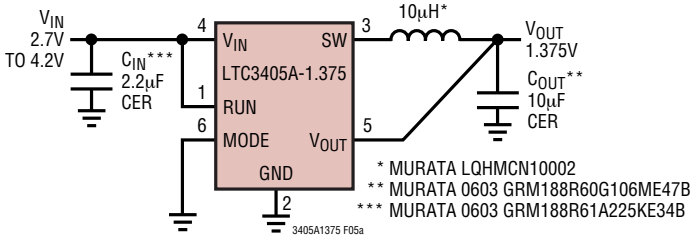


Figure 5a. Small Footprint Application

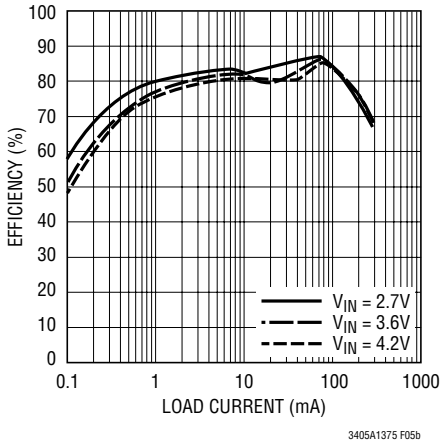


Figure 5b. LTC3405A-1.375 Small Footprint Efficiency

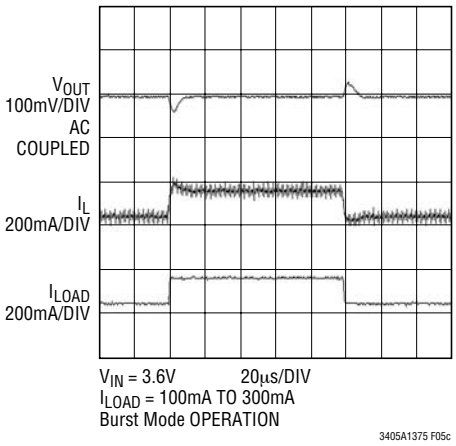
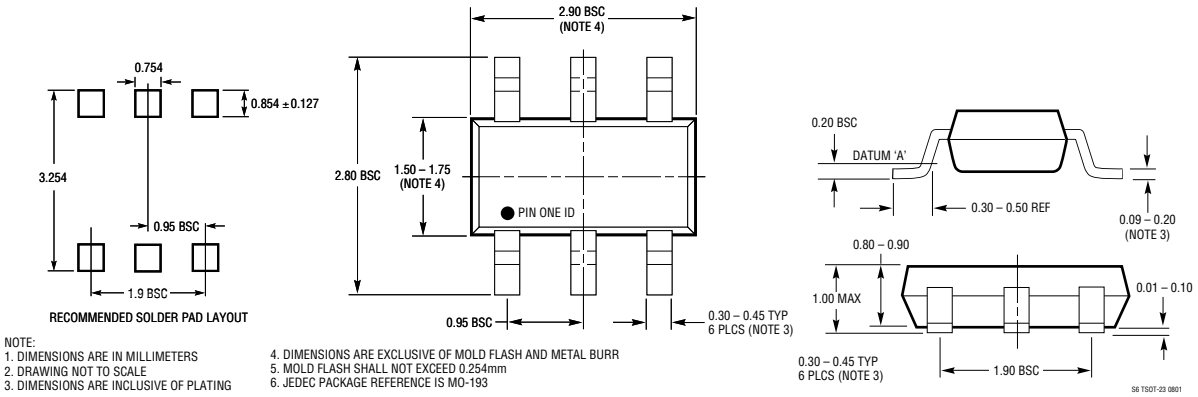


Figure 5c.

PACKAGE DESCRIPTION

S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1616	500mA (I_{OUT}), 1.4MHz, High Efficiency Step-Down DC/DC Converter	90% Efficiency, V_{IN} = 3.6V to 25V, V_{OUT} = 1.25V, I_Q = 1.9mA I_{SD} = <1μA, ThinSOT Package
LT1676	450mA (I_{OUT}), 100kHz, High Efficiency Step-Down DC/DC Converter	90% Efficiency, V_{IN} = 7.4V to 60V, V_{OUT} = 1.24V, I_Q = 3.2mA I_{SD} = 2.5μA, S8 Package
LT1765	25V, 2.75A (I_{OUT}), 1.25MHz, High Efficiency Step-Down DC/DC Converter	90% Efficiency, V_{IN} = 3.0V to 25V, V_{OUT} = 1.20V, I_Q = 1mA I_{SD} = 15μA, S8, TSSOP16E Packages
LT1776	500mA (I_{OUT}), 200kHz, High Efficiency Step-Down DC/DC Converter	90% Efficiency, V_{IN} = 7.4V to 40V, V_{OUT} = 1.24V, I_Q = 3.2mA I_{SD} = 30μA, N8,S8 Packages
LTC1878	600mA (I_{OUT}), 550kHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} = 2.7V to 6V, V_{OUT} = 0.8V, I_Q = 10μA I_{SD} = <1μA, MS8 Package
LTC1879	1.20A (I_{OUT}), 550kHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} = 2.7V to 10V, V_{OUT} = 0.8V, I_Q = 15μA I_{SD} = <1μA, TSSOP16 Package
LTC3404	600mA (I_{OUT}), 1.4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} = 2.7V to 6V, V_{OUT} = 0.8V, I_Q = 10μA I_{SD} = <1μA, MS8 Package
LTC3405/LTC3405A LTC3405A-1.5 LTC3405A-1.8	300mA (I_{OUT}), 1.5MHz, Synchronous Step-Down DC/DC Converters	95% Efficiency, V_{IN} = 2.7V to 6V, V_{OUT} = 0.8V, I_Q = 20μA I_{SD} = <1μA, ThinSOT Package
LTC3406/LTC3406B	600mA (I_{OUT}) 1.5MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} = 2.5V to 5.5V, V_{OUT} = 0.6V, I_Q = 20μA I_{SD} = <1μA, ThinSOT Package
LTC3411	1.25A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} = 2.5V to 5.5V, V_{OUT} = 0.8V, I_Q = 60μA I_{SD} = <1μA, MS10 Package
LTC3412	2.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} = 2.5V to 5.5V, V_{OUT} = 0.8V, I_Q = 60μA I_{SD} = <1μA, TSSOP16E Package
LTC3413	3A (I_{OUT}), Sink/Source, 2MHz, Monolithic Synchronous Regulator for DDR/QDR Memory Termination	90% Efficiency, V_{IN} = 2.25V to 5.5V, V_{OUT} = $V_{REF/2}$, I_Q = 280μA I_{SD} = <1μA, TSSOP16E Package
LT3430	60V, 2.75A (I_{OUT}), 200kHz, High Efficiency Step-Down DC/DC Converter	90% Efficiency, V_{IN} = 5.5V to 60V, V_{OUT} = 1.20V, I_Q = 2.5mA I_{SD} = 25μA, TSSOP16E Package
LTC3440	600mA (I_{OUT}), 2MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN} = 2.5V to 5.5V, V_{OUT} = 2.5V, I_Q = 25μA I_{SD} = <1μA, MS Package