查询LTC2420IS8供应商 捷多邦，专业PCB打样工厂，24小时加急出货

LTC2420

20-Bit µPower No Latency ΔΣ™ ADC in SO-8

FEATURES

- **20-Bit ADC in SO-8 Package**
- **8ppm INL, No Missing Codes at 20 Bits**
- **4ppm Full-Scale Error**
- **0.5ppm Offset**
- **1.2ppm Noise**
- **Digital Filter Settles in a Single Cycle. Each Conversion Is Accurate, Even After an Input Step**
- **Fast Mode: 16-Bit Noise, 12 Bits TUE at 100sps**
- Internal Oscillator—No External Components Required
- 110dB Min, 50Hz/60Hz Notch Filter
- Reference Input Voltage: 0.1V to V_{CC}
- Live Zero—Extended Input Range Accommodates 12.5% Overrange and Underrange
- Single Supply 2.7V to 5.5V Operation
- Low Supply Current (200µA) and Auto Shutdown
- Pin Compatible with 24-Bit LTC2400

APPLICATIONS

- Weight Scales
- Direct Temperature Measurement
- Gas Analyzers
- Strain Gauge Transducers
- Instrumentation
- Data Acquisition
- Industrial Process Control
- 4-Digit DVMs

DESCRIPTION

The LTC®2420 is a micropower 20-bit A/D converter with an integrated oscillator, 8ppm INL and 1.2ppm RMS noise that operates from 2.7V to 5.5V. It uses delta-sigma technology and provides a digital filter that settles in a single cycle for multiplexed applications. Through a single pin, the LTC2420 can be configured for better than 110dB rejection at 50Hz or 60Hz ±2%, or it can be driven by an external oscillator for a user-defined rejection frequency in the range 1Hz to 800Hz. The internal oscillator requires no external frequency setting components.

The converter accepts any external reference voltage from 0.1V to V_{CC}. With its extended input conversion range of –12.5% V_{REF} to 112.5% V_{REF}, the LTC2420 smoothly resolves the offset and overrange problems of preceding sensors or signal conditioning circuits.

The LTC2420 communicates through a flexible 3-wire digital interface which is compatible with SPI and MICROWIRE™ protocols.

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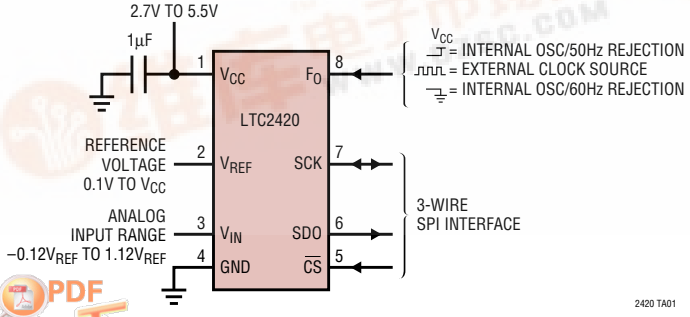
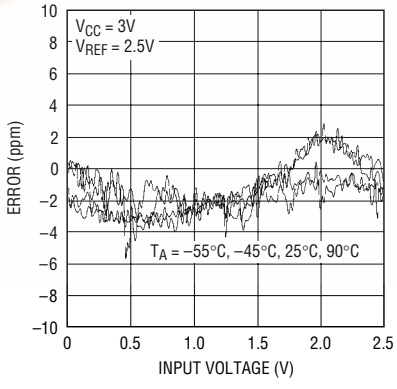
No Latency ΔΣ is a trademark of Linear Technology Corporation.
MICROWIRE is a trademark of National Semiconductor Corporation.

TYPICAL APPLICATION



2420 TA01

Total Unadjusted Error (3V Supply)



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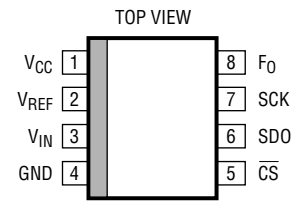
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) to GND ..... –0.3V to 7V
Analog Input Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Reference Input Voltage to GND .. –0.3V to (V_{CC} + 0.3V)
Digital Input Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Digital Output Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Operating Temperature Range
LTC2420C ..... 0°C to 70°C
LTC2420I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC2420CS8 LTC2420IS8
S8 PART MARKING
2420 2420I

Consult factory for Military grade parts.

CONVERTER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	0.1V ≤ V_{REF} ≤ V_{CC}, (Note 5)	●	20			Bits
Integral Nonlinearity	V_{REF} = 2.5V (Note 6) V_{REF} = 5V (Note 6)	● ●		4 8	10 20	ppm of V_{REF} ppm of V_{REF}
Integral Nonlinearity (Fast Mode)	V_{REF} = 5V, V_{REF} = 2.5V, 100 Samples/Second, f_O = 2.048MHz	●		40	250	ppm of V_{REF}
Offset Error	2.5V ≤ V_{REF} ≤ V_{CC}	●		0.5	10	ppm of V_{REF}
Offset Error (Fast Mode)	2.5V < V_{REF} < 5V, 100 Samples/Second, f_O = 2.048MHz			3		ppm of V_{REF}
Offset Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}			0.04		ppm of V_{REF}/°C
Full-Scale Error	2.5V ≤ V_{REF} ≤ V_{CC}	●		4	10	ppm of V_{REF}
Full-Scale Error (Fast Mode)	2.5V < V_{REF} < 5V, 100 Samples/Second, f_O = 2.048MHz			10		ppm of V_{REF}
Full-Scale Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}			0.04		ppm of V_{REF}/°C
Total Unadjusted Error	V_{REF} = 2.5V V_{REF} = 5V			8 16		ppm of V_{REF} ppm of V_{REF}
Output Noise	V_{IN} = 0V (Note 13)			6		μV_{RMS}
Output Noise (Fast Mode)	V_{REF} = 5V, 100 Samples/Second, f_O = 2.048MHz			20		μV_{RMS}
Normal Mode Rejection 60Hz ±2%	(Note 7)	●	110	130		dB
Normal Mode Rejection 50Hz ±2%	(Note 8)	●	110	130		dB
Power Supply Rejection, DC	V_{REF} = 2.5V, V_{IN} = 0V			100		dB
Power Supply Rejection, 60Hz ±2%	V_{REF} = 2.5V, V_{IN} = 0V, (Notes 7, 15)			110		dB
Power Supply Rejection, 50Hz ±2%	V_{REF} = 2.5V, V_{IN} = 0V, (Notes 8, 15)			110		dB

ANALOG INPUT AND REFERENCE

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range	(Note 14)	●	$-0.125 \cdot V_{REF}$		$1.125 \cdot V_{REF}$	V
V_{REF}	Reference Voltage Range		●	0.1		V_{CC}	V
$C_{S(IN)}$	Input Sampling Capacitance				1		pF
$C_{S(REF)}$	Reference Sampling Capacitance				1.5		pF
$I_{IN(LEAK)}$	Input Leakage Current	$\overline{CS} = V_{CC}$	●	–100	1	100	nA
$I_{REF(LEAK)}$	Reference Leakage Current	V_{REF} = 2.5V, $\overline{CS} = V_{CC}$	●	–100	1	100	nA

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage $\overline{CS}$, F_O	2.7V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 3.3V	●	2.5 2.0			V V
V_{IL}	Low Level Input Voltage $\overline{CS}$, F_O	4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V	●			0.8 0.6	V V
V_{IH}	High Level Input Voltage SCK	2.7V ≤ V_{CC} ≤ 5.5V (Note 9) 2.7V ≤ V_{CC} ≤ 3.3V (Note 9)	●	2.5 2.0			V V
V_{IL}	Low Level Input Voltage SCK	4.5V ≤ V_{CC} ≤ 5.5V (Note 9) 2.7V ≤ V_{CC} ≤ 5.5V (Note 9)	●			0.8 0.6	V V
I_{IN}	Digital Input Current $\overline{CS}$, F_O	0V ≤ V_{IN} ≤ V_{CC}	●	–10		10	µA
I_{IN}	Digital Input Current SCK	0V ≤ V_{IN} ≤ V_{CC} (Note 9)	●	–10		10	µA
C_{IN}	Digital Input Capacitance $\overline{CS}$, F_O				10		pF
C_{IN}	Digital Input Capacitance SCK	(Note 9)			10		pF
V_{OH}	High Level Output Voltage SDO	$I_O = -800\mu A$	●	$V_{CC} - 0.5$			V
V_{OL}	Low Level Output Voltage SDO	I_O = 1.6mA	●			0.4	V
V_{OH}	High Level Output Voltage SCK	$I_O = -800\mu A$ (Note 10)	●	$V_{CC} - 0.5$			V
V_{OL}	Low Level Output Voltage SCK	I_O = 1.6mA (Note 10)	●			0.4	V
I_{OZ}	High-Z Output Leakage SDO		●	–10		10	µA

POWER REQUIREMENTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current Conversion Mode Sleep Mode	 $\overline{CS}$ = 0V (Note 12) $\overline{CS} = V_{CC}$ (Note 12)	 ● ●		 200 20	 300 30	 µA µA

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range	20-Bit Effective Resolution 12-Bit Effective Resolution	● ●	2.56 2.56		307.2 2.048	kHz MHz
t_{HEO}	External Oscillator High Period		●	0.2		390	µs
t_{LEO}	External Oscillator Low Period		●	0.2		390	µs
t_{CONV}	Conversion Time	F_O = 0V F_O = V_{CC} External Oscillator (Note 11)	● ● ●	130.86 157.03	133.53 160.23 $20510/f_{EOSC}$ (in kHz)	136.20 163.44	ms ms ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Note 10) External Oscillator (Notes 10, 11)			19.2 $f_{EOSC}/8$		kHz kHz
D_{ISCK}	Internal SCK Duty Cycle	(Note 10)		45		55	%
f_{ESCK}	External SCK Frequency Range	(Note 9)	●			2000	kHz
t_{LESCK}	External SCK Low Period	(Note 9)	●	250			ns
t_{HESCK}	External SCK High Period	(Note 9)	●	250			ns
t_{DOUT_ISCK}	Internal SCK 24-Bit Data Output Time	Internal Oscillator (Notes 10, 12) External Oscillator (Notes 10, 11)	● ●	1.23	1.25 $192/f_{EOSC}$ (in kHz)	1.28	ms ms
t_{DOUT_ESCK}	External SCK 24-Bit Data Output Time	(Note 9)	●		$24/f_{ESCK}$ (in kHz)		ms
t_1	$\overline{CS}$ ↓ to SDO Low Z		●	0		150	ns
t2	$\overline{CS}$ ↑ to SDO High Z		●	0		150	ns
t3	$\overline{CS}$ ↓ to SCK ↓	(Note 10)	●	0		150	ns
t4	$\overline{CS}$ ↓ to SCK ↑	(Note 9)	●	50			ns
t_{KQMAX}	SCK ↓ to SDO Valid		●			200	ns
t_{KQMIN}	SDO Hold After SCK ↓	(Note 5)	●	15			ns
t_5	SCK Set-Up Before $\overline{CS}$ ↓		●	50			ns
t_6	SCK Hold After $\overline{CS}$ ↓		●			50	ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: All voltages are with respect to GND. V_{CC} = 2.7 to 5.5V unless otherwise specified. R_{SOURCE} = 0Ω.

Note 4: Internal Conversion Clock source with the F_O pin tied to GND or to V_{CC} or to external conversion clock source with f_{EOSC} = 153600Hz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: F_O = 0V (internal oscillator) or f_{EOSC} = 153600Hz ±2% (external oscillator).

Note 8: F_O = V_{CC} (internal oscillator) or f_{EOSC} = 128000Hz ±2% (external oscillator).

Note 9: The converter is in external SCK mode of operation such that the SCK pin is used as digital input. The frequency of the clock signal driving SCK during the data output is f_{ESCK} and is expressed in kHz.

Note 10: The converter is in internal SCK mode of operation such that the SCK pin is used as digital output. In this mode of operation the SCK pin has a total equivalent load capacitance C_{LOAD} = 20pF.

Note 11: The external oscillator is connected to the F_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 12: The converter uses the internal oscillator.
F_O = 0V or F_O = V_{CC}.

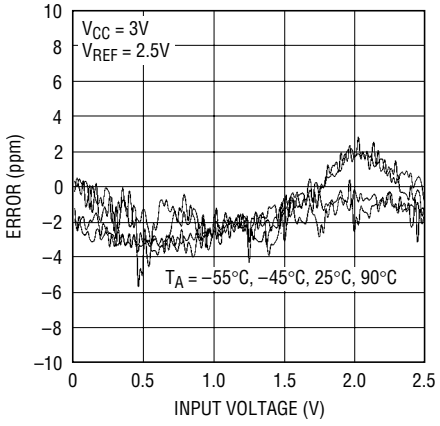
Note 13: The output noise includes the contribution of the internal calibration operations.

Note 14: For reference voltage values V_{REF} > 2.5V the extended input of $-0.125 \bullet V_{REF}$ to $1.125 \bullet V_{REF}$ is limited by the absolute maximum rating of the Analog Input Voltage pin (Pin 3). For 2.5V < $V_{REF} \leq$ $0.267V + 0.89 \bullet V_{CC}$ the input voltage range is –0.3V to $1.125 \bullet V_{REF}$. For $0.267V + 0.89 \bullet V_{CC} < V_{REF} \leq V_{CC}$ the input voltage range is –0.3V to V_{CC} + 0.3V.

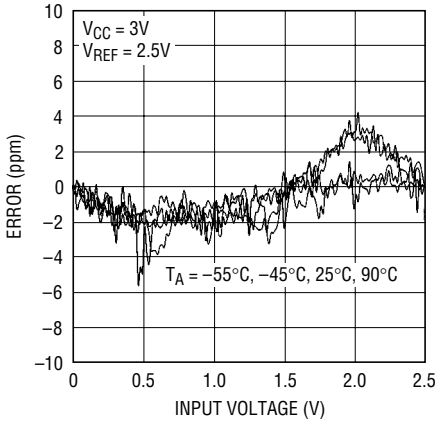
Note 15: V_{CC} (DC) = 4.1V, V_{CC} (AC) = $2.8V_{P-P}$.

TYPICAL PERFORMANCE CHARACTERISTICS

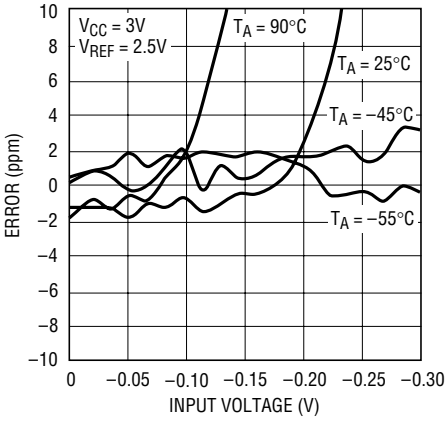
Total Unadjusted Error (3V Supply)



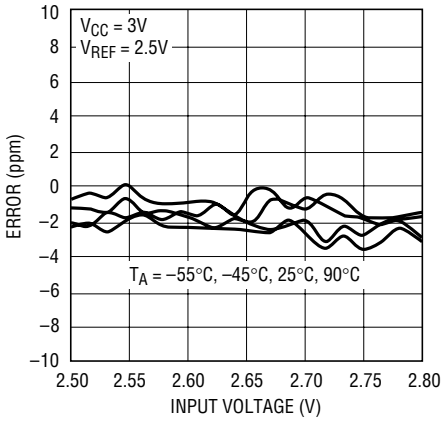
INL (3V Supply)



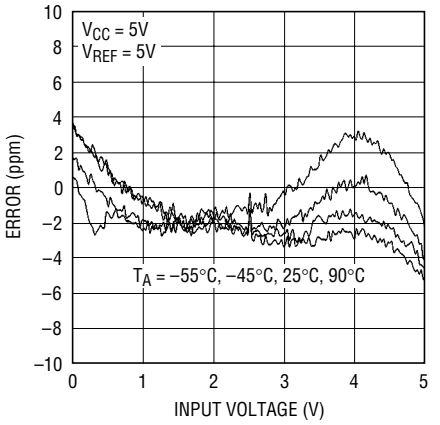
Negative Input Extended Total Unadjusted Error (3V Supply)



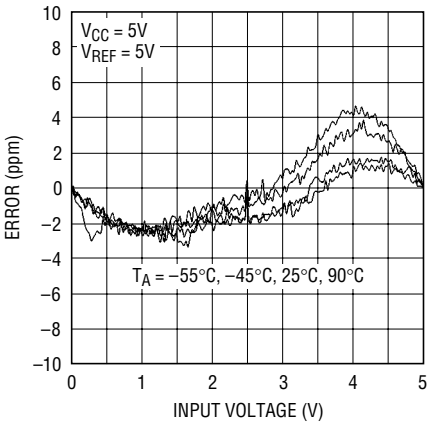
Positive Input Extended Total Unadjusted Error (3V Supply)



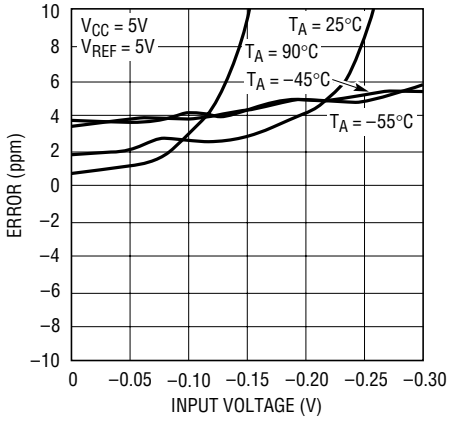
Total Unadjusted Error (5V Supply)



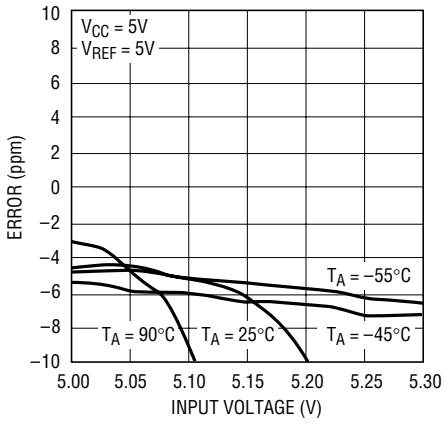
INL (5V Supply)



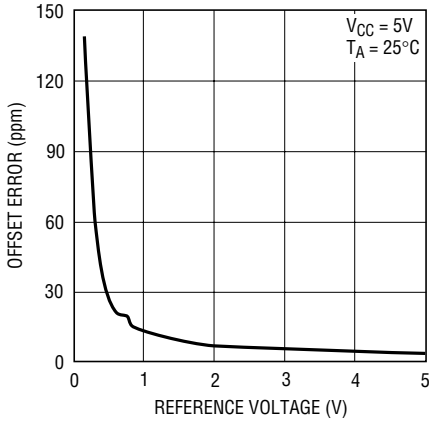
Negative Input Extended Total Unadjusted Error (5V Supply)



Positive Input Extended Total Unadjusted Error (5V Supply)

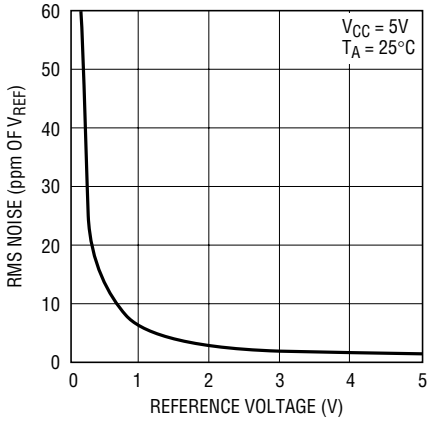


Offset Error vs Reference Voltage



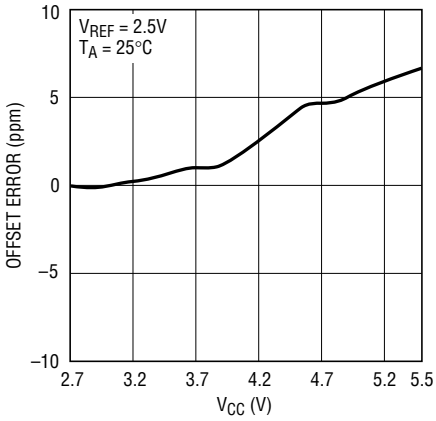
TYPICAL PERFORMANCE CHARACTERISTICS

RMS Noise vs Reference Voltage



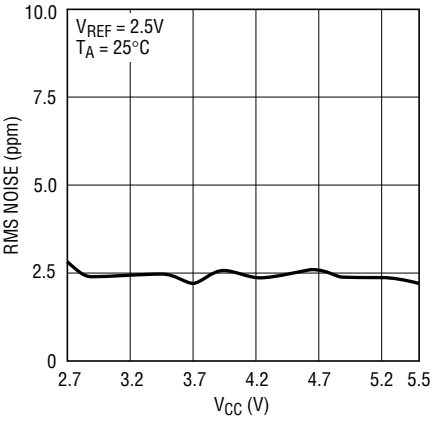
2420 G10

Offset Error vs V_{CC}



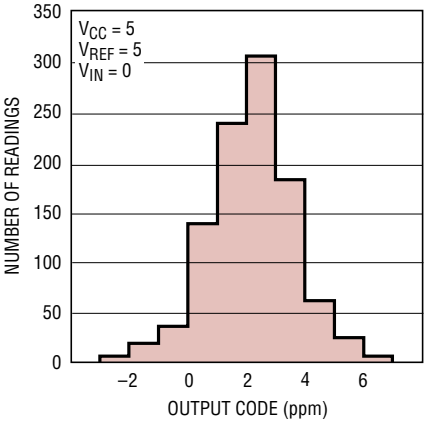
2420 G11

RMS Noise vs V_{CC}



2420 G12

Noise Histogram



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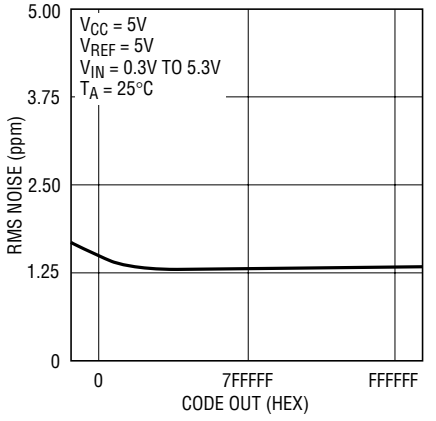
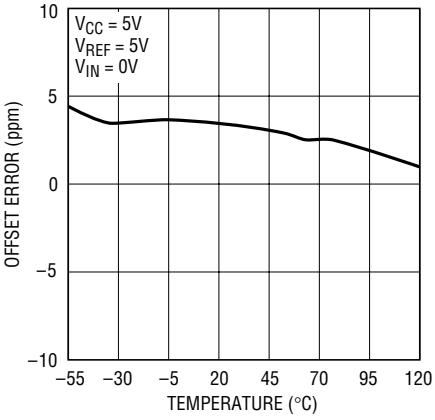
RMS Noise vs Code Out



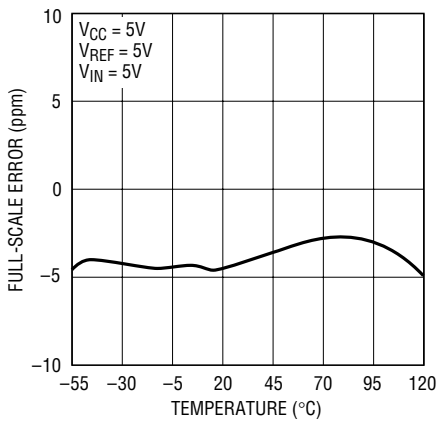
2420 G14

Offset Error vs Temperature



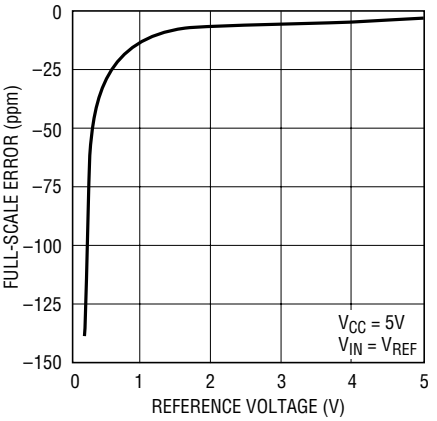
2420 G15

Full-Scale Error vs Temperature



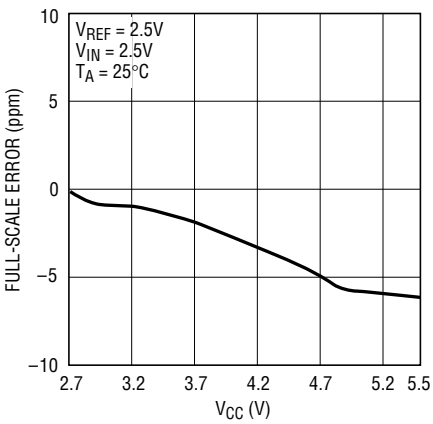
2420 G16

Full-Scale Error vs Reference Voltage



2420 G17

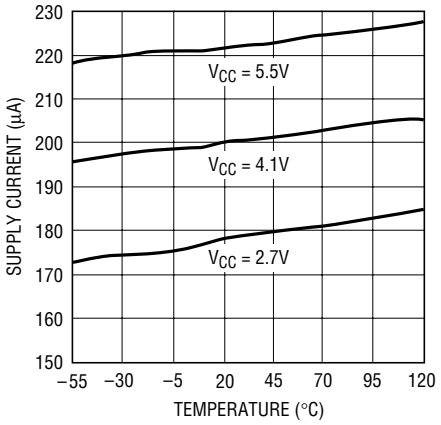
Full-Scale Error vs V_{CC}



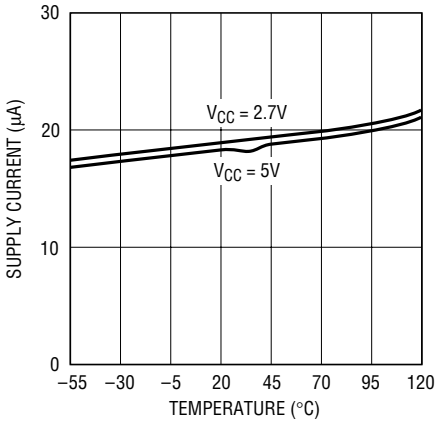
2420 G18

TYPICAL PERFORMANCE CHARACTERISTICS

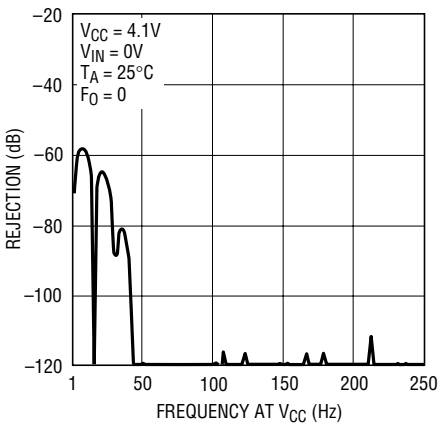
Conversion Current vs Temperature



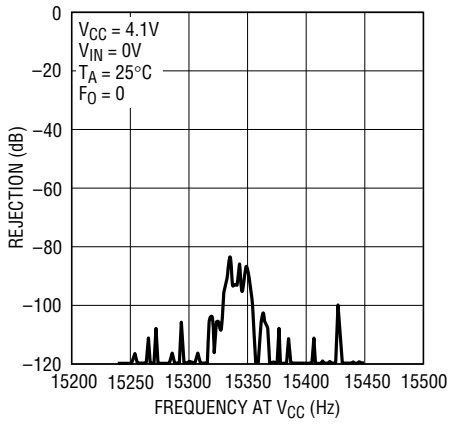
Sleep Current vs Temperature



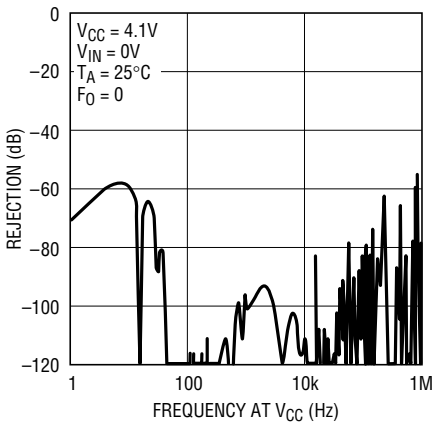
Rejection vs Frequency at V_{CC}



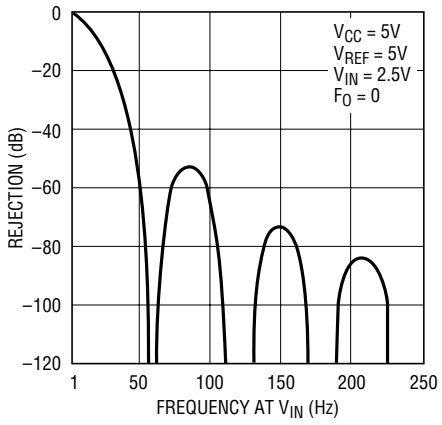
Rejection vs Frequency at V_{CC}



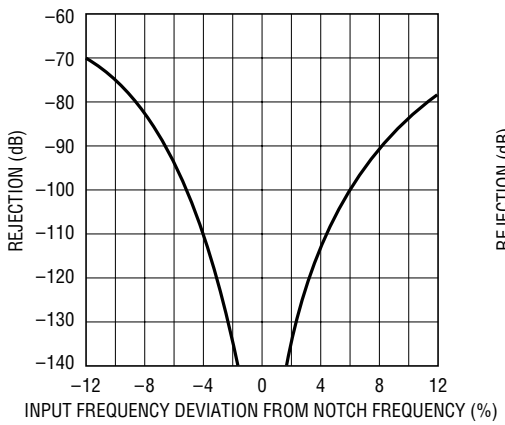
Rejection vs Frequency at V_{CC}



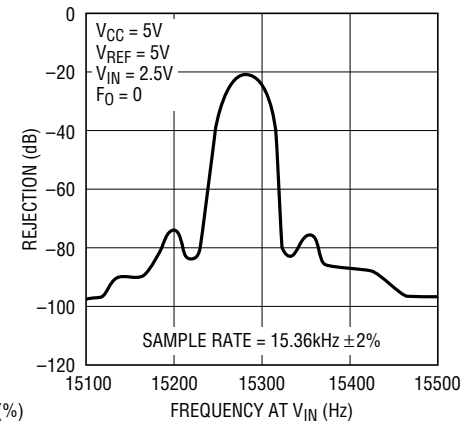
Rejection vs Frequency at V_{IN}



Rejection vs Frequency at V_{IN}



Rejection vs Frequency at V_{IN}



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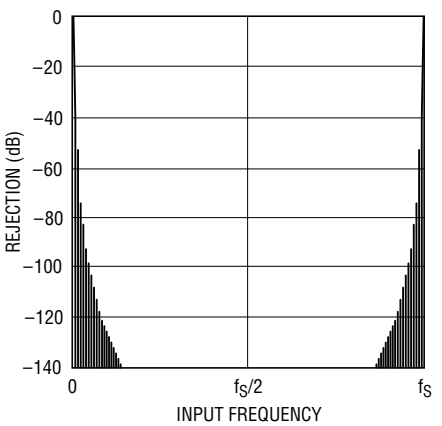
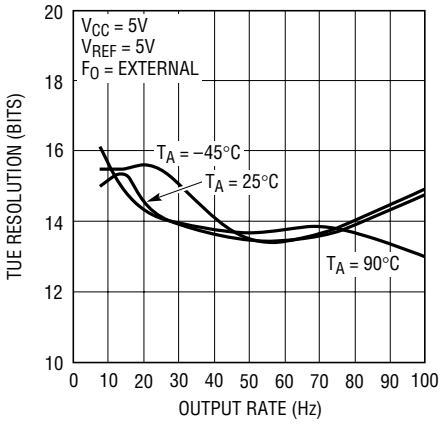
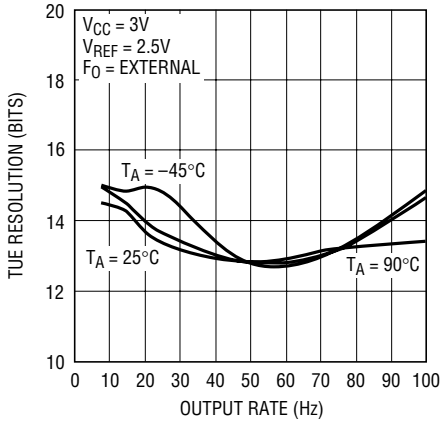


TYPICAL PERFORMANCE CHARACTERISTICS

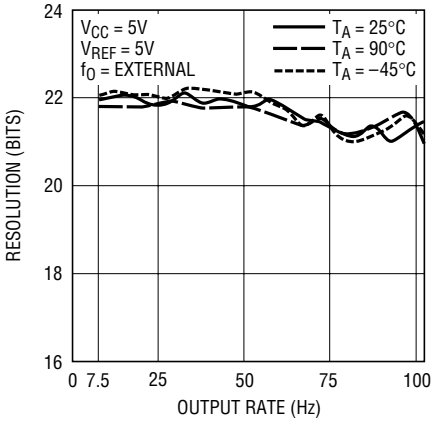
INL vs Output Rate



INL vs Output Rate



Resolution vs Output Rate



PIN FUNCTIONS

V_{CC} (Pin 1): Positive Supply Voltage. Bypass to GND (Pin 4) with a 10µF tantalum capacitor in parallel with 0.1µF ceramic capacitor as close to the part as possible.

V_{REF} (Pin 2): Reference Input. The reference voltage range is 0.1V to V_{CC}.

V_{IN} (Pin 3): Analog Input. The input voltage range is $-0.125 \cdot V_{REF}$ to $1.125 \cdot V_{REF}$. For $V_{REF} > 2.5V$ the input voltage range may be limited by the pin absolute maximum rating of –0.3V to V_{CC} + 0.3V.

GND (Pin 4): Ground. Shared pin for analog ground, digital ground, reference ground and signal ground. Should be connected directly to a ground plane through a minimum length trace or it should be the single-point-ground in a single point grounding system.

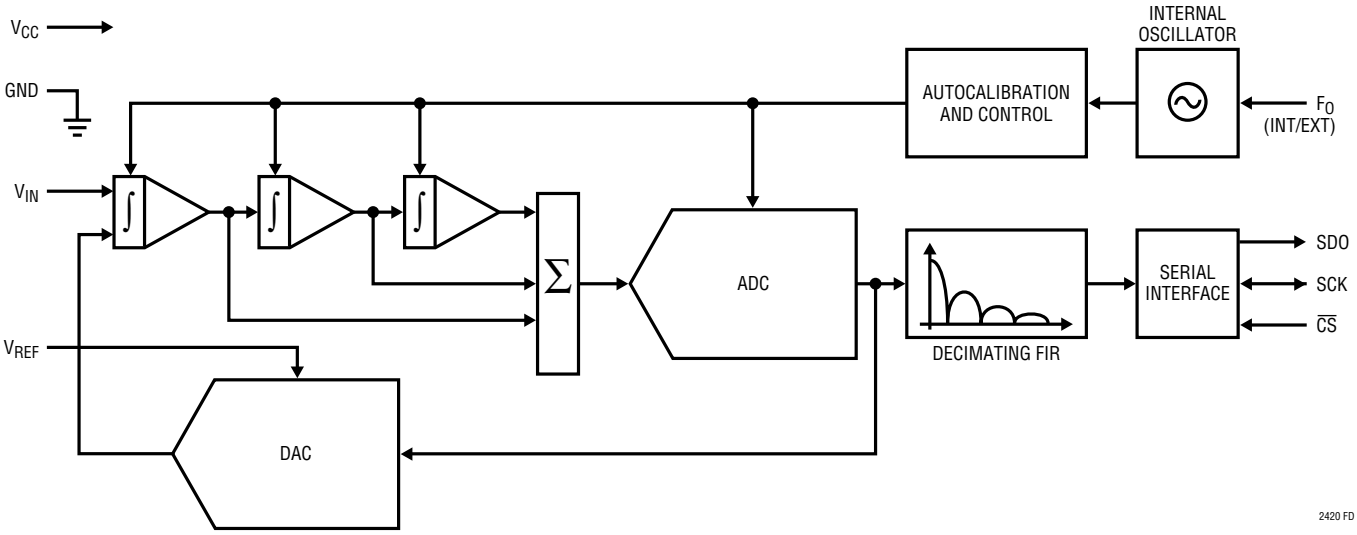
$\overline{CS}$ (Pin 5): Active LOW Digital Input. A LOW on this pin enables the SDO digital output and wakes up the ADC. Following each conversion, the ADC automatically enters the Sleep mode and remains in this low power state as long as $\overline{CS}$ is HIGH. A LOW on $\overline{CS}$ wakes up the ADC. A LOW-to-HIGH transition on this pin disables the SDO digital output. A LOW-to-HIGH transition on $\overline{CS}$ during the Data Output transfer aborts the data transfer and starts a new conversion.

SDO (Pin 6): Three-State Digital Output. During the data output period this pin is used for serial data output. When the chip select $\overline{CS}$ is HIGH ($\overline{CS} = V_{CC}$), the SDO pin is in a high impedance state. During the Conversion and Sleep periods, this pin can be used as a conversion status output. The conversion status can be observed by pulling $\overline{CS}$ LOW.

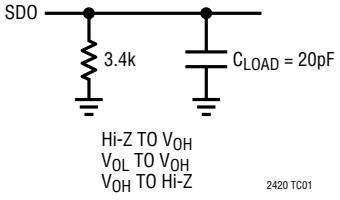
SCK (Pin 7): Bidirectional Digital Clock Pin. In Internal Serial Clock Operation mode, SCK is used as digital output for the internal serial interface clock during the data output period. In External Serial Clock Operation mode, SCK is used as digital input for the external serial interface. A weak internal pull-up is automatically activated in Internal Serial Clock Operation mode. The Serial Clock mode is determined by the level applied to SCK at power up and the falling edge of $\overline{CS}$.

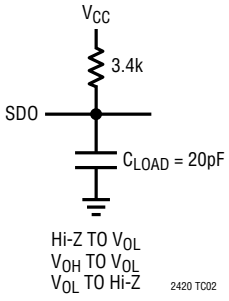
F_O (Pin 8): Frequency Control Pin. Digital input that controls the ADC's notch frequencies and conversion time. When the F_O pin is connected to V_{CC} ($F_O = V_{CC}$), the converter uses its internal oscillator and the digital filter's first null is located at 50Hz. When the F_O pin is connected to GND (F_O = OV), the converter uses its internal oscillator and the digital filter first null is located at 60Hz. When F_O is driven by an external clock signal with a frequency f_{EOSC}, the converter uses this signal as its clock and the digital filter first null is located at a frequency $f_{EOSC}/2560$.

FUNCTIONAL BLOCK DIAGRAM



TEST CIRCUITS





APPLICATIONS INFORMATION

The LTC2420 is pin compatible with the LTC2400. The two devices are designed to allow the user to incorporate either device in the same design with no modifications. While the LTC2420 output word length is 24 bits (as opposed to the 32-bit output of the LTC2400), its output clock timing can be identical to the LTC2400. As shown in Figure 1, the LTC2420 data output is concluded on the falling edge of the 24th serial clock (SCK). In order to maintain drop-in compatibility with the LTC2400, it is possible to clock the LTC2420 with an additional 8 serial clock pulses. This results in 8 additional output bits which are always logic HIGH.

Converter Operation Cycle

The LTC2420 is a low power, delta-sigma analog-to-digital converter with an easy to use 3-wire serial interface. Its operation is simple and made up of three states. The converter operating cycle begins with the conversion, followed by a low power sleep state and concluded with the data output (see Figure 2). The 3-wire interface consists of serial data output (SDO), a serial clock (SCK) and a chip select ($\overline{CS}$).

Initially, the LTC2420 performs a conversion. Once the conversion is complete, the device enters the sleep state. While in this sleep state, power consumption is reduced by an order of magnitude. The part remains in the sleep state as long as $\overline{CS}$ is logic HIGH. The conversion result is held indefinitely in a static shift register while the converter is in the sleep state.

Once $\overline{CS}$ is pulled LOW, the device begins outputting the conversion result. There is no latency in the conversion result. The data output corresponds to the conversion just performed. This result is shifted out on the serial data out pin (SDO) under the control of the serial clock (SCK). Data is updated on the falling edge of SCK allowing the user to reliably latch data on the rising edge of SCK, see Figure 4. The data output state is concluded once 24 bits are read out of the ADC or when $\overline{CS}$ is brought HIGH. The device automatically initiates a new conversion cycle and the cycle repeats.

Through timing control of the $\overline{CS}$ and SCK pins, the LTC2420 offers several flexible modes of operation (internal or external SCK and free-running conversion modes). These various modes do not require programming configuration registers; moreover, they do

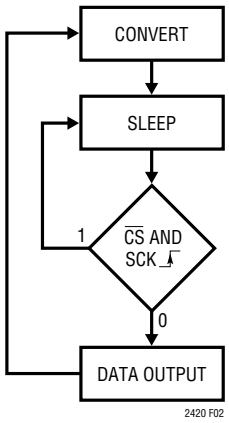


Figure 2. LTC2420 State Transition Diagram

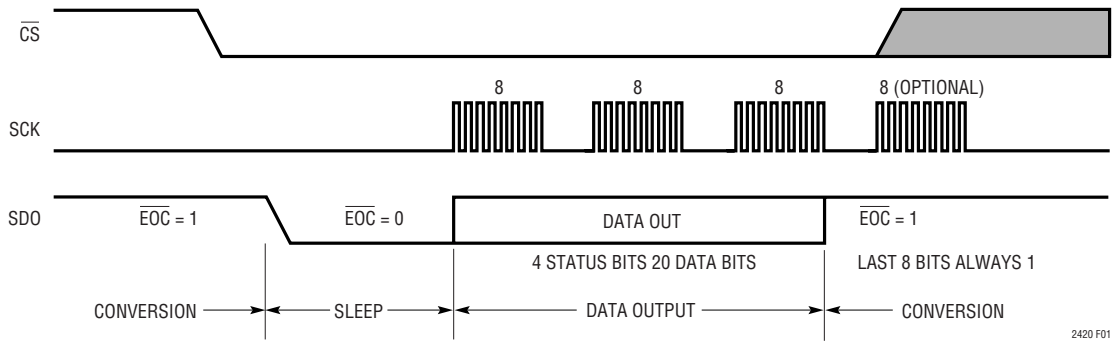


Figure 1. LTC2420 Compatible Timing with the LTC2400

APPLICATIONS INFORMATION

not disturb the cyclic operation described above. These modes of operation are described in detail in the Serial Interface Timing Modes section.

Conversion Clock

A major advantage delta-sigma converters offer over conventional type converters is an on-chip digital filter (commonly known as Sinc or Comb filter). For high resolution, low frequency applications, this filter is typically designed to reject line frequencies of 50Hz or 60Hz plus their harmonics. In order to reject these frequencies in excess of 110dB, a highly accurate conversion clock is required. The LTC2420 incorporates an on-chip highly accurate oscillator. This eliminates the need for external frequency setting components such as crystals or oscillators. Clocked by the on-chip oscillator, the LTC2420 rejects line frequencies (50Hz or 60Hz ±2%) a minimum of 110dB.

Ease of Use

The LTC2420 data output has no latency, filter settling or redundant data associated with the conversion cycle. There is a one-to-one correspondence between the conversion and the output data. Therefore, multiplexing an analog input voltage is easy.

The LTC2420 performs offset and full-scale calibrations every conversion cycle. This calibration is transparent to the user and has no effect on the cyclic operation described above. The advantage of continuous calibration is extreme stability of offset and full-scale readings with respect to time, supply voltage change and temperature drift.

Power-Up Sequence

The LTC2420 automatically enters an internal reset state when the power supply voltage V_{CC} drops below approximately 2.2V. This feature guarantees the integrity of the conversion result and of the serial interface mode selection which is performed at the initial power-up. (See the 2-wire I/O sections in the Serial Interface Timing Modes section.)

When the V_{CC} voltage rises above this critical threshold, the converter creates an internal power-on-reset (POR) signal with duration of approximately 0.5ms. The POR signal clears all internal registers. Following the POR signal, the LTC2420 starts a normal conversion cycle and follows the normal succession of states described above. The first conversion result following POR is accurate within the specifications of the device.

Reference Voltage Range

The LTC2420 can accept a reference voltage from 0V to V_{CC}. The converter output noise is determined by the thermal noise of the front-end circuits, and as such, its value in microvolts is nearly constant with reference voltage. A decrease in reference voltage will not significantly improve the converter's effective resolution. On the other hand, a reduced reference voltage will improve the overall converter INL performance. The recommended range for the LTC2420 voltage reference is 100mV to V_{CC}.

Input Voltage Range

The converter is able to accommodate system level offset and gain errors as well as system level overrange situations due to its extended input range, see Figure 3. The LTC2420 converts input signals within the extended input range of $-0.125 \cdot V_{REF}$ to $1.125 \cdot V_{REF}$.

For large values of V_{REF}, this range is limited by the absolute maximum voltage range of –0.3V to (V_{CC} + 0.3V). Beyond this range, the input ESD protection devices begin to turn on and the errors due to the input leakage current increase rapidly.

Input signals applied to V_{IN} may extend below ground by –300mV and above V_{CC} by 300mV. In order to limit any

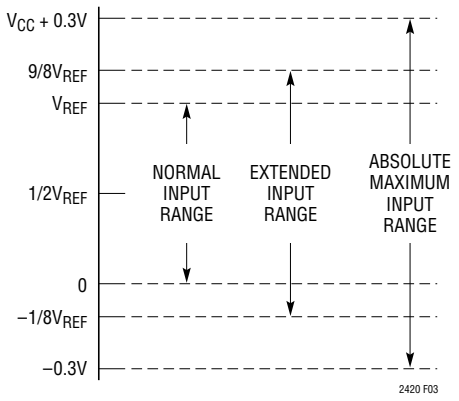


Figure 3. LTC2420 Input Range

APPLICATIONS INFORMATION

fault current, a resistor of up to 25k may be added in series with the V_{IN} pin without affecting the performance of the device. In the physical layout, it is important to maintain the parasitic capacitance of the connection between this series resistance and the V_{IN} pin as low as possible; therefore, the resistor should be located as close as practical to the V_{IN} pin. The effect of the series resistance on the converter accuracy can be evaluated from the curves presented in the Analog Input/Reference Current section. In addition, a series resistor will introduce a temperature dependent offset error due to the input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if V_{REF} = 5V. This error has a very strong temperature dependency.

Output Data Format

The LTC2420 serial output data stream is 24 bits long. The first 4 bits represent status information indicating the sign, input range and conversion state. The next 20 bits are the conversion result, MSB first.

Bit 23 (first output bit) is the end of conversion ($\overline{EOC}$) indicator. This bit is available at the SDO pin during the conversion and sleep states whenever the $\overline{CS}$ pin is LOW. This bit is HIGH during the conversion and goes LOW when the conversion is complete.

Bit 22 (second output bit) is a dummy bit (DMY) and is always LOW.

Bit 21 (third output bit) is the conversion result sign indicator (SIG). If V_{IN} is >0, this bit is HIGH. If V_{IN} is <0, this bit is LOW. The sign bit changes state during the zero code.

Bit 20 (fourth output bit) is the extended input range (EXR) indicator. If the input is within the normal input range $0 \le V_{IN} \le V_{REF}$, this bit is LOW. If the input is outside the normal input range, $V_{IN} > V_{REF}$ or $V_{IN} < 0$, this bit is HIGH.

The function of these bits is summarized in Table 1.

Table 1. LTC2420 Status Bits

Input Range	Bit 23 $\overline{EOC}$	Bit 22 DMY	Bit 21 SIG	Bit 20 EXR
$V_{IN} > V_{REF}$	0	0	1	1
$0 < V_{IN} \le V_{REF}$	0	0	1	0
$V_{IN} = 0^+/0^-$	0	0	1/0	0
$V_{IN} < 0$	0	0	0	1

Bit 19 (fifth output bit) is the most significant bit (MSB).

Bits 19-0 are the 20-bit conversion result MSB first.

Bit 0 is the least significant bit (LSB).

Data is shifted out of the SDO pin under control of the serial clock (SCK), see Figure 4. Whenever $\overline{CS}$ is HIGH, SDO remains high impedance and any SCK clock pulses are ignored by the internal data out shift register.

In order to shift the conversion result out of the device, $\overline{CS}$ must first be driven LOW. $\overline{EOC}$ is seen at the SDO pin of the device once $\overline{CS}$ is pulled LOW. $\overline{EOC}$ changes real time from HIGH to LOW at the completion of a conversion. This signal may be used as an interrupt for an external microcontroller. Bit 23 ($\overline{EOC}$) can be captured on the first rising edge of SCK. Bit 22 is shifted out of the device on the first falling edge of SCK. The final data bit (Bit 0) is shifted out on the falling edge of the 23rd SCK and may be latched on

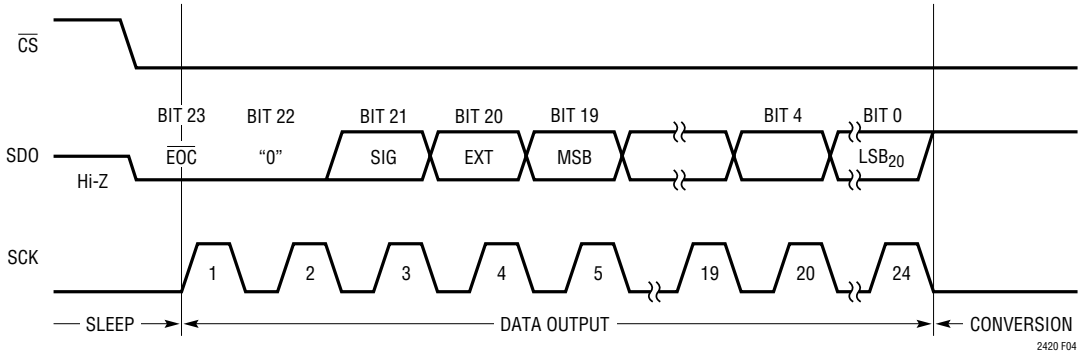


Figure 4. Output Data Timing

APPLICATIONS INFORMATION

the rising edge of the 24th SCK pulse. On the falling edge of the 24th SCK pulse, SDO goes HIGH indicating a new conversion cycle has been initiated. This bit serves as $\overline{EOC}$ (Bit 23) for the next conversion cycle. Table 2 summarizes the output data format.

As long as the voltage on the V_{IN} pin is maintained within the –0.3V to (V_{CC} + 0.3V) absolute maximum operating range, a conversion result is generated for any input value from $-0.125 \cdot V_{REF}$ to $1.125 \cdot V_{REF}$. For input voltages greater than $1.125 \cdot V_{REF}$, the conversion result is clamped to the value corresponding to $1.125 \cdot V_{REF}$. For input voltages below $-0.125 \cdot V_{REF}$, the conversion result is clamped to the value corresponding to $-0.125 \cdot V_{REF}$.

Frequency Rejection Selection (F_O Pin Connection)

The LTC2420 internal oscillator provides better than 110dB normal mode rejection at the line frequency and its harmonics for 50Hz±2% or 60Hz±2%. For 60Hz rejection, F_O (Pin 8) should be connected to GND (Pin 4) while for 50Hz rejection the F_O pin should be connected to V_{CC} (Pin 1).

The selection of 50Hz or 60Hz rejection can also be made by driving F_O to an appropriate logic level. A selection change during the sleep or data output states will not disturb the converter operation. If the selection is made during the conversion state, the result of the conversion in progress may be outside specifications but the following conversions will not be affected.

When a fundamental rejection frequency different from 50Hz or 60Hz is required or when the converter must be synchronized with an outside source, the LTC2420 can operate with an external conversion clock. The converter automatically detects the presence of an external clock signal at the F_O pin and turns off the internal oscillator. The frequency f_{EOSC} of the external signal must be at least 2560Hz (1Hz notch frequency) to be detected. The external clock signal duty cycle is not significant as long as the minimum and maximum specifications for the high and low periods t_{HEO} and t_{LEO} are observed.

While operating with an external conversion clock of a frequency f_{EOSC}, the LTC2420 provides better than 110dB normal mode rejection in a frequency range $f_{EOSC}/2560$ ±4% and its harmonics. The normal mode rejection as a function of the input frequency deviation from $f_{EOSC}/2560$ is shown in Figure 5.

Table 2. LTC2420 Output Data Format

Input Voltage	Bit 23 $\overline{EOC}$	Bit 22 DMY	Bit 21 SIG	Bit 20 EXR	Bit 19 MSB	Bit 18	Bit 17	Bit 16	Bit 15	…	Bit 0 LSB
$V_{IN} > 9/8 \cdot V_{REF}$	0	0	1	1	0	0	0	1	1	...	1
$9/8 \cdot V_{REF}$	0	0	1	1	0	0	0	1	1	...	1
V_{REF} + 1LSB	0	0	1	1	0	0	0	0	0	...	0
V_{REF}	0	0	1	0	1	1	1	1	1	...	1
$3/4V_{REF}$ + 1LSB	0	0	1	0	1	1	0	0	0	...	0
$3/4V_{REF}$	0	0	1	0	1	0	1	1	1	...	1
$1/2V_{REF}$ + 1LSB	0	0	1	0	1	0	0	0	0	...	0
$1/2V_{REF}$	0	0	1	0	0	1	1	1	1	...	1
$1/4V_{REF}$ + 1LSB	0	0	1	0	0	1	0	0	0	...	0
$1/4V_{REF}$	0	0	1	0	0	0	1	1	1	...	1
$0^+/0^-$	0	0	1/0*	0	0	0	0	0	0	...	0
–1LSB	0	0	0	1	1	1	1	1	1	...	1
$-1/8 \cdot V_{REF}$	0	0	0	1	1	1	1	0	0	...	0
$V_{IN} < -1/8 \cdot V_{REF}$	0	0	0	1	1	1	1	0	0	...	0

*The sign bit changes state during the 0 code.

APPLICATIONS INFORMATION

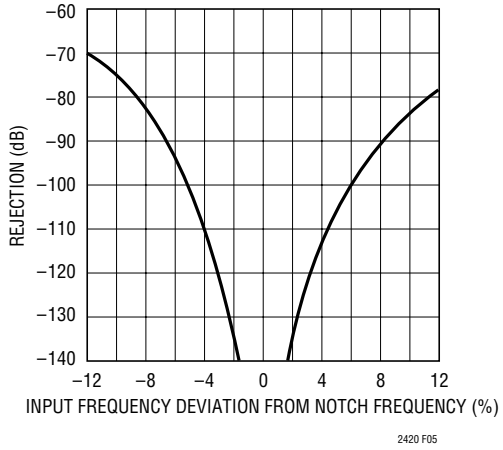


Figure 5. LTC2420 Normal Mode Rejection When Using an External Oscillator of Frequency f_{EOSC}

Whenever an external clock is not present at the F_O pin, the converter automatically activates its internal oscillator and enters the Internal Conversion Clock mode. The LTC2420 operation will not be disturbed if the change of conversion clock source occurs during the sleep state or during the data output state while the converter uses an external serial clock. If the change occurs during the conversion state, the result of the conversion in progress may be outside specifications but the following conversions will not be affected. If the change occurs during the data output state and the converter is in the Internal SCK mode, the serial clock duty cycle may be affected but the serial data stream will remain valid.

Table 3 summarizes the duration of each state as a function of F_O.

SERIAL INTERFACE

The LTC2420 transmits the conversion results and receives the start of conversion command through a synchronous 3-wire interface. During the conversion and sleep states, this interface can be used to assess the converter status and during the data output state it is used to read the conversion result.

Serial Clock Input/Output (SCK)

The serial clock signal present on SCK (Pin 7) is used to synchronize the data transfer. Each bit of data is shifted out the SDO pin on the falling edge of the serial clock.

In the Internal SCK mode of operation, the SCK pin is an output and the LTC2420 creates its own serial clock by dividing the internal conversion clock by 8. In the External SCK mode of operation, the SCK pin is used as input. The internal or external SCK mode is selected on power-up and then reselected every time a HIGH-to-LOW transition is detected at the $\overline{CS}$ pin. If SCK is HIGH or floating at power-up or during this transition, the converter enters the internal SCK mode. If SCK is LOW at power-up or during this transition, the converter enters the external SCK mode.

Table 3. LTC2420 State Duration

State	Operating Mode		Duration
CONVERT	Internal Oscillator	F_O = LOW (60Hz Rejection)	133ms
		F_O = HIGH (50Hz Rejection)	160ms
	External Oscillator	F_O = External Oscillator with Frequency f_{EOSC} kHz (f_{EOSC}/2560 Rejection)	20510/f_{EOSC}s
SLEEP			As Long As $\overline{CS}$ = HIGH Until $\overline{CS}$ = 0 and SCK ↓
DATA OUTPUT	Internal Serial Clock	F_O = LOW/HIGH (Internal Oscillator)	As Long As $\overline{CS}$ = LOW But Not Longer Than 1.26ms (24 SCK cycles)
		F_O = External Oscillator with Frequency f_{EOSC} kHz	As Long As $\overline{CS}$ = LOW But Not Longer Than 256/f_{EOSC}ms (24 SCK cycles)
	External Serial Clock with Frequency f_{SCK} kHz		As Long As $\overline{CS}$ = LOW But Not Longer Than 24/f_{SCK}ms (24 SCK cycles)

APPLICATIONS INFORMATION

Serial Data Output (SDO)

The serial data output pin, SDO (Pin 6), drives the serial data during the data output state. In addition, the SDO pin is used as an end of conversion indicator during the conversion and sleep states.

When $\overline{CS}$ (Pin 5) is HIGH, the SDO driver is switched to a high impedance state. This allows sharing the serial interface with other devices. If $\overline{CS}$ is LOW during the convert or sleep state, SDO will output $\overline{EOC}$. If $\overline{CS}$ is LOW during the conversion phase, the $\overline{EOC}$ bit appears HIGH on the SDO pin. Once the conversion is complete, $\overline{EOC}$ goes LOW. The device remains in the sleep state until the first rising edge of SCK occurs while $\overline{CS}$ is LOW.

Chip Select Input ($\overline{CS}$)

The active LOW chip select, $\overline{CS}$ (Pin 5), is used to test the conversion status and to enable the data output transfer as described in the previous sections.

In addition, the $\overline{CS}$ signal can be used to trigger a new conversion cycle before the entire serial data transfer has been completed. The LTC2420 will abort any serial data transfer in progress and start a new conversion cycle anytime a LOW-to-HIGH transition is detected at the $\overline{CS}$ pin after the converter has entered the data output state (i.e., after the first rising edge of SCK occurs while $\overline{CS}$ is LOW).

Finally, $\overline{CS}$ can be used to control the free-running modes of operation, see Serial Interface Timing Modes section. Grounding $\overline{CS}$ will force the ADC to continuously convert at the maximum output rate selected by F_O. Tying a capacitor to $\overline{CS}$ will reduce the output rate and power dissipation by a factor proportional to the capacitor's value, see Figures 13 to 15.

SERIAL INTERFACE TIMING MODES

The LTC2420's 3-wire interface is SPI and MICROWIRE compatible. This interface offers several flexible modes of operation. These include internal/external serial clock, 2- or 3-wire I/O, single cycle conversion and autostart. The following sections describe each of these serial interface timing modes in detail. In all these cases, the converter can use the internal oscillator (F_O = LOW or F_O = HIGH) or an external oscillator connected to the F_O pin. Refer to Table 4 for a summary.

External Serial Clock, Single Cycle Operation (SPI/MICROWIRE Compatible)

This timing mode uses an external serial clock to shift out the conversion result and a $\overline{CS}$ signal to monitor and control the state of the conversion cycle, see Figure 6.

The serial clock mode is selected on the falling edge of $\overline{CS}$. To select the external serial clock mode, the serial clock pin (SCK) must be LOW during each $\overline{CS}$ falling edge.

The serial data output pin (SDO) is Hi-Z as long as $\overline{CS}$ is HIGH. At any time during the conversion cycle, $\overline{CS}$ may be pulled LOW in order to monitor the state of the converter. While $\overline{CS}$ is pulled LOW, $\overline{EOC}$ is output to the SDO pin. $\overline{EOC}$ = 1 while a conversion is in progress and $\overline{EOC}$ = 0 if the device is in the sleep state. Independent of $\overline{CS}$, the device automatically enters the low power sleep state once the conversion is complete.

When the device is in the sleep state ($\overline{EOC}$ = 0), its conversion result is held in an internal static shift register. The device remains in the sleep state until the first rising edge of SCK is seen while $\overline{CS}$ is LOW. Data is shifted out the SDO pin on each falling edge of SCK. This enables

Table 4. LTC2420 Interface Timing Modes

Configuration	SCK Source	Conversion Cycle Control	Data Output Control	Connection and Waveforms
External SCK, Single Cycle Conversion	External	$\overline{CS}$ and SCK	$\overline{CS}$ and SCK	Figures 6, 7
External SCK, 2-Wire I/O	External	SCK	SCK	Figure 8
Internal SCK, Single Cycle Conversion	Internal	$\overline{CS}\downarrow$	$\overline{CS}\downarrow$	Figures 9, 10
Internal SCK, 2-Wire I/O, Continuous Conversion	Internal	Continuous	Internal	Figure 11
Internal SCK, Autostart Conversion	Internal	C_{EXT}	Internal	Figure 12

APPLICATIONS INFORMATION

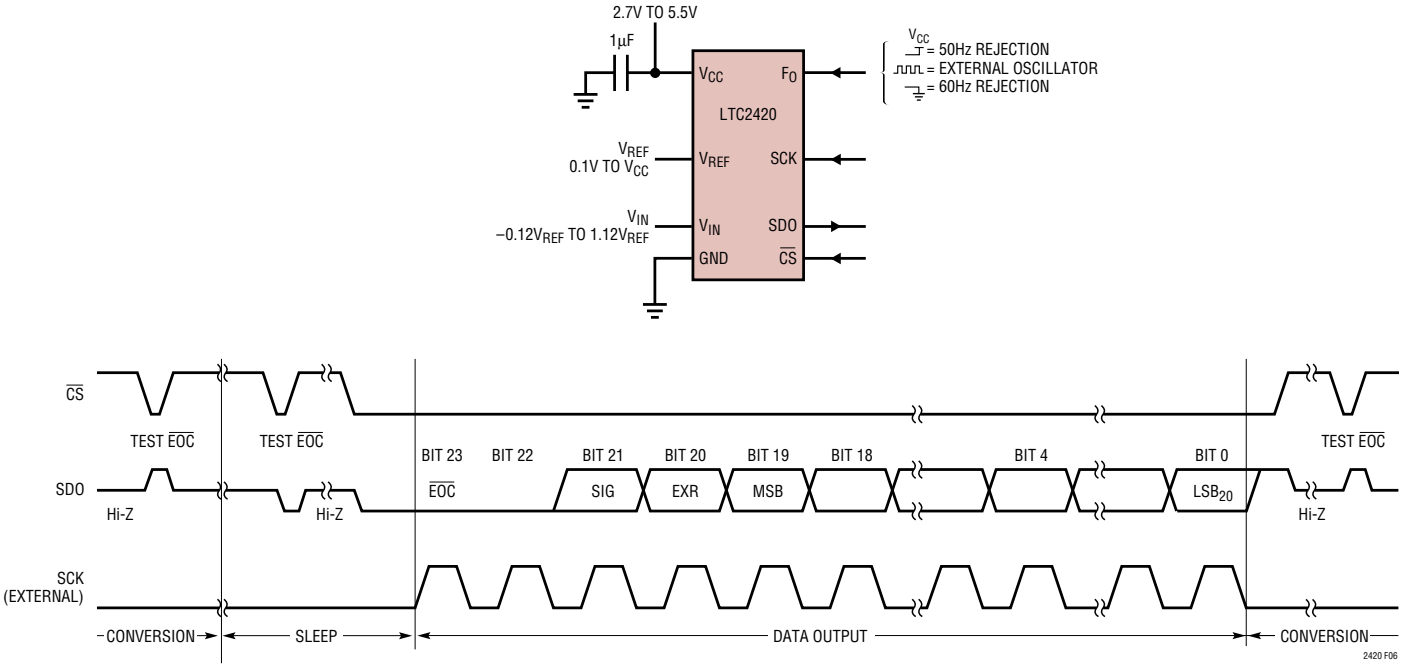


Figure 6. External Serial Clock, Single Cycle Operation

external circuitry to latch the output on the rising edge of SCK. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 24th rising edge of SCK. On the 24th falling edge of SCK, the device begins a new conversion. SDO goes HIGH ($\overline{EOC}$ = 1) indicating a conversion is in progress.

At the conclusion of the data cycle, $\overline{CS}$ may remain LOW and $\overline{EOC}$ monitored as an end-of-conversion interrupt. Alternatively, $\overline{CS}$ may be driven HIGH setting SDO to Hi-Z. As described above, $\overline{CS}$ may be pulled LOW at any time in order to monitor the conversion status.

Typically, $\overline{CS}$ remains LOW during the data output state. However, the data output state may be aborted by pulling $\overline{CS}$ HIGH anytime between the first rising edge and the 24th falling edge of SCK, see Figure 7. On the rising edge of $\overline{CS}$, the device aborts the data output state and immediately initiates a new conversion. This is useful for systems not requiring all 24 bits of output data, aborting an invalid conversion cycle or synchronizing the start of a conversion.

External Serial Clock, 2-Wire I/O

This timing mode utilizes a 2-wire serial I/O interface. The conversion result is shifted out of the device by an externally generated serial clock (SCK) signal, see Figure 8. $\overline{CS}$ may be permanently tied to ground (Pin 4), simplifying the user interface or isolation barrier.

The external serial clock mode is selected at the end of the power-on reset (POR) cycle. The POR cycle is concluded approximately 0.5ms after V_{CC} exceeds 2.2V. The level applied to SCK at this time determines if SCK is internal or external. SCK must be driven LOW prior to the end of POR in order to enter the external serial clock timing mode.

Since $\overline{CS}$ is tied LOW, the end-of-conversion ($\overline{EOC}$) can be continuously monitored at the SDO pin during the convert and sleep states. $\overline{EOC}$ may be used as an interrupt to an external controller indicating the conversion result is ready. $\overline{EOC}$ = 1 while the conversion is in progress and $\overline{EOC}$ = 0 once the conversion enters the low power sleep state. On the falling edge of $\overline{EOC}$, the conversion result is loaded

APPLICATIONS INFORMATION

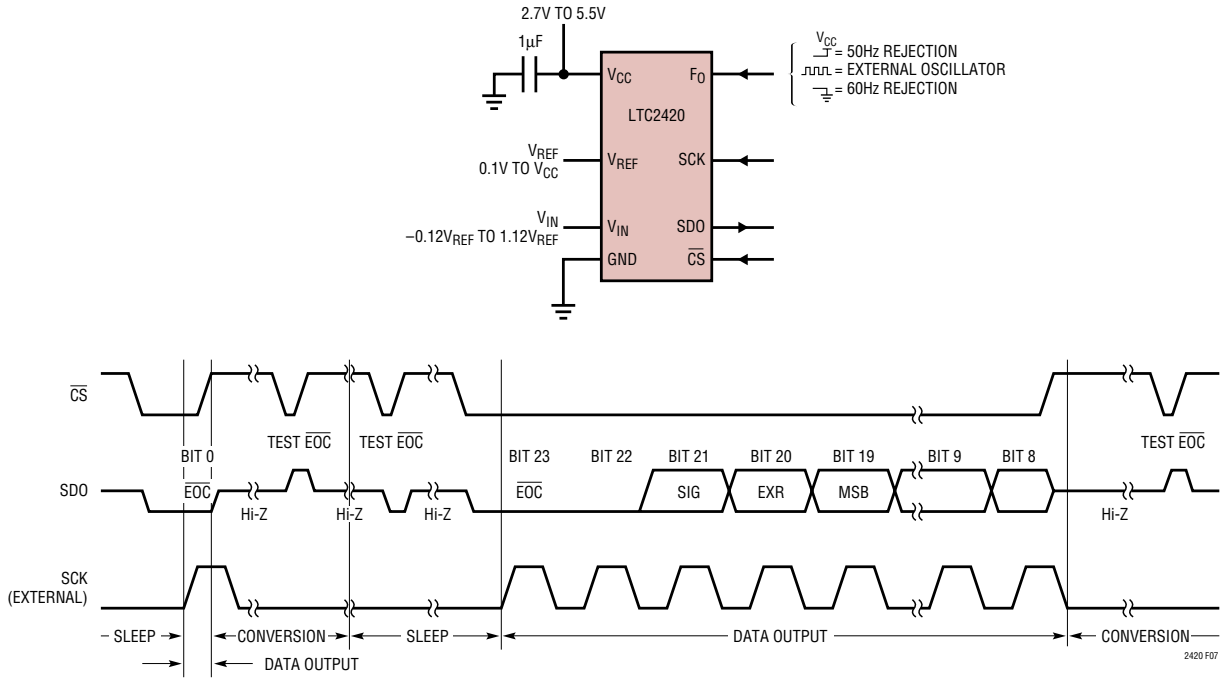


Figure 7. External Serial Clock, Reduced Data Output Length

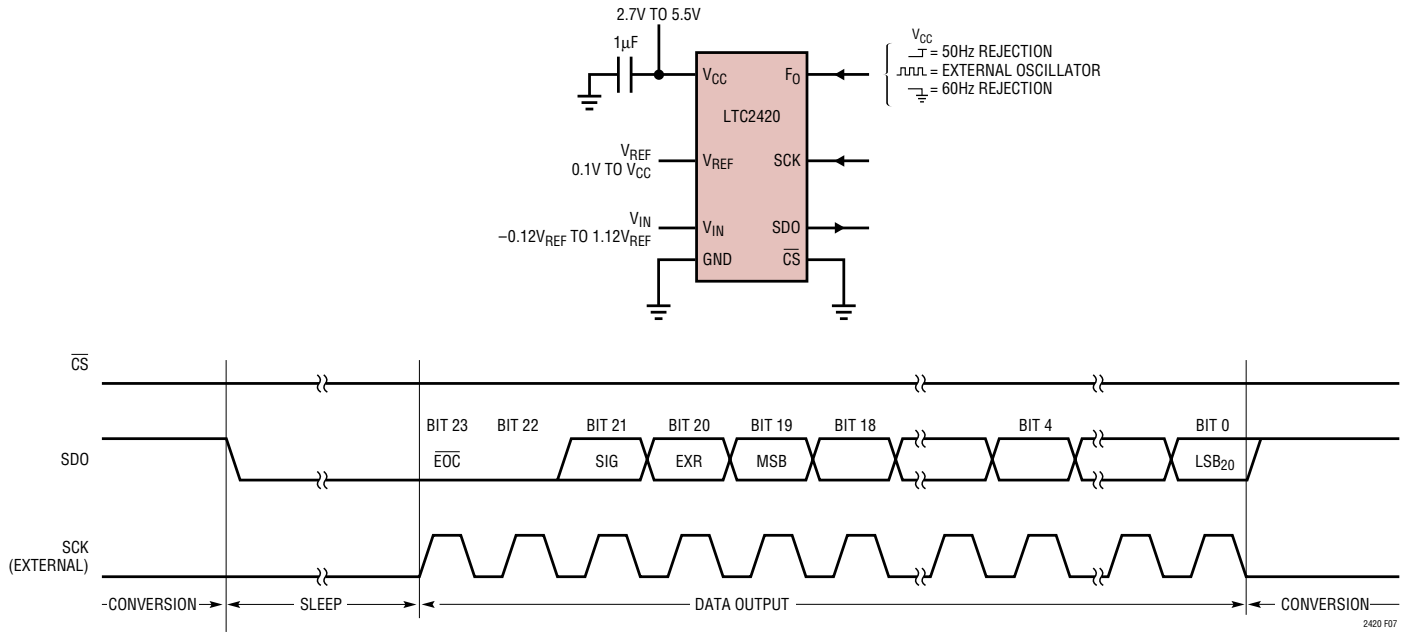


Figure 8. External Serial Clock, $\overline{CS}$ = 0 Operation

APPLICATIONS INFORMATION

into an internal static shift register. The device remains in the sleep state until the first rising edge of SCK. Data is shifted out the SDO pin on each falling edge of SCK enabling external circuitry to latch data on the rising edge of SCK. $\overline{EOC}$ can be latched on the first rising edge of SCK. On the 24th falling edge of SCK, SDO goes HIGH ($\overline{EOC}$ = 1) indicating a new conversion has begun.

Internal Serial Clock, Single Cycle Operation

This timing mode uses an internal serial clock to shift out the conversion result and a $\overline{CS}$ signal to monitor and control the state of the conversion cycle, see Figure 9.

In order to select the internal serial clock timing mode, the serial clock pin (SCK) must be floating (Hi-Z) or pulled HIGH prior to the falling edge of $\overline{CS}$. The device will not enter the internal serial clock mode if SCK is driven LOW on the falling edge of $\overline{CS}$. An internal weak pull-up resistor is active on the SCK pin during the falling edge of $\overline{CS}$; therefore, the internal serial clock timing mode is automatically selected if SCK is not externally driven.

The serial data output pin (SDO) is Hi-Z as long as $\overline{CS}$ is HIGH. At any time during the conversion cycle, $\overline{CS}$ may be pulled LOW in order to monitor the state of the converter. Once $\overline{CS}$ is pulled LOW, SCK goes LOW and $\overline{EOC}$ is output to the SDO pin. $\overline{EOC}$ = 1 while a conversion is in progress and $\overline{EOC}$ = 0 if the device is in the sleep state.

When testing $\overline{EOC}$, if the conversion is complete ($\overline{EOC}$ = 0), the device will exit the sleep state and enter the data output state if $\overline{CS}$ remains LOW. In order to prevent the device from exiting the low power sleep state, $\overline{CS}$ must be pulled HIGH before the first rising edge of SCK. In the internal SCK timing mode, SCK goes HIGH and the device begins outputting data at time $t_{EOCtest}$ after the falling edge of $\overline{CS}$ (if $\overline{EOC}$ = 0) or $t_{EOCtest}$ after $\overline{EOC}$ goes LOW (if $\overline{CS}$ is LOW during the falling edge of $\overline{EOC}$). The value of $t_{EOCtest}$ is 23µs if the device is using its internal oscillator (F_O = logic LOW or HIGH). If F_O is driven by an external oscillator of frequency f_{EOSC}, then $t_{EOCtest}$ is $3.6/f_{EOSC}$. If $\overline{CS}$ is pulled HIGH before time $t_{EOCtest}$, the device remains in the sleep state. The conversion result is held in the internal static shift register.

If $\overline{CS}$ remains LOW longer than $t_{EOCtest}$, the first rising edge of SCK will occur and the conversion result is serially shifted out of the SDO pin. The data output cycle begins on this first rising edge of SCK and concludes after the 24th rising edge. Data is shifted out the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the

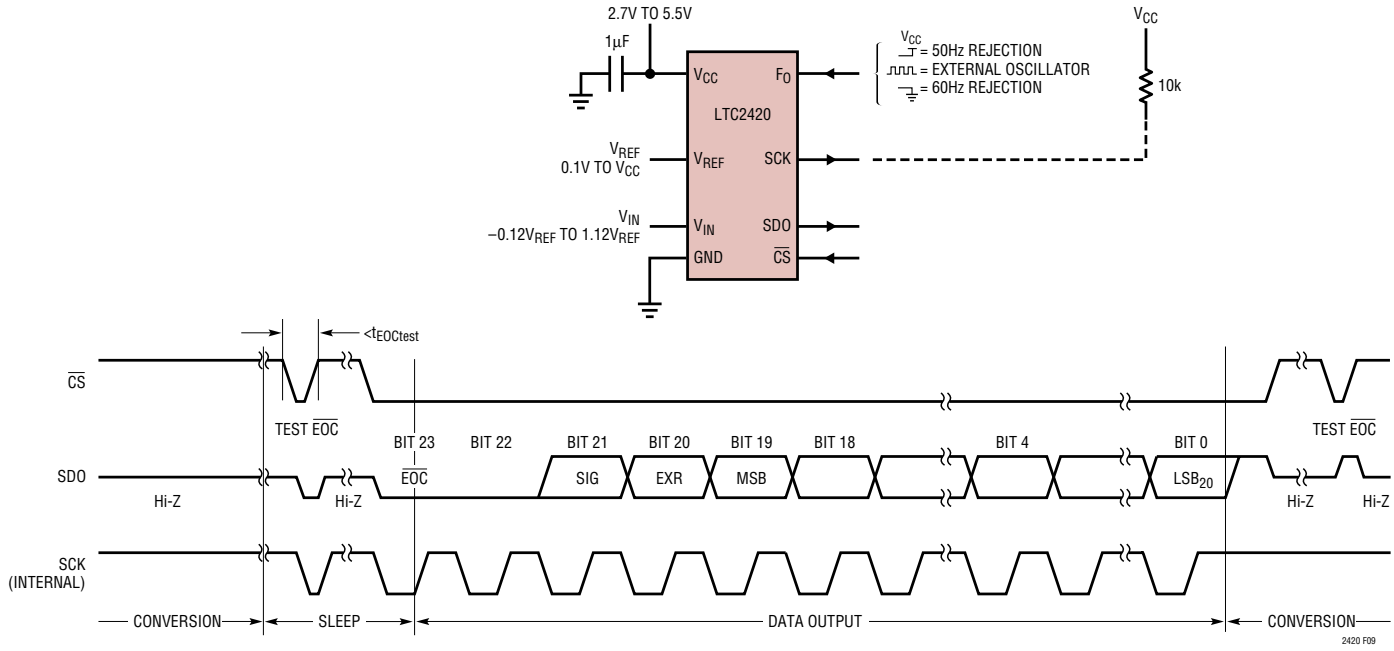


Figure 9. Internal Serial Clock, Single Cycle Operation

APPLICATIONS INFORMATION

conversion result into external circuitry. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result on the 24th rising edge of SCK. After the 24th rising edge, SDO goes HIGH ($\overline{EOC}$ = 1), SCK stays HIGH, and a new conversion starts.

Typically, $\overline{CS}$ remains LOW during the data output state. However, the data output state may be aborted by pulling $\overline{CS}$ HIGH anytime between the first and 24th rising edge of SCK, see Figure 10. On the rising edge of $\overline{CS}$, the device aborts the data output state and immediately initiates a new conversion. This is useful for systems not requiring all 24 bits of output data, aborting an invalid conversion cycle, or synchronizing the start of a conversion. If $\overline{CS}$ is pulled HIGH while the converter is driving SCK LOW, the internal pull-up is not available to restore SCK to a logic HIGH state. This will cause the device to exit the internal serial clock mode on the next falling edge of $\overline{CS}$. This can be avoided by adding an external 10k pull-up resistor to the SCK pin or by never pulling $\overline{CS}$ HIGH when SCK is LOW.

Whenever SCK is LOW, the LTC2420's internal pull-up at pin SCK is disabled. Normally, SCK is not externally driven if the device is in the internal SCK timing mode. However, certain applications may require an external driver on SCK. If this driver goes Hi-Z after outputting a LOW signal, the LTC2420's internal pull-up remains disabled. Hence, SCK remains LOW. On the next falling edge of $\overline{CS}$, the device is switched to the external SCK timing mode. By adding an external 10k pull-up resistor to SCK, this pin goes HIGH once the external driver goes Hi-Z. On the next $\overline{CS}$ falling edge, the device will remain in the internal SCK timing mode.

A similar situation may occur during the sleep state when $\overline{CS}$ is pulsed HIGH-LOW-HIGH in order to test the conversion status. If the device is in the sleep state ($\overline{EOC}$ = 0), SCK will go LOW. Once $\overline{CS}$ goes HIGH (within the time period defined above as $t_{EOCtest}$), the internal pull-up is activated. For a heavy capacitive load on the SCK pin, the internal pull-up may not be adequate to return SCK to a HIGH level before $\overline{CS}$ goes low again. This is not a concern under normal conditions where $\overline{CS}$ remains LOW after detecting $\overline{EOC}$ = 0. This situation is easily overcome by adding an external 10k pull-up resistor to the SCK pin.

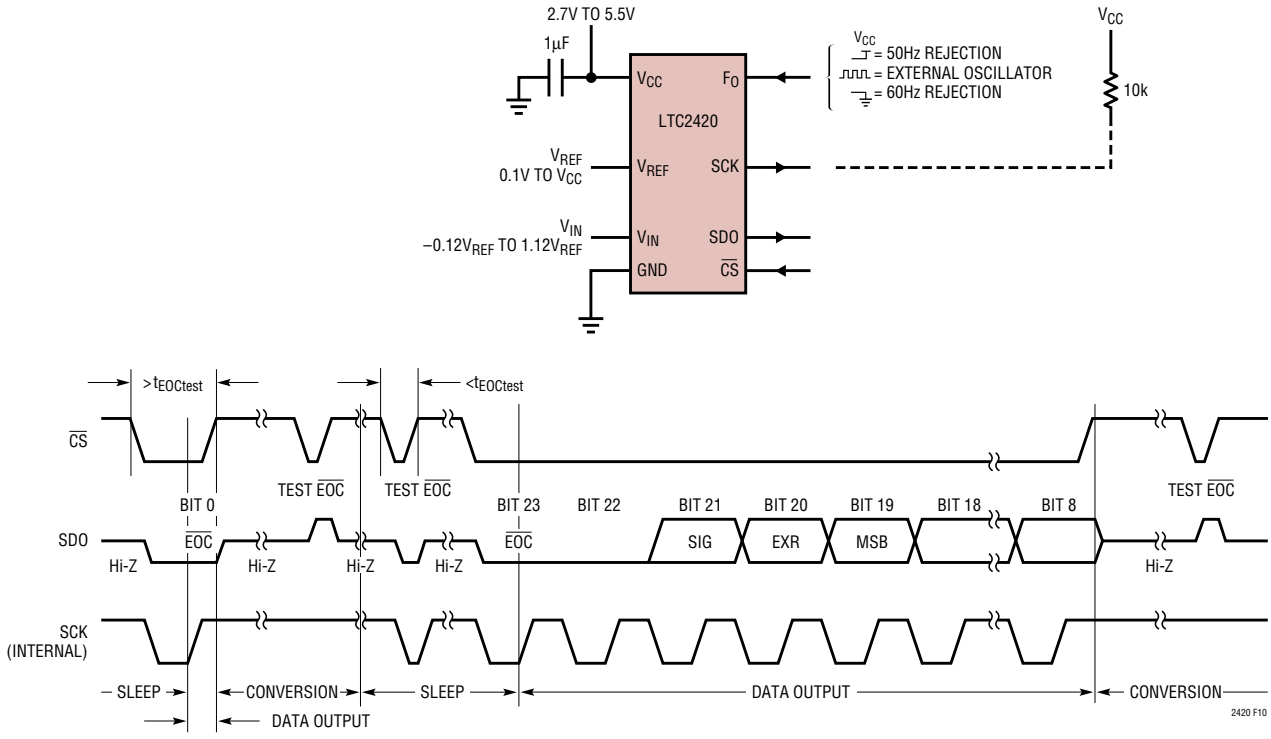


Figure 10. Internal Serial Clock, Reduced Data Output Length

APPLICATIONS INFORMATION

Internal Serial Clock, 2-Wire I/O, Continuous Conversion

This timing mode uses a 2-wire, all output (SCK and SDO) interface. The conversion result is shifted out of the device by an internally generated serial clock (SCK) signal, see Figure 11. $\overline{CS}$ may be permanently tied to ground (Pin 4), simplifying the user interface or isolation barrier.

The internal serial clock mode is selected at the end of the power-on reset (POR) cycle. The POR cycle is concluded approximately 0.5ms after V_{CC} exceeds 2.2V. An internal weak pull-up is active during the POR cycle; therefore, the internal serial clock timing mode is automatically selected if SCK is not externally driven LOW (if SCK is loaded such that the internal pull-up cannot pull the pin HIGH, the external SCK mode will be selected).

During the conversion, the SCK and the serial data output pin (SDO) are HIGH ($\overline{EOC}$ = 1). Once the conversion is complete, SCK and SDO go LOW ($\overline{EOC}$ = 0) indicating the conversion has finished and the device has entered the low power sleep state. The part remains in the sleep state a minimum amount of time (1/2 the internal SCK period) then immediately begins outputting data. The data output cycle begins on the first rising edge of SCK and ends after the 24th rising edge. Data is shifted out the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 24th rising edge of SCK. After the 24th rising edge, SDO goes HIGH ($\overline{EOC}$ = 1) indicating a new conversion is in progress. SCK remains HIGH during the conversion.

Internal Serial Clock, Autostart Conversion

This timing mode is identical to the internal serial clock, 2-wire I/O described above with one additional feature. Instead of grounding $\overline{CS}$, an external timing capacitor is tied to $\overline{CS}$.

While the conversion is in progress, the $\overline{CS}$ pin is held HIGH by an internal weak pull-up. Once the conversion is complete, the device enters the low power sleep state and an internal 25nA current source begins discharging the

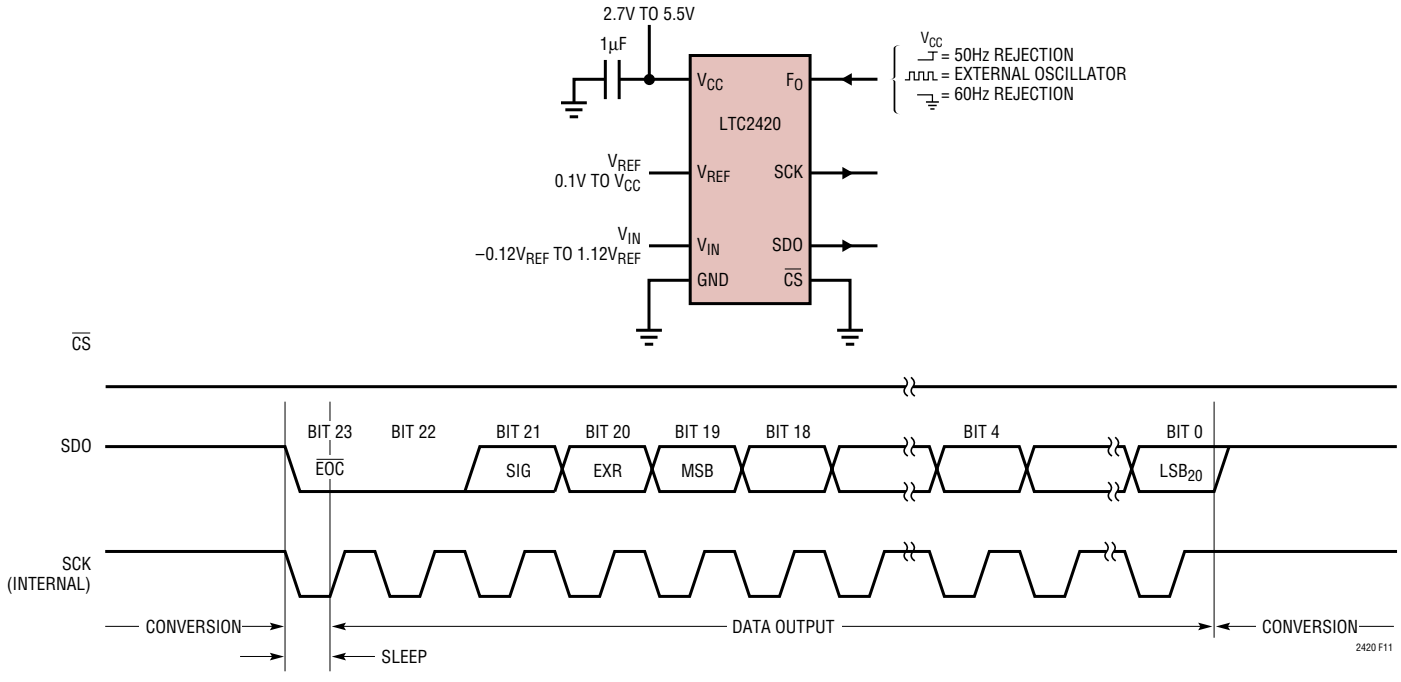


Figure 11. Internal Serial Clock, Continuous Operation

APPLICATIONS INFORMATION

capacitor tied to $\overline{CS}$, see Figure 12. The time the converter spends in the sleep state is determined by the value of the external timing capacitor, see Figures 13 and 14. Once the voltage at $\overline{CS}$ falls below an internal threshold (≈1.4V), the device automatically begins outputting data. The data output cycle begins on the first rising edge of SCK and ends on the 24th rising edge. Data is shifted out the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. After the 24th rising edge, $\overline{CS}$ is pulled HIGH and a new conversion is immediately started. This is useful in applications requiring periodic monitoring and ultralow power. Figure 15 shows the average supply current as a function of capacitance on $\overline{CS}$.

It should be noticed that the external capacitor discharge current is kept very small in order to decrease the converter power dissipation in the sleep state. In the autostart mode the analog voltage on the $\overline{CS}$ pin cannot be observed without disturbing the converter operation using a regular oscilloscope probe. When using this configuration, it is important to minimize the external leakage current at the $\overline{CS}$ pin by using a low leakage external capacitor and properly cleaning the PCB surface.

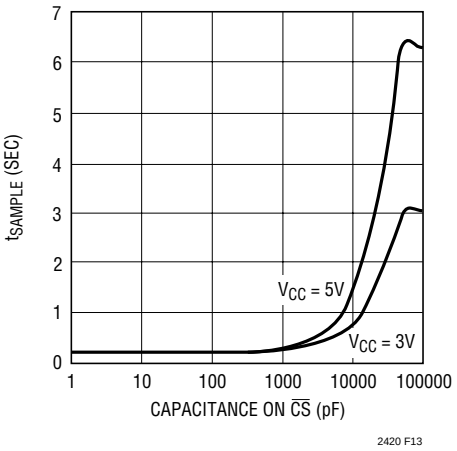


Figure 13. $\overline{CS}$ Capacitance vs f_{SAMPLE}

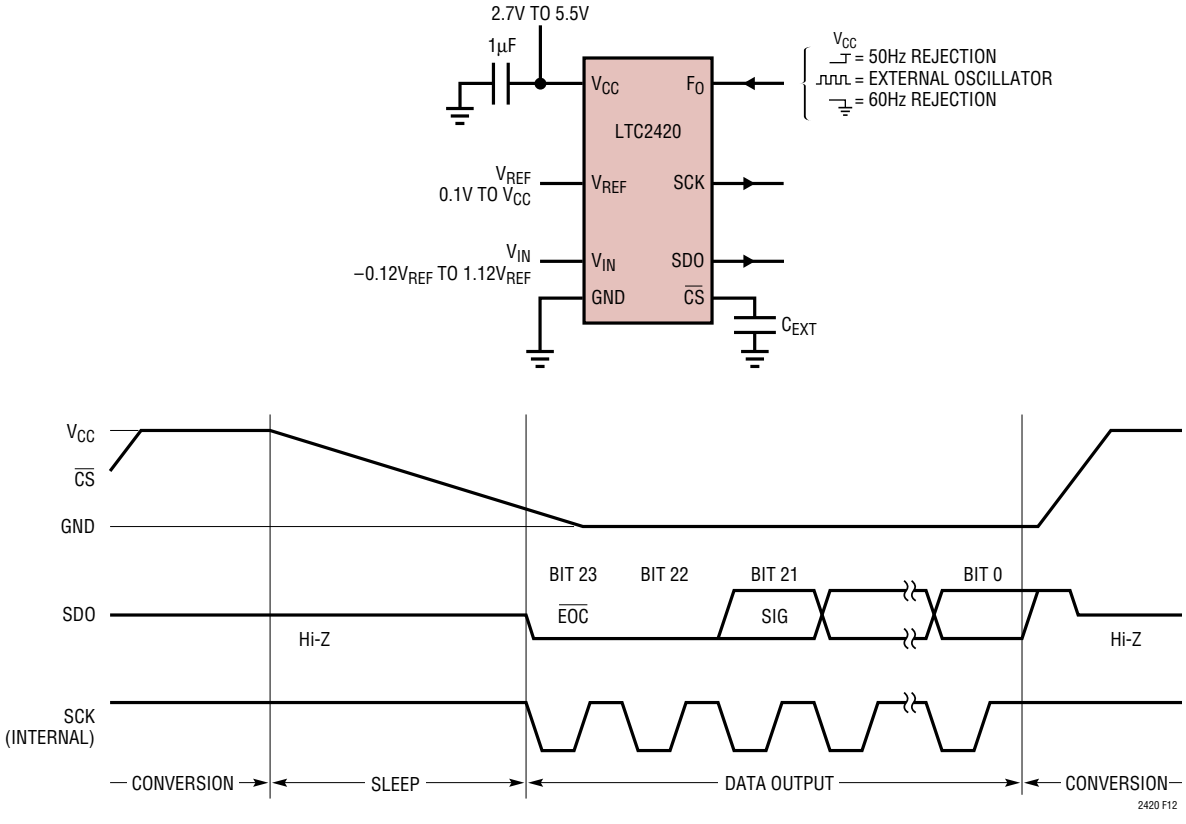


Figure 12. Internal Serial Clock, Autostart Operation

APPLICATIONS INFORMATION

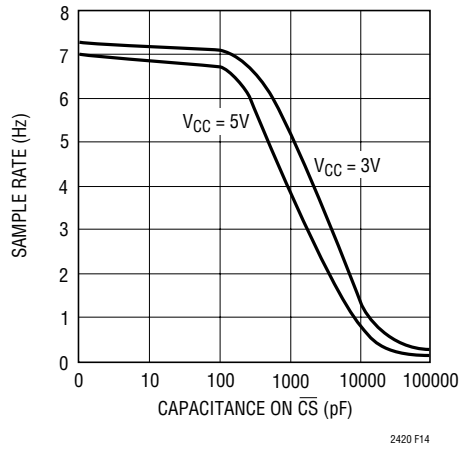


Figure 14. $\overline{CS}$ Capacitance vs Output Rate

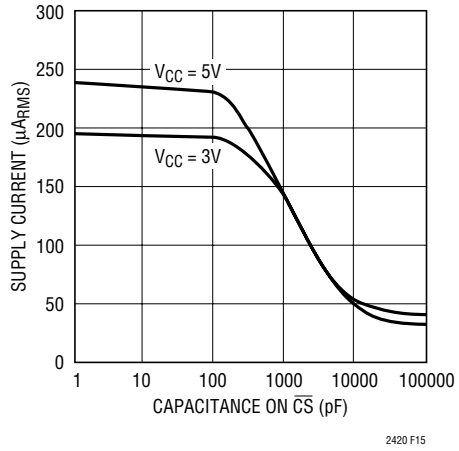


Figure 15. $\overline{CS}$ Capacitance vs Supply Current

The internal serial clock mode is selected every time the voltage on the $\overline{CS}$ pin crosses an internal threshold voltage. An internal weak pull-up at the SCK pin is active while $\overline{CS}$ is discharging; therefore, the internal serial clock timing mode is automatically selected if SCK is floating. It is important to ensure there are no external drivers pulling SCK LOW while $\overline{CS}$ is discharging.

DIGITAL SIGNAL LEVELS

The LTC2420's digital interface is easy to use. Its digital inputs (F_O, $\overline{CS}$ and SCK in External SCK mode of operation) accept standard TTL/CMOS logic levels and the internal hysteresis receivers can tolerate edge rates as slow as 100µs. However, some considerations are required to take advantage of exceptional accuracy and low supply current.

The digital output signals (SDO and SCK in Internal SCK mode of operation) are less of a concern because they are not generally active during the conversion state.

In order to preserve the LTC2420's accuracy, it is very important to minimize the ground path impedance which may appear in series with the input and/or reference signal and to reduce the current which may flow through this path. The GND pin should be connected to a low resistance ground plane through a minimum length trace. The use of multiple via holes is recommended to further reduce the connection resistance. The LTC2420's power supply current flowing through the 0.01Ω resistance of the common ground pin will develop a 2.5µV offset signal. For a reference voltage V_{REF} = 2.5V, this represents a 1ppm offset error.

In an alternative configuration, the GND pin of the converter can be the single-point-ground in a single point grounding system. The input signal ground, the reference signal ground, the digital drivers ground (usually the digital ground) and the power supply ground (the analog ground) should be connected in a star configuration with the common point located as close to the GND pin as possible.

The power supply current during the conversion state should be kept to a minimum. This is achieved by restricting the number of digital signal transitions occurring during this period.

While a digital input signal is in the range 0.5V to (V_{CC} – 0.5V), the CMOS input receiver draws additional current from the power supply. It should be noted that, when any one of the digital input signals (F_O, $\overline{CS}$ and SCK in External SCK mode of operation) is within this range, the LTC2420 power supply current may increase even if the signal in question is at a valid logic level. For micropower operation and in order to minimize the potential errors due to additional ground pin current, it is recommended to drive all digital input signals to full CMOS levels [V_{IL} < 0.4V and V_{OH} > (V_{CC} – 0.4V)].

Severe ground pin current disturbances can also occur due to the undershoot of fast digital input signals. Undershoot and overshoot can occur because of the impedance mismatch at the converter pin when the transition time of an external control signal is less than twice the

APPLICATIONS INFORMATION

propagation delay from the driver to LTC2420. For reference, on a regular FR-4 board, signal propagation velocity is approximately 183ps/inch for internal traces and 170ps/inch for surface traces. Thus, a driver generating a control signal with a minimum transition time of 1ns must be connected to the converter pin through a trace shorter than 2.5 inches. This problem becomes particularly difficult when shared control lines are used and multiple reflections may occur. The solution is to carefully terminate all transmission lines close to their characteristic impedance.

Parallel termination near the LTC2420 pin will eliminate this problem but will increase the driver power dissipation. A series resistor between 27Ω and 56Ω placed near the driver or near the LTC2420 pin will also eliminate this problem without additional power dissipation. The actual resistor value depends upon the trace impedance and connection topology.

Driving the Input and Reference

The analog input and reference of the typical delta-sigma analog-to-digital converter are applied to a switched capacitor network. This network consists of capacitors switching between the analog input (V_{IN}), ground (Pin 4) and the reference (V_{REF}). The result is small current spikes seen at both V_{IN} and V_{REF}. A simplified input equivalent circuit is shown in Figure 16.

The key to understanding the effects of this dynamic input current is based on a simple first order RC time constant model. Using the internal oscillator, the LTC2420's internal switched capacitor network is clocked at 153,600Hz corresponding to a 6.5μs sampling period. Fourteen time constants are required each time a capacitor is switched in order to achieve 1ppm settling accuracy.

Therefore, the equivalent time constant at V_{IN} and V_{REF} should be less than 6.5μs/14 = 460ns in order to achieve 1ppm accuracy.

Input Current (V_{IN})

If complete settling occurs on the input, conversion results will be uneffected by the dynamic input current. If the settling is incomplete, it does not degrade the linearity performance of the device. It simply results in an offset/full-scale shift, see Figure 17. To simplify the analysis of input dynamic current, two separate cases are assumed: large capacitance at V_{IN} (C_{IN} > 0.01μF) and small capacitance at V_{IN} (C_{IN} < 0.01μF).

If the total capacitance at V_{IN} (see Figure 18) is small (<0.01μF), relatively large external source resistances (up to 80k for 20pF parasitic capacitance) can be tolerated without any offset/full-scale error. Figures 19 and 20 show a family of offset and full-scale error curves for various small valued input capacitors (C_{IN} < 0.01μF) as a function of input source resistance.

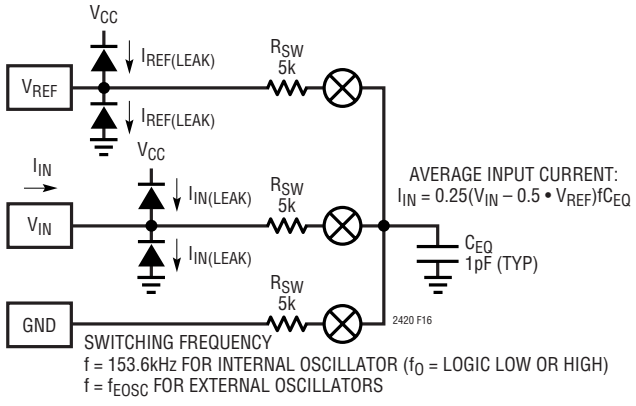


Figure 16. LTC2420 Equivalent Analog Input Circuit

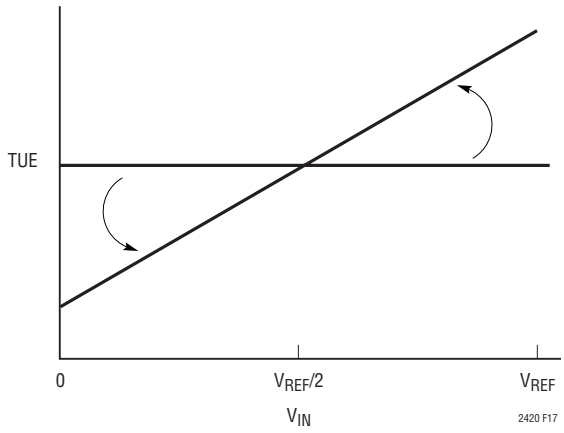


Figure 17. Offset/Full-Scale Shift

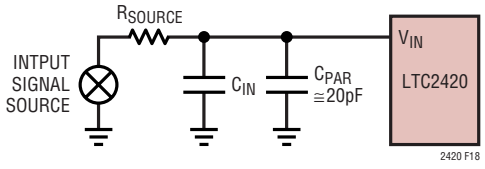


Figure 18. An RC Network at V_{IN}

APPLICATIONS INFORMATION

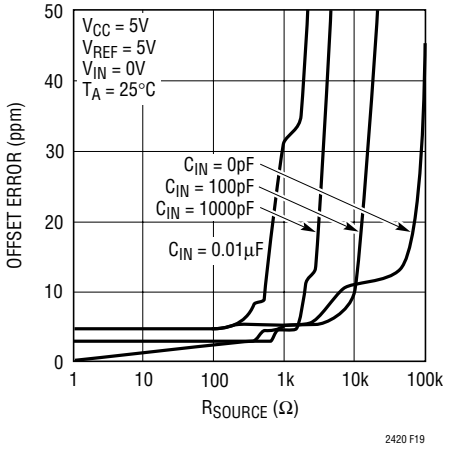


Figure 19. Offset vs R_{SOURCE} (Small C)

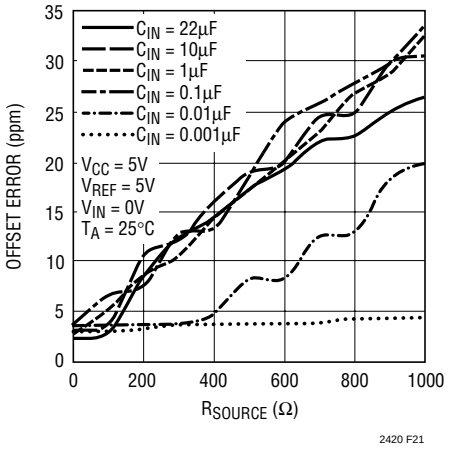


Figure 21. Offset vs R_{SOURCE} (Large C)

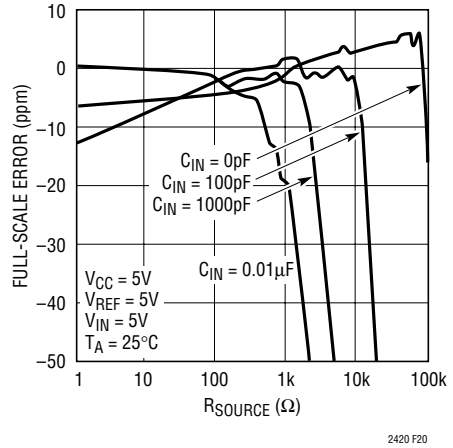


Figure 20. Full-Scale Error vs R_{SOURCE} (Small C)

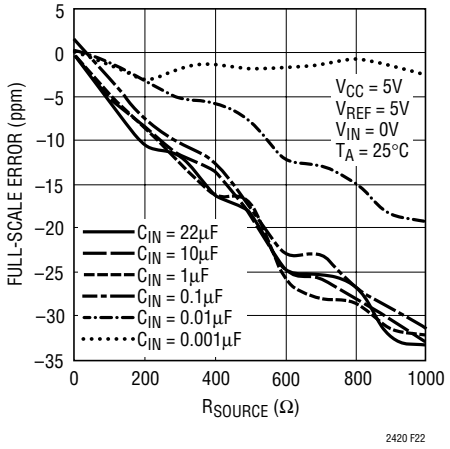


Figure 22. Full-Scale Error vs R_{SOURCE} (Large C)

For large input capacitor values (C_{IN} > 0.01µF), the input spikes are averaged by the capacitor into a DC current. The gain shift becomes a linear function of input source resistance independent of input capacitance, see Figures 21 and 22. The equivalent input impedance is 16.6MΩ. This results in ±150nA of input dynamic current at the extreme values of V_{IN} (V_{IN} = 0V and V_{IN} = V_{REF}, when V_{REF} = 5V). This corresponds to a 0.3ppm shift in offset and full-scale readings for every 10Ω of input source resistance.

In addition to the input current spikes, the input ESD protection diodes have a temperature dependent leakage current. This leakage current, nominally 1nA (±10nA max), results in a fixed offset shift of 10µV for a 10k source resistance.

Reference Current (V_{REF})

Similar to the analog input, the reference input has a dynamic input current. This current has negligible effect on the offset. However, the reference current at V_{IN} = V_{REF} is similar to the input current at full-scale. For large values of reference capacitance (C_{VREF} > 0.01µF), the full-scale error shift is 0.03ppm/Ω of external reference resistance independent of the capacitance at V_{REF}, see Figure 23. If the capacitance tied to V_{REF} is small (C_{VREF} < 0.01µF), an input resistance of up to 80k (20pF parasitic capacitance at V_{REF}) may be tolerated, see Figure 24.

Unlike the analog input, the integral nonlinearity of the device can be degraded with excessive external RC time constants tied to the reference input. If the capacitance at

APPLICATIONS INFORMATION

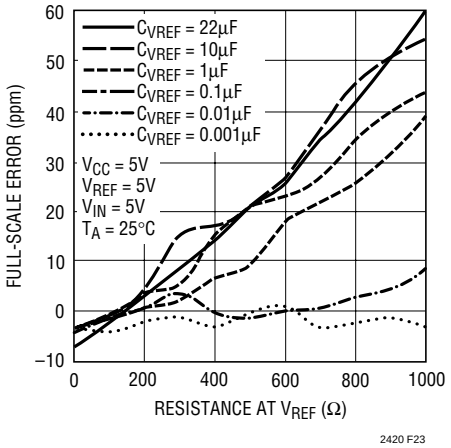


Figure 23. Full-Scale Error vs R_{VREF} (Large C)

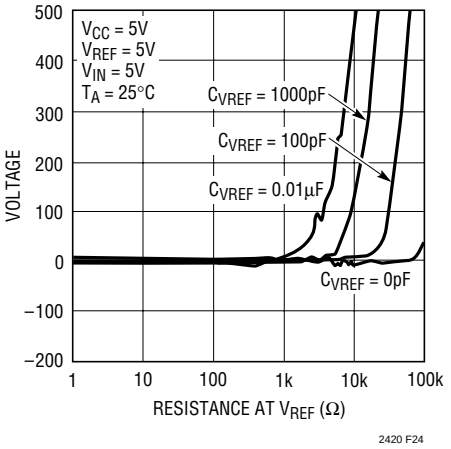


Figure 24. Full-Scale Error vs R_{VREF} (Small C)

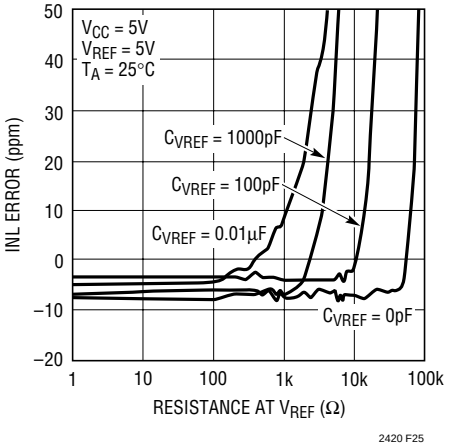


Figure 25. INL Error vs R_{VREF} (Small C)

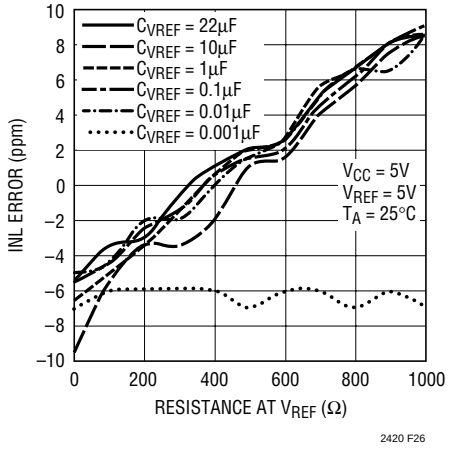


Figure 26. INL Error vs R_{VREF} (Large C)

node V_{REF} is small (C_{VREF} < 0.01µF), the reference input can tolerate large external resistances without reduction in INL, see Figure 25. If the external capacitance is large (C_{VREF} > 0.01µF), the linearity will be degraded by 0.015ppm/Ω independent of capacitance at V_{REF}, see Figure 26.

In addition to the dynamic reference current, the V_{REF} ESD protection diodes have a temperature dependent leakage current. This leakage current, nominally 1nA (±10nA max), results in a fixed full-scale shift of 10µV for a 10k source resistance.

ANTIALIASING

One of the advantages delta-sigma ADCs offer over conventional ADCs is on-chip digital filtering. Combined with a large oversampling ratio, the LTC2420 significantly simplifies antialiasing filter requirements.

The digital filter provides very high rejection except at integer multiples of the modulator sampling frequency (f_S), see Figure 27. The modulator sampling frequency is 256 • F_O, where F_O is the notch frequency (typically 50Hz or 60Hz). The bandwidth of signals not rejected by the digital filter is narrow (≈ 0.2%) compared to the bandwidth of the frequencies rejected.

APPLICATIONS INFORMATION

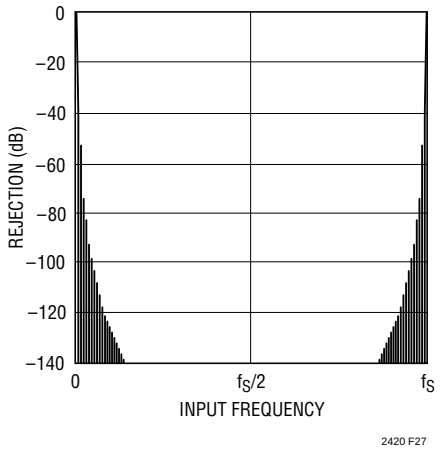


Figure 27. Sinc^4 Filter Rejection

As a result of the oversampling ratio (256) and the digital filter, minimal (if any) antialias filtering is required in front of the LTC2420. If passive RC components are placed in front of the LTC2420 the input dynamic current should be considered (see Input Current section). In cases where large effective RC time constants are used, an external buffer amplifier may be required to minimize the effects of input dynamic current.

The modulator contained within the LTC2420 can handle large-signal level perturbations without saturating. Signal levels up to 40% of V_{REF} do not saturate the analog modulator. These signals are limited by the input ESD protection to 300mV below ground and 300mV above V_{CC}.

Operation at Higher Data Output Rates

The LTC2420 typically operates with an internal oscillator of 153.6kHz. This corresponds to a notch frequency of 60Hz and an output rate of 7.5 samples/second. The internal oscillator is enabled if the F_O pin is logic LOW (logic HIGH for a 50Hz notch). It is possible to drive the F_O pin with an external oscillator for higher data output rates. As shown in Figure 28, an external clock of 2.048MHz applied to the F_O pin results in a notch frequency of 800Hz with a data output rate of 100 samples/second.

Figure 29 shows the total unadjusted error (Offset Error + Full-Scale Error + INL + DNL) as a function of the output data rate with a 5V reference. The relationship between the

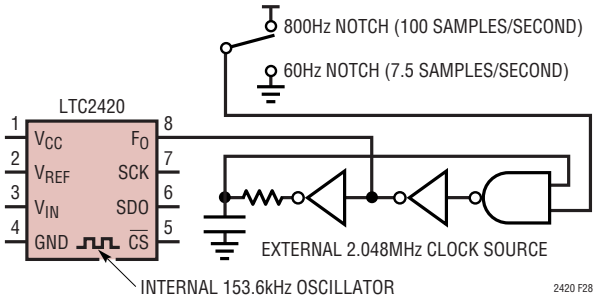


Figure 28. Selectable 100 Samples/Second Turbo Mode

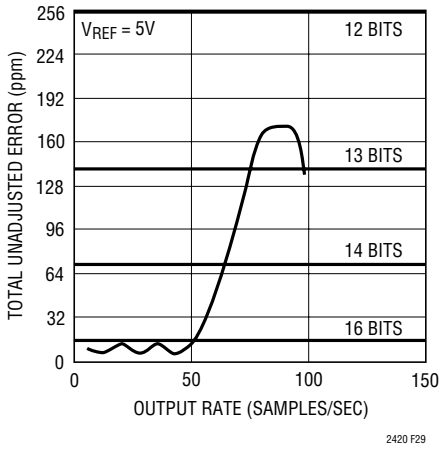


Figure 29. Total Error vs Output Rate (V_{REF} = 5V)

output data rate (ODR) and the frequency applied to the F_O pin (F_O) is:

$$ODR = F_O/20480$$

For output data rates up to 50 samples/second, the total unadjusted error (TUE) is better than 16 bits, and better than 12 bits at 100 samples/second. As shown in Figure 30, for output data rates of 100 samples/second, the TUE is better than 15 bits for V_{REF} below 2.5V. Figure 31 shows an unaveraged total unadjusted error for the LTC2420 operating at 100 samples/second with V_{REF} = 2.5V. Figure 32 shows the same device operating with a 5V reference and an output data rate of 7.5 samples/second.

At 100 samples/second, the LTC2420 can be used to capture transient data. This is useful for monitoring settling or auto gain ranging in a system. The LTC2420 can monitor signals at an output rate of 100 samples/second.

APPLICATIONS INFORMATION

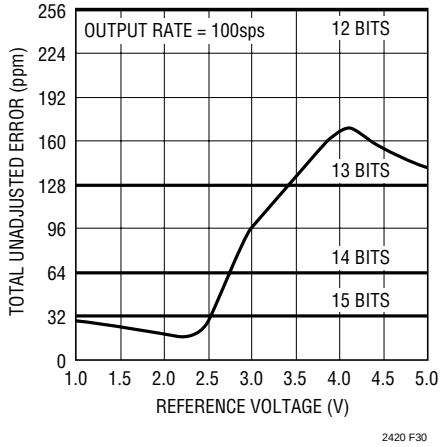


Figure 30. Total Error vs V_{REF} (Output Rate = 100sps)

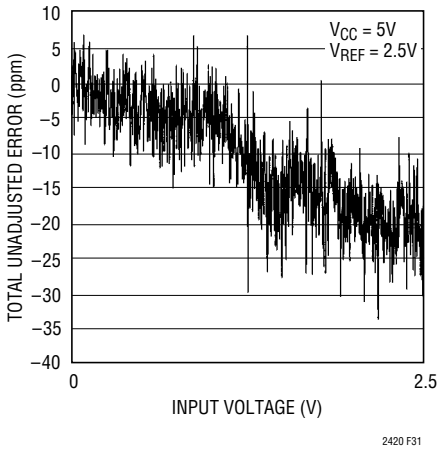


Figure 31. Total Unadjusted Error at 100 Samples/Second (No Averaging)

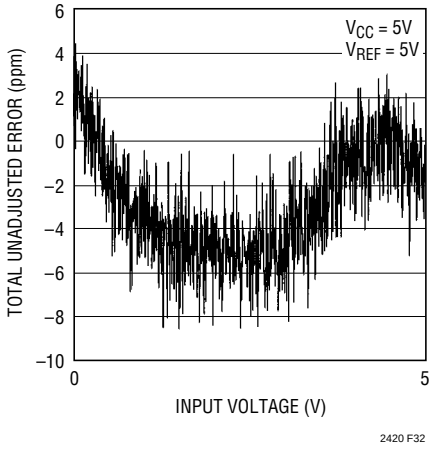
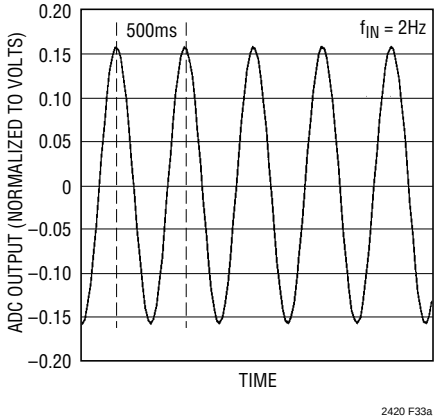


Figure 32. Total Unadjusted Error at 7.5 Samples/Second (No Averaging)

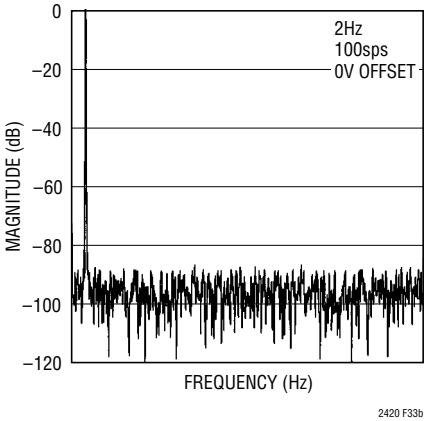
After acquiring 100 samples/second data the F_O pin may be driven LOW enabling 60Hz rejection to 110dB and the highest possible DC accuracy. The no latency architecture of the LTC2420 allows consecutive readings (one at 100 samples/second the next at 7.5 samples/second) without interaction between the two readings.

As shown in Figure 33, the LTC2420 can capture transient data with 90dB of dynamic range (with a 300mV_{P-P} input signal at 2Hz). The exceptional DC performance of the LTC2420 enables signals to be digitized independent of a large DC offset. Figures 34a and 34b show the dynamic performance with a 15Hz signal superimposed on a 2V DC level. The same signal with no DC level is shown in Figures 34c and 34d.

APPLICATIONS INFORMATION

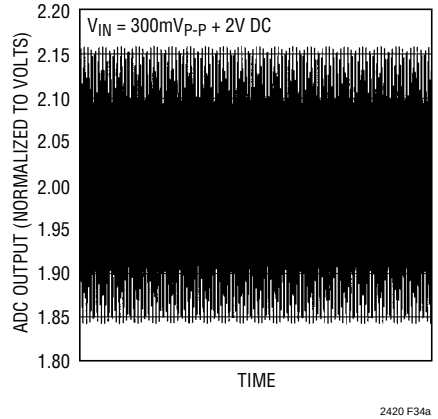


33a. Digitized Waveform

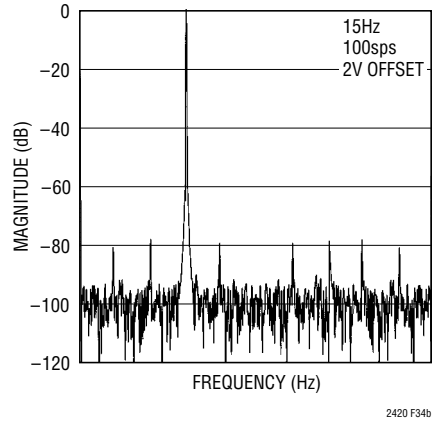


33b. Output FFT

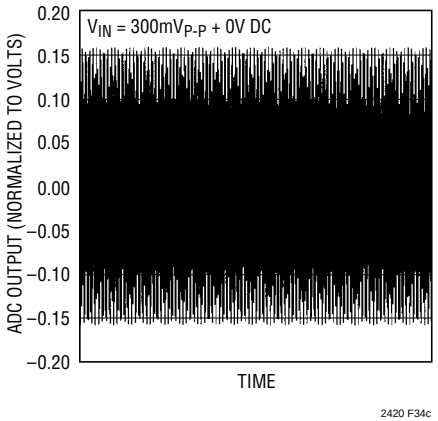
Figure 33. Transient Signal Acquisiton



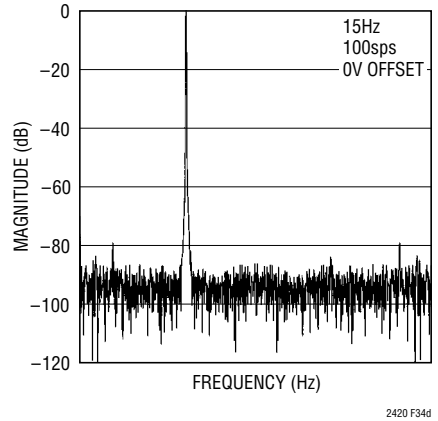
34a. Digitized Waveform with 2V DC Offset



34b. FFT Waveform with 2V DC Offset



34c. Digitized Waveform with No Offset



34d. FFT Waveform with No Offset

Figure 34. Using the LTC2420's High Accuracy Wide Dynamic Range to Digitize a 300mV_{P-P} 15Hz Waveform with a Large DC Offset (V_{CC} = 5V, V_{REF} = 5V)

TYPICAL APPLICATIONS

SYNCHRONIZATION OF MULTIPLE LTC2420s

Since the LTC2420's absolute accuracy (total unadjusted error) is 10ppm, applications utilizing multiple matched ADCs are possible.

Simultaneous Sampling with Two LTC2420s

One such application is synchronizing multiple LTC2420s, see Figure 35. The start of conversion is synchronized to the rising edge of $\overline{CS}$. In order to synchronize multiple LTC2420s, $\overline{CS}$ is a common input to all the ADCs. To prevent the converters from autostarting a new conversion at the end of data output read, 23 or fewer SCK clock signals are applied to the LTC2420 instead of 24 (the 24th falling edge would start a conversion). The exact timing and frequency for the SCK signal is not critical since it is only shifting out the data. In this case, two LTC2420's simultaneously start and end their conversion cycles under the external control of $\overline{CS}$.

Increasing the Output Rate Using Multiple LTC2420s

A second application uses multiple LTC2420s to increase the effective output rate by 4×, see Figure 36. In this case, four LTC2420s are interleaved under the control of separate $\overline{CS}$ signals. This increases the effective output rate from 7.5Hz to 30Hz (up to a maximum of 400Hz). Additionally, the one-shot output spectrum is unfolded allowing further digital signal processing of the conversion results. SCK and SDO may be common to all four LTC2420s. The four $\overline{CS}$ rising edges equally divide one LTC2420 conversion cycle (7.5Hz for 60Hz notch frequency). In order to synchronize the start of conversion to $\overline{CS}$, 23 or less SCK clock pulses must be applied to each ADC.

Both the synchronous and 4× output rate applications use the external serial clock and single cycle operation with reduced data output length (see Serial Interface Timing Modes section and Figure 7). An external oscillator clock is applied commonly to the F_O pin of each LTC2420 in order to synchronize the sampling times. Both circuits may be extended to include more LTC2420s.

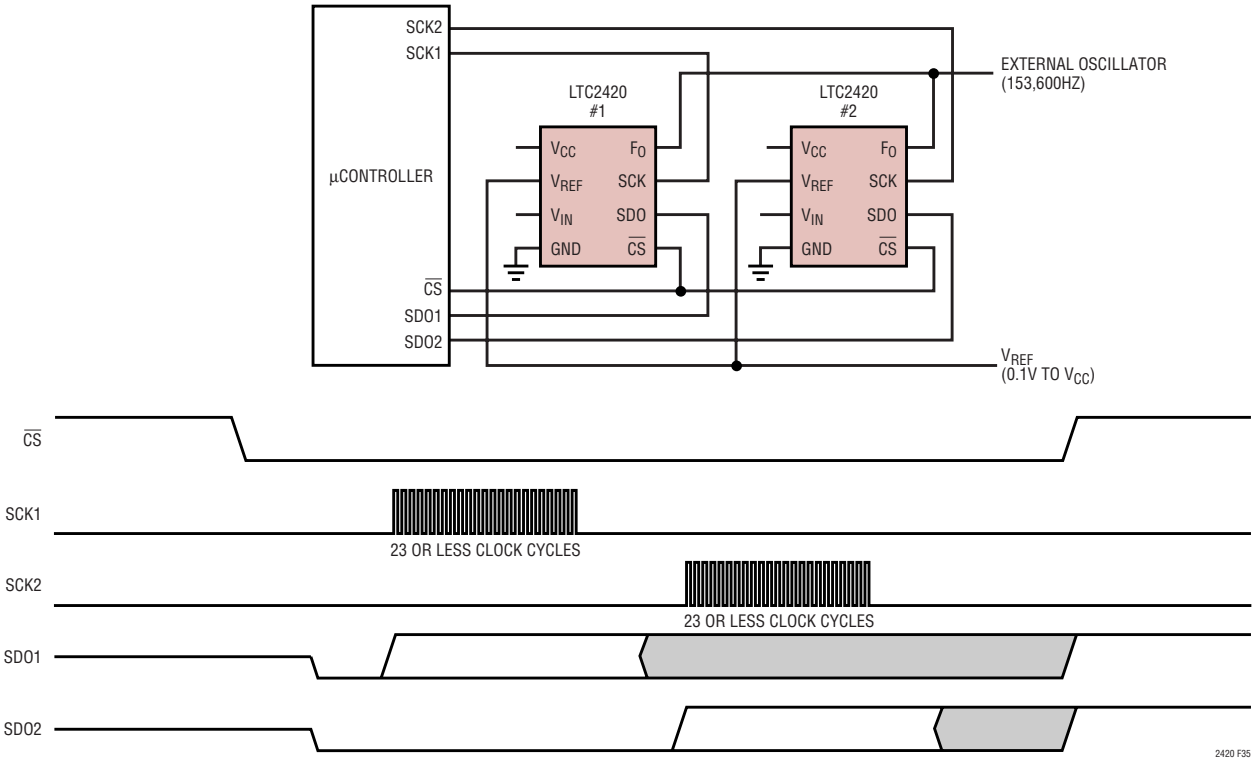


Figure 35. Synchronous Conversion—Extendable

TYPICAL APPLICATIONS

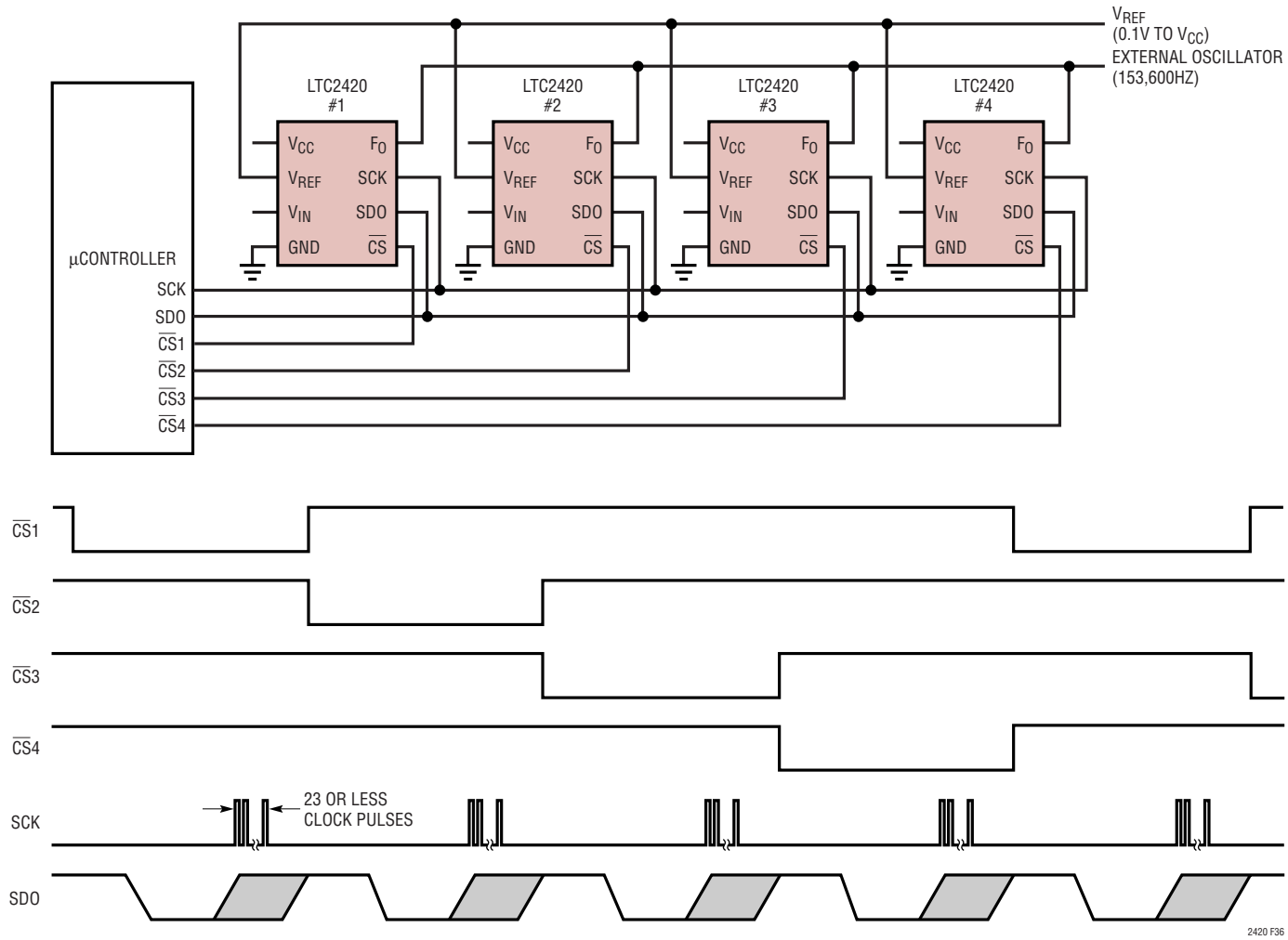


Figure 36. 4× Output Rate LTC2420 System

TYPICAL APPLICATIONS

Single-Chip Instrumentation Amplifier for the LTC2420

The circuit in Figure 37 is a simple solution for processing differential signals in pressure transducer, weigh scale or strain gauge applications that can operate on a supply voltage range of ±5V to ±15V. The circuit uses an LT®1920 single-chip instrumentation amplifier to perform a differential to single-ended conversion. The amplifier's output voltage is applied to the LTC2420's input and converted to a digital value with an overall accuracy exceeding 17 bits (0.0008%). Key circuit performance results are shown in Table 5.

The practical gain range for this topology as shown is from 5 to 100 because the LTC2420's wide dynamic range makes gains below 5 virtually unnecessary, whereas gains up to 100 significantly reduce the input referred noise.

The optional passive RC lowpass filter between the amplifier's output and the LTC2420's input attenuates high frequency noise and its effects. Typically, the filter reduces the magnitude of averaged noise by 30% and improves resolution by 0.5 bit without compromising linearity. Resistor R2 performs two functions: it isolates C1 from the LTC2420's input and limits the LTC2420's input current should its input voltage drop below –300mV or swing above V_{CC} + 300mV.

The LT1920 is the choice for applications where low cost is important. For applications where more precision is required, the LT1167 is a pin-to-pin alternative choice with a lower offset voltage, lower input bias current and higher gain accuracy than the LT1920. The LT1920's maximum total input-referred offset (V_{OST}) is 135µV for a gain of 100. At the same gain, the LT1167's V_{OST} is 63µV. At gains of 10 or 100, the LT1920's maximum gain error is 0.3% and its maximum gain nonlinearity is 30ppm. At the same gains, the LT1167's maximum gain error is 0.1% and its maximum gain nonlinearity is 15ppm. Table 6 summarizes the performance of Figure 37's circuit using the LT1167.

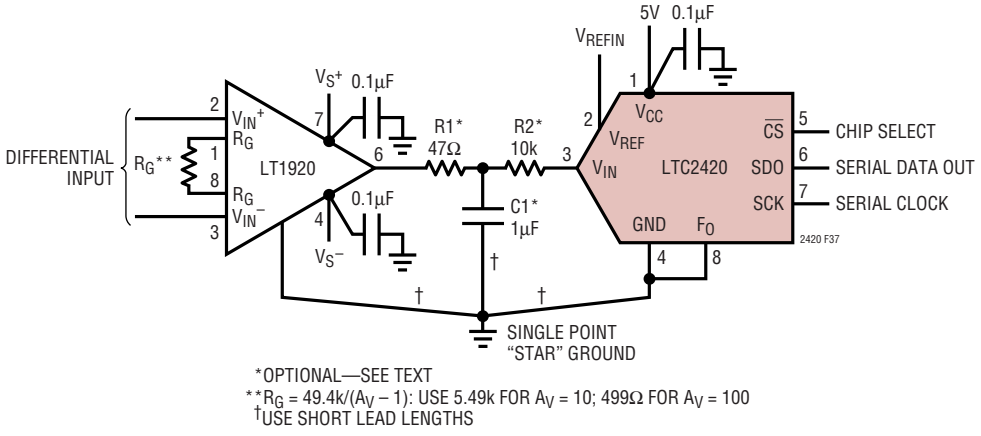


Figure 37. The LT1920 is a Simple Solution That Converts a Differential Input to a Ground Referred Single-Ended Signal for the LTC2420

TYPICAL APPLICATIONS

Table 5. Typical Performance of the LTC2420 ADC When Used with the LT1920 Instrumentation Amplifiers in Figure 34's Differential Digitizing Circuit

	V_S = ±5V		V_S = ±15V		
PARAMETER	**A_V = 10**	**A_V = 100**	**A_V = 10**	**A_V = 100**	**TOTAL (UNITS)**
Differential Input Voltage Range	–30 to 400	–3 to 40	–30 to 500	–3 to 50	mV
Zero Error	–160	–2650	–213	–2625	µV
Maximum Input Current		2.0			nA
Nonlinearity	±8.2	±7.4	±6.5	±6.1	ppm
Noise (Without Averaging)	1.8*	0.25*	1.5*	0.27*	μV_{RMS}
Noise (Averaged 64 Readings)	0.2*	0.03*	0.19*	0.03*	μV_{RMS}
Resolution (with Averaged Readings)	21	20.6	21.3	20.5	Bits
Overall Accuracy (Uncalibrated)	17.2	17.3	17.5	18.2	Bits
Common Mode Rejection Ratio		≥120			dB
Common Mode Range	2/–1.5**	2.2/–1.7**	11.5/–11**	11.7/–11.2**	V

*Input referred noise for the respective gain. **Typical values based on single lab tested sample of each amplifier.

Table 6. Typical Performance of the LTC2420 ADC When Used with the LT1167 Instrumentation Amplifiers in Figure 34's Differential Digitizing Circuit

	V_S = ±5V		V_S = ±15V		
PARAMETER	**A_V = 10**	**A_V = 100**	**A_V = 10**	**A_V = 100**	**TOTAL (UNITS)**
Differential Input Voltage Range	–30 to 400	–3 to 40	–30 to 500	–3 to 50	mV
Zero Error	–94	–1590	–110	–1470	µV
Maximum Input Current		0.5			nA
Nonlinearity	±4.1	±4.4	±4.1	±3.7	ppm
Noise (Without Averaging)	1.4*	0.19*	1.5*	0.18*	μV_{RMS}
Noise (Averaged 64 Readings)	0.18*	0.02*	0.19*	0.02*	μV_{RMS}
Resolution (with Averaged Readings)	21.4	21.0	21.3	21.1	Bits
Overall Accuracy (Uncalibrated)	18.2	18.1	18.2	19.4	Bits
Common Mode Rejection Ratio		≥120			dB
Common Mode Range	2/–1.5**	2.2/–1.7**	11.5/–11**	11.7/–11.2**	V

*Input referred noise for the respective gain. **Typical values based on single lab tested sample of each amplifier.

TYPICAL APPLICATIONS

Using a Low Power Precision Reference

The circuit in Figure 38 shows the connections and bypassing for an LT1461-2.5 as a 2.5V reference. The LT1461 is a bandgap reference capable of 3ppm/°C temperature stability yet consumes only 45μA of current. The 1k resistor between the reference and the ADC reduces the transient load changes associated with sampling and produces optimal results. This reference will not impact the noise level of the LTC2420 if signals are less than 60% full scale, and only marginally increases noise approaching full scale. Even lower power references can be used if only the lower end of the LTC2420 input range is required.

A Differential to Single-Ended Analog Front End

Figure 39 shows the LT1167 as a means of sensing differential signals. The noise performance of the LT1167 is such that for gains less than 200, the noise floor of the LTC2420 remains the dominant noise source. At the point where the noise of the amplifier begins to dominate, the input referred noise is essentially that of the instrumentation amplifier. The linearity of the instrumentation amplifier does, however, degrade at higher gains. As a result, if the full linearity of the LTC2420 is desired, gain in the instrumentation amplifier should be limited to less than 100, possibly requiring averaging multiple samples to extend the resolution below the noise floor. The noise level of the LT1167 at gains greater than 100 is on the order of $50nV_{RMS}$, although, 1/f noise and temperature effects may degrade this below 0.1Hz. The introduction of a filter between the amplifier and the LTC2420 may improve noise levels under some circumstances by reducing noise bandwidth. Note that temperature offset drift effects envelope detection in the input of the LT1167 if exposed to RFI, thermocouple voltages in connectors, resistors and soldered junctions can all compromise results, appearing as drift or noise. Turbulent airflow over this circuitry should be avoided.

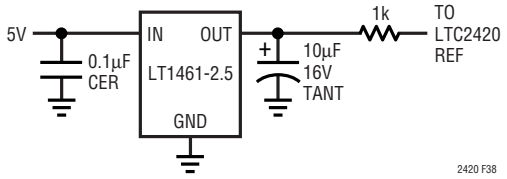
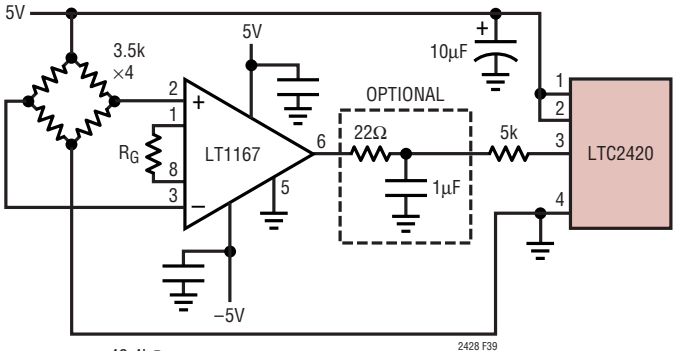


Figure 38. Low Power Reference



$A_V = \frac{49.4k\Omega}{R_G} + 1$

RECOMMENDED R_G: 500Ω, 0.1%
5ppm/°C

Figure 39. A Differential to Single-Ended Analog Front End

TYPICAL APPLICATIONS

2.048MHz Oscillator for 100sps Output Ratio

The oscillator circuit shown in Figure 40 can be used to drive the F_O pin, boosting the conversion rate of the LTC2420 for applications that do not require a notch at 50Hz or 60Hz. This oscillator is not sensitive to hysteresis voltage of a Schmitt trigger device as are simpler relaxation oscillators using the 74HC14 or similar devices. The circuit can be tuned over a 3:1 range with only one resistor and can be gated. The use of transmission gates could be used to shift the frequency in order to provide setable conversion rates.

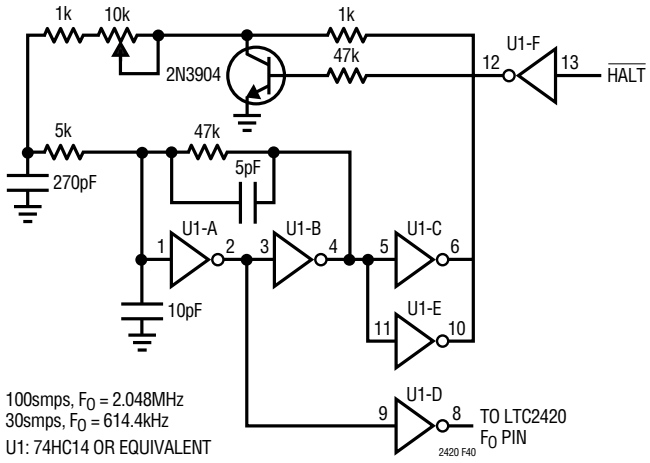
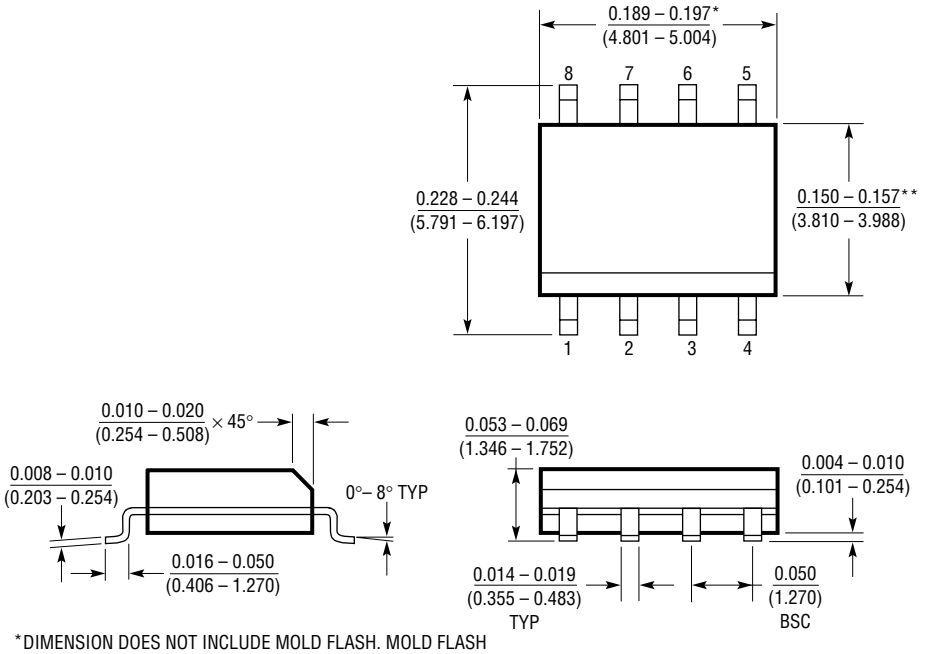


Figure 40. 2.048MHz Oscillator for 100sps Output Rate

PACKAGE INFORMATION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

SO8 1298

TYPICAL APPLICATION

The circuit shown in Figure 41 enables pseudodifferential measurements of several bridge transducers and absolute temperature measurement. The LTC1391 is an 8-to-1 analog multiplexer.

Consecutive readings are performed on each side of the bridge by selecting the appropriate channel on the LTC1391. Each output is digitized and the results digitally subtracted to obtain the pseudodifferential result. Several bridge transducers may be digitized in this manner.

In order to measure absolute temperature with a thermocouple, cold junction compensation must be performed. Channel 6 measures the output of the thermocouple while channel 7 measures the output of the cold junction sensor (diode, thermistor, etc.). This enables digital cold junction compensation of the thermocouple output. The temperature measurement may then be used to compensate the temperature effects of the bridge transducers.

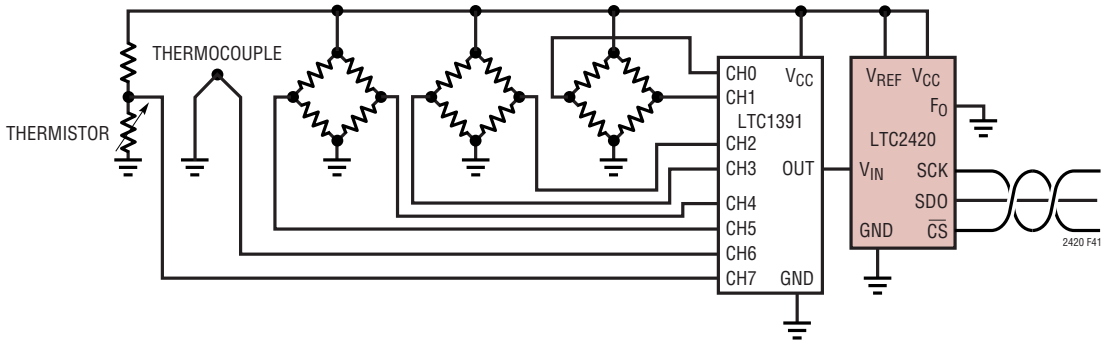


Figure 41. Pseudodifferential Multichannel Bridge Digitizer and Digital Cold Junction Compensation

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1019	Precision Bandgap Voltage Reference, 2.5V, 5V	3ppm/°C Drift, 0.05% Max
LT1025	Micropower Thermocouple Cold Junction Compensator	0.5°C Initial Accuracy, 80μA Supply Current
LTC1043	Dual Precision Instrumentation Switched Capacitor Building Block	Precise Charge, Balanced Switching, Low Power
LTC1050	Precision Chopper Stabilized Op Amp	No External Components 5μV Offset, 1.6μV_{P-P} Noise
LT1236A-5	Precision Bandgap Voltage Reference, 5V	0.05% Max, 5ppm/°C Drift
LTC1391	8-Channel Multiplexer	Low R_{ON}: 45Ω, Low Charge Injection, Serial Interface
LT1460	Micropower Series Voltage Reference	0.075% Max, 10ppm/°C Max Drift, 2.5V, 5V and 10V Versions
LTC2400	24-Bit μPower, No Latency ΔΣ ADC in SO-8	4ppm INL, 10ppm TUE, 200μA, Pin Compatible with LTC2420
LTC2401/LTC2402	1-/2-Channel, 24-Bit No Latency ΔΣ ADCs	24 Bits in MSOP Package
LTC2404/LTC2408	4-/8-Channel, 24-Bit No Latency ΔΣ ADC	4ppm INL, 10ppm TUE, 200μA
LTC2410	24-Bit No Latency ΔΣ ADC with Differential Inputs	800nV Noise, Differential Reference, 2.7V to 5.5V Operation
LTC2411	24-Bit No Latency ΔΣ ADC with Differential Inputs/Reference	1.6μV Noise, Fully Differential, 10-Lead MSOP Package
LTC2413	24-Bit No Latency ΔΣ ADC	Simultaneous 50Hz to 60Hz Rejection 0.16ppm Noise
LTC2424/LTC2428	4-/8-Channel 20-Bit No Latency ΔΣ ADCs	8ppm INL, 1.2ppm Noise, Fast Mode