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High Efficiency, High Density, PolyPhase Converters for High Current Applications

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INTRODUCTION

As logic systems get larger and more complex, their supply current requirements continue to rise. Systems requiring 100A are fairly common. A high current power supply to meet such requirements usually requires paralleling several power regulators to alleviate the thermal stress on the individual power components. A power supply designer is left with the choice of how to drive these paralleled regulators: brute-force single-phase or smart PolyPhase™.

A PolyPhase converter interleaves the clock signals of the paralleled power stages, reducing input and output ripple current without increasing the switching frequency. The decreased power loss from the ESR of the input capacitor and the low switching losses associated with MOSFETs at relatively low switching frequencies help achieve high power conversion efficiency. The size and cost of the input capacitors are also greatly reduced as a result of input ripple current cancellation. Since output ripple current cancellation also occurs, lower value inductors can be used. This results in improved dynamic response to load transients. A combination of lower current rating and decreased inductance also allows the use of smaller-sized, low profile, surface mounted inductors. For multioutput applications, PolyPhase converters may also provide the benefit of smaller input capacitors.

Previously, the implementation of multiphase designs was difficult and expensive because of complex timing and current-sharing requirements. The newly developed LTC1629 solves these problems for high current, single output designs, while the LTC1628 addresses dual-output applications. Both ICs are dual, current mode, PolyPhase controllers that can drive two synchronous buck stages simultaneously. The features of the LTC1629 include a unity-gain differential amplifier for true remote sensing, low impedance gate drives, current-sharing, overvoltage protection, optional overcurrent latch-off and foldback current limit. Additionally, the LTC1629 can be configured for 2-, 3-, 4-, 6- and 12-phase operation with a simple phase selection signal (high, low or open). Optimizing the number of phases can help achieve the smallest and the most cost-effective power supply design.

This application note analyzes the performance of PolyPhase converters and provides guidelines for selecting the phase number and designing a PolyPhase converter using the LTC1629. The following questions will be answered as the discussion goes on:

- How much do I gain by using a PolyPhase architecture?
- How many phases do I need for my application?
- How do I design a PolyPhase converter?

HOW DO POLYPHASE TECHNIQUES EFFECT CIRCUIT PERFORMANCE?

In general, PolyPhase operation improves the large signal performance of a switched mode power converter, by such means as reducing ripple current and ripple voltage. A synchronous buck converter is used as an example in this application note to analyze the effects of PolyPhase techniques on circuit performance.

High current outputs usually require paralleling several regulators. The single-regulator approach is not feasible because of the unacceptable thermal stress on the individual power components. Paralleled regulators are synchronized to have the same switching frequency to eliminate beat frequency noise at both the input and output terminals. Based on the phase relationship between the paral-

leled regulators, these converters can be divided into two types: single-phase and PolyPhase. To balance the thermal stress in each component, paralleled regulators must also share the load current.

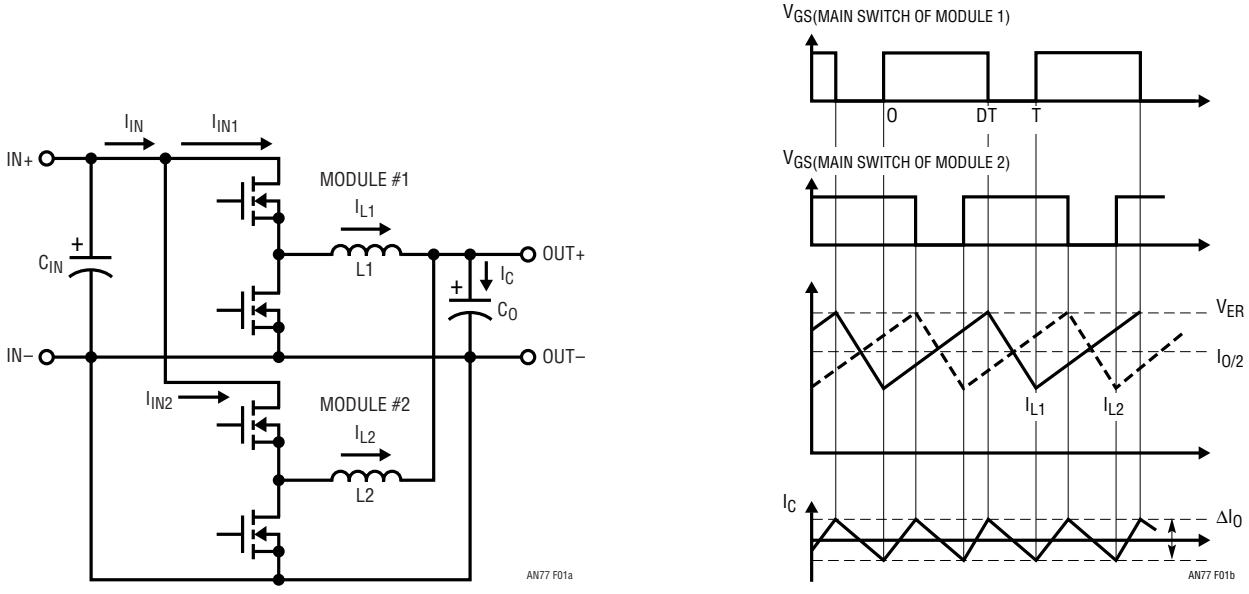
In this application note, the number of channels refers to the number of the paralleled regulators in one supply. The following symbols are defined to facilitate reference:

- V_O: DC output voltage
- I_O: DC output current
- V_{IN}: DC input voltage
- T: switching period
- mc: number of paralleled channels
- m: number of phases. The possible phase numbers are usually determined by the channel number, mc. For example, if mc = 6, the possible phase numbers are m = 1, 2, 3, 6.
- C_O: output capacitor
- ESR: equivalent series resistance of C_O
- L_f: output inductor
- D: duty cycle, approximated by V_O/V_{IN} in buck circuits

Current-Sharing

The current-sharing can be easily achieved by implementing peak current mode control. In a current mode control regulator, the load current is proportional to the error voltage in the voltage feedback loop. If the paralleled regulators see the same error voltage, they will source equal currents. A 2-channel circuit is used as the example to explain this current-sharing mechanism.

As shown in Figure 1, peak current mode control requires that the high side switch turn off when the peak inductor current (I_{L1}, I_{L2}) intersects the error voltage, V_{ER}, resulting in the same peak inductor currents. If the inductors are identical, the peak-to-peak ripple currents of the inductors will be the same. The DC currents of two inductors, which are the peak current less half of the peak-to-peak ripple current, will be equivalent. Two modules therefore share the load current equally. The same current-sharing mechanism can be extended to any number of channels in parallel. This current-sharing scheme will prevent an individual module from suffering excessive current stress in steady state operation and during line/load transient conditions. Note that the sharing mechanism is open loop, so no oscillations will occur due to current-sharing.



(a) (b)

Figure 1. 2-Channel Converter: (a) Schematic and (b) Typical Waveforms

Output Ripple Current Cancellation and Reduced Output Ripple Voltage

The phase relationship of Figure 1(b) shows how ripple current cancellation at the output works. Because of the 180 degree phase difference between the two converters, the two inductor ripple currents in the two-phase converter tend to cancel each other, resulting in a smaller ripple current flowing into the output capacitor. The frequency of the output ripple current is doubled as well. All of these factors contribute to a smaller output capacitor for the same ripple voltage requirement.

Figure 2 shows the measured waveforms of the inductor currents and output ripple currents in a 2-channel converter. The output ripple cancellation reduces the output ripple current from $14A_{P-P}$ (single-phase) to $6A_{P-P}$ (dual-phase). The ripple frequency in the dual-phase circuit is twice the switching frequency.

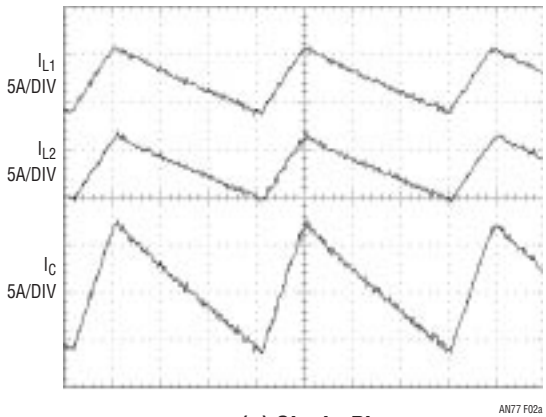
To quantify the output ripple current amplitude in an m-phase circuit, a closed-form expression was developed. The derivation starts with the 2-phase circuit shown in Figure 1. During the interval [from DT, T] when the high side switch in module 1 is off and the high side switch of module 2 is on, the inductor current in module 1 decreases and the inductor current in module 2 increases. The net ripple current flowing into the output capacitors is smaller. The output ripple current for the 2-phase circuit is derived as:

$$\Delta I_O = \frac{2V_O(1-D)T}{L_f}\,\frac{\left|1-2D\right|}{\left|1-2D\right|+1} \qquad (1)$$

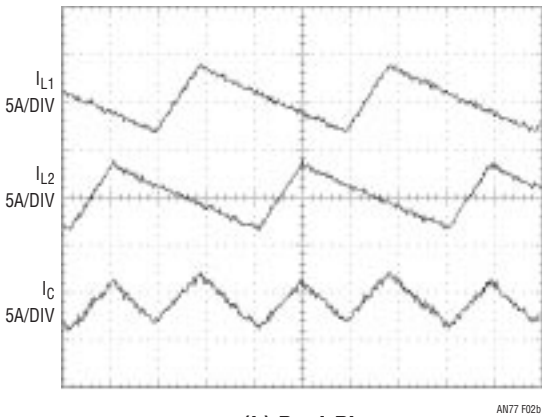
See Appendix A for the detailed derivation procedure. By extending the same derivation procedure to an *m*-phase configuration, the output ripple current for an *m*-phase circuit is obtained.

Output ripple current peak-to-peak amplitude in *m*-phase circuit:

$$\Delta I_O = \begin{cases} \dfrac{V_O T\left(1-D\right)}{L_f}, & m = 1 \\ \dfrac{mc \bullet V_O T}{L_f} \bullet \dfrac{\prod_{i=1}^{m}\left|\dfrac{i}{m}-D\right|}{\prod_{i=1}^{m-1}\left(\left|\dfrac{i}{m}-D\right|+\dfrac{1}{m}\right)}, & m = 2,3,\ldots \end{cases} \qquad (2)$$



(a) Single-Phase



(b) Dual-Phase

Figure 2. Output Ripple Current Waveforms In a 2-Channel Circuit. I_{L1} and I_{L2} Are the Inductor Currents In Two Channels and I_C Is the Net Ripple Current Flowing Into Output Capacitor. Test Conditions: V_{IN} = 12V, V_O = 2V, I_O = 20A

The output ripple voltage is estimated to be:

$$\Delta V_{O,PP} < \frac{\Delta I_O T}{8mC_O} + \Delta I_O \bullet ESR \qquad (3)$$

The first term in equation (3) represents the ripple voltage on the pure capacitive components of C_O and the second term represents the ripple voltage generated on the ESR of C_O. Intuitively, a higher phase number helps reduce the ripple component in the first term, and therefore, the overall ripple voltage amplitude at the output. Another interesting fact that can be observed is that the output ripple current and voltage will reach zero if the duty cycle is equal to one of the following critical points:

$$D_{crit} = \frac{i}{m}, \qquad i = 1,2,\ldots,m-1 \qquad (4)$$

In a buck converter, the duty cycle is the ratio of the output voltage and input voltage. By interpreting equation (4) in terms of V_{IN} and V_O, the zero output ripple conditions can be rewritten as:

$$\frac{V_O}{V_{IN}} = \frac{i}{m}, \qquad i = 1,2,\ldots,m-1 \qquad (5)$$

The plots in Figure 3 demonstrate the influence of phase number and duty cycle on the output ripple current. In this plot, the output ripple current is normalized against the inductor ripple current at zero duty cycle ($DIr = V_O T/L_f$). The following assumptions are made: the number of channels equals the phase number, the output voltage is fixed and the power conversion efficiency is assumed to be 100%. This plot can be used to estimate the output ripple current without tedious calculations.

The output ripple current approaches zero when the duty cycle is near the critical points for the selected phase number. For a buck circuit, the duty cycle is approximately the ratio of V_O/V_{IN}. Therefore, if the input and output voltages are relatively fixed, there exists an optimum phase number to minimize the output ripple voltage.

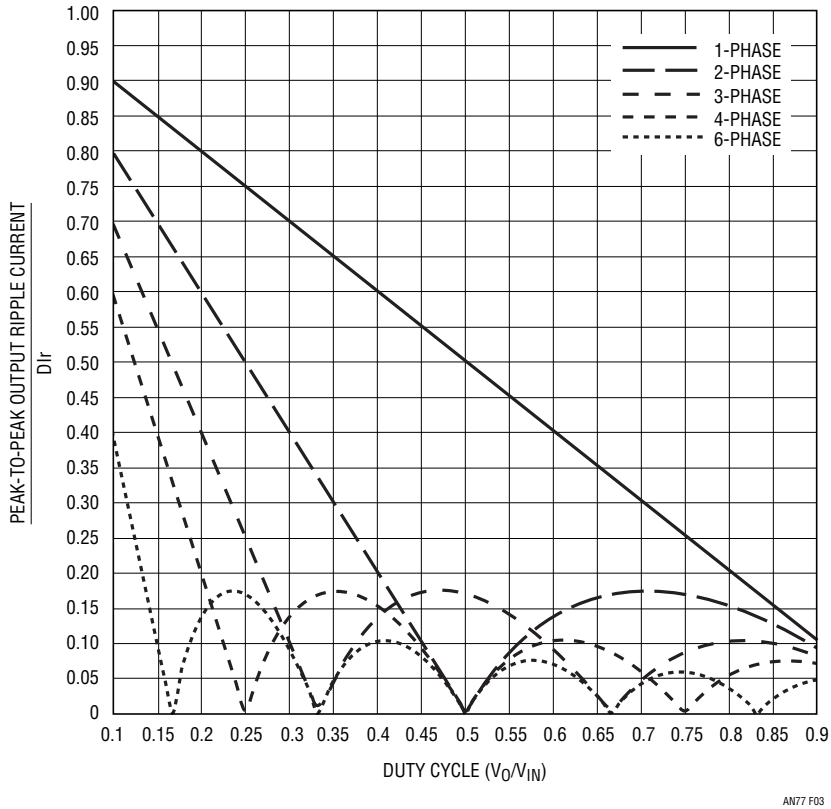


Figure 3. Normalized Output Ripple Current vs Duty Cycle, DIr = $\frac{V_O T}{L_f}$

Assuming that the maximum available phase number is six and the efficiency is 100%, the optimum phase numbers for some common input and output voltages are shown in Table 1.

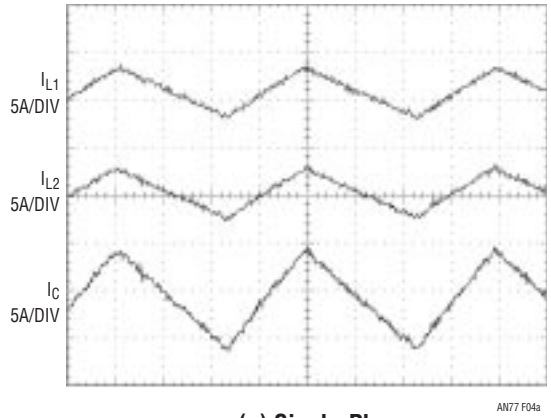
Table 1. Optimum Phase Number for Minimizing the Ripple Currents (Assuming That the Maximum Phase Number Is 6 and the Efficiency Is 100%)

	V_O = 1.2V	V_O = 1.5V	V_O = 2.0V	V_O = 2.5V
V_{IN} = 5V	4	6	5	2, 4, 6[1]
V_{IN} = 12V	6	6	6	5

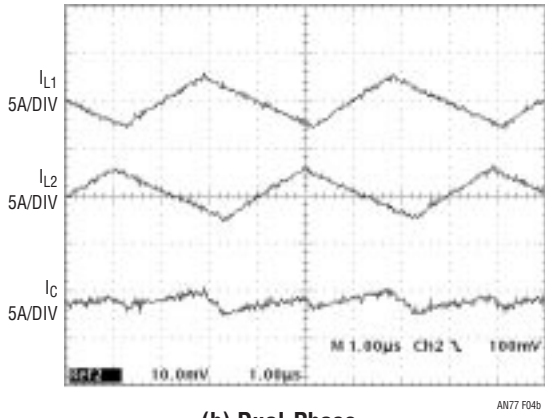
[1] 6 is the optimum phase number for minimum input ripple current.

For high step-down ratio or low duty cycle applications (for example, V_{IN} = 12V, V_O = 1.2V, D = 0.1), a high phase number helps reduce the maximum ripple current. For wide duty cycle range applications, high phase number tends to, but does not necessarily, yield lower output ripple current. The optimum phase number needs to be evaluated over the complete operating duty cycle range. The reduction in the ripple current by increasing phase number is not significant above four phases in most duty cycle ranges.

Figure 4 shows the measured output ripple current near the critical duty cycle point, which is D_{crit} = 0.5 for a 2-phase circuit. The test conditions were V_{IN} = 5V, V_O = 2V, I_O = 20A, f_S = 250kHz. Because of the voltage drop across the MOSFET switches, the operating duty cycle was very close to 50%. The dual-phase technique was able to reduce the output ripple current considerably, from $10A_{P-P}$ (in the single-phase circuit) to $2.5A_{P-P}$. As a result, the output ripple voltage near the critical duty cycle point is negligible, as shown in Figure 5.

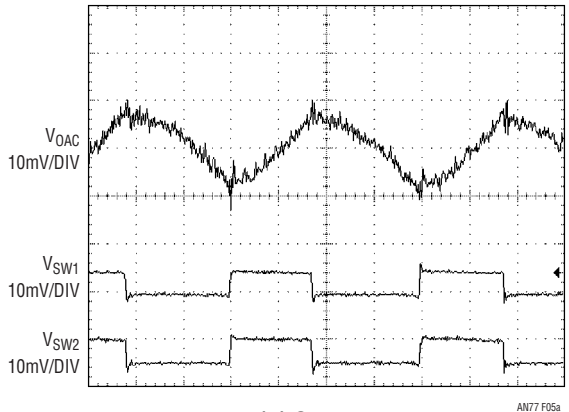


(a) Single-Phase

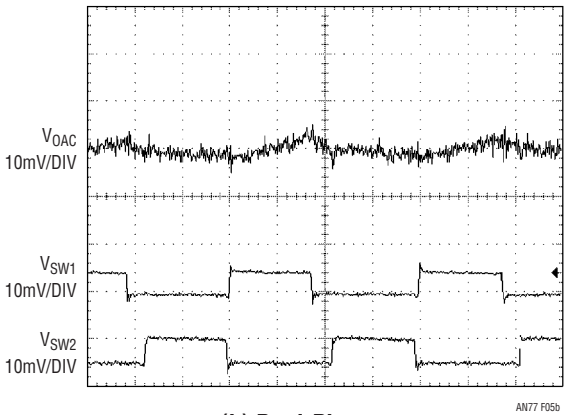


(b) Dual-Phase

Figure 4. Experimental Waveforms of Output Ripple Current Near Critical Duty Cycle Point (V_{IN} = 5V, V_O = 2V, I_O = 20A, f_S = 250kHz): Top Trace, Inductor 1 Current; Middle Trace, Inductor 2 Current; Bottom Trace, Output Ripple Current



(a) Single-Phase



(b) Dual-Phase

Figure 5 Measured Output Ripple Voltage (Top Trace) near Critical Duty Cycle Point (V_{IN} = 5V, V_O = 2V, I_O = 20A, f_S = 250kHz, V_{SW1} and V_{SW2} are the switch node voltages across the bottom FETs)

Improved Load Transient Response

The influences of PolyPhase techniques on the load transient performance are numerous. First, the reduced output ripple voltage allows more room for voltage variations during the load transient because the ripple voltage will consume a smaller portion of the total error budget. With the same number of capacitors on the output terminals of the power supply, the sum of the overshoot and undershoot can be reduced dramatically. Second, the reduced ripple current allows the use of lower value inductors. This speeds up the output current slew rate of the power supply. Consequently, PolyPhase helps improve the load transient performance of the power supply. Figure 6 shows the output voltages during a load transient. It is noted that the two circuits have the same electrical design. The dual-phase technique reduces the voltage variation from $69mV_{P-P}$ to $58mV_{P-P}$, a 16% reduction with no changes in component values. The inductor values could be reduced while still achieving lower output ripple voltage than the single-phase design, and further improvement in the peak-to-peak voltage variations for the load transient response could be realized.

Input Ripple Current Cancellation

The input current of a buck converter is discontinuous. With the input supply mainly sourcing DC current, the input capacitor supplies a pulsating current to the buck converter. In a single-phase circuit, the high side switches of the paralleled buck modules turn on simultaneously. The input capacitor needs to provide the sum of the pulsed currents. In a PolyPhase circuit, however, the paralleled buck stages switch at different times and the pulsating current flowing through the input capacitor is reduced dramatically.

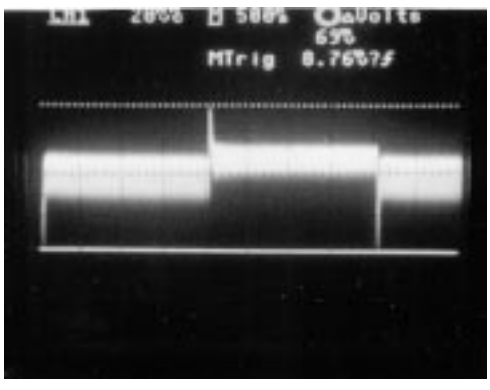
Figure 7 shows the measured input ripple current in a 2-channel converter. The PolyPhase converter reduces the peak amplitude of the input ripple current by half and doubles the ripple frequency. The reduced ripple current amplitude results in a much smaller RMS current in the input capacitor. Because the power loss on the ESR of the input capacitor is proportional to the square of the RMS current, the loss reduction can be significant. The size of the input capacitor is reduced and the life of the capacitor will likely be improved. The increased ripple frequency and the reduced ripple amplitude also facilitate EMI filtering.

In order to quantitatively evaluate the input ripple current in an m-phase circuit, a close-form expression is derived by using some mathematical manipulations on the input ripple current waveforms.

Input ripple current RMS value:

$$I_{irms} = \sqrt{\left(D-\frac{k}{m}\right)\left(\frac{k+1}{m}-D\right)I_0^2 + \frac{mc^2}{12mD^2}\left(\frac{V_0(1-D)T}{L_f}\right)^2 \bullet \sqrt{\left[(k+1)^2\left(D-\frac{k}{m}\right)^3 + k^2\left(\frac{k+1}{m}-D\right)^3\right]}} \quad (6)$$

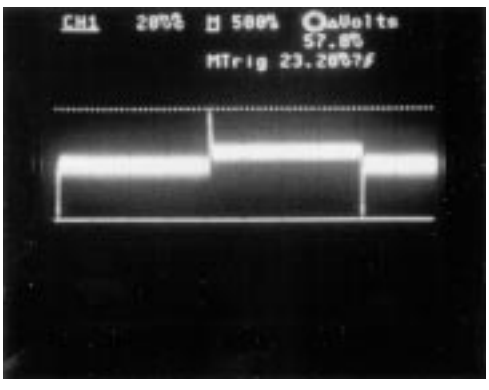
where k = FLOOR(m•D), m = 1, 2, …



V_{OAC} 20mV/DIV

AN77 F06a

(a) Single-Phase



V_{OAC} 20mV/DIV

AN77 F06b

(b) Dual-Phase

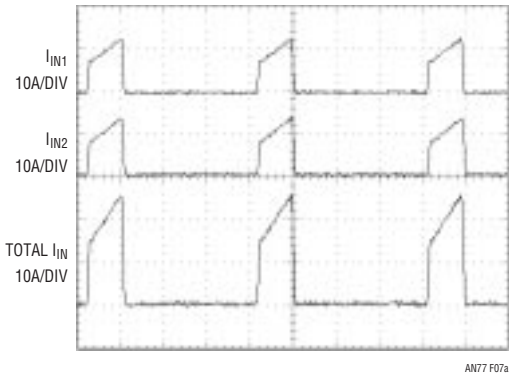
Figure 6. Measured Output Voltage During Load Transients (V_{IN} = 12V, V_O = 2V, f_s = 250kHz. Load steps: 5A to 20A and 20A to 5A, 50µs rise and fall times. Time scale: 500µs/DIV)

The variable k is determined by the phase number (m) and the duty cycle (D). For example, in a five-phase converter, at 45% duty cycle, k = FLOOR(5 • 0.45) = 2. The FLOOR(x) function provides a greatest integer that is smaller than or equal to x.

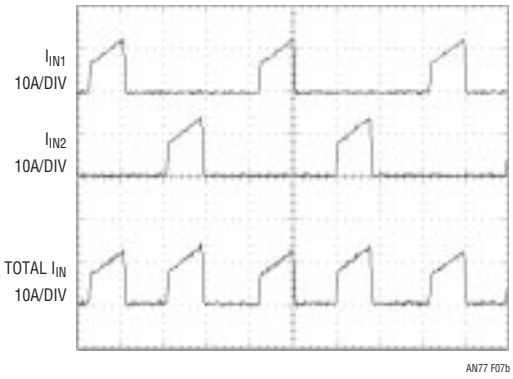
As indicated in equation (6), the input ripple current of a PolyPhase converter consists of two major factors: the DC load current (first term) and the inductor ripple current (second term). Since the inductor ripple current is almost unaffected by the load conditions, the maximum RMS input ripple current is reached at full load.

Usually, the size of the input capacitor is determined by the power dissipation on its ESR. The full load condition contributes to a maximum RMS input ripple current, and therefore, determines the size of the input capacitor.

Figure 8 plots the RMS input ripple current against the duty cycle for different phase configurations. In this plot, the RMS input ripple current is normalized against the DC load current. The output voltage is assumed fixed at 5V and the input voltage is varied, resulting in a duty cycle range from 0.1 to 0.9. Several facts can be observed from the curves.



(a) Single-Phase



(b) Dual-Phase

Figure 7 Measured Input Ripple Current: I_{in1} and I_{in2} are the ripple currents into the paralleled modules. Total I_{in} is the net ripple current into the input capacitor. (V_{IN} = 12V, V_O = 2V, I_O = 20A, f_s = 250kHz)

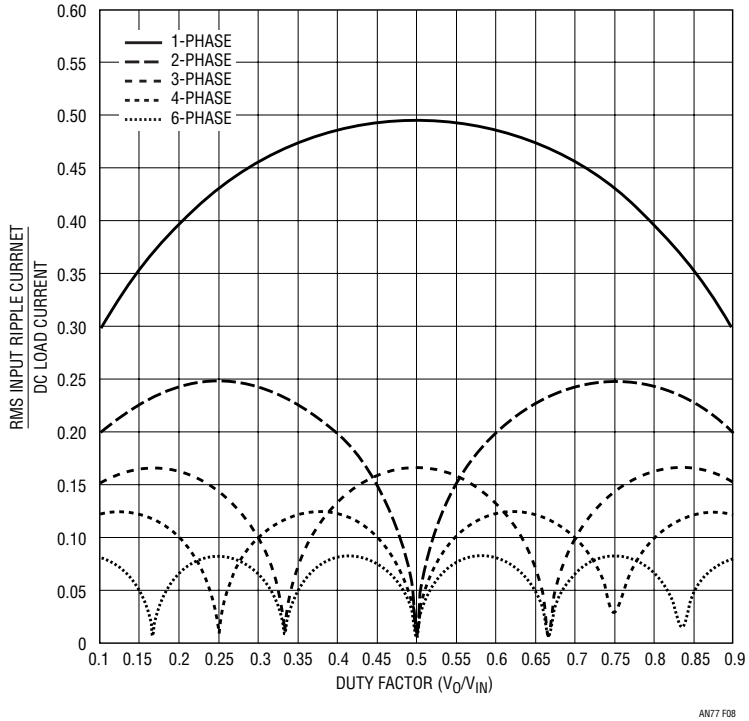


Figure 8. Normalized RMS Input Ripple Current

When the duty cycles are close to the critical duty cycle points (determined in equation (4)), the first term in equation (6) is zero. The RMS input ripple current reaches the local minimum values. These values are not zero due to the output inductor ripple current. Consequently, there exists an optimum phase number to achieve the minimum RMS input ripple current for a fixed input and output application. For some common input and output voltages, the optimum phase numbers for minimizing the input ripple current are shown in Table 1. Note that these are the same as the values for the minimum output ripple voltage. For a wide duty cycle range application, higher phase number helps reduce the maximum input ripple current. But the reduction in the input ripple current by increasing phase number may not be significant at higher phase numbers in certain duty cycle ranges. The optimum phase number needs to be evaluated over the complete operating duty cycle range.

Figure 9 shows the experimental waveform of the input ripple currents in a 2-channel circuit. The circuit operated at close to 50% duty cycle, which is the critical duty cycle point for the two-phase circuit. Compared to the single-phase technique, the PolyPhase technique reduced the ripple current in the input capacitor dramatically.

DESIGN CONSIDERATIONS

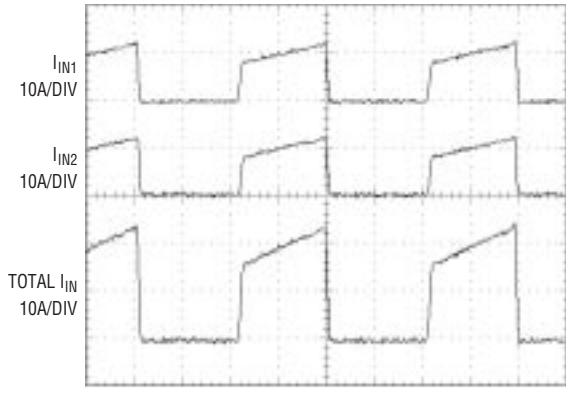
Similar to the design of conventional paralleled regulators, the design of a PolyPhase converter involves the choice of the number of paralleled channels and the selection of the power components (MOSFETs, inductors, capacitors, etc.).

Usually, the number of phases is set to be equal to the number of channels. However, the number of channels and the number of phases may be different. The number of channels is usually determined by the total load current and the acceptable current stress in each channel. For example, if the required load current is 60A and the maximum current stress per channel is 15A, 4 channels need to be paralleled. The number of phases, on the other hand, can be selected to minimize the input and output filter capacitors. Note that each phase must have an equal number of channels. In this example, a 4-channel configuration, one, two or four phases may be used.

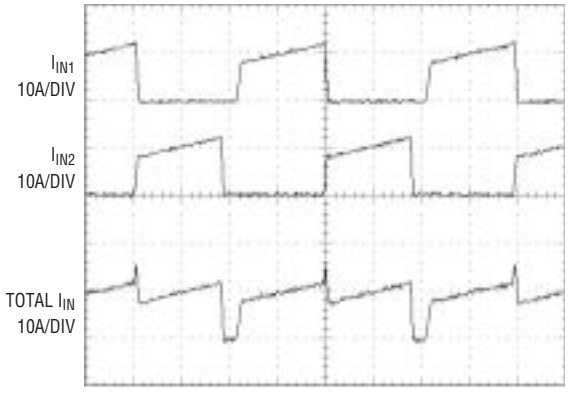
Selection of phase number

As discussed in the previous section, the selection of a different number of phases will greatly affect the input and output ripple current.

For a narrow input and output range, the duty cycle range is relatively narrow. The optimum phase number should be chosen such that the circuit operates at or near one of the critical duty cycle points (determined by equation 4). For some practical input voltages and output voltages, the optimum phase numbers for the minimum input ripple currents and the lowest output ripple voltage are listed in Table 1. For wide input or output voltage range, the phase number should be chosen such that the worst-case RMS input ripple current and the worst-case output ripple voltage are minimized for the complete operating duty cycle range.



(a) Single-Phase



(b) Dual-Phase

Figure 9. Input Current Near Critical Duty Cycle In a 2-Channel (V_{IN} = 5V, V_O = 2V, I_O = 20A, f_s = 250kHz)

PolyPhase Converters using the LTC1629

The LTC1629 integrates proprietary phase-locked-loop-based phasing circuitry. Each IC can be synchronized to an external signal at the PLLIN pin and produce a CLKOUT signal to synchronize other ICs. Table 2 shows the phase function table of the LTC1629. By applying the command signal ($INTV_{CC}$, open or SGND) to the PHASMD pin and connecting the CLKOUT pin of one IC to the PLLIN pin of the next one, different numbers of phases can be achieved. Figure 11 shows 2-phase, 3-phase, 4-phase, 6-phase and 12-phase configurations using the LTC1629.

A higher number of phases is usually needed for very high output current or multioutput applications. For example, in a 2-output system, 3.3V/90A and 5V/60A, if each output is provided by a 6-phase power supply, the two power supplies can be interleaved by using a 12-phase configuration. As shown in Figure 12, U1, U2 and U3 are used to produce the 3.3V output, and U4, U5, and U6 are used for the 5V output. The resulting input ripple current frequency is twelve times the switching frequency and the ripple current amplitude is reduced.

Table 2. Phase Function Table for LTC1629

PHASMD	0V	OPEN	$INTV_{CC}$
PLLIN	0°	0°	0°
CONTROLLER 1	0°	0°	0°
CONTROLLER 2	180°	180°	240°
CLKOUT	60°	90°	120°

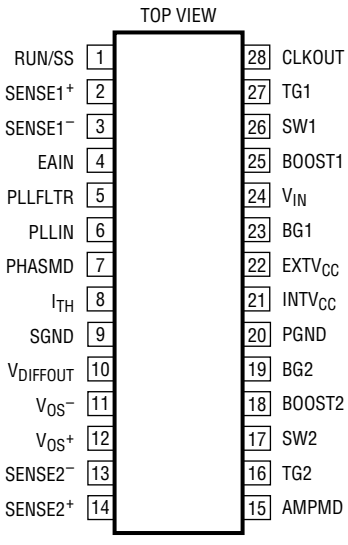


Figure 10. Pinouts of LTC1629

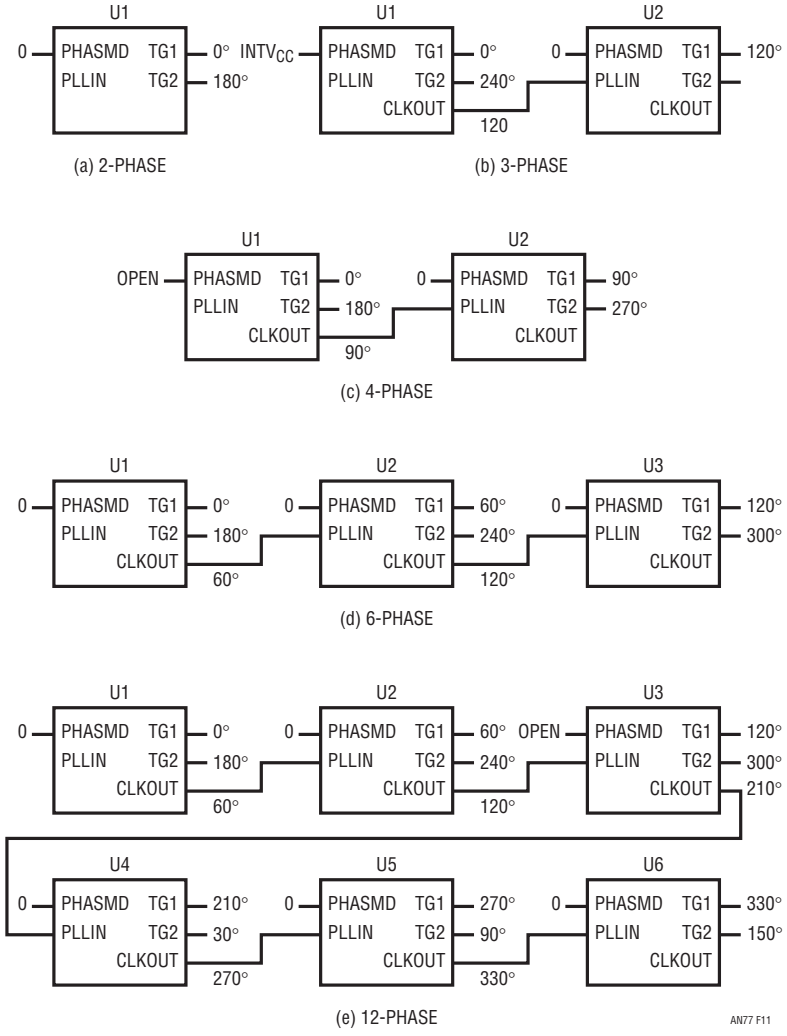


Figure 11. Configuration of Different Phases Using the LTC1629

The LTC1629 includes a unity gain differential amplifier, enabling true remote sensing of the output voltage. This is particularly useful for maintaining tight output voltage regulation for high current applications. Each LTC1629 based regulator consists of two synchronous buck stages and two or more power regulators can be paralleled directly. The inherent peak current mode control permits automatic current-sharing. When several LTC1629-based regulators are in parallel, the LTC1629 of the master regulator senses the output voltage (V_O+, V_O–) via its on-chip differential amplifier and divides this voltage ($V_{DIFFOUT}$) down through the resistor divider to utilize the built-in 0.8V reference for output voltage regulation. This control voltage is then fed to the EAIN pins (error amplifier input) of each LTC1629. Since the error amplifier inside the LTC1629 is a g_m transconductance amplifier, directly paralleling the I_{TH} pins (error amplifier outputs) and the EAIN pins is allowed. The paralleled regulators now share the same error voltage. Because the load current of a current mode regulator is proportional to the error voltage, the paralleled regulators must source equal currents.

Layout Considerations

To take full advantage of the ripple cancellation of the PolyPhase technique, the input capacitors and output capacitors are ideally placed at the summation points of all the input ripple currents and all the output ripple currents, respectively. Figure 13 shows the layout for a 2-phase converter. In practice, the filter capacitors may be placed across the individual modules' inputs and outputs (such as A1B1, A2B2, etc.). The traces (AA1, AA2, BB1, BB2, etc.) between modules should be the shortest and widest possible to balance the current stress in each capacitor. The impedance of the traces highlighted in Figure 13 should be minimized. It is preferable that these traces be large copper planes. It is also important that the sources of bottom MOSFETs (B1, B2, etc.) be connected to the input filter capacitors before joining the ground plane (CD). Otherwise, the ground noise generated by the pulsating current through the trace inductance will be seen on the output terminals as spikes.

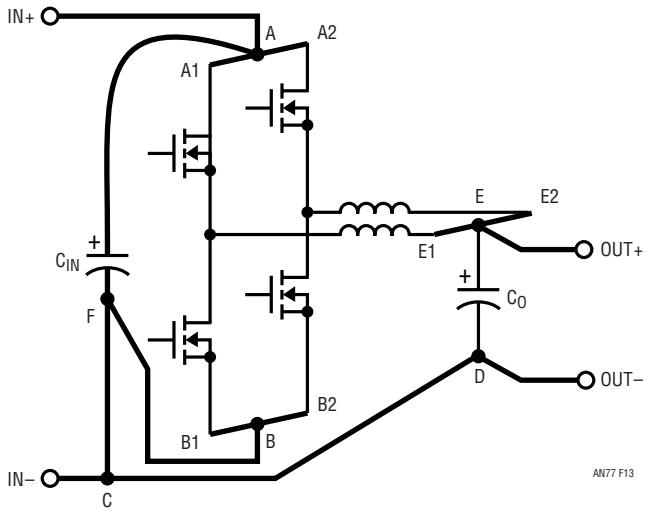


Figure 13. Layout Diagram of Power Stage for 2-Phase Converter

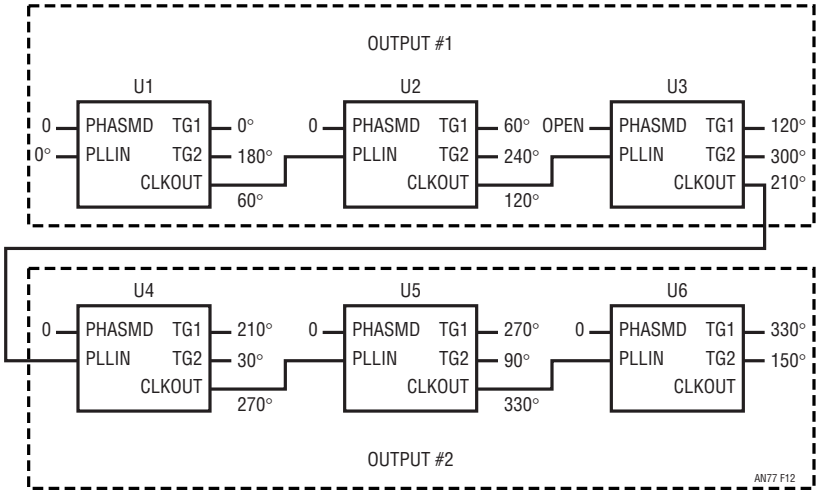


Figure 12. 2-Output System Using 12-Phase Configuration

DESIGN EXAMPLE: 100A POLYPHASE POWER SUPPLY

The specifications for a high current PolyPhase power supply are as follows:

- Input: 12V (±10%)
- Outputs: 3.3V at 90A nominal, 100A maximum
- Load regulation: <20mV from 0A to full load
- Switching Noise: peak-to-peak voltage <1% of DC voltage
- Efficiency:
- >89% at V_{IN} = 12V, V_O = 3.3V, I_O = 90A;

Design Details

To utilize off-the-shelf, surface mount inductors and to avoid the use of very thick PCB copper traces, it is desirable to limit the individual module current to about 16A. Six channels are needed for this application. The design now becomes only a 15A regulator which gets repeated six times.

MOSFETs

The selection of MOSFETs is determined by the current requirement and switching frequency. Low $R_{DS(ON)}$ MOSFETs usually drive down the conduction losses but tend to introduce high switching related losses at high switching frequencies because of the large gate charge and parasitic capacitances. For a given current requirement and selected switching frequency, both $R_{DS(ON)}$ and gate charge (Q_g) should be evaluated to minimize the sum of the conduction losses, driving losses and the switching loss. For the specified application, a number of MOSFETs can be good choices: Si4420 (Siliconix), FDS6670A (Fairchild), FDS7760A (Fairchild) and IRF7811 or IRF7805 (International Rectifier). In this application, we need two MOSFETs for each high side switch and three MOSFETs for each low side switch. The power dissipation in the MOSFETs includes the conduction loss, switching loss and reverse recovery loss of the body diodes in the low side MOSFETs. The gate driving loss is seen by the controller IC. In this design, if Si4420s are used, each top MOSFET dissipates about 0.5W and each low side MOSFET consumes about 0.9W. Based on the thermal resistance provided in the datasheet, 30°C/W junction-to-ambient, the maximum junction temperature of the MOSFETs is about 30°C above the ambient temperature. Refer to the LTC1629 data sheet and the literature from the MOSFET vendors for more information on estimating the power loss of MOSFETs.

Inductors

The selection of inductors is driven by the load current amplitude and the switching frequency. The LTC1629 senses the inductor current with a current sense resistor. The inductor ripple current must be large enough to produce a reasonable AC sense voltage on the small value sense resistor required for a high current application. A reasonable starting point is to choose an inductor such that its ripple current amplitude is about 40% of the maximum channel current. It is estimated that an inductor value between 1.0µH and 1.6µH will be suitable for 3.3V output at a frequency of 200kHz. A number of off-the-shelf, surface mount inductors are available for the specified application: P1608 (Pulse), PE53691 (Pulse), ETQP6F1R3L (Panasonic) and CEPH149-1R6MC (Sumida). Any inductor of similar inductance value and current capability should work correctly.

The maximum available phase number is six and the possible phase number options are 1, 2, 3 and 6. By using equations (1~6), the ripple currents at the input and output for different-phase configuration are estimated as in Table 3.

A six-phase configuration minimizes both the input capacitor size and output ripple voltage. Compared to the single-phase technique, the six-phase technique reduces the input ripple current by more than 81%, and the output ripple by more than 96%. Therefore, the six-phase configuration was adopted for this design.

Capacitors

The selection of the input capacitors is driven by the RMS value of the input ripple current. Large capacitor ripple currents introduce high power losses due to the ESR of the capacitor. The resulting internal heating tends to reduce the capacitor life. Low ESR capacitors must be used. This design uses Sanyo OS-CON capacitors (16SA150M 150µF/16V) whose maximum allowable ripple current is rated at about $3.26A_{RMS}$. The input RMS ripple current for the six-phase configuration is estimated to be about $8.5A_{RMS}$. Therefore, a minimum of three OS-CON capacitors are needed. If a conventional single-phase technique were used instead, the input RMS ripple current would be about $46.8A_{RMS}$. A minimum of fifteen OS-CON capacitors would then be needed. Therefore, the use of an LTC1629 based PolyPhase design saves at least twelve (15 – 3 = 12) OS-CON capacitors.

The output capacitors are KEMET (T510X477M006AS 470µF/6.3V), ultralow ESR (30mohm), surface mount tantulum capacitors. The peak-to-peak ripple current is estimated to be $2.1A_{P-P}$. It would be $57.1A_{P-P}$ if a conventional single-phase approach were taken instead.

Test results

The complete schematic diagram is shown in Figure 14. The power supply consists of six buck channels and three LTC1629s. Figure 15 shows the measured waveforms of gate voltages and switch-node voltages in a typical six-phase converter. The gate voltages and switch-node voltages of six buck stages are interleaved 60 degrees output of phase. Since the inductor current is driven by the difference between the switch-node voltage and the DC output voltage, the ripple currents in the six inductors are also 60 degrees out of phase. As a result, the amplitude of the net ripple current flowing into the output capacitor decreases substantially and the ripple frequency increases to six times the switching frequency. The output switching noise and the power loss from the ESR are greatly attenuated.

Figure 16 shows the output voltage, which was measured at the output capacitor (C14 in the schematics). The output ripple voltage is less than $10mV_{P-P}$ at 90A output current and the ripple frequency is six times the switching frequency.

Efficiency was measured under different loading conditions. Figure 17 shows the efficiency curve. For most of the load range, the efficiency was about 90%. At 100A, the efficiency was measured 89.4%.

Table 3. Input and Output Ripple Current for Different Phase Configurations

Channels	6	6	6	6
Phases	1	2	3	6
Input Ripple Current (A_{RMS})	46.8	25.7	15.2	8.5
Output Ripple Current (A_{P-P})	57.1	19.0	6.3	2.1

Assuming that the efficiency is 100%, the inductance is 1.3µH, frequency is 200kHz

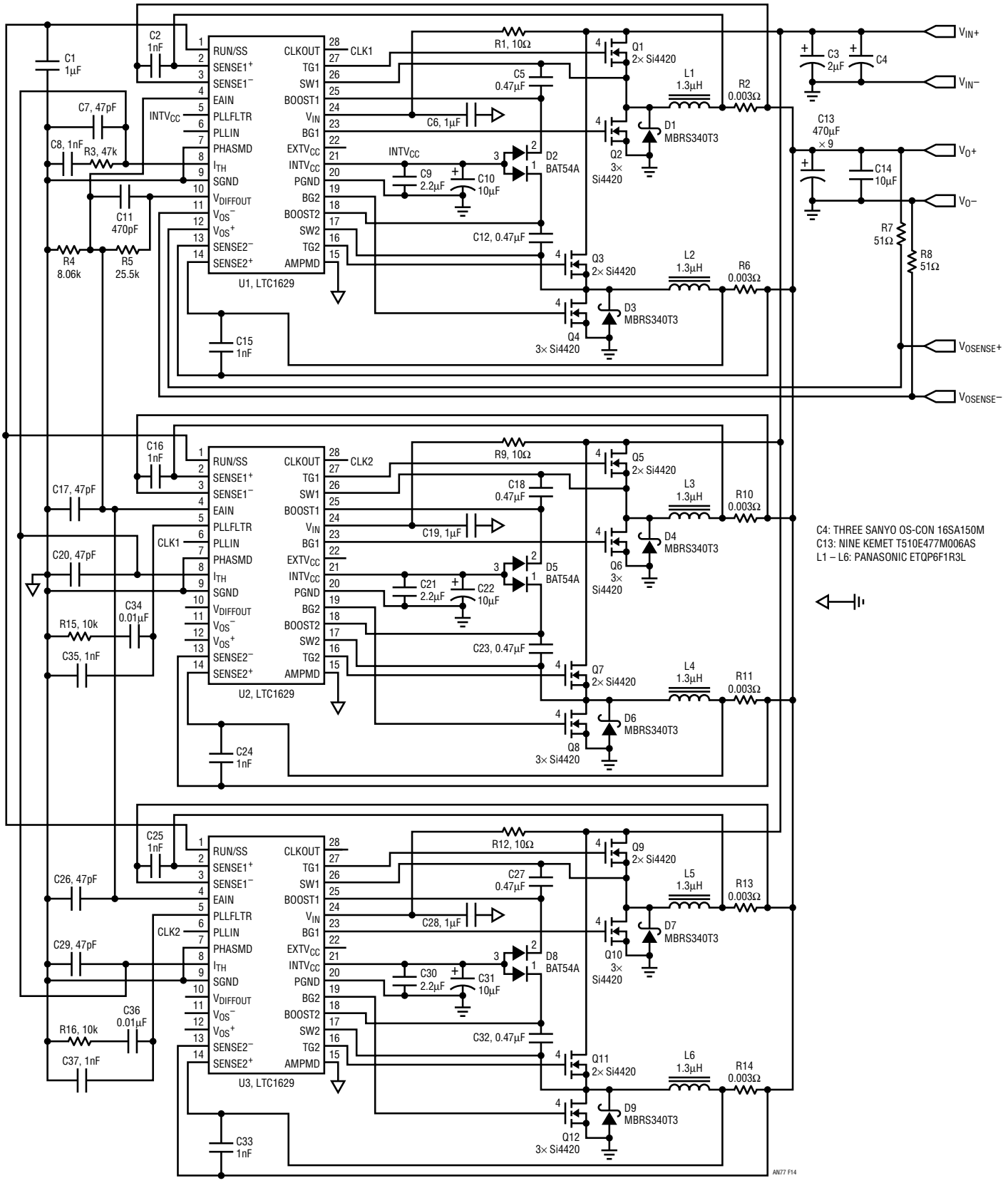
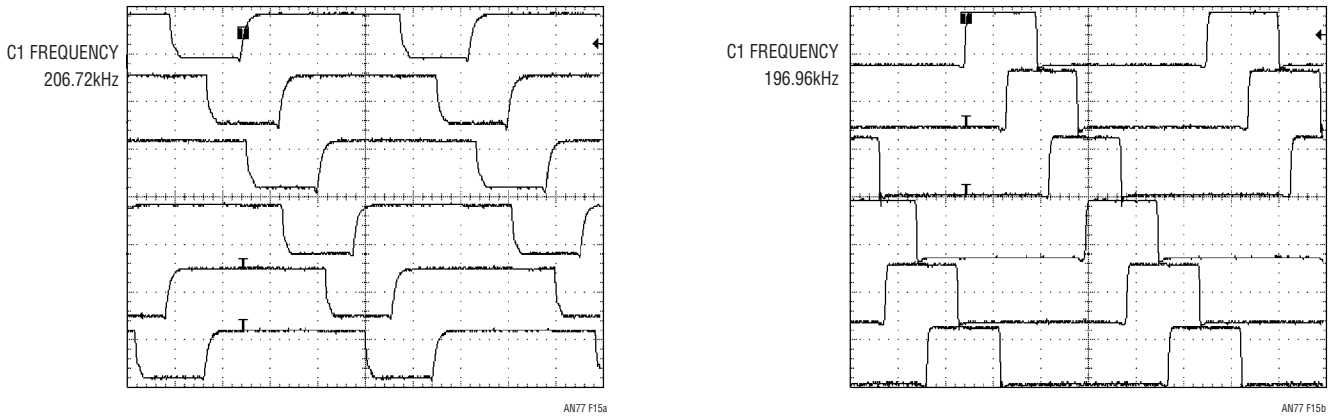


Figure 14. Schematic Diagram of 3.3V/100A Six-Phase Converter



(a) Voltage Scale: 5V/DIV, Time Scale: 1μs/DIV **(b) Voltage Scale: 10V/DIV, Time Scale: 1μs/DIV**

Figure 15. Typical Waveforms of 6-phase Converter: (a) Gate Voltages, (b) Switch-Node Voltages (Drain-to-Source Voltage of the Synchronous Switch)

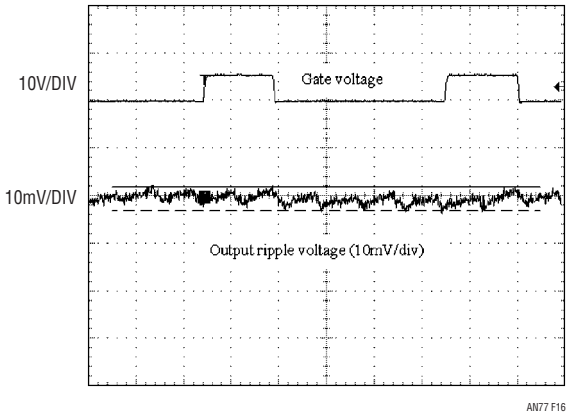


Figure 16. Output Ripple Voltage Waveforms (Time Scale: 1us/DIV): V_{IN} = 12V, V_O = 3.3V, I_O = 90A

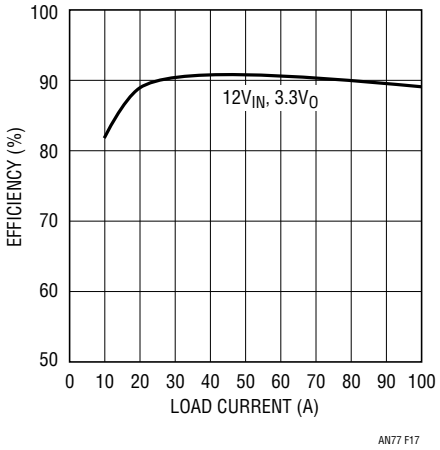


Figure 17. Measured Efficiency at Different Load

SUMMARY

PolyPhase converters reduce the input and output ripple currents by interleaving the clock signals of paralleled power stages. With a proper choice of phase number, the output ripple voltage and the input capacitor size can be minimized without increasing the switching frequency. Lower output ripple voltage and smaller output inductors help improve the circuit's dynamic performance during load transients. The low switching losses and driving losses of MOSFETs at relatively low switching frequency, and the reduced power losses due to ESRs of the capacitors, help achieve high efficiency.

The LTC1629 dual, PolyPhase current mode controller is able to achieve the benefits of the PolyPhase technique without complicating the control circuit. The LTC1629 helps minimize the external component count and simplify the complete power supply design by integrating two PWM current mode controllers, true remote sensing, selectable phasing control, current-sharing capability, high current MOSFET drivers and protection features (such as overvoltage protection, optional overcurrent latch-off and foldback current limit) into one IC. The resulting manufacturing simplicity helps improve power supply reliability. The high current MOSFET drivers allow the use of low $R_{DS(ON)}$ MOSFETs to minimize the conduction losses for high current applications. Lower current ratings on the individual inductors and MOSFETs also make it possible to use low profile, surface mount components. Therefore, an LTC1629-based PolyPhase high current converter can achieve high efficiency, small size and low profile simultaneously. The savings on the input and output capacitors, inductors and heat sinks minimize the overall cost and size of the complete power supply.

APPENDIX A

DERIVATION OF OUTPUT RIPPLE CURRENT IN A 2-PHASE CIRCUIT

During the interval from DT to T as shown in Figure 1, the high side switch in module 1 is off and the high side switch of module 2 is on. The inductor current in module 1 decreases and the inductor current in module 2 increases. The variations of these inductors are estimated to be:

$$\Delta I_{L1} = \frac{-V_O(1-D)T}{L_f} \quad (A1)$$

$$\Delta I_{L2} = \frac{(V_{IN}-V_O)(1-D)T}{L_f} \quad (A2)$$

where $$D = \frac{V_O}{V_{IN}} \quad (A3)$$

The net output ripple current is the sum of these inductor ripple currents:

$$\Delta I_O = \left|\Delta I_{L1} + \Delta I_{L2}\right| = \frac{V_O(1-D)T}{L_f}\frac{\left|1-2D\right|}{D} \quad (A4)$$

Equation (A4) is derived based on the waveform shown in Figure 1, where D is greater than 0.5. When D is smaller than 0.5, one can easily derive the output ripple current as:

$$\Delta I_O = \left|\Delta I_{L1} + \Delta I_{L2}\right| = \frac{V_O(1-D)T}{L_f}\frac{\left|1-2D\right|}{1-D} \quad (A5)$$

By combining equations (A4) and (A5), we can derive the output ripple current for the 2-phase configuration as:

$$\Delta I_O = \left|\Delta I_{L1} + \Delta I_{L2}\right| = \frac{2V_O(1-D)T}{L_f}\frac{\left|1-2D\right|}{\left|1-2D\right|+1} \quad (A6)$$