LTC1274/LTC1277

12-Bit, 10mW, 100ksps ADCs with 1µA Shutdown

FEATURES

- **Low Power Dissipation: 10mW**
- **Sample Rate: 100ksps**
- Samples Inputs Beyond Nyquist, 72dB S/(N + D) and 82dB THD at f_{IN} = 100kHz
- Single Supply 5V or ±5V Operation
- **Power Shutdown to 1µA in Sleep Mode**
- 180µA Nap Mode (LTC1277) with Instant Wake-Up
- Internal Reference Can Be Overdriven
- Internal Synchronized Clock
- 0V to 4.096V or ±2.048V Input Ranges (1mV/LSB)
- 24-Lead SO Package

APPLICATIONS

- Battery-Powered Portable Systems
- High Speed Data Acquisition for PCs
- Digital Signal Processing
- Multiplexed Data Acquisition Systems
- Audio and Telecom Processing
- Spectrum Analysis

DESCRIPTION

The LTC®1274/LTC1277 are 8µs sampling 12-bit A/D converters which draw only 2mA (typ) from single 5V or ±5V supplies. These easy-to-use devices come complete with a 2µs sample-and-hold, a precision reference and an internally trimmed clock. Unipolar and bipolar conversion modes add to the flexibility of the ADCs.

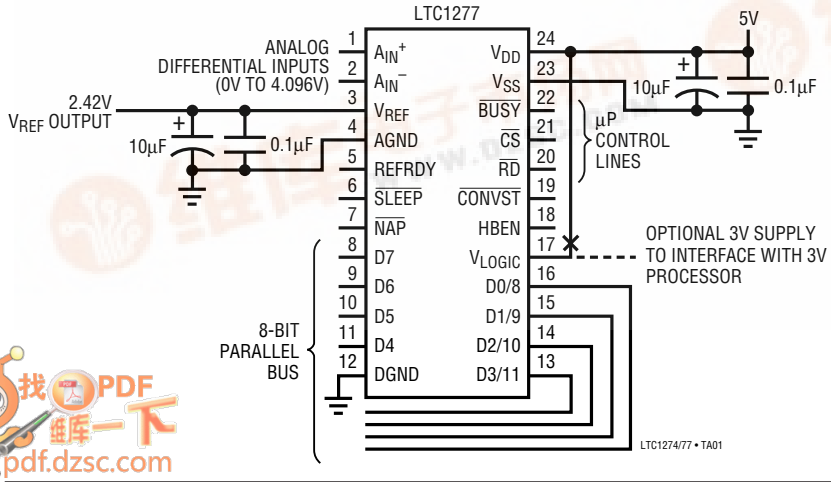
Two power-down modes are available in the LTC1277. In Nap mode, the LTC1277 draws only 180µA and the instant wake-up from Nap mode allows the LTC1277 to be powered down even during brief inactive periods. In Sleep mode only 1µA will be drawn. A REFRDY signal is used to show the ADC is ready to sample after waking up from Sleep mode. The LTC1274 also provides the Sleep mode and REFRDY signal.

The A/D converters convert 0V to 4.096V unipolar inputs from a single 5V supply or ±2.048V bipolar inputs from ±5V supplies.

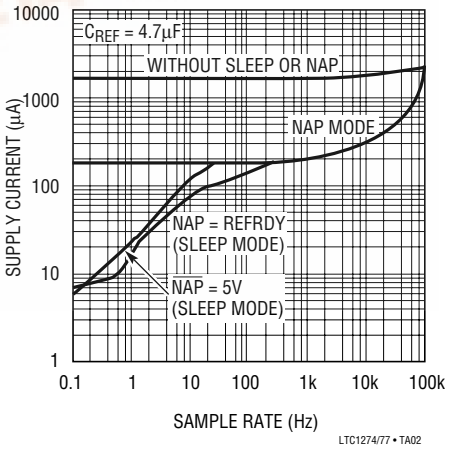
The LTC1274 has a single-ended input and a 12-bit parallel data format. The LTC1277 offers a differential input and a 2-byte read format. The bipolar mode is formatted as 2's complement for the LTC1274 and offset binary for the LTC1277.

TYPICAL APPLICATION

Single 5V Supply, 10mW, 100kHz, 12-Bit ADC



Supply Current vs Sample Rate with Sleep and Nap Modes



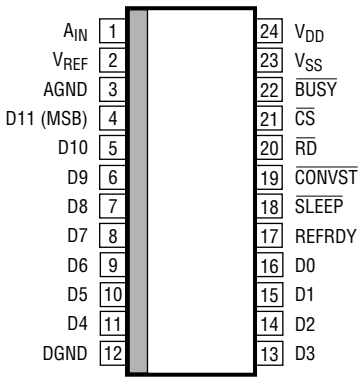
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{DD}) 7V
Negative Supply Voltage (V_{SS})
  Bipolar Operation Only ..... –6V to GND
Total Supply Voltage (V_{DD} to V_{SS})
  Bipolar Operation Only 12V
Analog Input Voltage (Note 3)
  Unipolar Operation ..... – 0.3V to V_{DD} + 0.3V
  Bipolar Operation..... V_{SS} – 0.3V to V_{DD} + 0.3V
Digital Input Voltage (Note 4)
  Unipolar Operation ..... – 0.3V to 12V
  Bipolar Operation..... V_{SS} – 0.3V to 12V
Digital Output Voltage
  Unipolar Operation ..... –0.3V to V_{DD} + 0.3V
  Bipolar Operation..... –0.3V to V_{DD} + 0.3V
Power Dissipation..... 500mW
Operating Temperature Range
  Commercial ..... 0°C to 70°C
  Industrial ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW

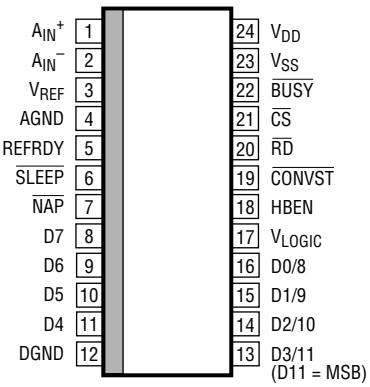


SW PACKAGE
24-LEAD PLASTIC SO WIDE

T_{JMAX} = 110°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC1274CSW
LTC1274ISW

TOP VIEW



SW PACKAGE
24-LEAD PLASTIC SO WIDE

T_{JMAX} = 110°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC1277CSW
LTC1277ISW

Consult factory for Military grade parts.

CONVERTER CHARACTERISTICS

With Internal Reference (Notes 5, 6)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			Bits
Integral Linearity Error	(Note 7)	●			±1	LSB
Differential Linearity Error		●			±1	LSB
Unipolar Offset Error		 ●			±6 ±8	LSB LSB
Bipolar Offset Error	(Note 8)	 ●			±8 ±10	LSB LSB
Gain Error					±20	LSB
Gain Error Tempco	$I_{OUT(REF)}$ = 0	●		±10	±45	ppm/°C

ANALOG INPUT (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 10)	4.75V ≤ V_{DD} ≤ 5.25V (Unipolar) 4.75V ≤ V_{DD} ≤ 5.25V, −5.25V ≤ V_{SS} ≤ −2.45V (Bipolar)	● ●		0 to 4.096 ±2.048		V V
I_{IN}	Analog Input Leakage Current	$\overline{CS}$ = High	●			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions (Sample Mode) During Conversions (Hold Mode)			45 5		pF pF

DYNAMIC ACCURACY (Notes 5, 9)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	50kHz Input Signal 100kHz Input Signal	 ●	 70	73 72.5		dB dB
THD	Total Harmonic Distortion Up to 5th Harmonic	50kHz Input Signal 100kHz Input Signal	 ●		−84 −82	 −76	dB dB
	Peak Harmonic or Spurious Noise	50kHz Input Signal 100kHz Input Signal	 ●		−84 −82	 −76	dB dB
IMD	Intermodulation Distortion	fa = 96.95kHz, fb = 97.68kHz 2nd Order Terms 3rd Order Terms			−78 −81		dB dB
	Full Power Bandwidth				2		MHz
	Full Linear Bandwidth [S/(N + D) ≥ 68dB]				350		kHz

INTERNAL REFERENCE CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0		2.400	2.420	2.440	V
V_{REF} Output Tempco	I_{OUT} = 0	●		±10	±45	ppm/°C
V_{REF} Line Regulation	4.75V ≤ V_{DD} ≤ 5.25V −5.25V ≤ V_{SS} ≤ −4.75V			0.01 0.01		LSB/V LSB/V
V_{REF} Load Regulation	−5mA ≤ I_{OUT} ≤ 70µA			2		LSB/mA

DIGITAL INPUTS AND DIGITAL OUTPUTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.75V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage, All Logic Outputs	V_{DD} = 4.75V I_O = −10µA I_O = −200µA	 ●	 4.0	 4.70 	 	 V V
		V_{LOGIC} = 2.7V (LTC1277) I_O = −10µA I_O = −200µA			 2.65 2.60		 V V
V_{OL}	Low Level Output Voltage, All Logic Outputs	V_{DD} = 4.75V I_O = 160µA I_O = 1.6mA	 ●		 0.05 0.10	 0.4	 V V
		V_{LOGIC} =2.7V (LTC1277) I_O = 160µA I_O = 1.6mA			 0.05 0.10		 V V

DIGITAL INPUTS AND DIGITAL OUTPUTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{OZ}	High-Z Output Leakage D11 to D0/8	V_{OUT} = 0V to V_{DD}, $\overline{CS}$ High	●			±10	µA
C_{OZ}	High-Z Output Capacitance D11 to D0/8	$\overline{CS}$ High (Note 10)	●			15	pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}			10		mA

POWER REQUIREMENTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage (Notes 11, 12)	Unipolar and Bipolar Mode		4.75		5.25	V
V_{LOGIC}	Logic Supply (Notes 11,12)	Unipolar and Bipolar Mode (LTC1277)			2.7 to 5.25		V
V_{SS}	Negative Supply Voltage (Note 11)	Bipolar Mode Only		–2.45		–5.25	V
I_{DD}	Positive Supply Current	f_{SAMPLE} = 100ksps	●		2	4	mA
		$\overline{NAP}$ = 0V (LTC1277 Only)	●		180	320	µA
		$\overline{SLEEP}$ = 0V	●		0.3	5	µA
I_{SS}	Negative Supply Current	f_{SAMPLE} = 100ksps, Bipolar Mode Only	●		40	70	µA
		$\overline{SLEEP}$ = 0V	●		0.3	5	µA
P_{DISS}	Power Dissipation	f_{SAMPLE} = 100ksps	●		10	20	mW
		$\overline{NAP}$ = 0V (LTC1277 Only)	●		0.9	1.8	mW
		$\overline{SLEEP}$ = 0V (Unipolar/Bipolar)	●			25/50	µW

TIMING CHARACTERISTICS (Note 5) See Figures 13 to 17.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency	(Note 11)	●	100			ksps
t_{CONV}	Conversion Time		●		6	8	µs
t_{ACQ}	Acquisition Time		●		0.35	2	µs
t_1	$\overline{CS}$↓ to $\overline{RD}$↓ Setup Time	(Note 10)	●	0			ns
t_2	$\overline{CS}$↓ to $\overline{CONVST}$↓ Setup Time	(Note 10)	●	30			ns
t_3	$\overline{NAP}$↑ to $\overline{CONVST}$↓ Wake-Up Time	(LTC1277 Only) (Note 11)			620		ns
t_4	$\overline{CONVST}$ Low Time	(Note 13)	●	40			ns
t_5	$\overline{CONVST}$↓ to $\overline{BUSY}$↓ Delay	C_L = 100pF	●		70	150	ns
t_6	Data Ready Before $\overline{BUSY}$↑	C_L = 100pF	●	20	65		ns
t_7	Delay Between Conversions	(Note 11)	●		0.35	2	µs
t_8	Wait Time $\overline{RD}$↓ After $\overline{BUSY}$↑	(Note 10)	●	– 20			ns
t_9	Data Access Time After $\overline{RD}$↓	C_L = 20pF (Note 10)			50	110	ns
			●			140	ns
		C_L = 100pF			65	125	ns
			●			170	ns
t_{10}	Bus Relinquish Time	C_L = 100pF		20	60	90	ns
			●	20		100	ns
t_{11}	$\overline{RD}$ Low Time	(Note 10)	●	t_9			ns
t_{12}	$\overline{CONVST}$ High Time	(Notes 10, 13)	●	40			ns
t_{13}	Aperture Delay of Sample-and-Hold				35		ns
t_{14}	$\overline{SLEEP}$↑ to REFRDY↑ Wake-Up Time	10µF Bypass at V_{REF} Pin			4.2		ms
		4.7µF Bypass at V_{REF} Pin			3.3		ms
t_{15}	HBEN↑ to High Byte Data Valid	C_L = 100pF (LTC1277 Only)	●		35	100	ns

TIMING CHARACTERISTICS (Note 5) See Figures 13 to 17.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{16}	HBEN↓ to Low Byte Data Valid	C_L = 100pF (LTC1277 Only)	●		45	100	ns
t_{17}	HBEN↑ to $\overline{RD}$↓ Setup Time	(Note 10) (LTC1277 Only)	●	10			ns
t_{18}	$\overline{RD}$↑ to HBEN↓ Setup Time	(Note 10) (LTC1277 Only)	●	10			ns

The ● denotes specifications which apply over the full operating temperature range; all other limits and typicals T_A = 25°C.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND and AGND wired together and V_{LOGIC} is tied to V_{DD} in LTC1277 (unless otherwise noted).

Note 3: When these pin voltages are taken below V_{SS} (ground for unipolar mode) or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 60mA below V_{SS} (ground for unipolar mode) or above V_{DD} without latch-up.

Note 4: When these pin voltages are taken below V_{SS} (ground for unipolar mode), they will be clamped by internal diodes. This product can handle input currents greater than 60mA below V_{SS} (ground for unipolar mode) without latch-up. These pins are not clamped to V_{DD}.

Note 5: V_{DD} = 5V (V_{SS} = –5V for bipolar mode), V_{LOGIC} = V_{DD} (LTC1277), f_{SAMPLE} = 100ksps, t_r = t_f = 5ns unless otherwise specified.

Note 6: Linearity, offset and full-scale specifications apply for unipolar and bipolar modes.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: For LTC1274, bipolar offset is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111. For LTC1277, bipolar offset voltage is measured from –0.5LSB when the output code flickers between 0111 1111 1111 and 1000 0000 0000.

Note 9: The AC tests apply to bipolar mode only and the S/(N + D) is 71dB (typ) for unipolar mode at 100kHz input frequency.

Note 10: Guaranteed by design, not subject to test.

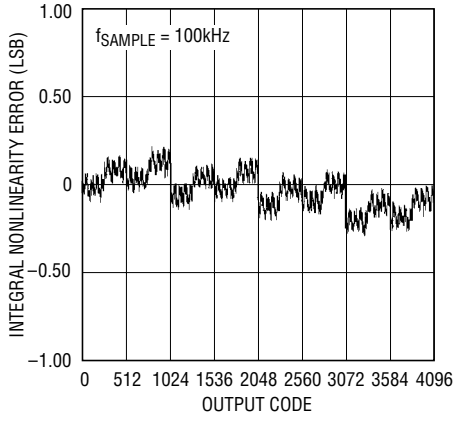
Note 11: Recommended operating conditions.

Note 12: A_{IN} must not exceed V_{DD} or fall below V_{SS} by more than 50mV to specified accuracy.

Note 13: The falling $\overline{CONVST}$ edge starts a conversion. If $\overline{CONVST}$ returns high at a bit decision point during the conversion it can create small errors. For best performance ensure that $\overline{CONVST}$ returns high either within 400ns after conversion start (i.e., before the first bit decision) or after $\overline{BUSY}$ rises (i.e., after the last bit test). See timing diagrams Modes 1a and 1b (Figures 13, 14).

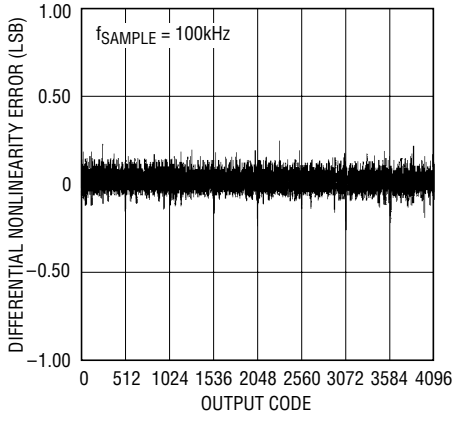
TYPICAL PERFORMANCE CHARACTERISTICS

Integral Nonlinearity vs Output Code



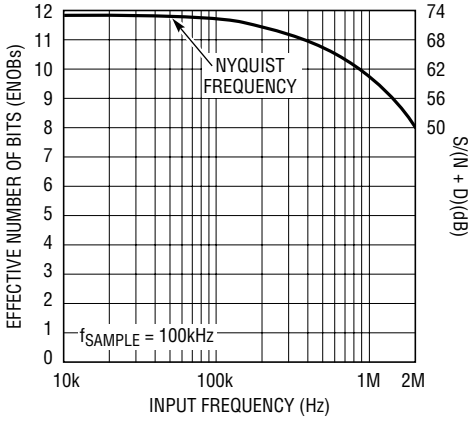
LT1274/77 • TPC01

Differential Nonlinearity vs Output Code



LT1274/77 • TPC02

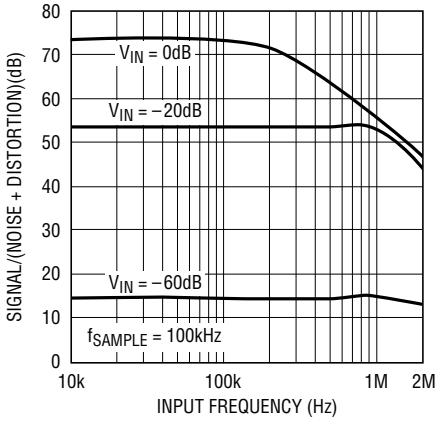
ENOBs and S/(N + D) vs Input Frequency



LTC1274/77 • TPC03

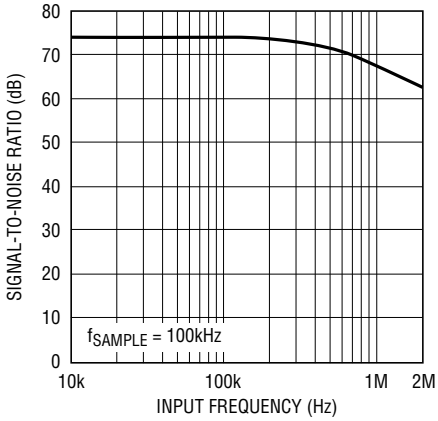
TYPICAL PERFORMANCE CHARACTERISTICS

S/(N + D) vs Input Frequency and Amplitude



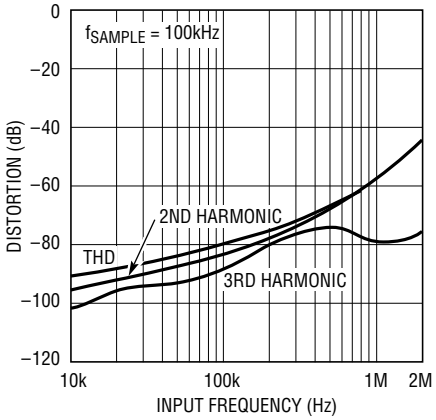
LTC1274/77 • TPC04

Signal-to-Noise Ratio (Without Harmonics) vs Input Frequency



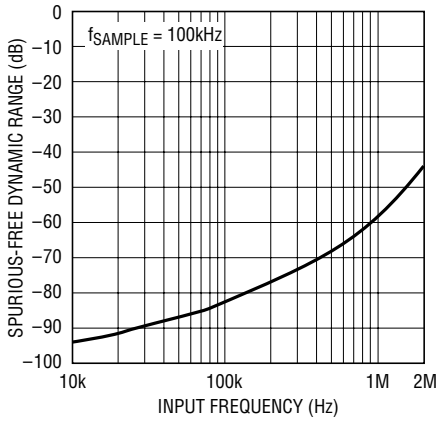
LTC1274/77 • TPC05

Distortion vs Input Frequency



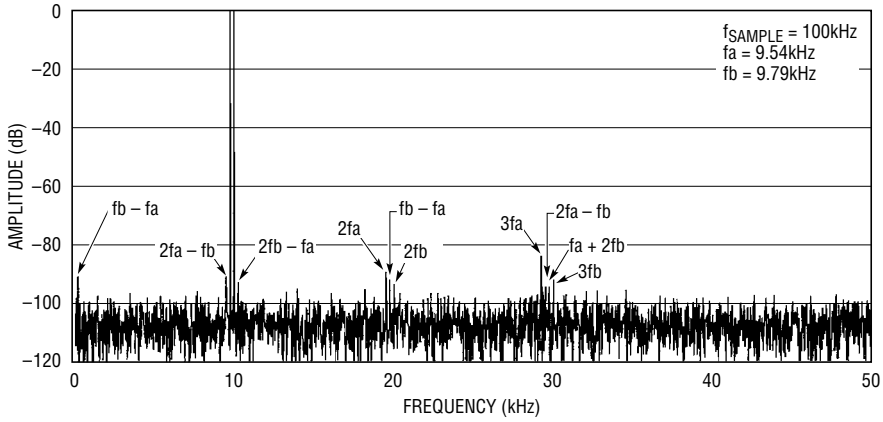
LTC1274/77 • TPC06

Spurious-Free Dynamic Range vs Input Frequency



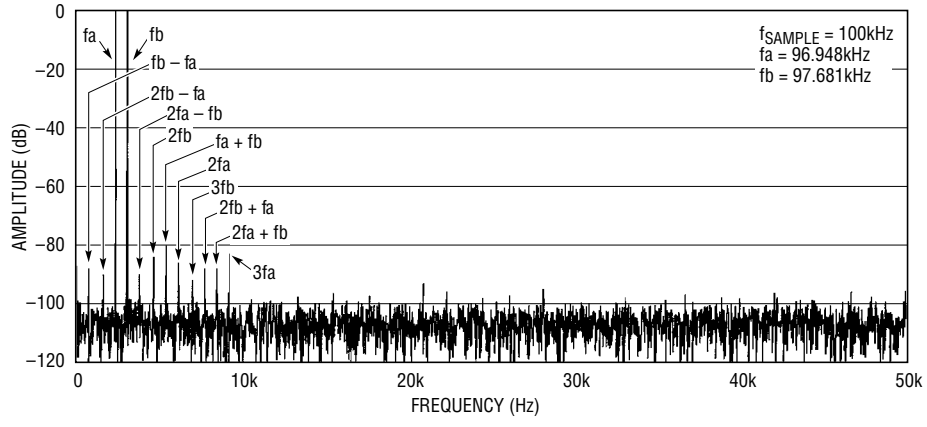
LTC1274/77 • TPC07

Intermodulation Distortion Plot



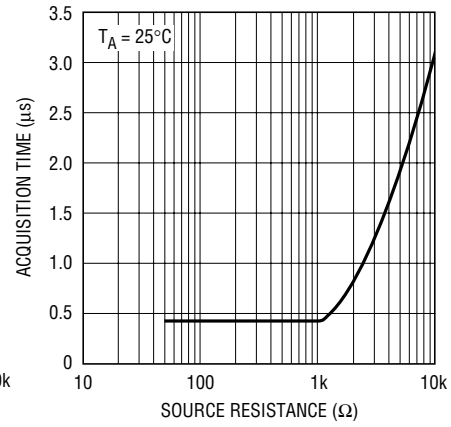
LTC1274/77 • TPC08

Intermodulation Distortion Plot



LTC1274/77 • TPC09

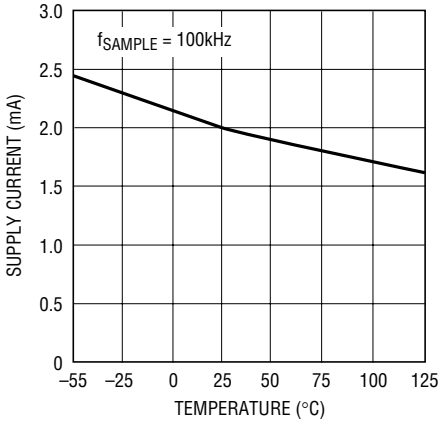
Acquistion Time vs Source Impedance



LTC1274/75 • TPC10

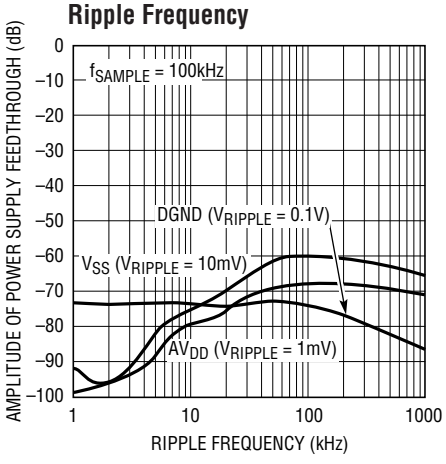
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Temperature



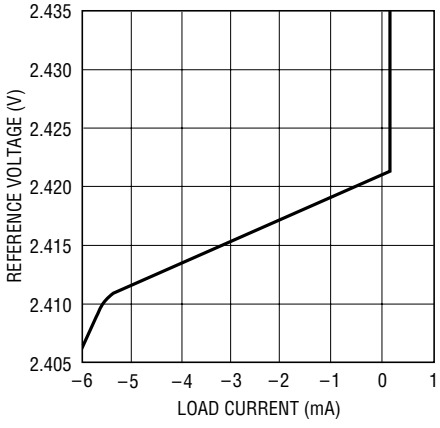
LT1274/77 • TPC11

Power Supply Feedthrough vs Ripple Frequency



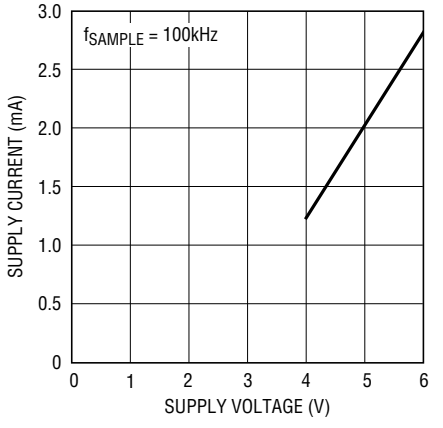
LTC1274/77 • TPC12

Reference Voltage vs Load Current



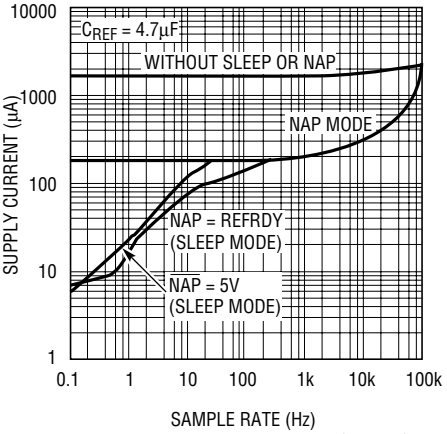
LT1274/77 • TPC13

Supply Current vs Supply Voltage



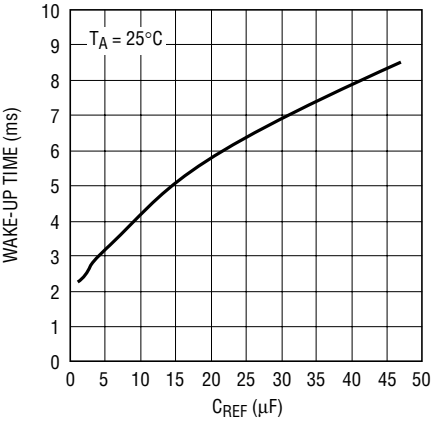
LTC1274/77 • TPC14

Supply Current vs Sample Rate With Sleep and Nap Modes



LTC1274/77 • TPC15

Wake-Up Time vs C_{REF} (Sleep Mode)



LTC1274/77 • TPC16

PIN FUNCTIONS

LTC1274

A_{IN} (Pin 1): Analog Input. 0V to 4.096V, unipolar (V_{SS} = 0V) or ±2.048V, bipolar (V_{SS} = –5V).

V_{REF} (Pin 2): 2.42V Reference Output. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic). V_{REF} can be overdriven positive with an external reference voltage.

AGND (Pin 3): Analog Ground.

D11 to D4 (Pins 4 to 11): Three-State Data Outputs. D11 is the Most Significant Bit.

DGND (Pin 12): Digital Ground.

D3 to D0 (Pins 13 to 16): Three-State Data Outputs.

REFRDY (Pin 17): Reference Ready Signal. It goes high when the reference has settled after $\overline{SLEEP}$ indicating that the ADC is ready to sample.

$\overline{SLEEP}$ (Pin 18): $\overline{SLEEP}$ Mode Input. Tie this pin to low to put the ADC in Sleep mode and save power (REFRDY will go low). The device will draw 1µA in this mode.

$\overline{CONVST}$ (Pin 19): Conversion Start Signal. This active low signal starts a conversion on its falling edge (to recognize $\overline{CONVST}$, $\overline{CS}$ has to be low.)

PIN FUNCTIONS

$\overline{RD}$ (Pin 20): Read Input. This enables the output drivers when $\overline{CS}$ is low.

$\overline{CS}$ (Pin 21): The Chip Select input must be low for the ADC to recognize $\overline{CONVST}$ and $\overline{RD}$ inputs.

$\overline{BUSY}$ (Pin 21): The $\overline{BUSY}$ output shows the converter status. It is low when a conversion is in progress. The rising Busy edge can be used to latch the conversion result.

V_{SS} (Pin 23): Negative 5V Supply. Negative 5V will select bipolar operation. Bypass to AGND with 0.1µF ceramic. Tie this pin to analog ground to select unipolar operation.

V_{DD} (Pin 24): Positive 5V Supply. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic).

LTC1277

A_{IN}^+ (Pin 1): Positive Analog Input. ($A_{IN}^+ - A_{IN}^-$) = 0V to 4.096V, unipolar (V_{SS} = 0V) or ±2.048V, bipolar (V_{SS} = –5V).

A_{IN}^- (Pin 2): Negative Analog Input. This pin needs to be free of noise during conversion. For single-ended inputs tie A_{IN}^- to analog ground.

V_{REF} (Pin 3): 2.42V Reference Output. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic). V_{REF} can be overdriven positive with an external reference voltage.

AGND (Pin 4): Analog Ground.

REFRDY (Pin 5): Reference Ready Signal. It goes high when the reference has settled after $\overline{SLEEP}$ indicating that the ADC is ready to sample.

$\overline{SLEEP}$ (Pin 6): $\overline{SLEEP}$ Mode Input. Tie this pin to low to put the ADC in Sleep mode and save power (REFRDY will go LOW). The device will draw 1µA in this mode.

$\overline{NAP}$ (Pin 7): $\overline{NAP}$ Mode Input. Pulling this pin low will shut down all currents in the ADC except the reference. In this mode the ADC draws 180µA. Wake-up from Nap mode is about 620ns.

D7 to D4* (Pins 8 to 11): Three-State Data Outputs.

DGND (Pin 12): Digital Ground.

D3/11 to D0/8* (Pins 13 to 16): Three-State Data Outputs. D11 is the Most Significant Bit.

V_{LOGIC} (Pin 17): 5V or 3V Digital Power Supply. This pin allows a 5V or 3V logic interface with the processor. All logic outputs (Data Bits, $\overline{BUSY}$ and REFRDY) will swing between 0V and V_{LOGIC}.

HBEN (Pin 18): High Byte Enable Input. The four Most Significant Bits will appear at Pins 13 to 16 when this pin is high. The LTC1277 uses straight binary for unipolar mode and offset binary for bipolar mode.

$\overline{CONVST}$ (Pin 19): Conversion Start Signal. This active low signal starts a conversion on its falling edge (to recognize $\overline{CONVST}$, $\overline{CS}$ has to be low).

$\overline{RD}$ (Pin 20): Read Input. This enables the output drivers when $\overline{CS}$ is low.

$\overline{CS}$ (Pin 21): The Chip Select input must be low for the ADC to recognize $\overline{CONVST}$ and $\overline{RD}$ inputs.

$\overline{BUSY}$ (Pin 22): The $\overline{BUSY}$ output shows the converter status. It is low when a conversion is in progress.

V_{SS} (Pin 23): Negative 5V Supply. Negative 5V will select bipolar operation. Bypass to AGND with 0.1µF ceramic. Tie this pin to analog ground to select unipolar operation.

V_{DD} (Pin 24): 5V Positive Supply. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic).

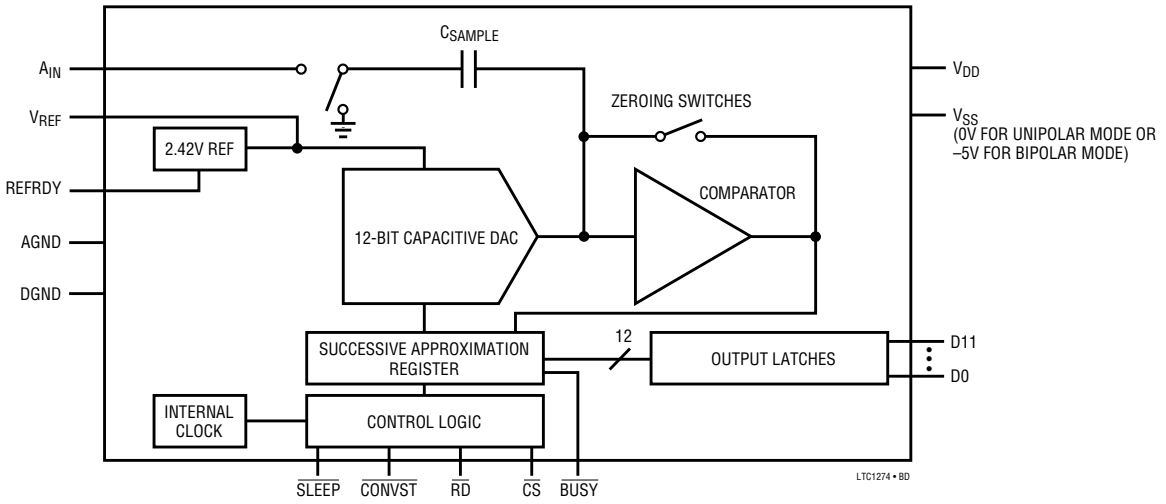
Table 1. LTC1277 Two-Byte Read Data Bus Status

DATA OUTPUTS	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
Low Byte	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
High Byte	Low	Low	Low	Low	DB11	DB10	DB9	DB8

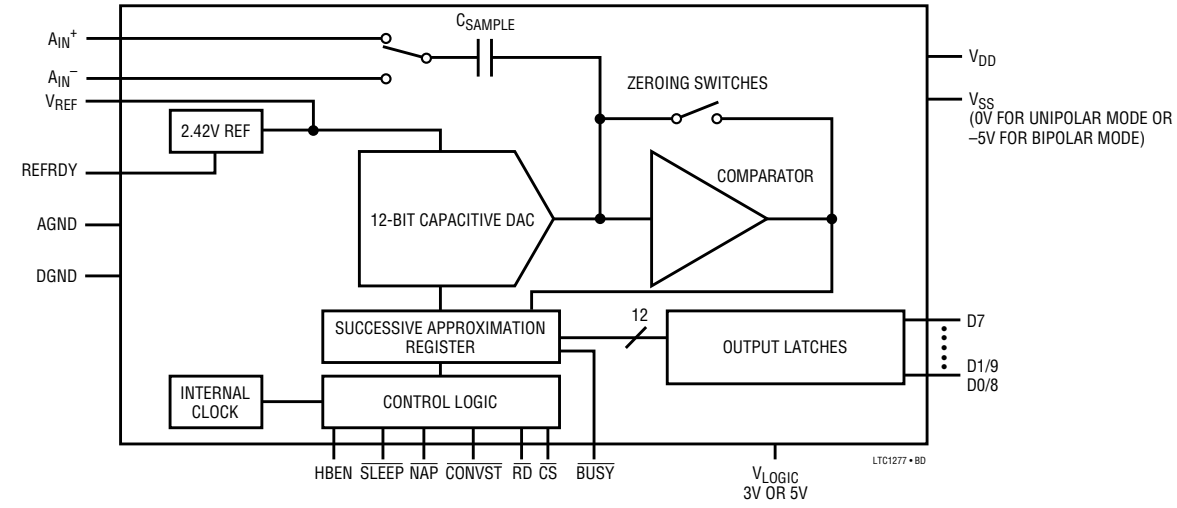
*The LTC1277 bipolar mode is in offset binary.

BLOCK DIAGRAMS

LTC1274

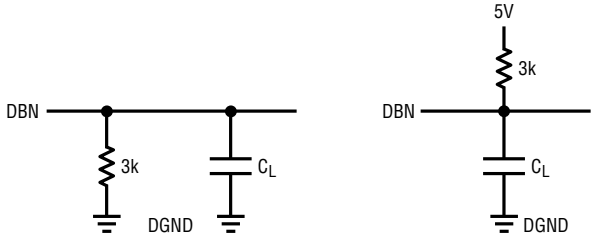


LTC1277



TEST CIRCUITS

Load Circuits for Access Timing

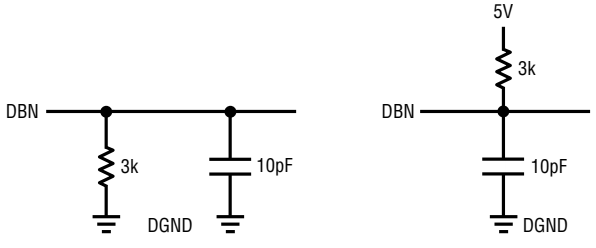


A) HIGH-Z TO V_{OH} (t_9) AND V_{OL} TO V_{OH} (t_6)

B) HIGH-Z TO V_{OL} (t_9) AND V_{OH} TO V_{OL} (t_6)

1274/77 • TC01

Load Circuits for Output Float Delay



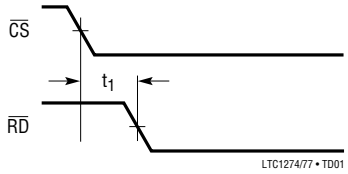
A) V_{OH} TO HIGH-Z

B) V_{OL} TO HIGH-Z

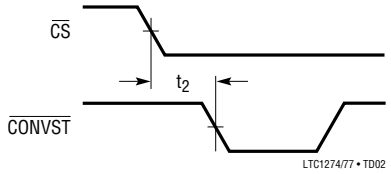
1274/77 • TC02

TIMING DIAGRAMS

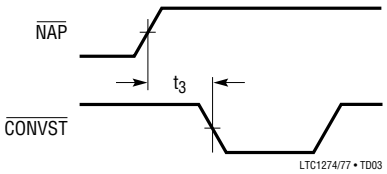
$\overline{CS}$ to $\overline{RD}$ Setup Timing



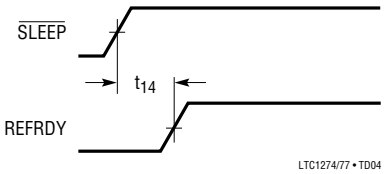
$\overline{CS}$ to $\overline{CONVST}$ Setup Timing



$\overline{NAP}$ to $\overline{CONVST}$ Wake-Up Timing (LTC1277)



$\overline{SLEEP}$ to REFRDY Wake-Up Timing



APPLICATIONS INFORMATION

CONVERSION DETAILS

The LTC1274/LTC1277 use a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog signal to a 12-bit parallel output. The ADCs are complete with a precision reference and an internal clock. The control logic provides easy interface to microprocessors and DSPs. (Please refer to the Digital Interface section for the data format.)

Conversion start is controlled by the $\overline{CS}$ and $\overline{CONVST}$ inputs. At the start of conversion the successive approximation register (SAR) is reset. Once a conversion cycle has begun it cannot be restarted.

During conversion, the internal 12-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 1, the A_{IN} (LTC1274) or A_{IN}^+ (LTC1277) input connects to the sample-and-hold capacitor during the acquire phase, and the comparator offset is nulled by the feedback switch. In this acquire phase, a minimum delay of 2µs will provide enough time for the sample-and-hold capacitor to acquire the analog signal. During the convert phase, the comparator feedback switch opens, putting the comparator into the compare mode. The input switch connects C_{SAMPLE} to ground (LTC1274) or A_{IN}^- (LTC1277), injecting the analog input charge onto the summing junction. This input charge is successively compared with the binary-weighted charges supplied by the capacitive DAC. Bit decisions are made by the high speed comparator. At the end of a conversion, the DAC output balances the A_{IN} (LTC1274) or $A_{IN}^+ - A_{IN}^-$ (LTC1277) input charge. The SAR contents (a 12-bit data word) which represent the A_{IN} (LTC1274) or $A_{IN}^+ - A_{IN}^-$ (LTC1277) are loaded into the 12-bit output latches.

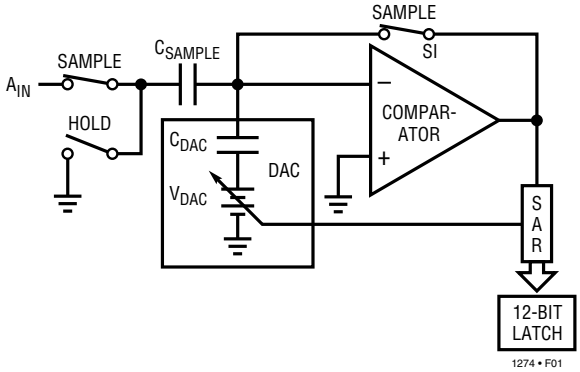


Figure 1. LTC1274 A_{IN} Input

DYNAMIC PERFORMANCE

The LTC1274/LTC1277 have excellent high speed sampling capability. FFT (Fast Fourier Transform) test techniques are used to test the ADCs' frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output

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using an FFT algorithm, the ADCs' spectral content can be examined for frequencies outside the fundamental. Figures 2a and 2b show typical LTC1274 FFT plots.

Signal-to-Noise Ratio

The Signal-to-Noise plus Distortion Ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies above DC and below half the sampling frequency. Figure 2a shows a typical spectral content with a 100kHz sampling rate and a 48.85kHz input. The dynamic performance is excellent for input frequencies well beyond Nyquist as shown in Figure 2b and Figure 3.

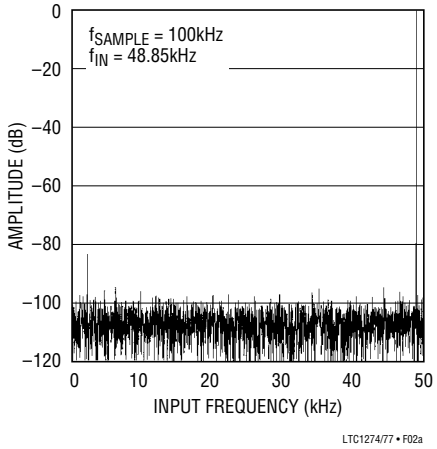

Figure 2a. LTC1274 Nonaveraged, 4096 Point FFT Plot with 50kHz Input Frequency

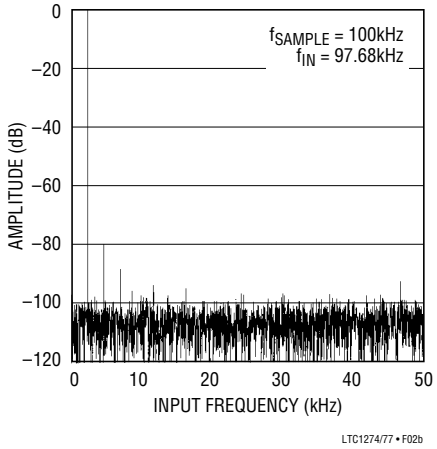

Figure 2b. LTC1274 Nonaveraged, 4096 Point FFT Plot with 100kHz Input Frequency

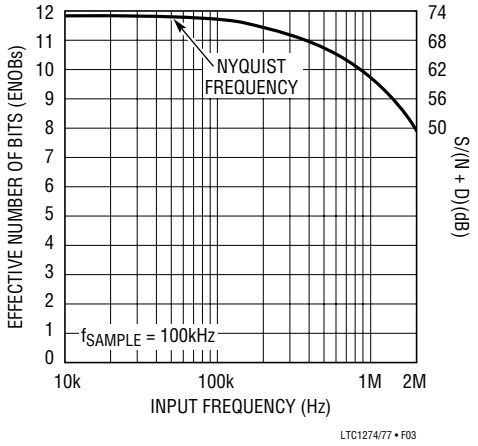

Figure 3. ENOBs and S/(N + D) vs Input Frequency

Effective Number of Bits

The Effective Number of Bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to the S/(N + D) by the equation:

$$N = [S/(N + D) – 1.76]/6.02$$

where N is the Effective Number of Bits of resolution and S/(N + D) is expressed in dB. At the maximum sampling rate of 100kHz, the LTC1274/LTC1277 maintain very good ENOBs over 300kHz. Refer to Figure 3.

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20\log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 \ldots + V_N^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through Nth harmonics. THD versus input fre-

APPLICATIONS INFORMATION

quency is shown in Figure 4. The ADCs have good distortion performance up to the Nyquist frequency and beyond.

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include (fa + fb) and (fa – fb) while the 3rd order IMD terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb). If the two input sine waves are equal in magnitude, the value (in decibels) of the 2nd order IMD products can be expressed by the following formula:

$$\text{IMD (fa} \pm \text{fb)} = 20\log \frac{\text{Amplitude at (fa} \pm \text{fb)}}{\text{Amplitude at fa}}$$

Figure 5 shows the IMD performance at a 97kHz input.

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full scale input signal.

Full-Power and Full-Linear Bandwidth

The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full-scale input signal.

The full-linear bandwidth is the input frequency at which the S/(N + D) has dropped to 68dB (11 effective bits). The LTC1274/LTC1277 have been designed to optimize input bandwidth, allowing ADCs to undersample input signals with frequencies above the converter's Nyquist frequency. The noise floor stays very low at high frequencies; S/(N + D) becomes dominated by distortion at frequencies far beyond Nyquist.

Driving the Analog Input

The analog input of the LTC1274/LTC1277 is easy to drive. It draws only one small current spike while charging the sample-and-hold capacitor at the end of conversion. During conversion the analog input draws only a small leakage current. The only requirement is that the amplifier driving the analog input must settle after the small current spike before the next conversion starts. Any op amp that settles in 2µs to small current transients will allow maximum speed operation. If slower op amps are used, more settling time can be provided by increasing the time between conversions. Suitable devices capable of driving the ADC A_{IN} input include the LT®1006, LT1007, LT1220, LT1223 and LT1224 op amps.

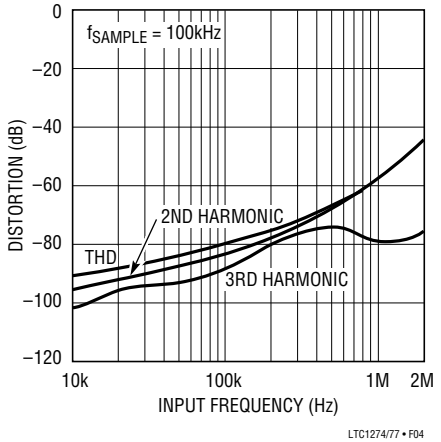

Figure 4. Distortion vs Input Frequency

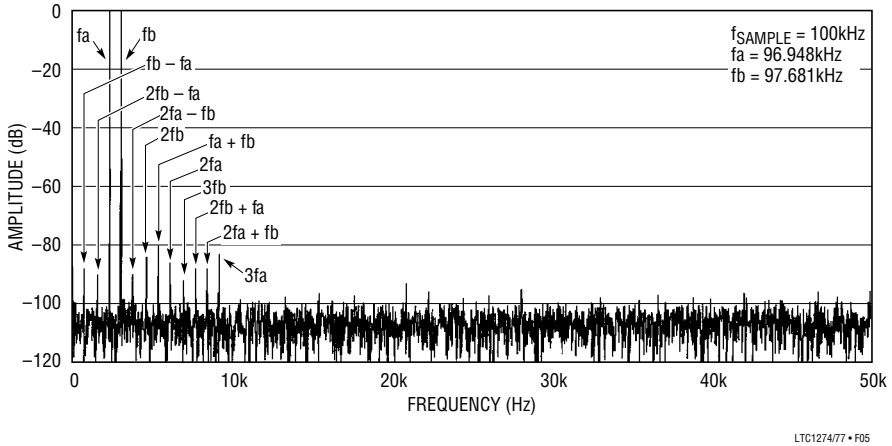

Figure 5. Intermodulation Distortion

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LTC1277 A_{IN}^+/A_{IN}^- Input Settling

The input capacitor for the LTC1277 is switched onto the A_{IN}^+ input during the sample phase. The voltage on the A_{IN}^+ input must settle completely within the sample period. At the end of the sample phase the input capacitor switches to the A_{IN}^- input and the conversion starts. During the conversion the A_{IN}^+ input voltage is effectively "held" by the sample-and-hold and will not affect the conversion result. It is critical that the A_{IN}^- input voltage be free of noise and settles completely during the conversion.

Internal Reference

The ADCs have an on-chip, temperature compensated, curvature corrected bandgap reference which is factory trimmed to 2.42V. It is internally connected to the DAC and is available at Pin 2 (LTC1274) or Pin 3 (LTC1277) to provide up to 1mA current to an external load.

For minimum code transition noise the reference output should be decoupled with a capacitor to filter wideband noise from the reference (10µF tantalum in parallel with a 0.1µF ceramic).

The V_{REF} pin can be driven with a DAC or other means to provide input span adjustment. The V_{REF} pin must be driven to at least 2.45V to prevent conflict with the internal reference. The reference should be driven to no more than 3V to keep the input span within the 5V supply in unipolar mode. In bipolar mode the reference should be driven to no more than 5V, the positive supply voltage of the chip.

Figure 6 shows an LT1006 op amp driving the Reference pin. In unipolar mode, the reference can be driven up to 2.95V at which point it will provide a 0V to 5V input span. For the bipolar mode, the reference can be driven up to 5V at which point it will provide a ±4.23V input span. Figure 7 shows a typical reference, the LT1019A-2.5 connected to the LTC1274. This will provide an improved drift (equal to the maximum 5ppm/°C of the LT1019A-2.5) and a ±2.115V (bipolar) or 4.231V (unipolar) full scale.

BOARD LAYOUT AND BYPASSING

Wire wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the LTC1274/LTC1277, a printed circuit board is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC. The analog input should be screened by AGND.

High quality tantalum and ceramic bypass capacitors should be used at the V_{DD} and V_{REF} pins as shown in

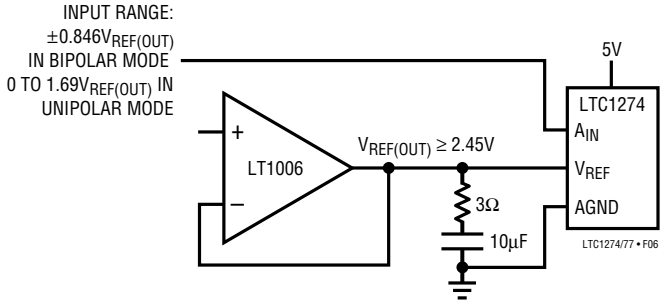

Figure 6. Driving the V_{REF} with the LT1006 Op Amp

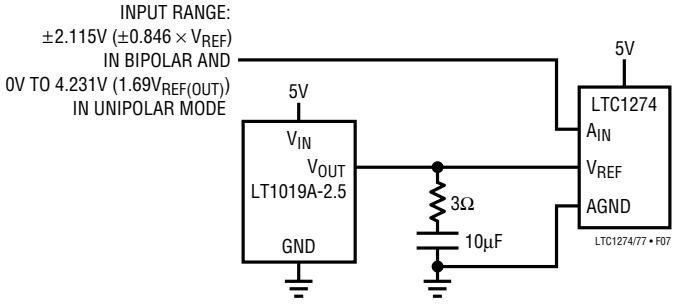

Figure 7. Supplying a 2.5V Reference Voltage to the LTC1274 with the LT1019A-2.5

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Figure 8. For bipolar mode, a 0.1µF ceramic provides adequate bypassing for the V_{SS} pin. The capacitors must be located as close to the pins as possible. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

Input signal leads to A_{IN} and signal return leads from AGND (Pin 3 for LTC1274, Pin 4 for LTC1277) should be kept as short as possible to minimize input noise coupling. In applications where this is not possible a shielded cable between source and ADC is recommended.

Also, since any potential difference in grounds between the signal source and the ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedances as much as possible.

A single point analog ground separate from the logic system ground should be established with an analog ground plane at AGND or as close as possible to the ADC. DGND (Pin 12) and all other analog grounds should be connected to this single analog ground point. No other digital grounds should be connected to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible. In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a Wait state during conversion or by using three-state buffers to isolate the ADC data bus. Figure 9 is a typical application circuit for the LTC1274.

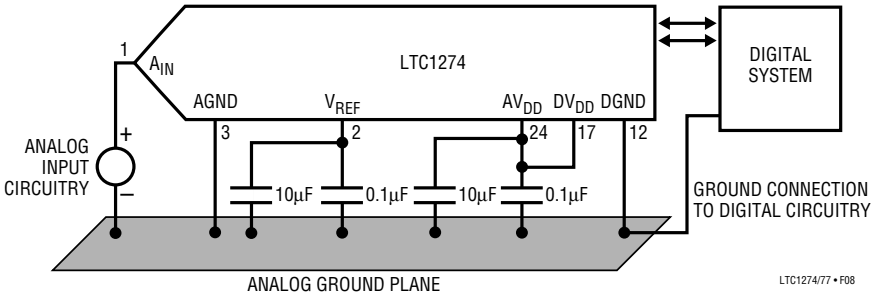

Figure 8. Power Supply Grounding Practice

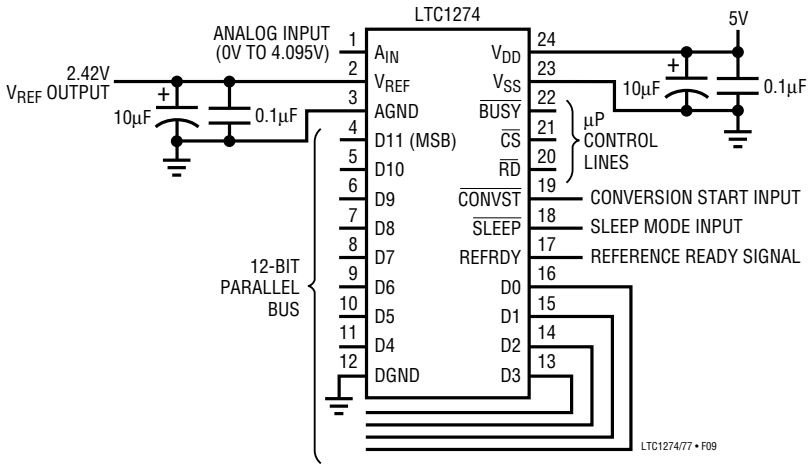

Figure 9. LTC1274 Typical Circuit

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DIGITAL INTERFACE

The ADCs are designed to interface with microprocessors as a memory mapped device. The $\overline{CS}$ and $\overline{RD}$ control inputs are common to all peripheral memory interfacing. A separate $\overline{CONVST}$ is used to initiate a conversion. Figures 10a to 10c are the input/output characteristics of the ADCs. The code transitions occur midway between successive integer LSB values (i.e., 0.5LSB, 1.5LSB, 2.5LSB…FS – 1.5LSV). The output code is scaled such that 1.0LSB = FS/4096 = 4.096V/4096 = 1.0mV.

Unipolar Offset and Full-Scale Error Adjustments

In applications where absolute accuracy is important, then offset and full-scale errors can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 11a shows the extra components required for full-scale error adjustment. If both offset and full-scale adjustments are needed, the circuit in Figure 11b can be used. For zero offset error, apply 0.50mV (i.e., 0.5LSB) at the input and adjust the offset trim until the LTC1274/LTC1277 output code flickers between 0000 0000 0000 and 0000 0000 0001. For zero full-scale error, apply an analog input of 4.0945V (i.e., FS – 1.5LSB or last code transition) at the input and adjust R5 until the ADC output code flickers between 1111 1111 1110 and 1111 1111 1111.

Bipolar Offset and Full-Scale Error Adjustments

Bipolar offset and full-scale errors are adjusted in a similar fashion to the unipolar case. Again, bipolar offset must be

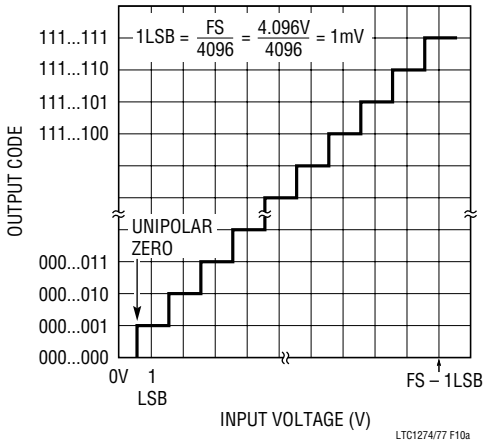

Figure 10a. LTC1274/LTC1277 Unipolar Transfer Characteristics

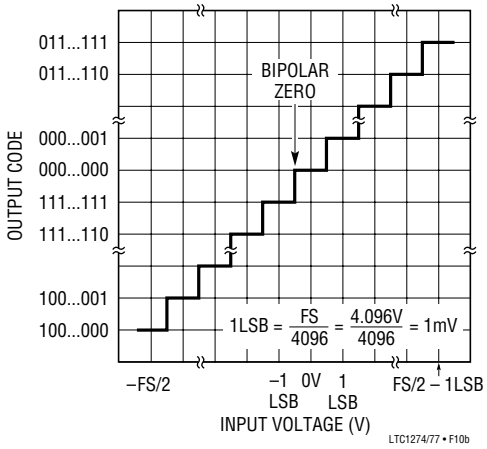

Figure 10b. LTC1274 Bipolar Transfer Characteristics (2's Complement)

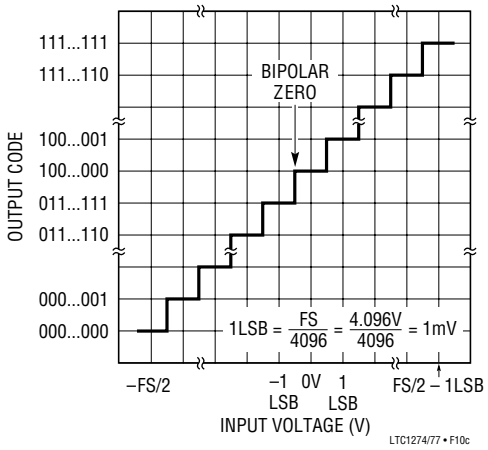

Figure 10c. LTC1277 Bipolar Transfer Characteristics (Offset Binary)

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adjusted before full-scale error. Bipolar offset error adjustment is achieved by trimming the offset adjust while the input voltage is 0.5LSB below ground. This is done by applying an input voltage of –0.50mV (–0.5LSB) to the input in Figure 11c and adjusting the R8 until the ADC's output code flickers between 0000 0000 0000 and 1111 1111 1111 in LTC1274 or between 0111 1111 1111 and 1000 0000 0000 in LTC1277. For full-scale adjustment, an input voltage of 2.0465V (FS – 1.5LSBs) is applied to the input and R5 is adjusted until the output code flickers between 0111 1111 1110 and 0111 1111 1111 in LTC1274 or between 1111 1111 1110 and 1111 1111 1111 in LTC1277.

Internal Clock

The A/D converters have an internal clock that eliminates the need of synchronization between the external clock and the $\overline{CS}$ and $\overline{RD}$ signals found in other ADCs. The internal clock is factory trimmed to achieve a typical conversion time of 6µs. No external adjustments are required and with the maximum acquisition time of 2µs throughput performance of 100ksps is assured.

Timing and Control

Conversion start and data read operations are controlled by three digital inputs in the LTC1274: $\overline{CS}$, $\overline{CONVST}$ and $\overline{RD}$. For the LTC1277 there are four digital inputs: $\overline{CS}$, $\overline{CONVST}$, $\overline{RD}$ and HBEN. Figure 12 shows the logic structure associated with these inputs for LTC1277. A falling edge on $\overline{CONVST}$ will start a conversion after the ADC has been selected (i.e., $\overline{CS}$ is low). Once initiated, it cannot be restarted until the conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output and this is low while conversion is in progress. The High Byte Enable input (HBEN) in the LTC1277 is to multiplex the 12 bits of conversion data onto the lower D7 to D0/8 outputs.

Figures 13 through 17 show several different modes of operation. In modes 1a and 1b (Figures 13 and 17) $\overline{CS}$ and $\overline{RD}$ are both tied low. The falling edge of $\overline{CONVST}$ starts the conversion. The data outputs are always enabled and data can be latched with the $\overline{BUSY}$ rising edge. Mode 1a shows operation with a narrow logic low $\overline{CONVST}$ pulse. Mode 1b shows a narrow logic high $\overline{CONVST}$ pulse.

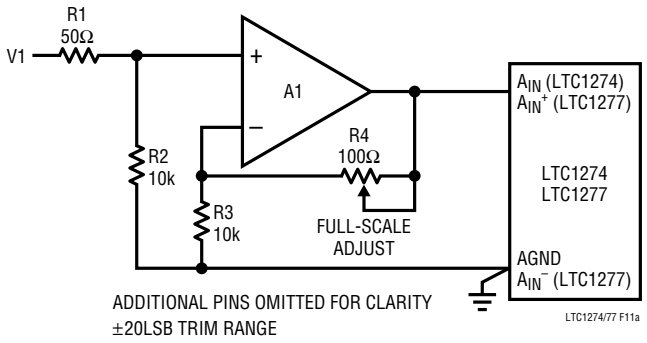

Figure 11a. Full-Scale Adjust Circuit

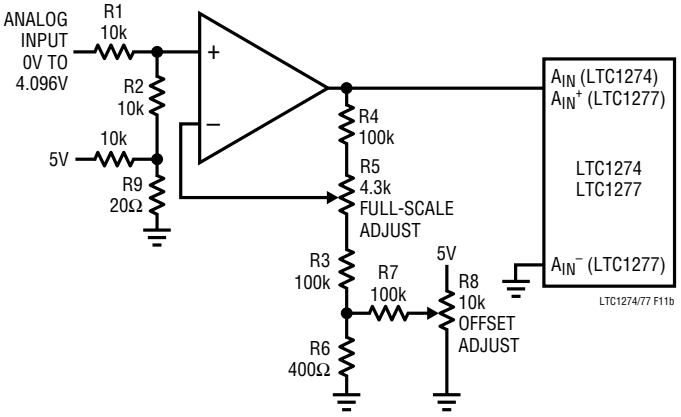

Figure 11b. LTC1274/LTC1277 Unipolar Offset and Full-Scale Adjust Circuit

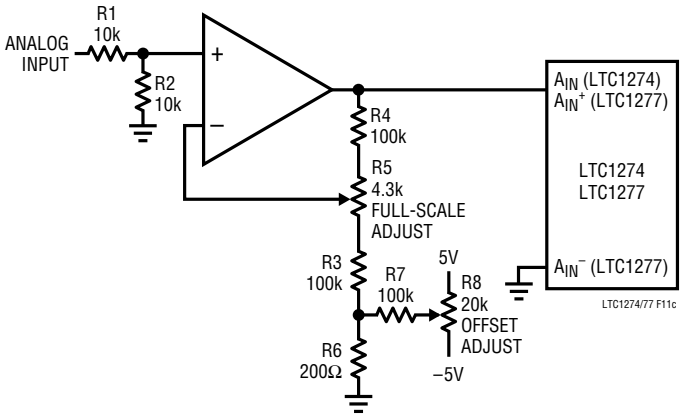

Figure 11c. LTC1274/LTC1277 Bipolar Offset and Full-Scale Adjust Circuit

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The narrow logic pulse on $\overline{CONVST}$ ensures that $\overline{CONVST}$ doesn't return high during the conversion (see Note 13 following the Timing Characteristics table).

In Mode 2 (Figure 15) $\overline{CS}$ is tied low. The falling edge of $\overline{CONVST}$ signal again starts the conversion. Data outputs both are in three-state until read by the MPU with the $\overline{RD}$ signal. Mode 2 can be used for operation with a shared MPU databus.

In slow memory and ROM modes (Figures 16 and 17) $\overline{CS}$ is tied low and $\overline{CONVST}$ and $\overline{RD}$ are tied together. The MPU starts the conversion and reads the output with the $\overline{RD}$ signal. Conversions are started by the MPU or DSP (no external sample clock).

In slow memory mode the processor applies a logic low to $\overline{RD}$ (= $\overline{CONVST}$), starting the conversion. $\overline{BUSY}$ goes low, forcing the processor into a Wait state. The previous conversion result appears on the data outputs. When the conversion is complete, the new conversion results appear on the data outputs; $\overline{BUSY}$ goes high releasing the processor; the processor applies a logic high to $\overline{RD}$ (= $\overline{CONVST}$) and reads the new conversion data.

In ROM mode the processor applies a logic low to $\overline{RD}$ (= $\overline{CONVST}$), starting a conversion and reading the previous conversion result. After the conversion is complete, the processor can read the new result and initiate another conversion.

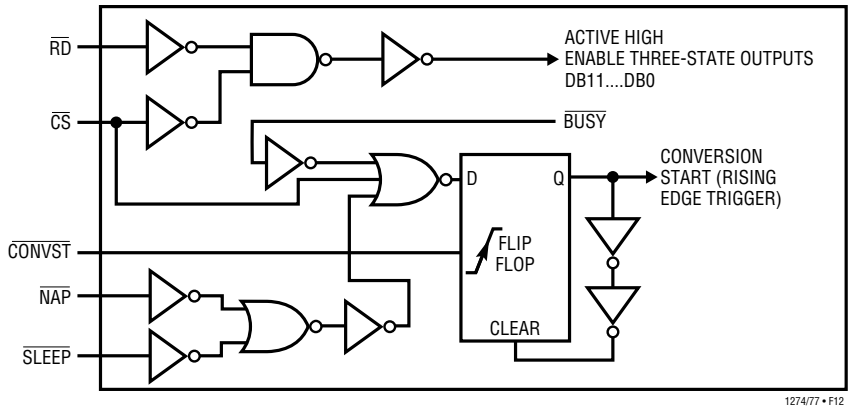


Figure 12. Internal Logic for Control Inputs $\overline{CS}$, $\overline{RD}$, $\overline{CONVST}$, $\overline{NAP}$ and $\overline{SLEEP}$ (LTC1277)

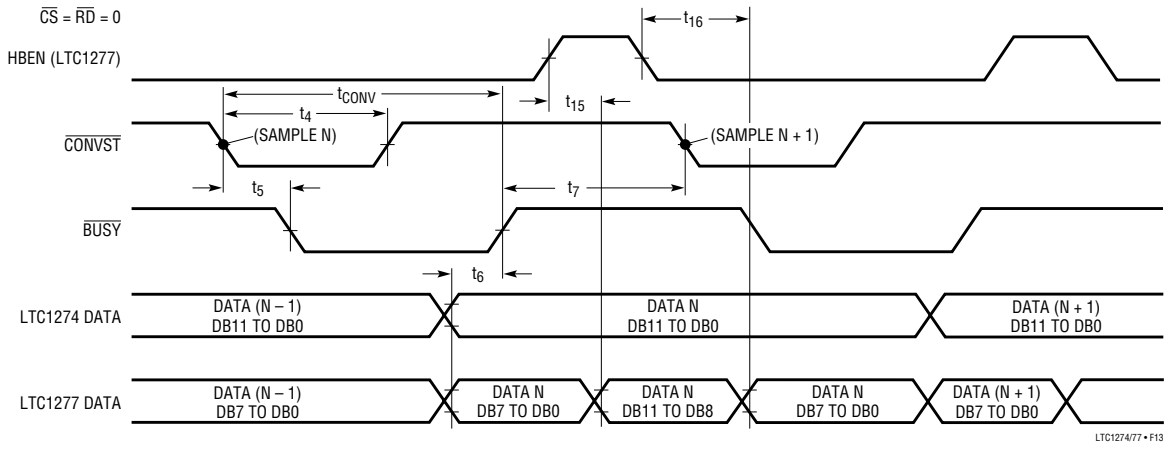
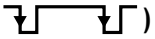


Figure 13. Mode 1a. $\overline{CONVST}$ Starts a Conversion. Data Outputs Always Enabled

($\overline{CONVST}$ =  **)**

APPLICATIONS INFORMATION

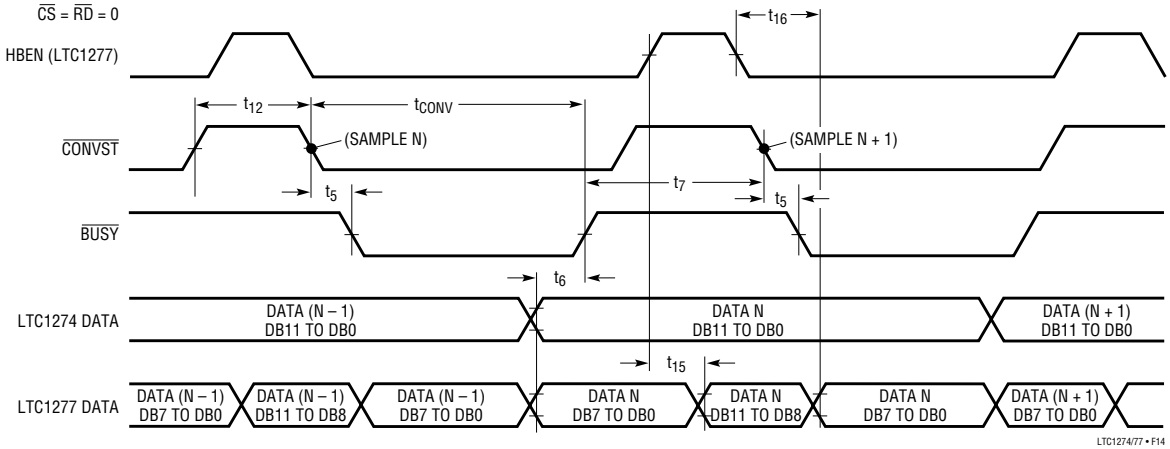


Figure 14. Mode 1b. $\overline{CONVST}$ Starts a Conversion. Data Outputs Always Enabled ($\overline{CONVST}$ = ⎍⎍)

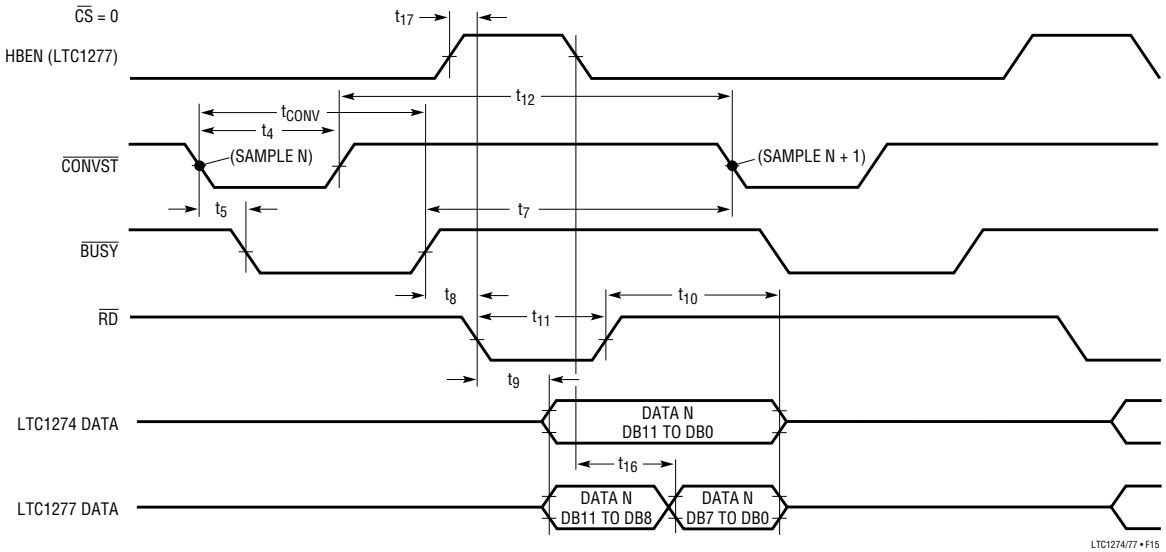


Figure 15. Mode 2. $\overline{CONVST}$ Starts a Conversion. Data is Read by $\overline{RD}$

APPLICATIONS INFORMATION

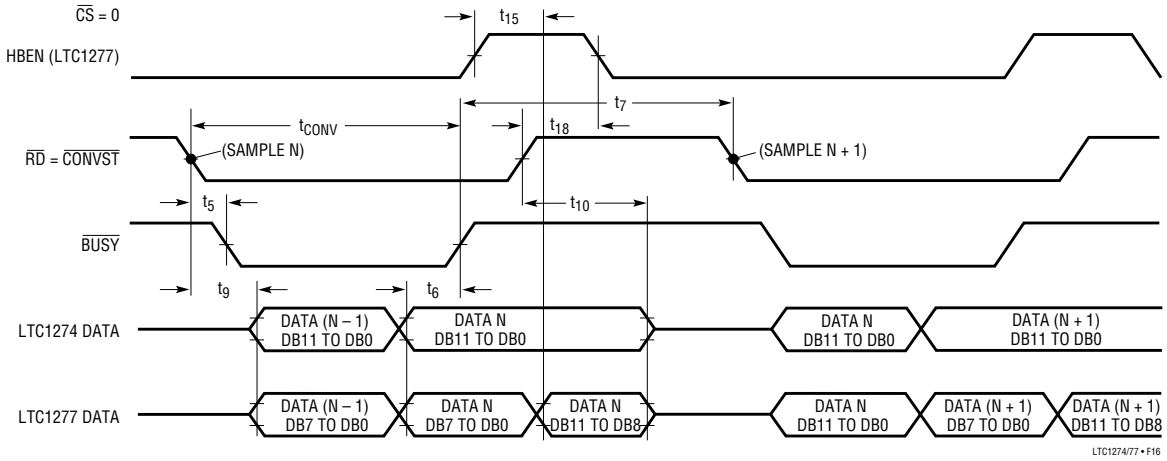


Figure 16. Slow Memory Mode

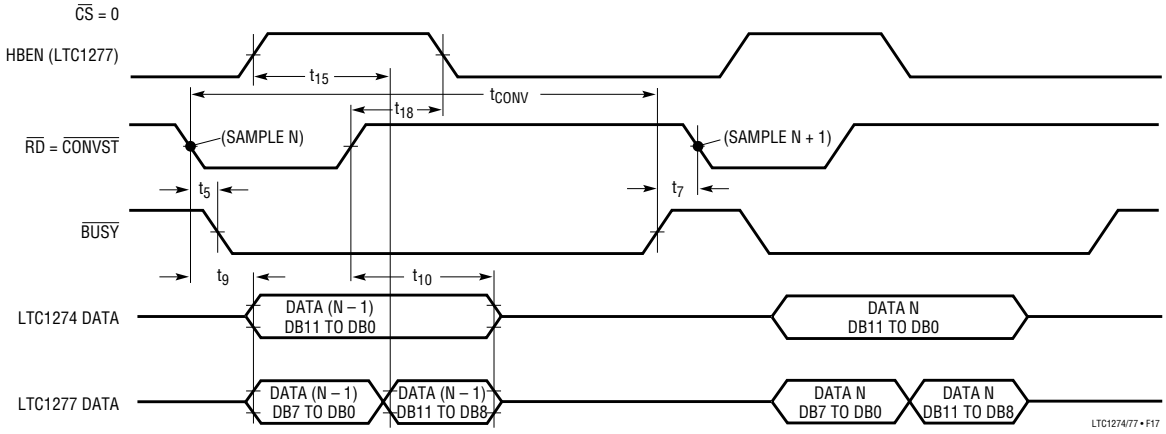


Figure 17. ROM Mode Timing

Power Shutdown

The LTC1274/LTC1277 provide shutdown features that will save power when the ADC is in inactive periods. Both ADCs have a Sleep mode. To power down the ADCs, $\overline{SLEEP}$ (Pin 18 in LTC1274 or Pin 6 in LTC1277) needs to be driver low. When in Sleep mode, the LTC1274/LTC1277 will not start a conversion even though the $\overline{CONVST}$ goes low. The parts draw 1μA. After release from the Sleep mode, the ADCs need 3ms (4.7μF bypass capacitor on V_{REF} pin) to wake up and a REFRDY signal will go to high to indicate the ADC is ready to do conversions.

The LTC1277 has an additional Nap mode. When $\overline{NAP}$ (Pin 7) is tied low, all the power is off except the internal reference which is still active and provides 2.42V output voltage to the other circuitry. In this mode the ADC draws 0.9mW instead of 10mW (for minimum power, the logic inputs must be within 600mV from the supply rails). The wake-up time from the power shutdown to active state is 620ns. The typical performance graph on the front page of this data sheet shows that the power will be reduced greatly by using the Sleep and Nap modes.

APPLICATIONS INFORMATION

In the Sleep mode, the comparator of the ADC will start consuming power after the rising edge of $\overline{SLEEP}$ as shown in Figure 18a. If REFRDY is tied to $\overline{NAP}$, the comparator will be powered up after REFRDY's rising edge. Hence more power will be saved as in Figure 18b.

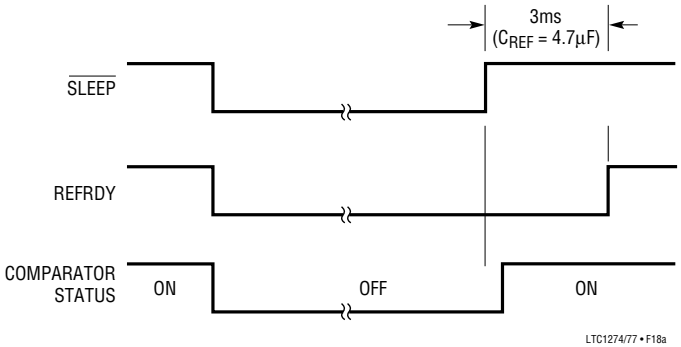


Figure 18a. Power Saved in Sleep Mode ($\overline{NAP}$ = HIGH)

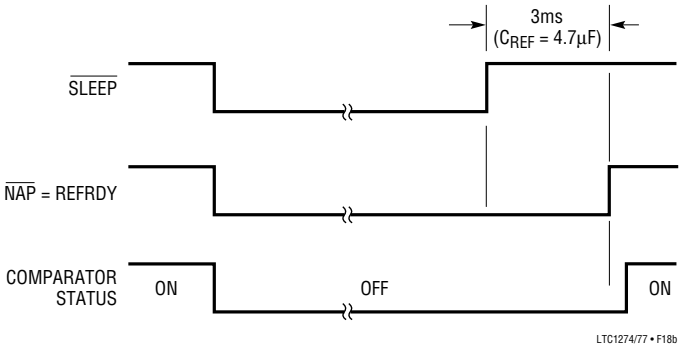
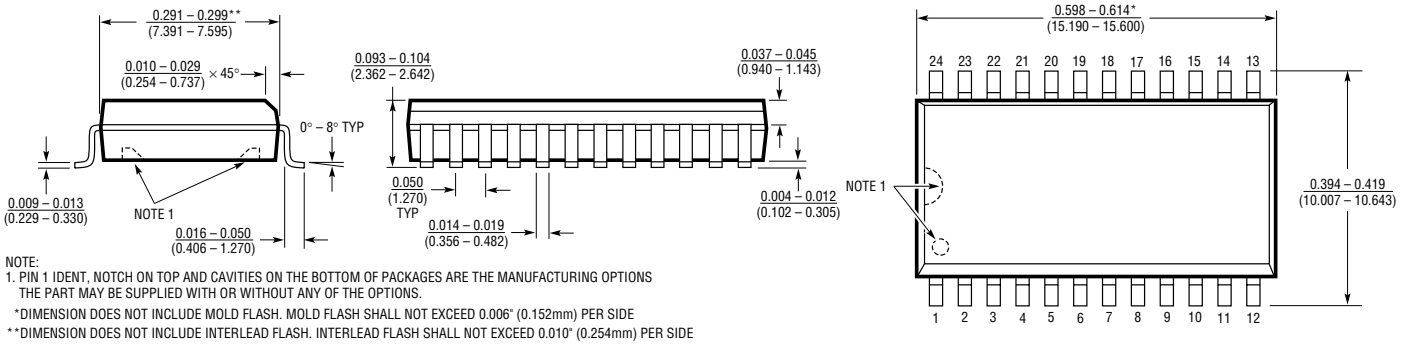


Figure 18b. Power Saved in Sleep Mode ($\overline{NAP}$ = REFRDY)

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

SW Package
24-Lead Plastic Small Outline (Wide 0.300)
(LTC DWG # 05-08-1620)



NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS
THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1272	12-Bit, 3µs, 250kHz Sampling A/D Converter	Single 5V, Sampling 7572 Upgrade
LTC1273/75/76	12-Bit, 300ksps Sampling A/D Converters with Reference	Complete with Clock, Reference
LTC1278	12-Bit, 500ksps Sampling A/D Converter with Shutdown	70dB SINAD at Nyquist, Low Power
LTC1279	12-Bit, 600ksps Sampling A/D Converter with Shutdown	70dB SINAD at Nyquist, Low Power
LTC1282	12-Bit, 140ksps Sampling A/D Converter with Reference	3V or ±3V ADC with Reference, Clock
LTC1409	12-Bit, 800ksps Sampling A/D Converter with Shutdown	Fast, Complete Low Power ADC, 80mV
LTC1410	12-Bit, 1.25Msps Sampling A/D Converter with Shutdown	Fast, Complete Wideband ADC, 160mV